Cache Coherence

Sidney Primas and Dinis Cheian

Progress

Exercise	Passed All	Passed Some	Passed None
Refined DCache (1.1)	✓		
Store Queue (1.2)	✓		
LHUSM (1.3)	✓		
Message Fifo (2.1)	✓		
Message Router (2.2)	✓		
Coherent DCache (2.3)	✓		
PPP (2.4)	✓		
RefDMem (2.5)	✓		
Three Cycle Processor (2.6)	✓		
Six Cycle Processor (2.7)	✓		
Atomic Instructions (2.8)	✓		
Store Queue (2.9)	✓		
LHUSM (2.10)		✓	

Not Passed on LHUSM:

- On Three: SpinLock
- Six Stage: SpinLock, Multiply2, MdDecker

Debugging - Sc_test

- During the Sc-test we passed tb2 but not tb4.
- Error due to possible deadlock.
- Managed to pass by increasing the waiting time.
- **Solution**: implement round robin in Message Router.

Debugging - Lr and Sc

- Error while processing a Sc miss. The committed Cache Line did not match the expected Cache Line.

- Narrowed down to the case when Sc Miss and the linkAddr did not match Cache Addr anymore at the moment of Response from the Memory.

- **Solution**: write to Cache even if linkAddr does not match Cache Line Addr.

Debugging - Fence

- **Issue**: With STQ, McDeckker deadlocks with Six Stage Core.

- **Symptom**: After Fence op, Core 1 deadlocks and we never process the Fence op. Never execute rule mvStoreToCache.

- **Techniques**: Determine reason for deadlock, investigate instructions before deadlock, investigate/ alter assembly code, etc

- **Solution**: Empty StoreQ in handleProcReq Rule.

Debugging - LHUSM

- **Issue**: With LHUSM, Deadlock during spin_lock with three stage cores.

- **Symptom**: Deadlock occurs during first Load Hit in Cache during a Store Miss. Load Hit from STQ works.

- **Solution:** In progress…

Improvements for Class

- Develops methods to incrementally compile code.
- Minimize number of tests.
- Spend more time on the hardware side (gates).