# A Parametrizable Processor

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# Motivation

- Efficient system-on-a-chip solutions
- Wide spectrum of requirements
  - Performance
  - Area / Power
- Tuning without engineering

# Overview

- One-Rule Synchronous Processor
- Combinational stages packaged as functions
- Parameter-controlled configuration
- Optimization (performance/area):
  - Compiler macros
  - Aggressive compiler
- Results / tradeoffs

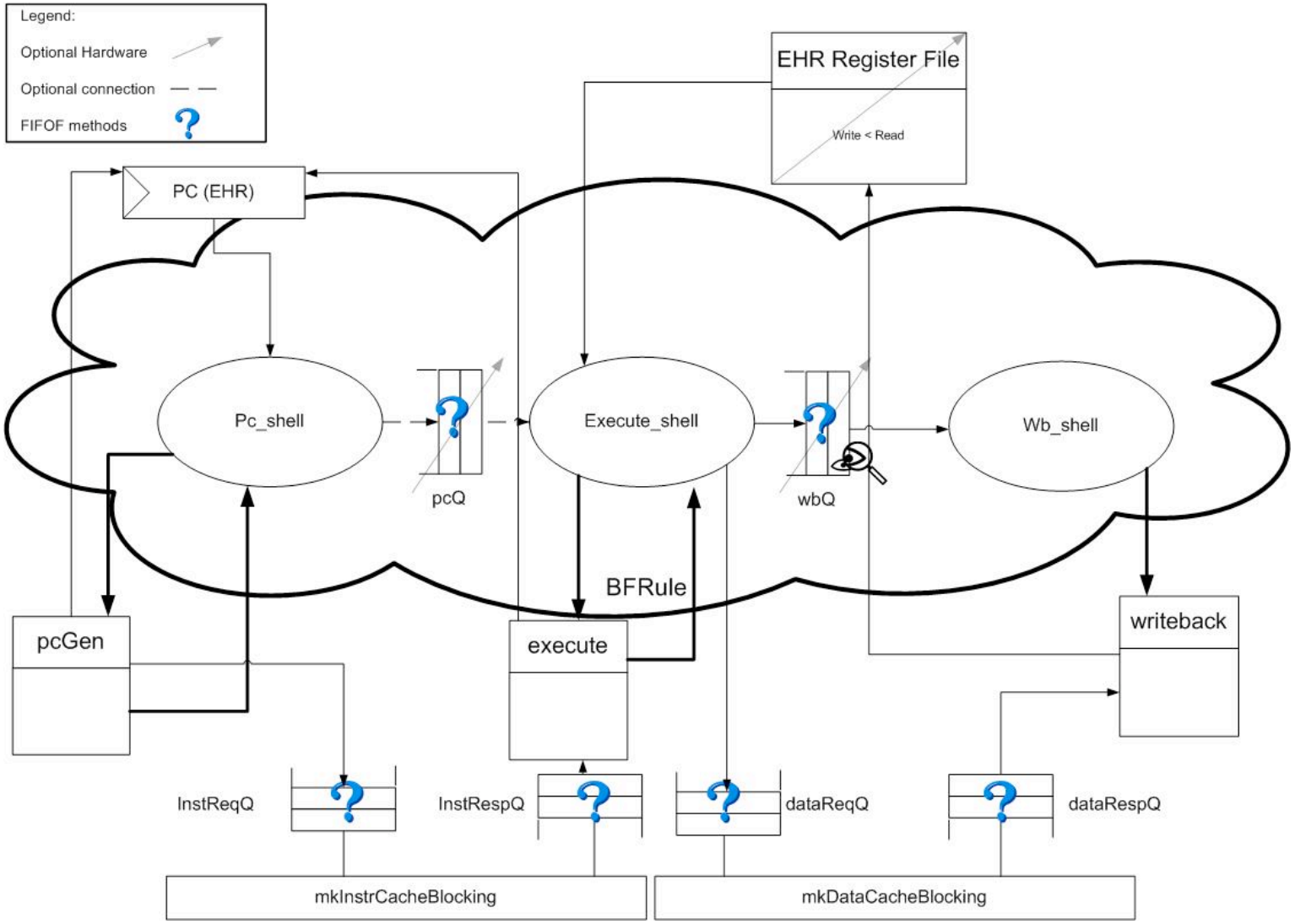
# One Rule to rule them all

- Explicit guards (WILL_FIRE)
  - FIFOF Methods
  - Data Memory
  - Writeback stage guard
- Customized SFIFO
  - *First, find, find2, notFull, notEmpty, deq < enq < clear*
  - *Guards < Actions*
  - *Writeback < Execute*
  - *No Bypassing*

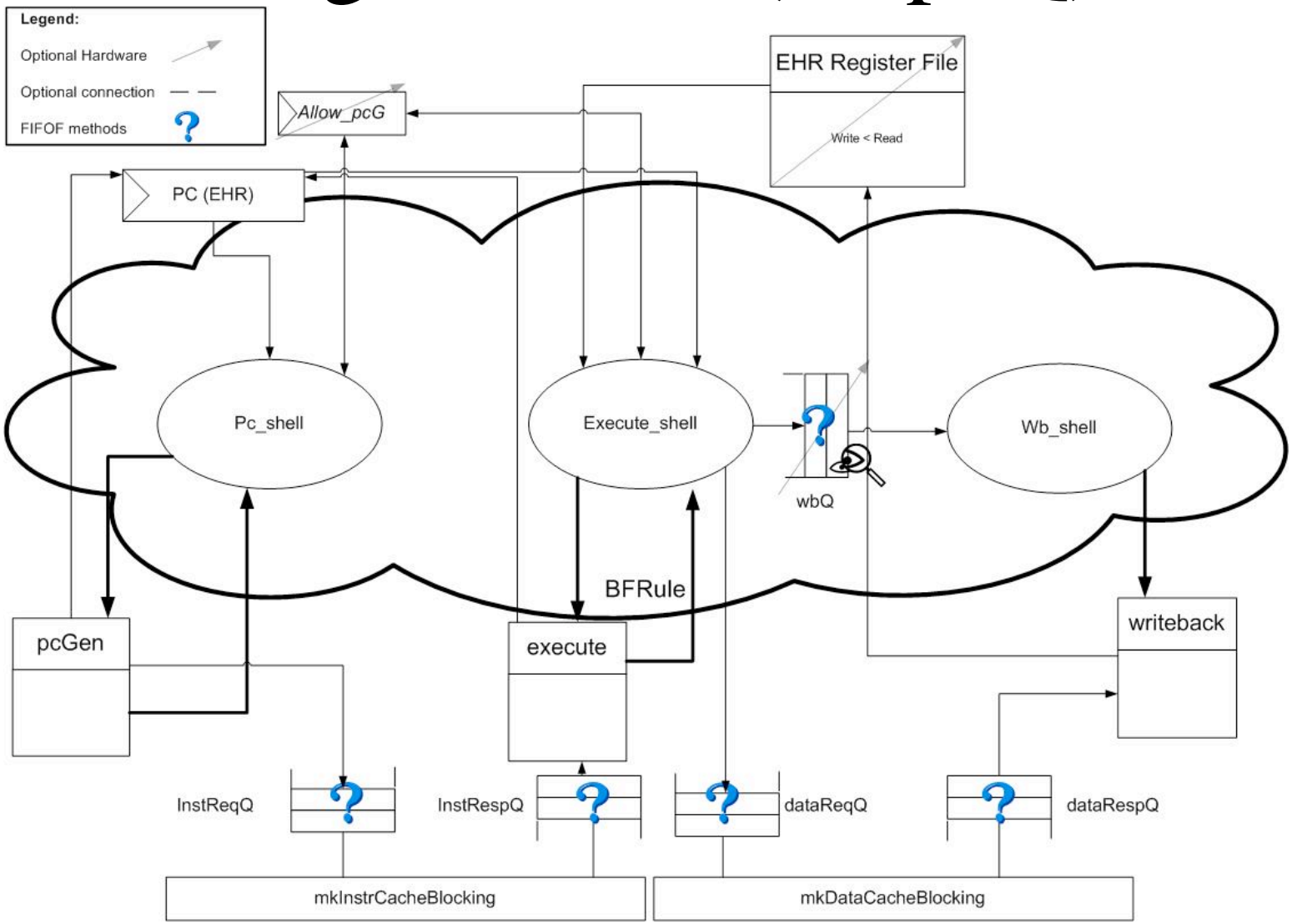
# Packaging for Abstraction

- Achieve highly modular parameterization
- Combinational workhorse unchanged
  - Can be packaged/abstracted into functions
  - ActionValue functions

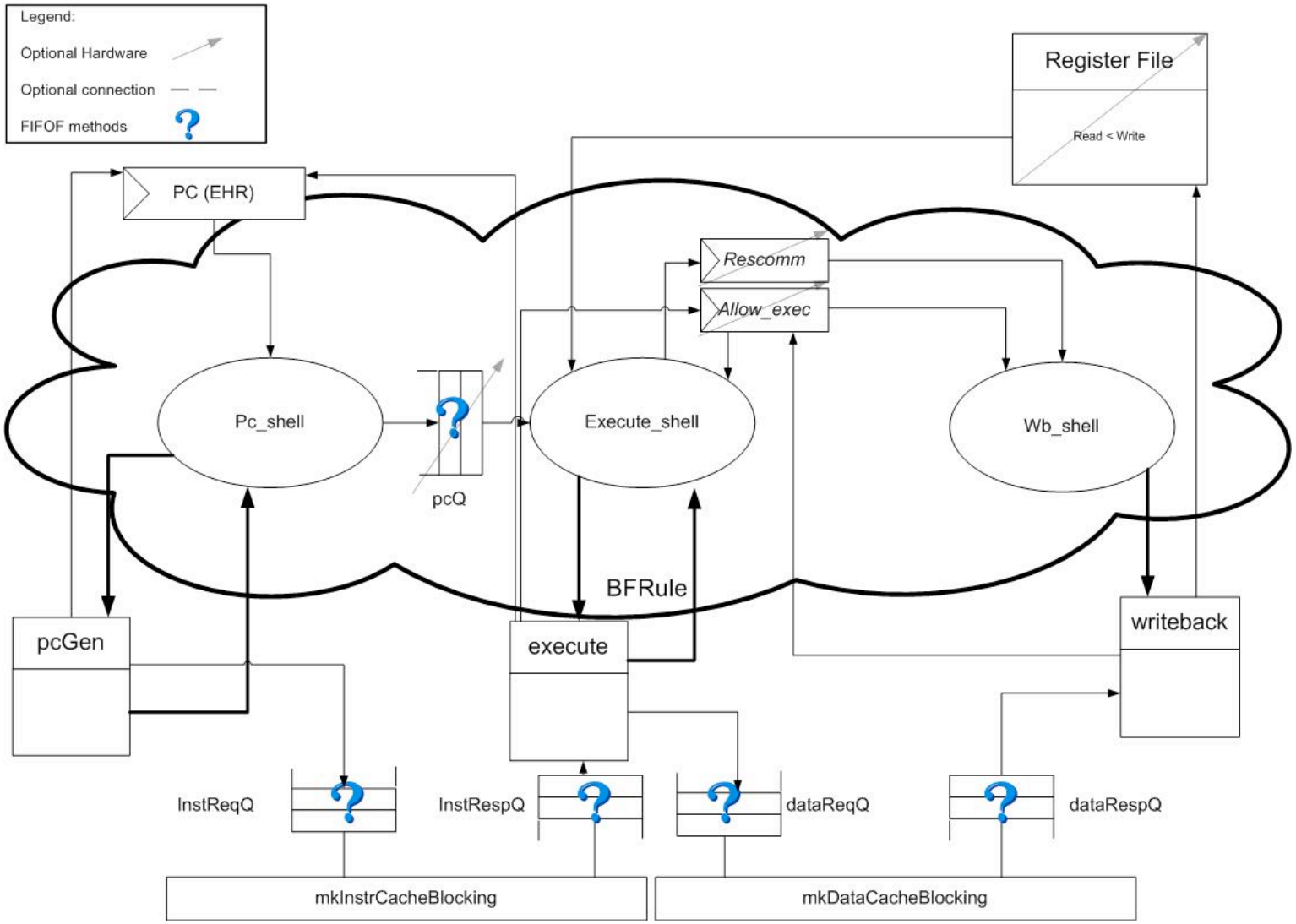
# 3-stage packaged version



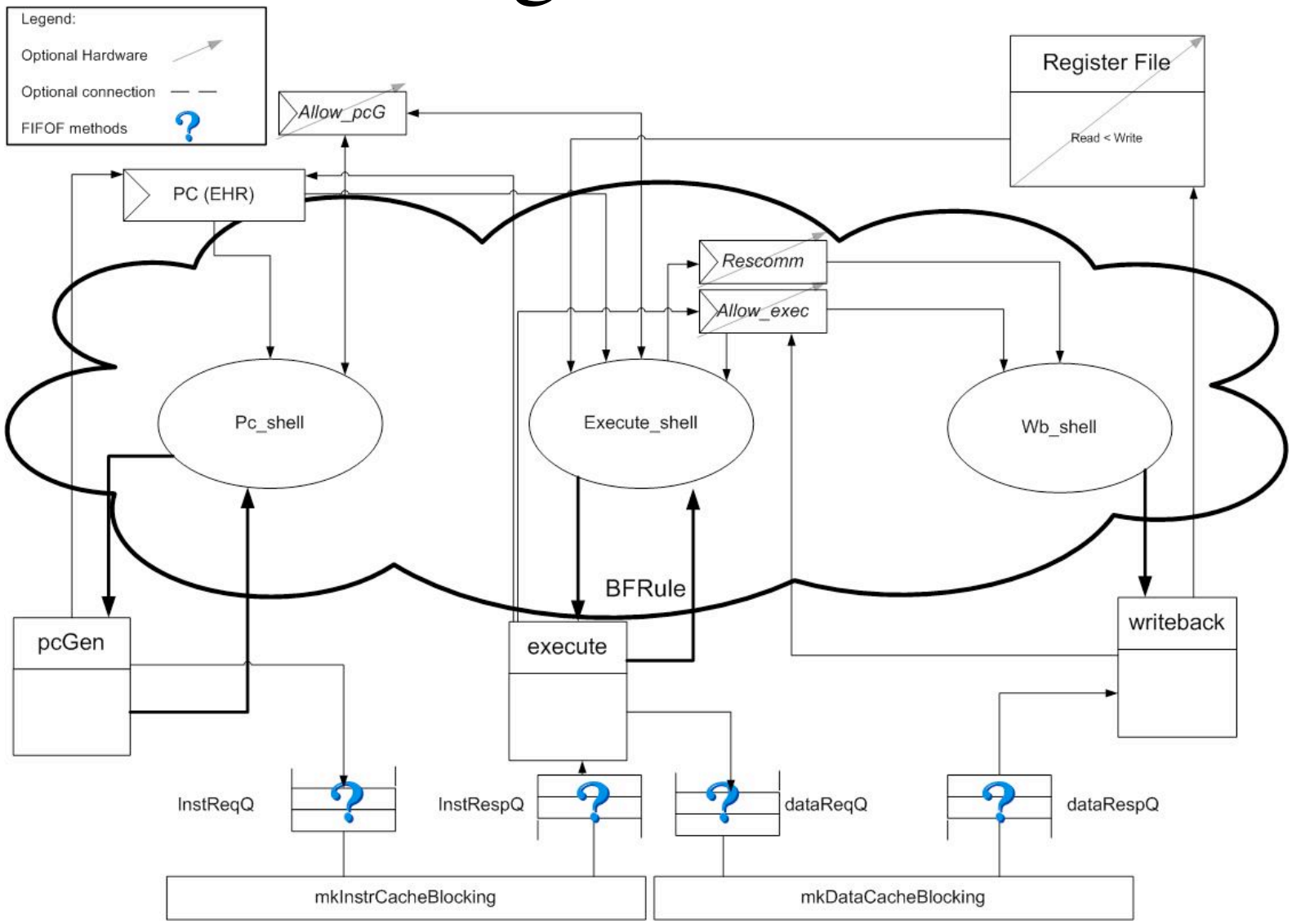
# 2-stage version (no pcQ)



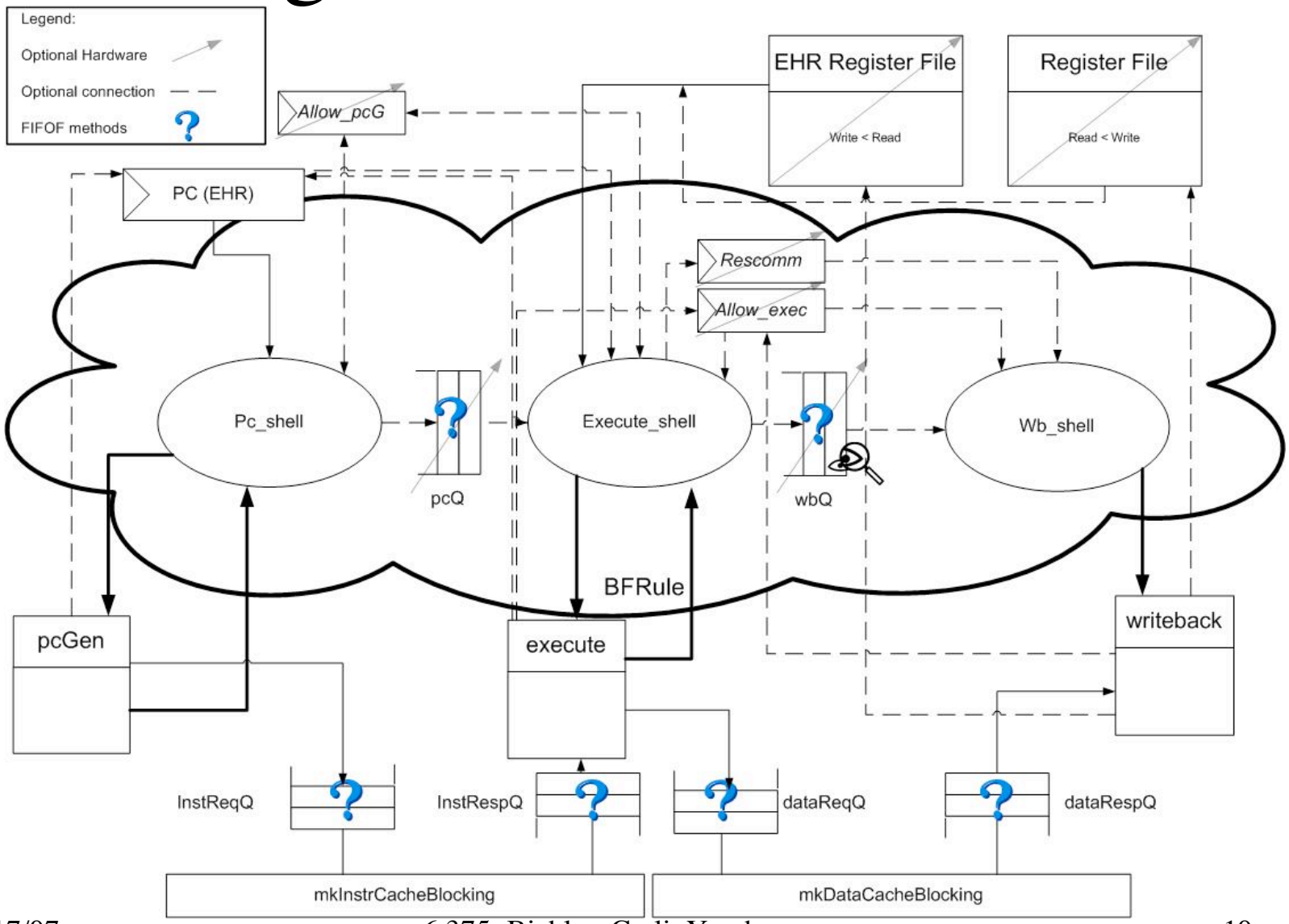
# 2-stage version (no wbQ)



# 1-stage version



# High-level schematics



# 2-stage Exploration

- Instruction memory
  - Never skipped
  - High latency
- Data memory
  - Only used on memory LD/ST instructions
  - Pipeline causes stalls
  - On branches/jumps no need for writeback
- However, specific SOC tasks can benefit from alternative solutions

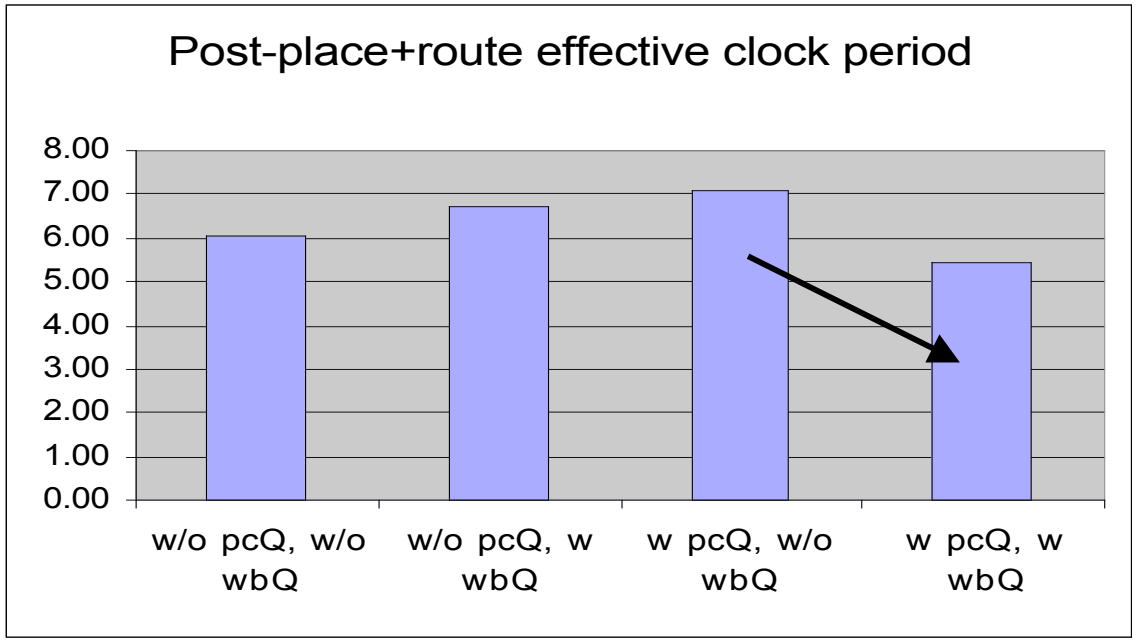
# Test Strategy

- Custom Makefile
  - Scans and changes parameters automatically
  - Synthesizes various configurations
  - Reports IPC, IPS, clock period, area

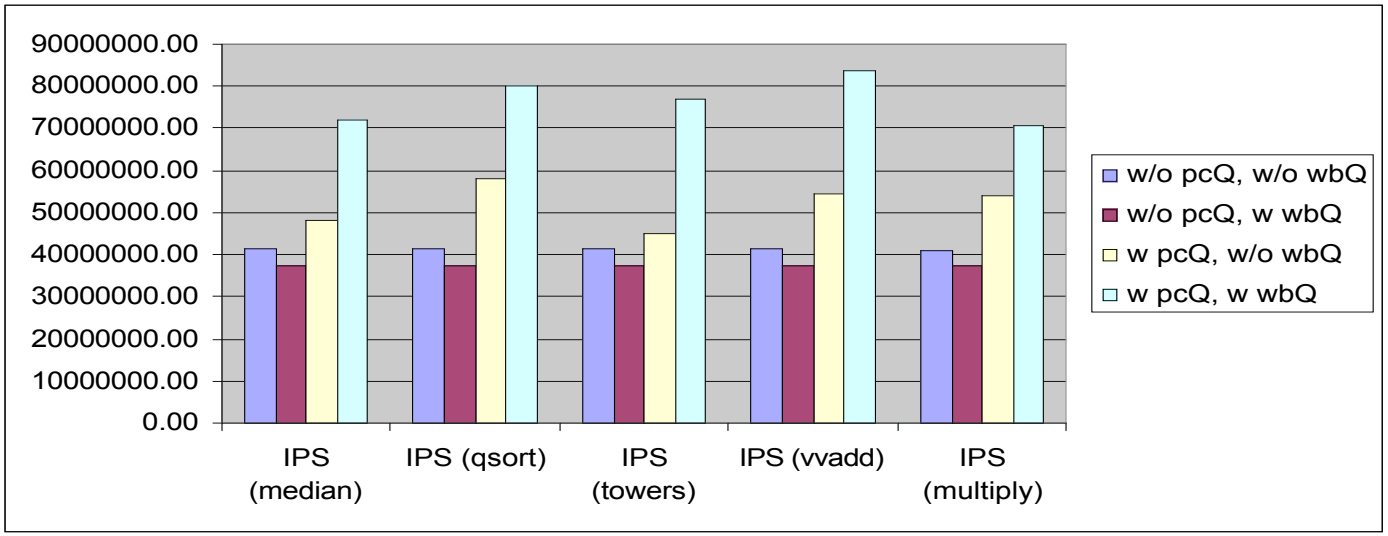
# Results: Clock Period

*Expectation:*

*Effective clock period is expected to decrease with the number of pipelined stages, as we make the critical path shorter*

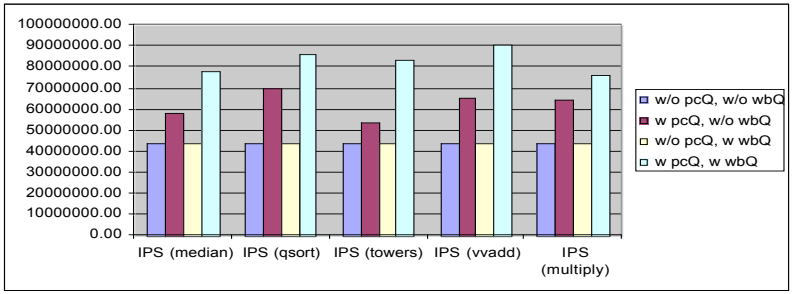


# Results: IPS



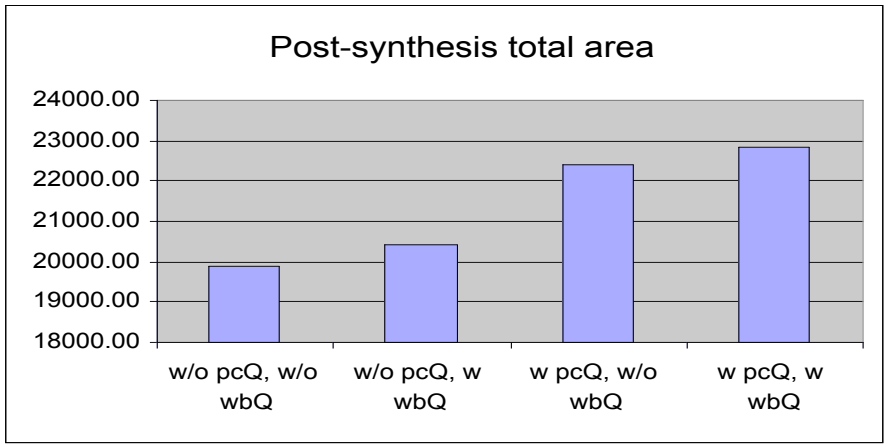

non-EHR RegFile

*Design exploration*



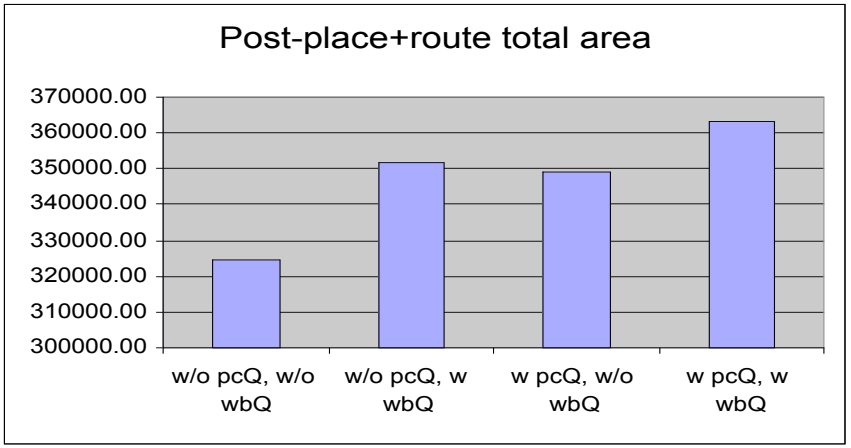

EHR RegFile

# Results: Area

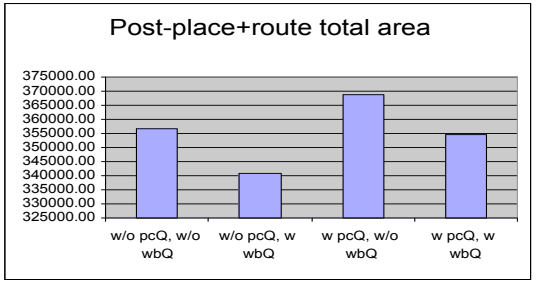



*Expectation:*

*Area should increase with the number of pipelined stages*

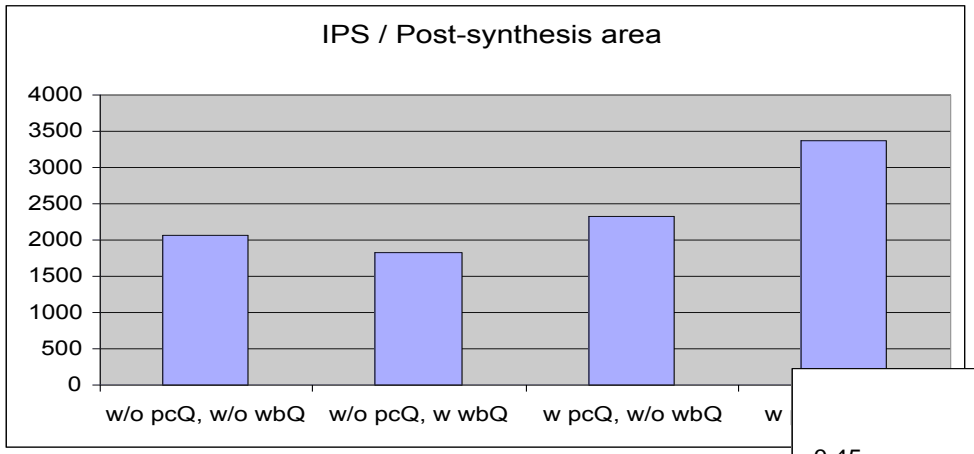


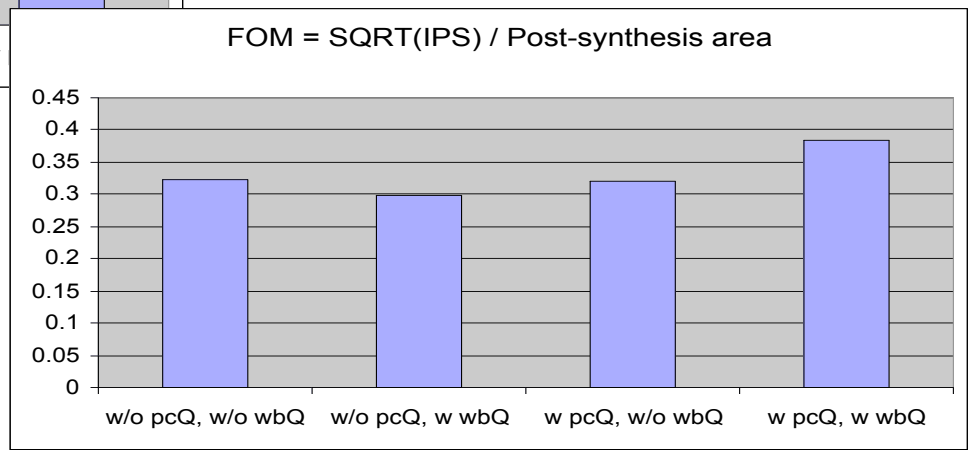

non-EHR RegFile




EHR RegFile

# Performance/Area Tradeoffs




$$FOM \propto \frac{IPS}{Area \times Power}$$

# Conclusions

- Task-specific, customizable and flexible processor design
- User-defined parameter controls degree of parallelism / number of stages
- Each configuration optimized for area and performance
- Balanced tradeoff between configurations