Data Movement Control on a PowerPC

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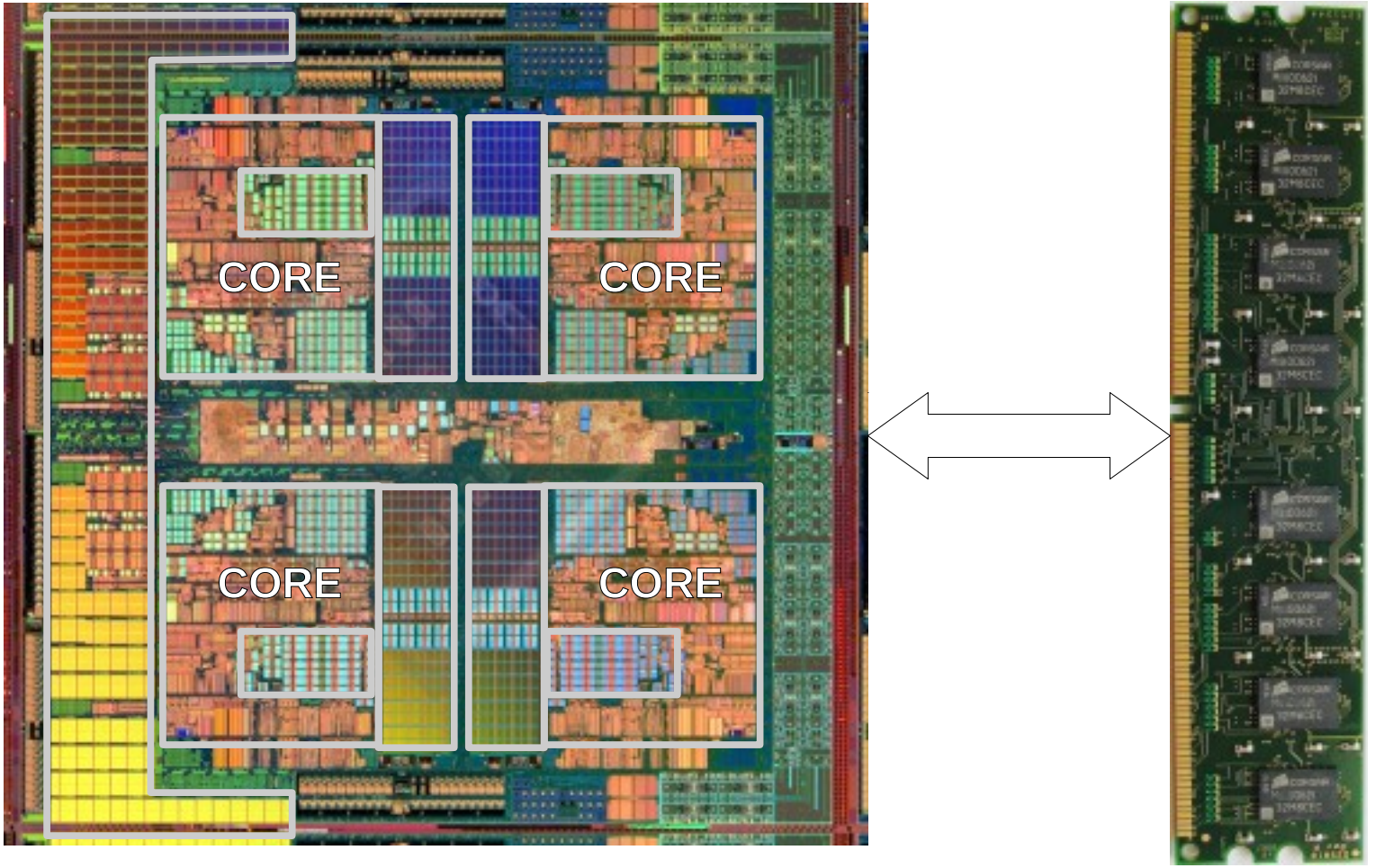
What this presentation is about

- Intuition for why multicore caches are underutilized
- Preliminary design for three new instructions
  - Toy benchmarks show improved performance

Caches are crucial for performance



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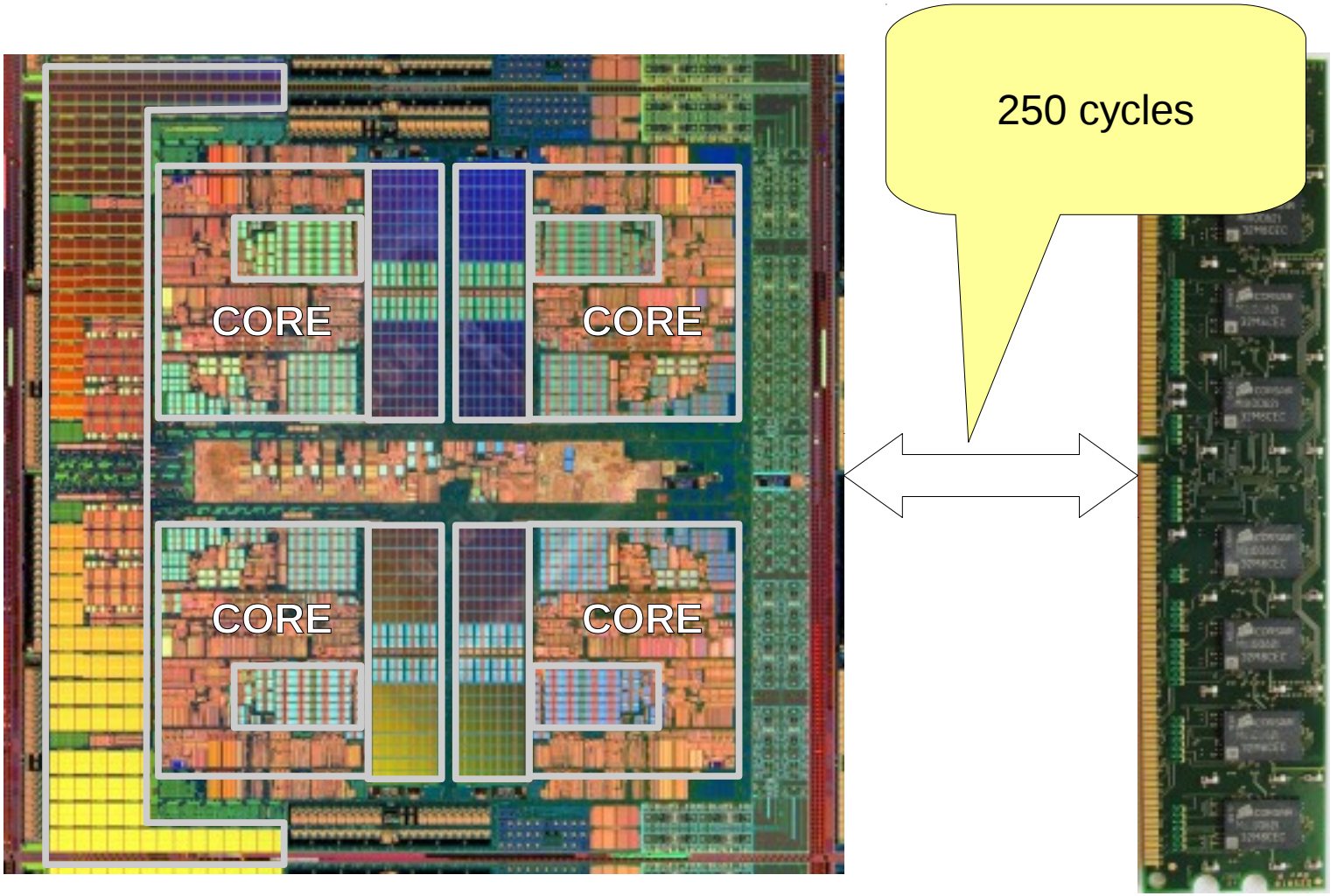
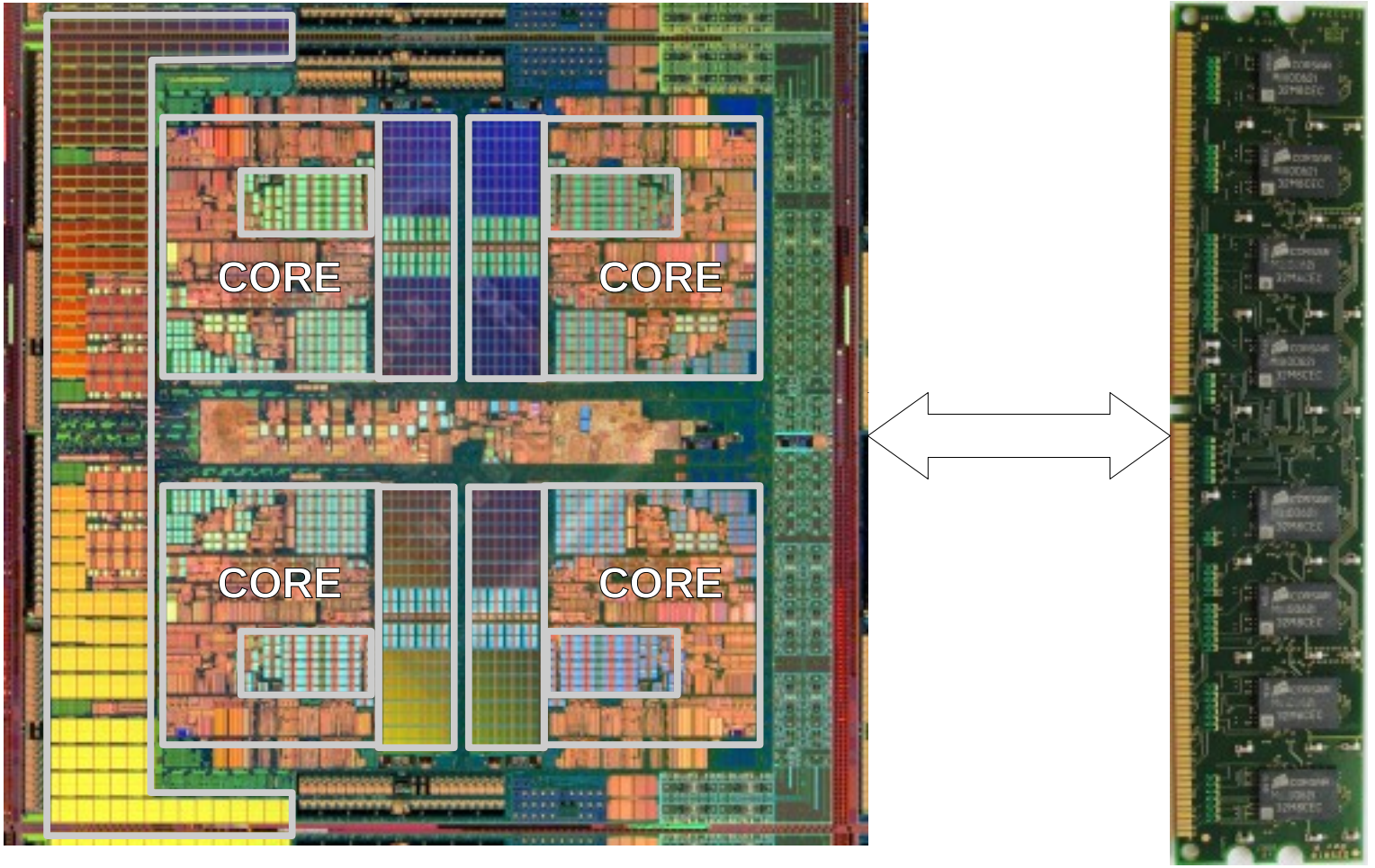


Potential solution is one giant shared cache



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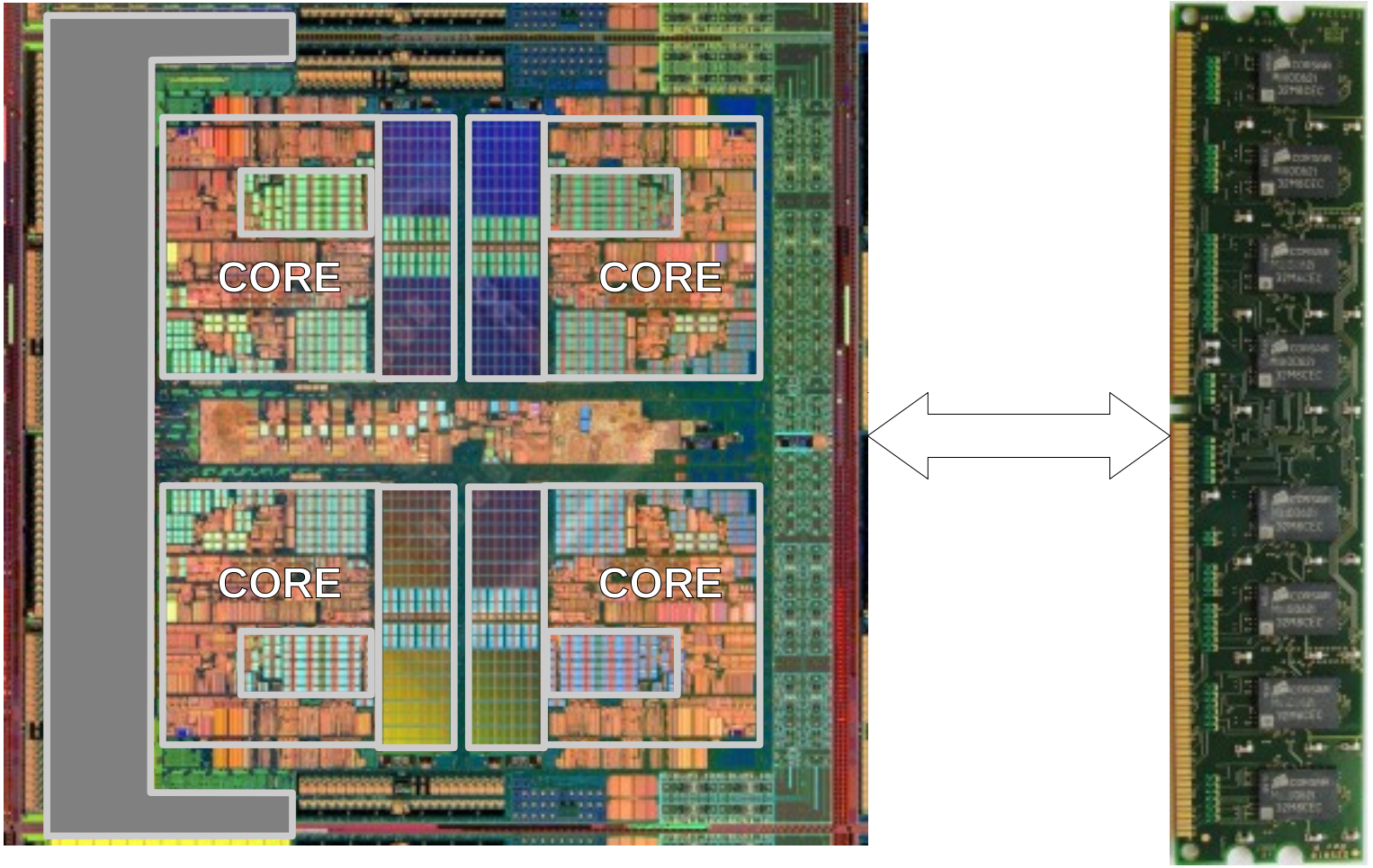

- Applications have access to entire cache capacity, no false sharing issues, etc.

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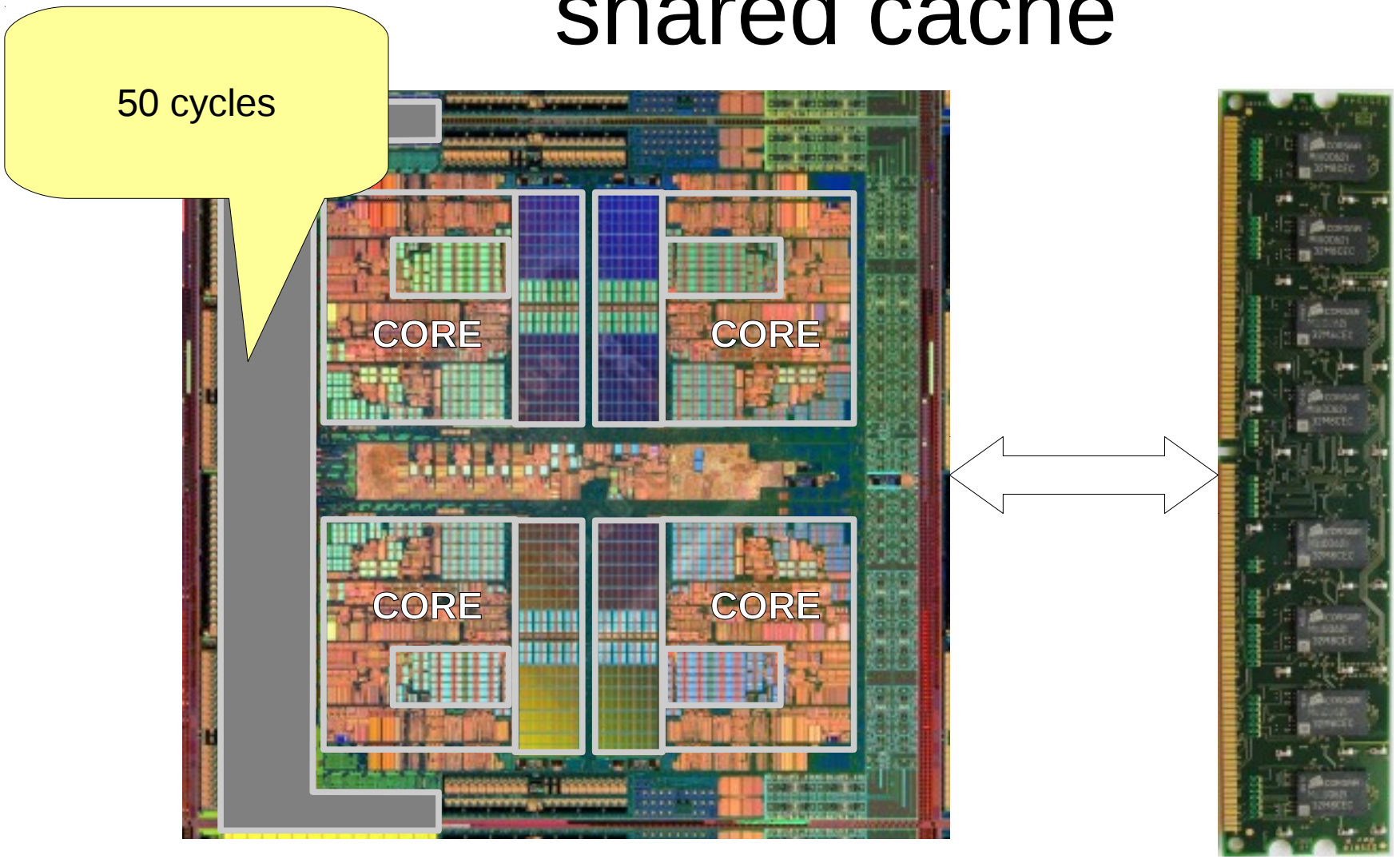

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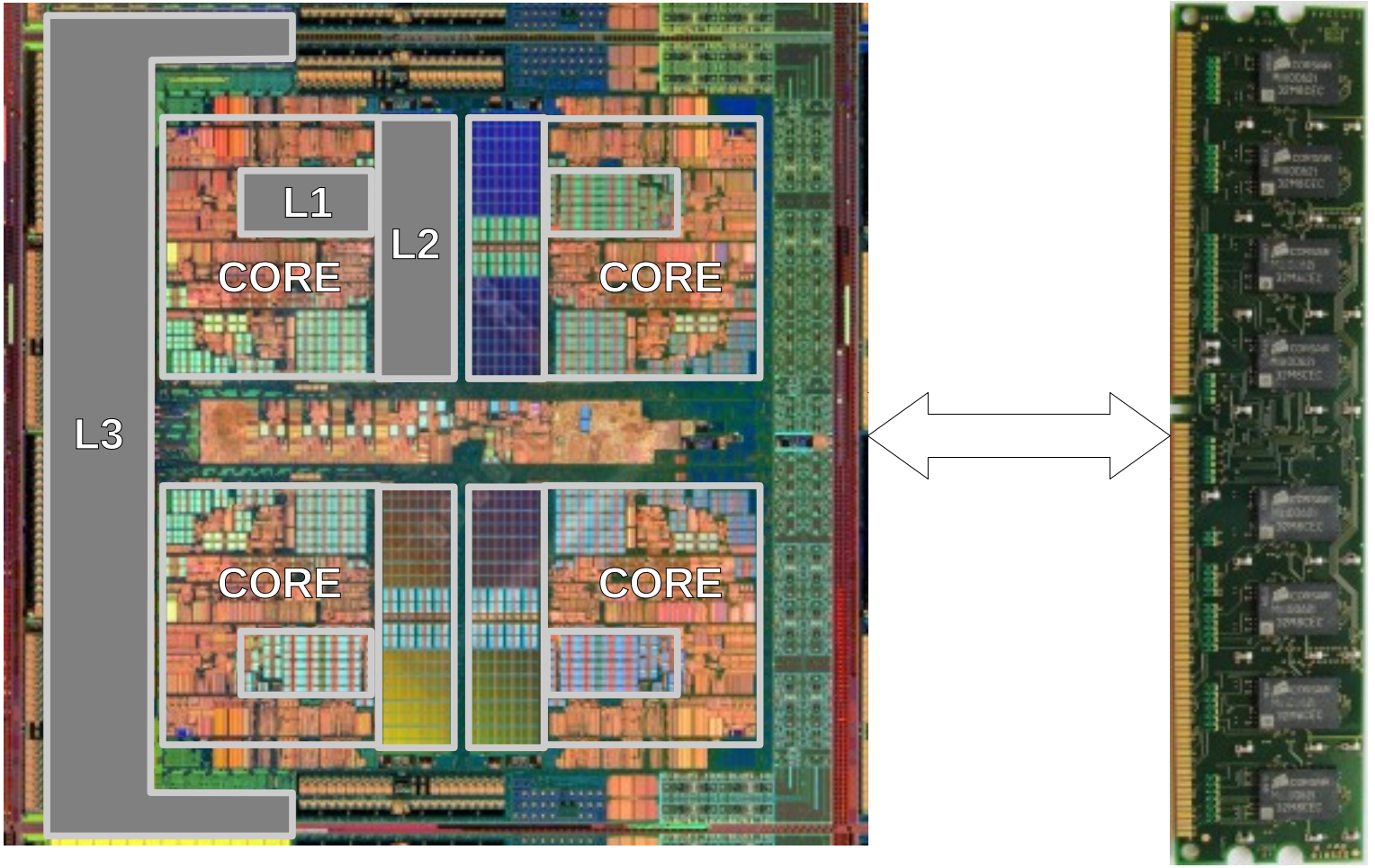
Multicore caches are distributed



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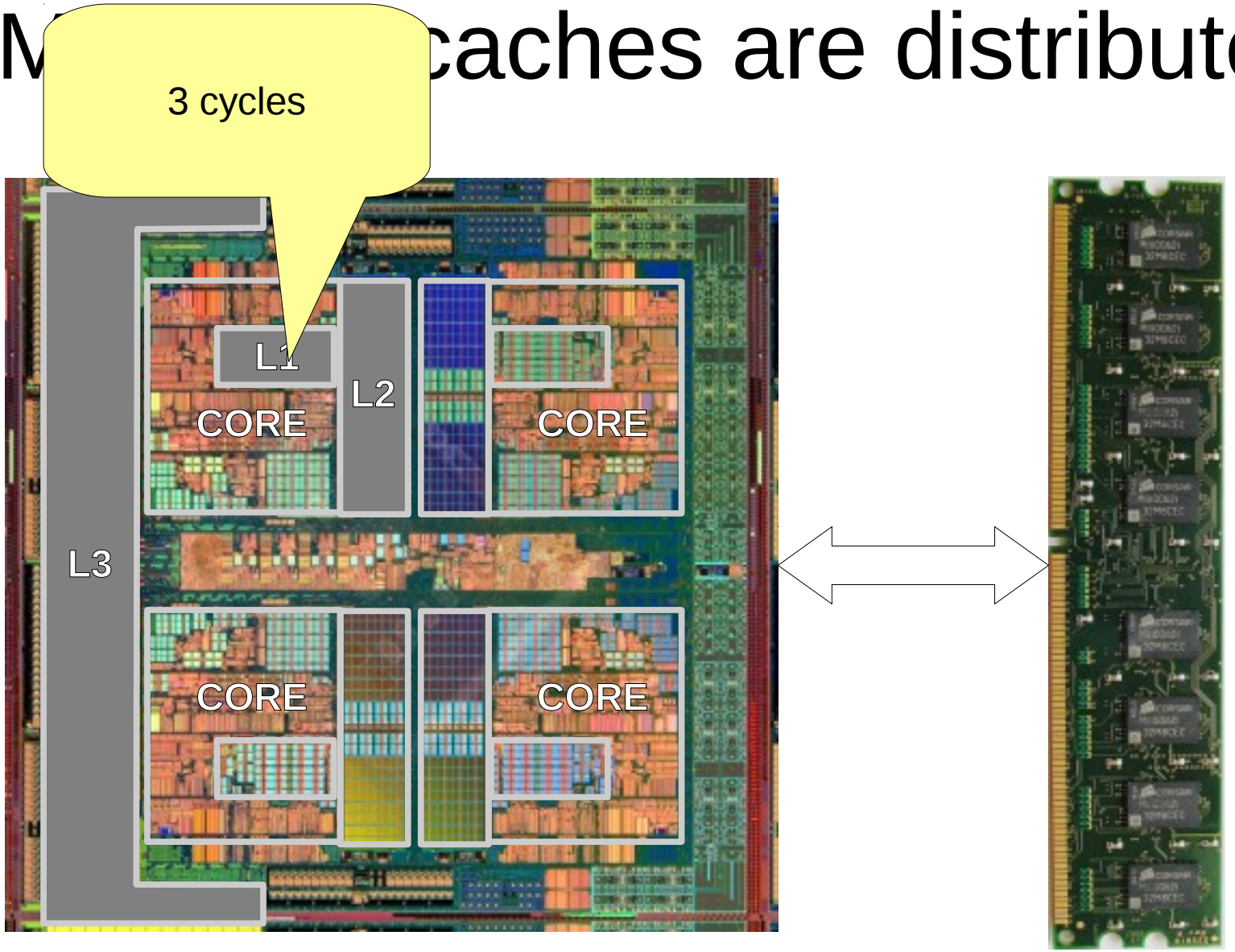

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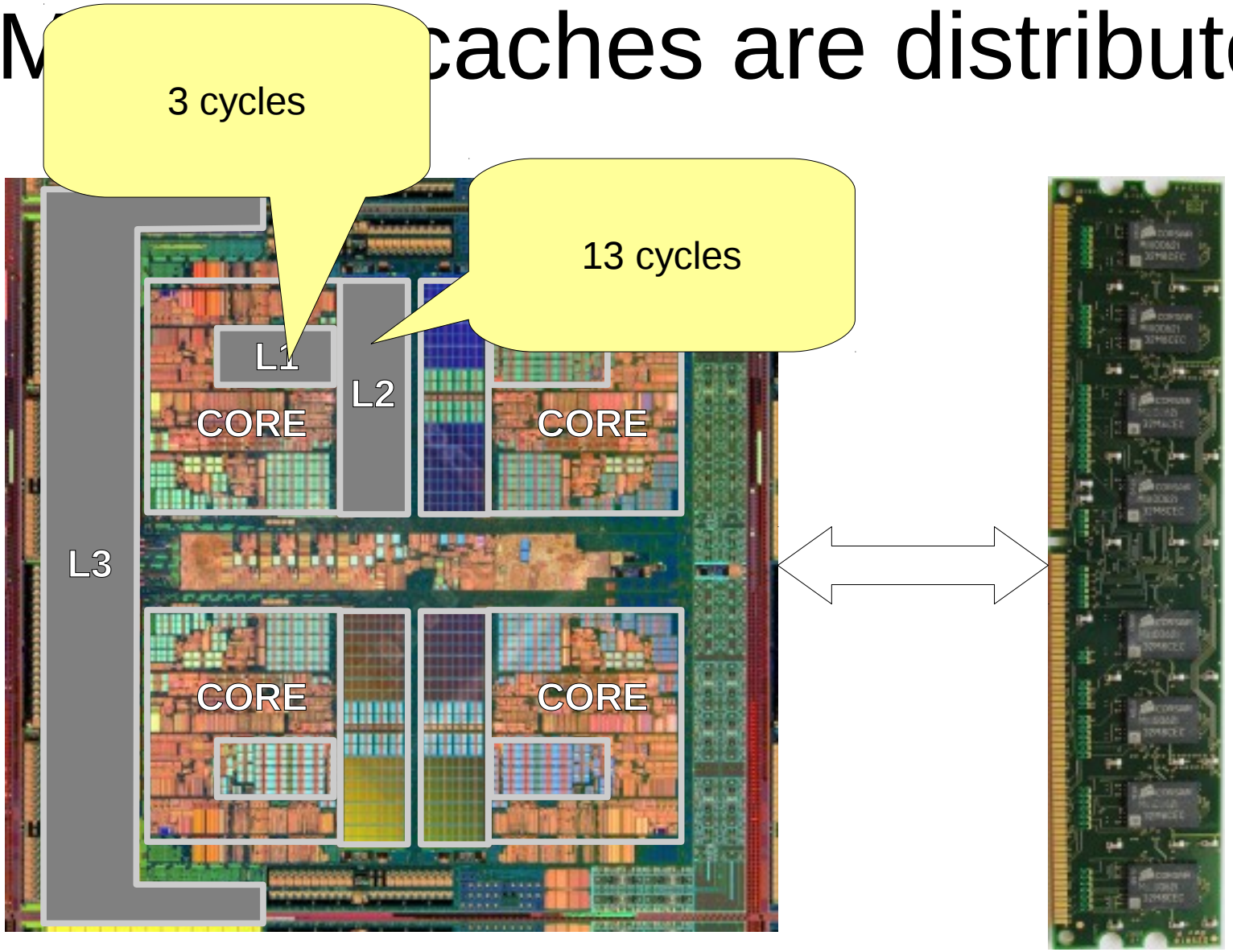

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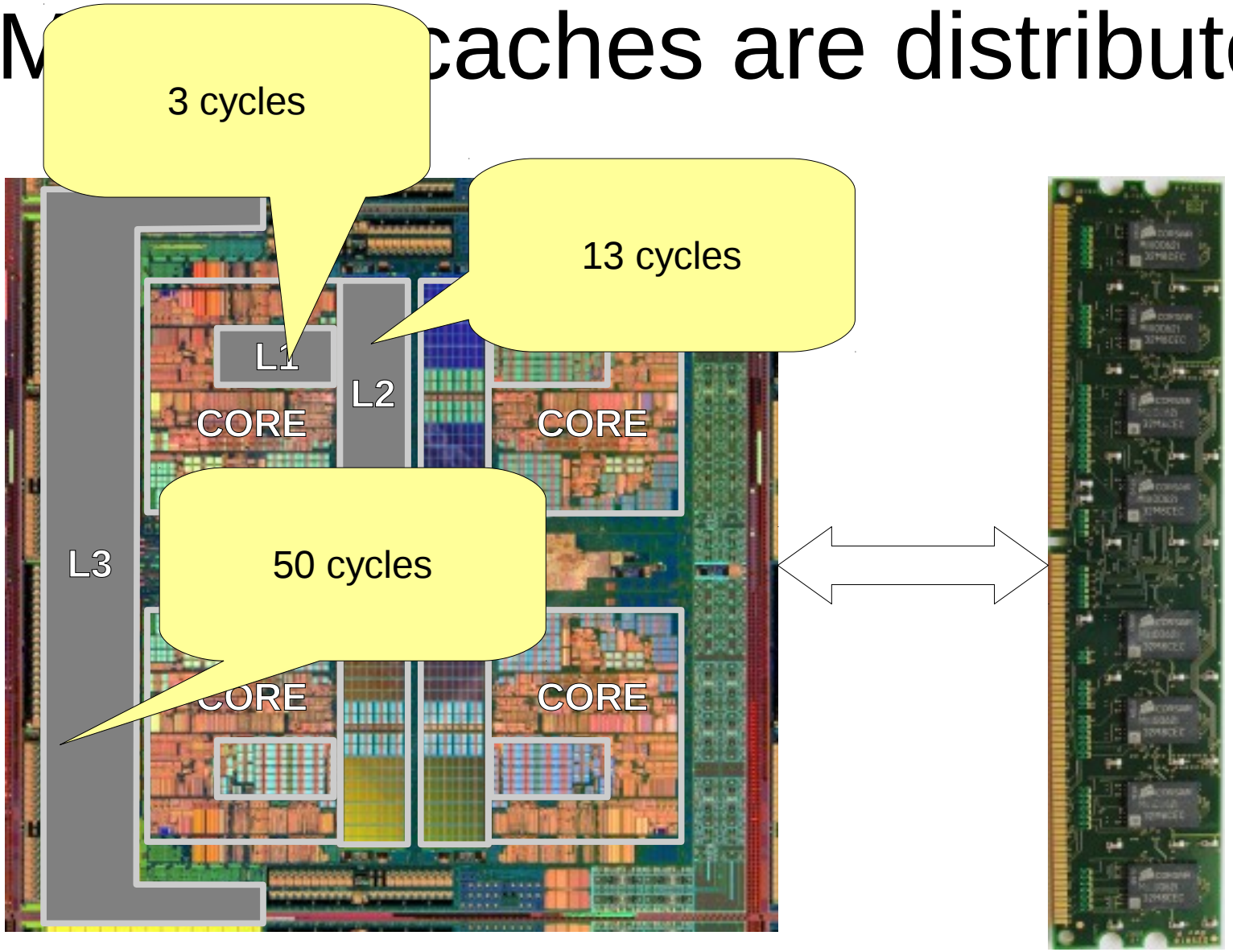
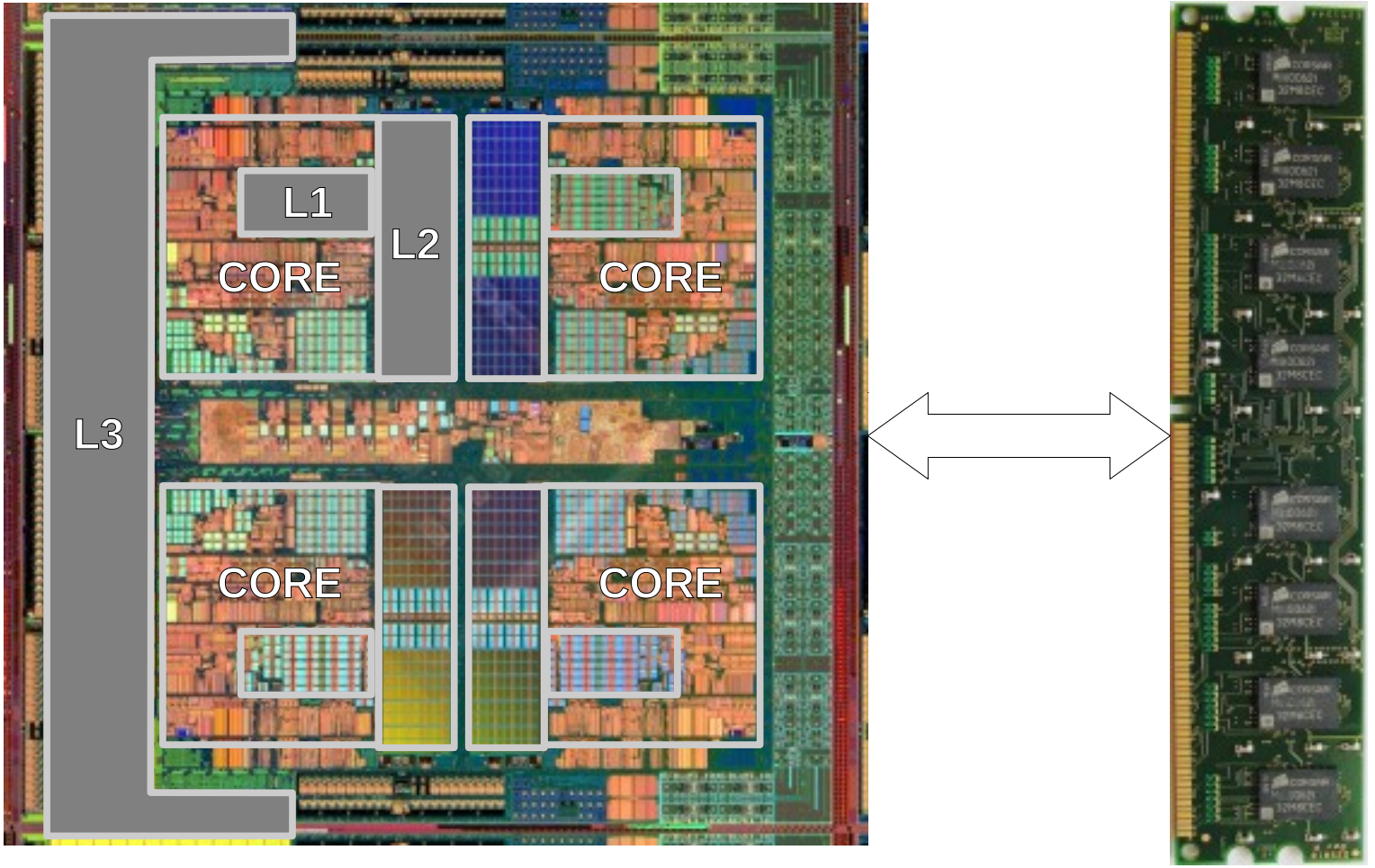
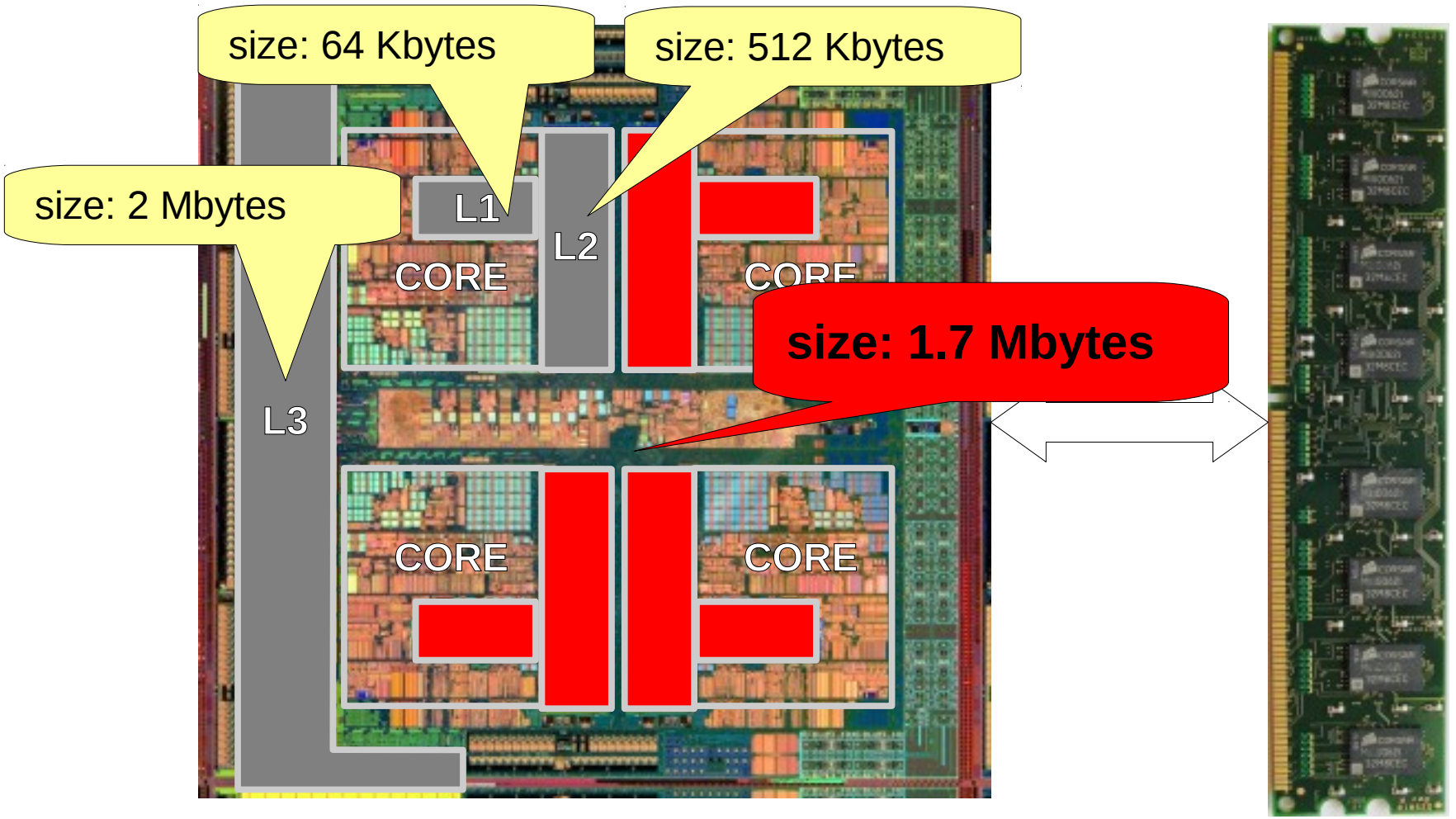


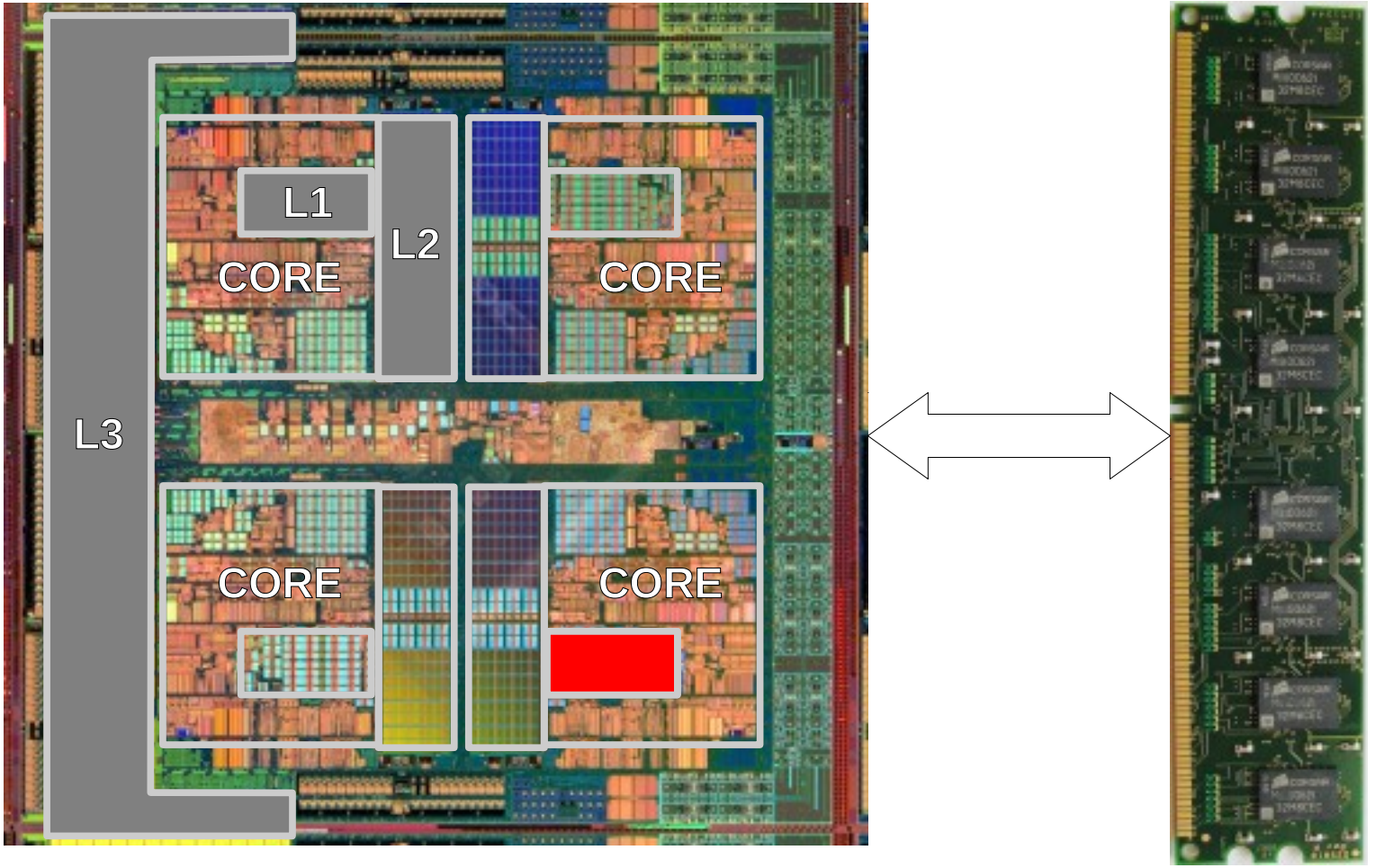
Difficult to use multicore caches efficiently



Hard to access all of on-chip cache



Expensive to access far away caches



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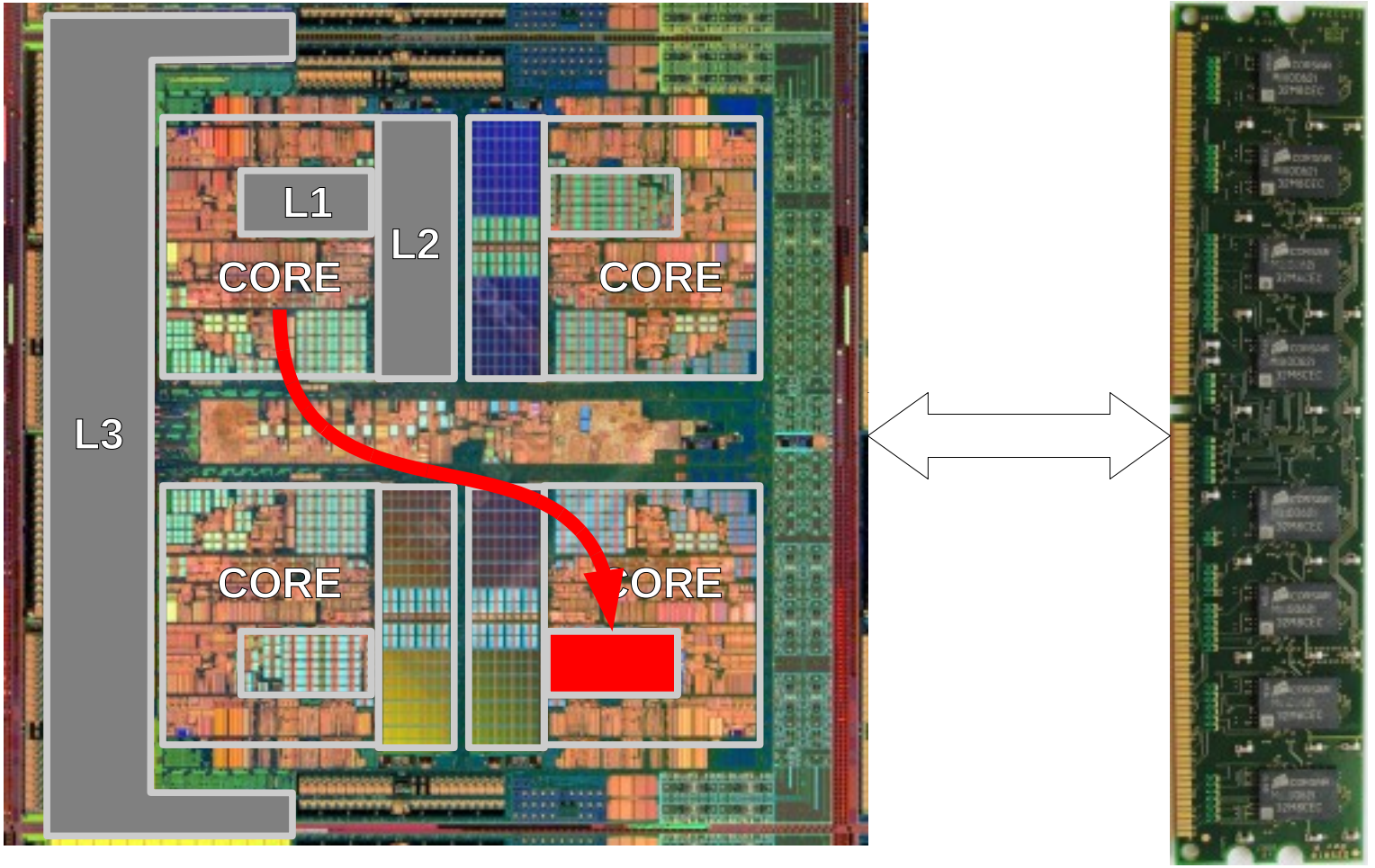

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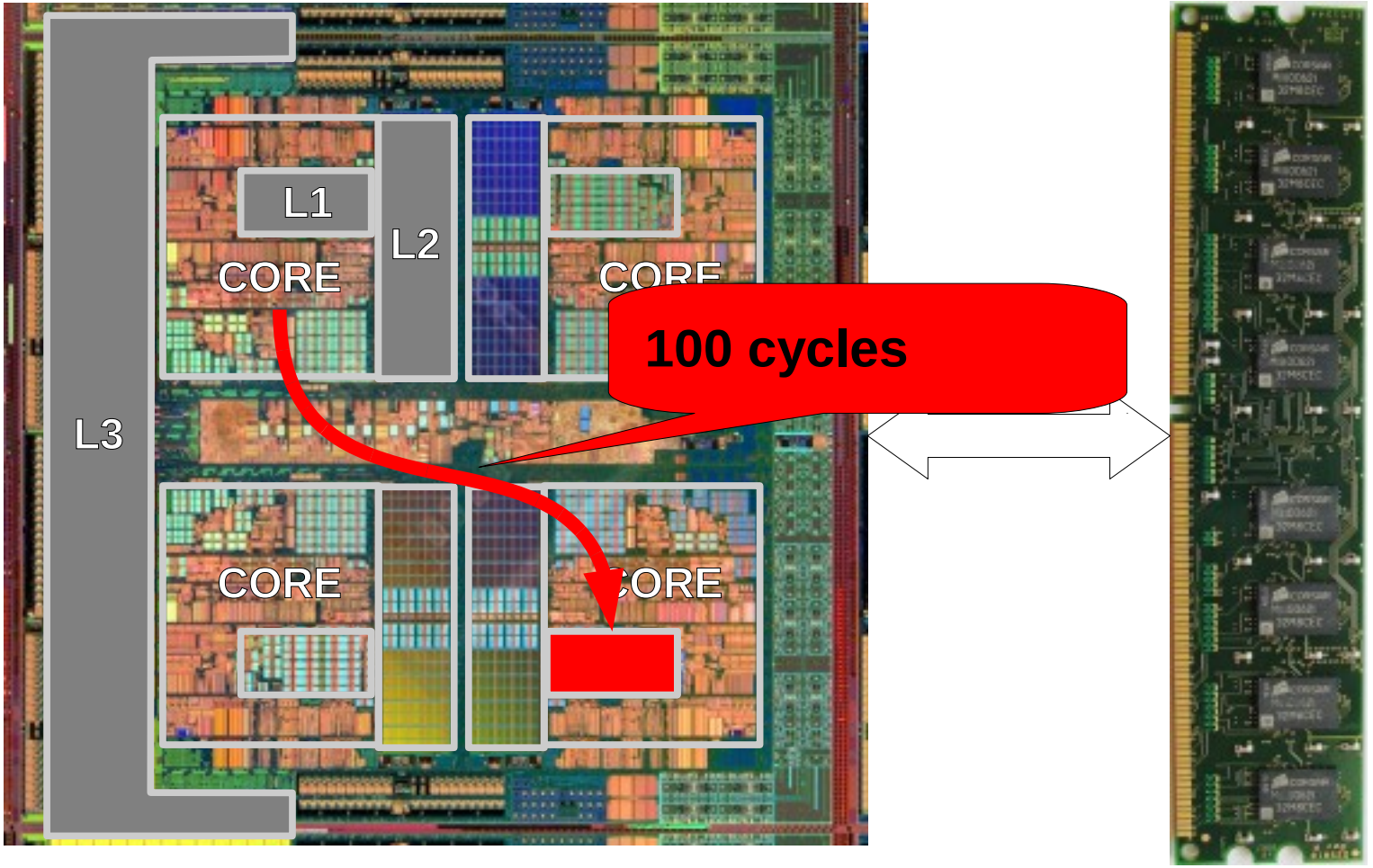

Prototype extensions to hardware: DMC instructions

- `cpush`: store a cache line in another core's cache
- `clookup`: lookup which cache holds an address
- `cmsg`: efficient access to data in another core's cache

- Provide some of the benefits of a single fast shared cache

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Memory hierarchy

- Per-core L1 caches
- Inclusive shared L2
- MSI cache coherence protocol

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- If `address` is marked S in source L1, copy to destination, and mark S.
- If `address` is marked M in source L1, set source copy to I, copy to destination, and mark M.
- If `address` is marked I in source L1, ignore

`cpush` example: thread migration

- To migrate thread:
  - source core: saves register values in buffer
  - source core: puts buffer on destination core's run-queue
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  - source core: saves register values in buffer
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- Source core's cache will hold the buffer and thread's working set
- Use `cpush` to move the buffer and thread's working set

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- If `address` is M or S in source L1, return source ID
- If `address` is invalid in source L1, it's marked S or M in L2 directory, return remote ID
- If `address` in invalid in source L1, and invalid in L2 directory, return -1

`clookup` example: cache management run-times?

- Originally implemented `clookup` to help test `cmsg`
- Some software run-times try to manage cache contents.
- Maintain a map from object/address to cache

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  - Inaccurate
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- Some software run-times try to manage cache contents.
- Maintain a map from object/address to cache
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- Replace software map with `clookup`

`cmsg`: efficient access to data in another core's cache

- `cmsg address, pc, argument`
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Cost roughly equivalent to L2 cache miss, or ½ the cost of inter-core miss

`cmsg` example: shared data structures

- Many applications used shared data structures
- E.g. Linux uses linked lists in many subsystems

```
do_something:
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Three cache misses:
`list_entry`
`list_entry->next->prev`
`list_entry->prev->next`

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- Source calls cmsg(lock, do_something) and destination calls cmsg(sourceId) to reply
  - About the cost of one inter-core cache miss

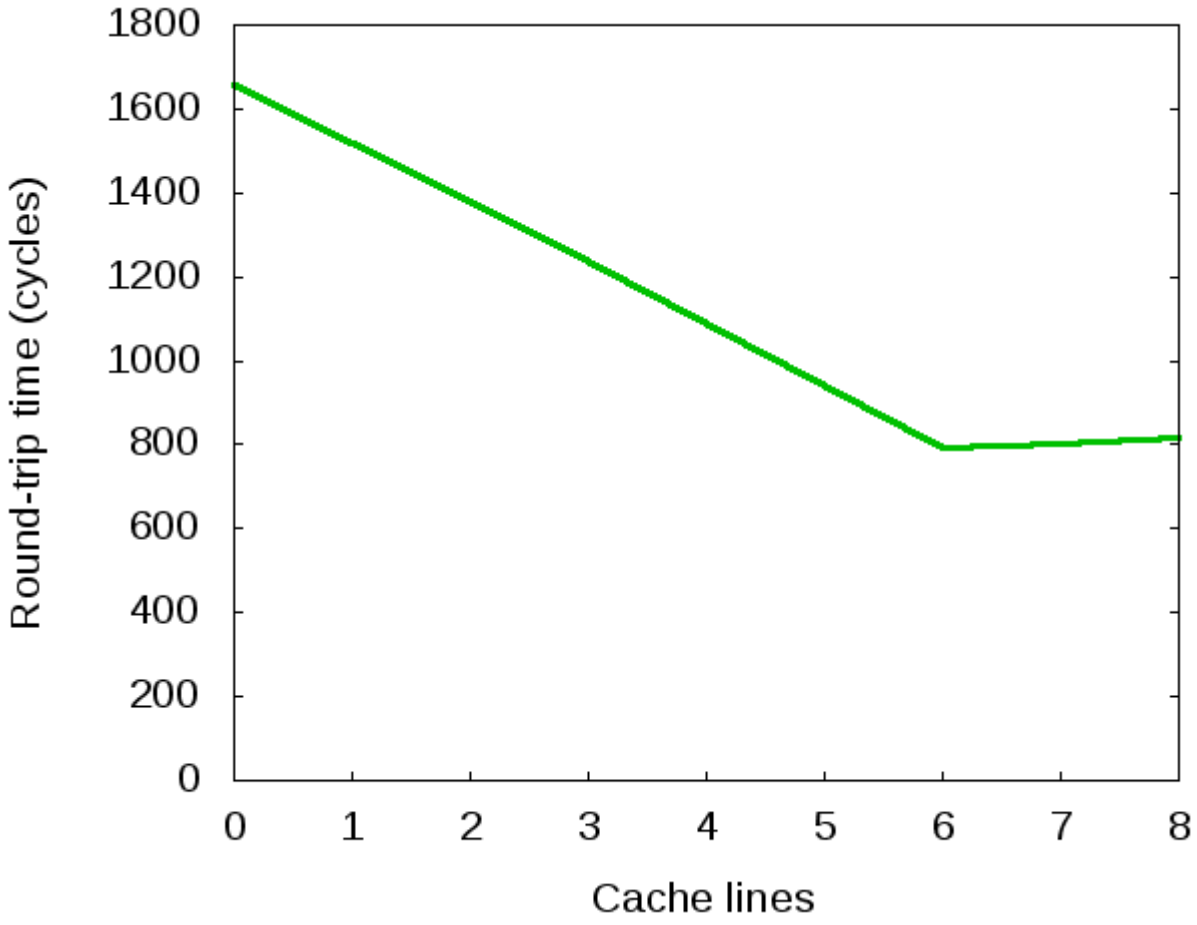
DMC implementation

- Modified an existing PowerPC implementation
  - Runs as on an FPGA as a cycle accurate simulator
  - FPGA is important
- Added/modified about 1000 lines of BSV
- Wrote a software run-time in about 2000 lines of C for testing and benchmarking

Preliminary evaluation

- Can software improve performance using DMC instructions?
  - Thread migration benchmark
  - List manipulation benchmark
- Dual core, L2 access 31 cycles, DRAM access 255 cycles
- Caveats: no hardware pre-fetching, no SMT, etc.

`cpush` improves thread migration performance



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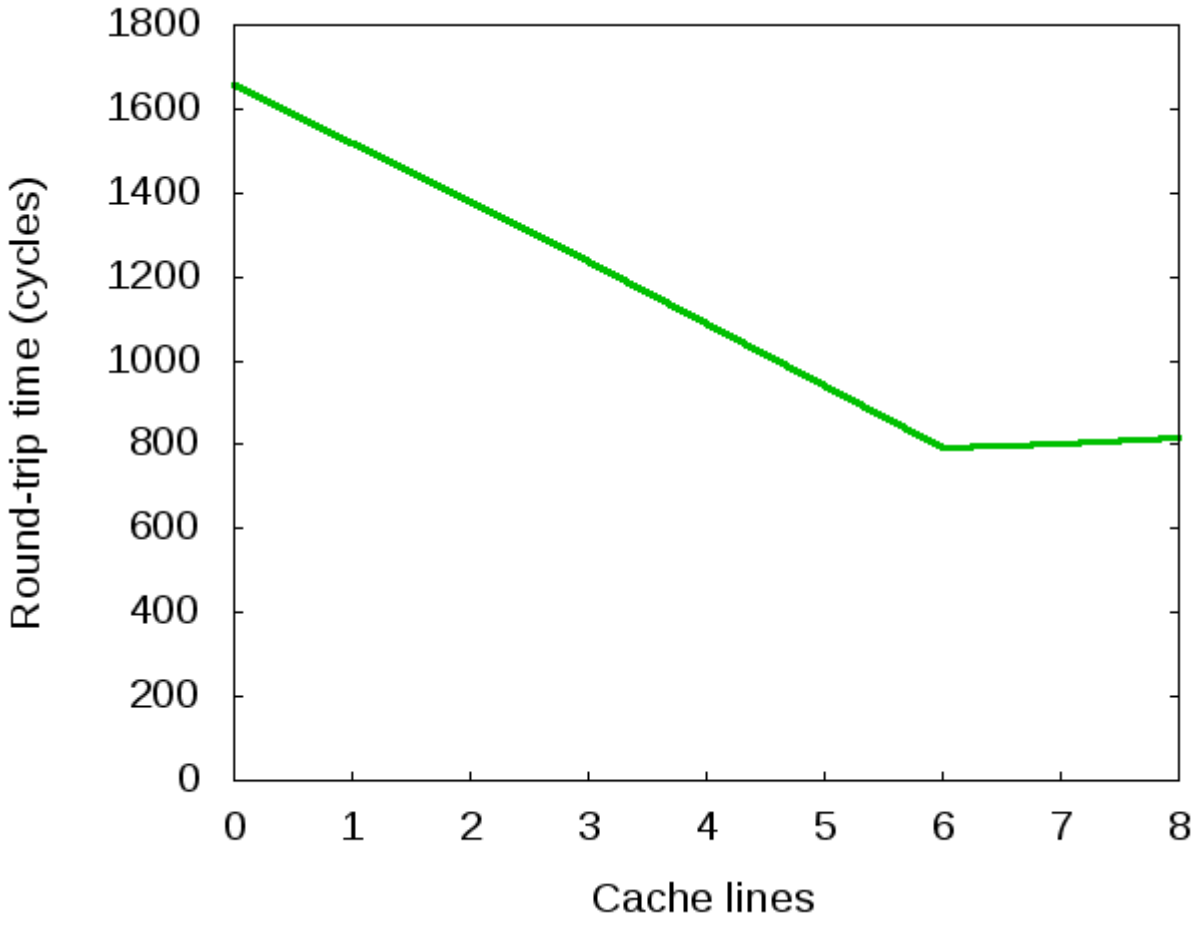
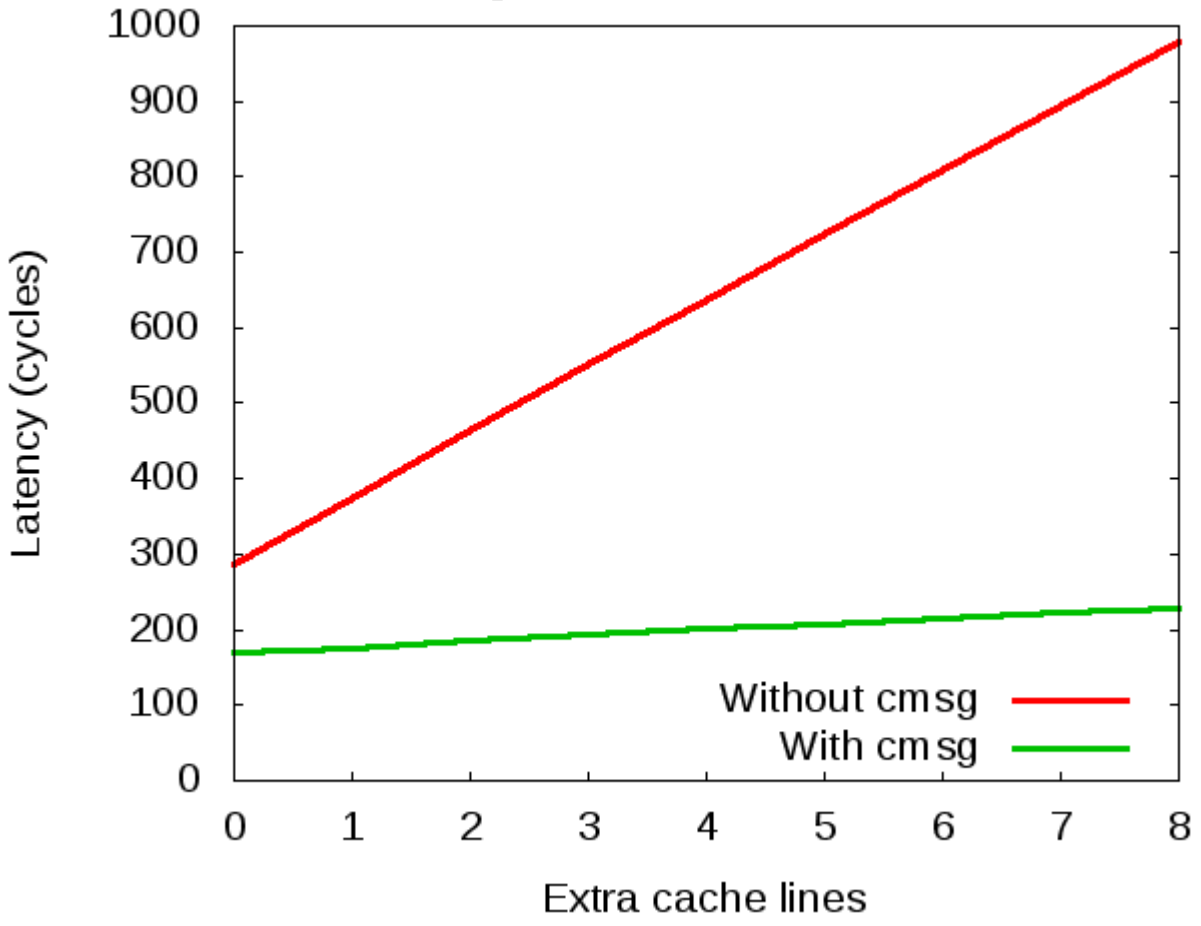


- Pushing 6 cache lines cuts latency in half
- For more the 6 the messages FIFOs fill up

`cmsg` improves the performance of list operations



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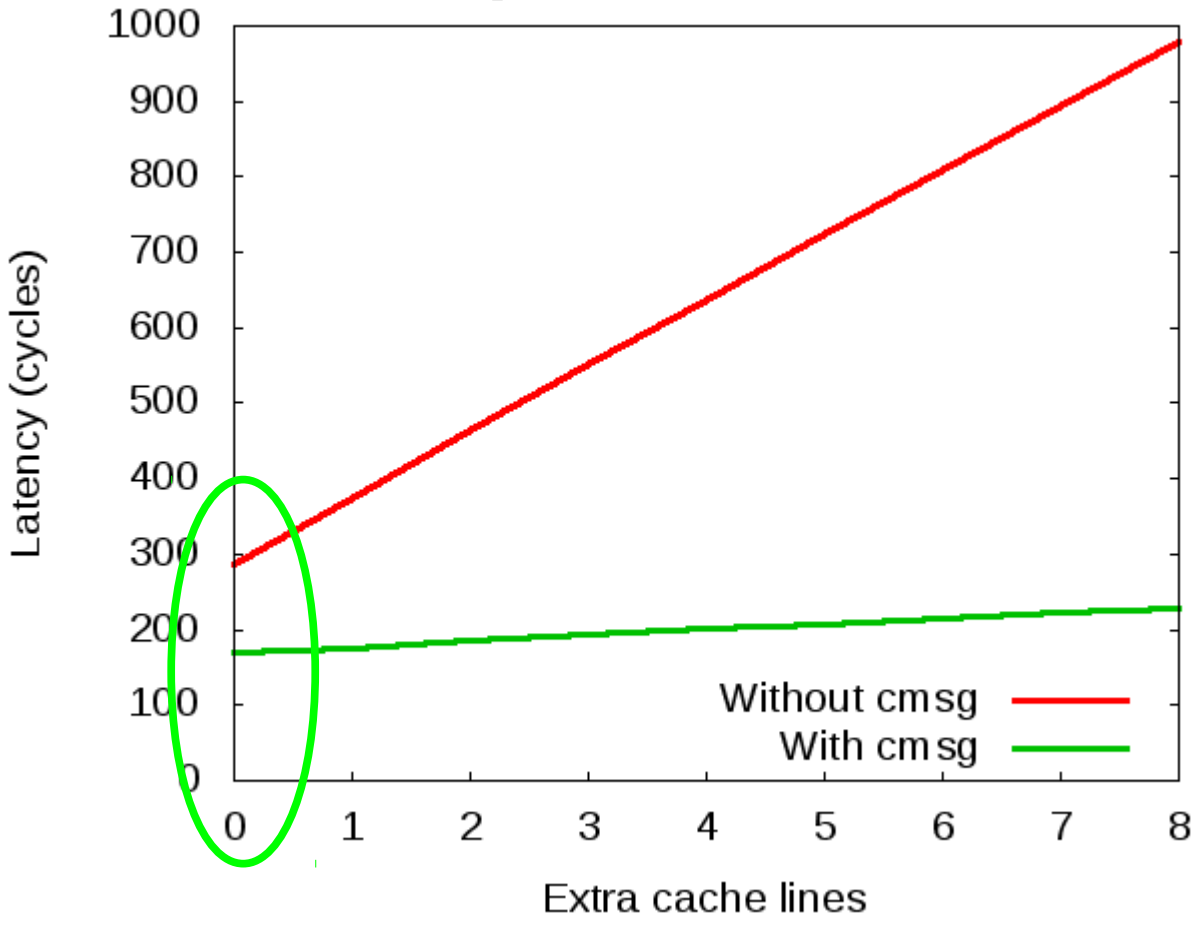

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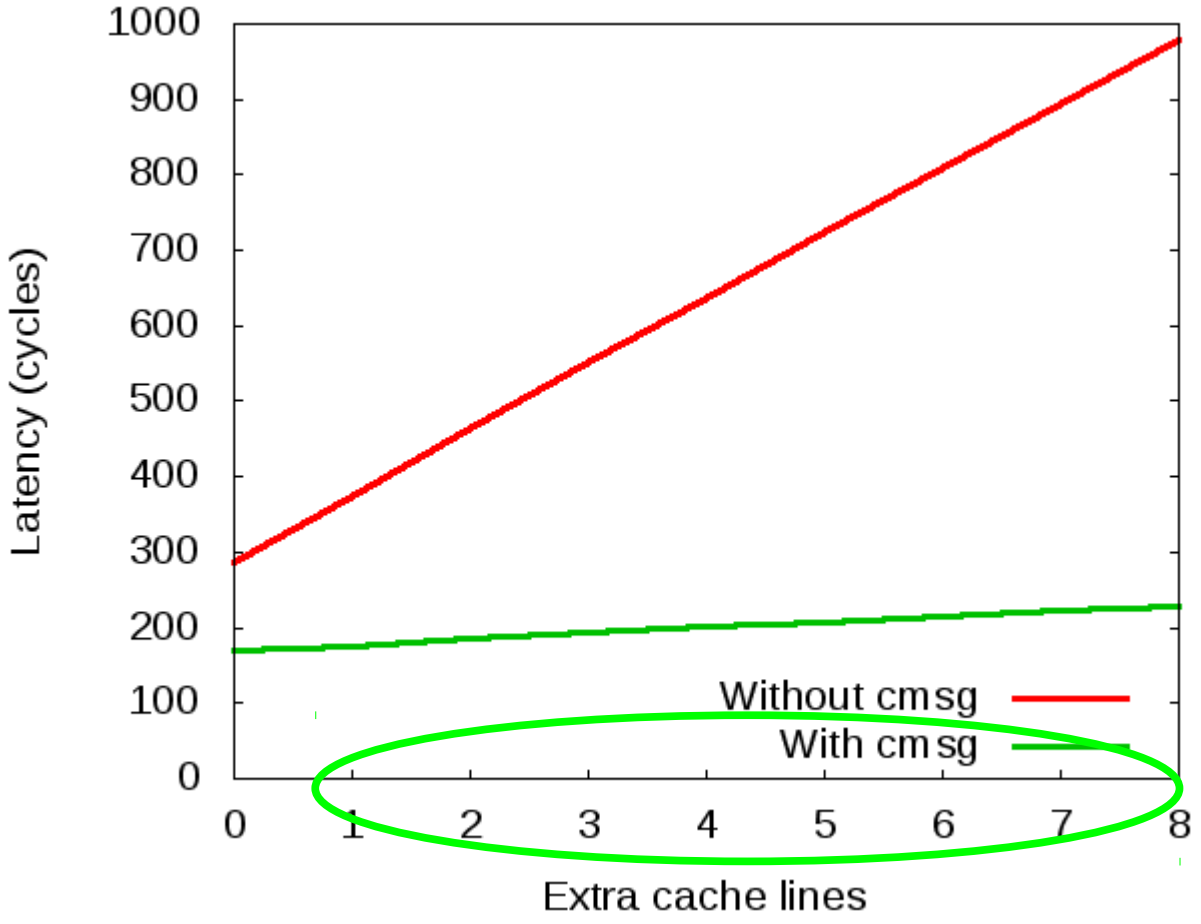

- Reduce update latency by ½
- More benefit as benchmark updates more meta-data

Future work

- `cmsg` loose ends
  - How to handle multiple address spaces?
  - How to deal with fairness?
- When shouldn't applications use DMC instructions?
- Experiment with real applications

Related work

- Managing multicore caches
- Computation migration systems

Conclusion

- Three new instructions (`cpush`, `clookup`, and `cmsg`) for managing cache contents
- Promising preliminary results
- Next step: generalize to real workloads