

6.375 Spring 2013 Final Project

1 Introduction

The second half of the 6.375 course is devoted entirely to final projects. Groups of two to three people will work together to design and implement a complex digital system involving an FPGA.

Groups will be assigned a graduate student mentor. In place of lectures we will have weekly group meetings involving the group members, mentor, TA, and Arvind. You are responsible for preparing progress reports for each meeting leading up to a final report, presentation, and demonstration of the working design on an FPGA.

This document describes the deliverables and milestones expected of you during the course of the final project. If you fail to keep pace with these milestones, the work required of you at the end of the term will be overwhelming.

2 Deliverables and Milestones

All documents should be submitted by emailing them to both 6.375-staff@mit.edu and your mentor. They should include the group number and names of all group members. Reports must be submitted in the PDF format. Presentations may be submitted in PDF or Powerpoint format.

Reports for weekly meetings should be submitted the day before the meeting. This will allow your mentor, TA, and Arvind enough time to review the reports before the meeting. It is important you submit your reports in a timely fashion, because we have many of them we need to review before the meetings start. Weekly meetings are held in Arvind's office, 32-G866.

Figure 1 summarizes the schedule.

Preliminary Proposal

Monday, March 18

An approximately one page description of your project idea is due. Include the problem you would like to solve and the benefit of solving or modeling the problem on an FPGA.

If you have already formed a group, submit one preliminary proposal for the group. It is not required you have formed a group by this point, but we encourage you to advertise your final project

Week	Date	Deliverable
0	Monday, March 18	Preliminary Proposal
0	Wednesday, March 20	Project Idea Presentation
1	Week of April 1	Final Proposal, High-Level Design and Test Plan
2	Week of April 8	Microarchitectural Description
3	Week of April 15	Implementation Status and Planned Exploration
4	Week of April 22	First Synthesis Results
5	Week of April 29	Simulation Demonstration
6	Week of May 6	FPGA Demonstration
7	Wednesday, May 15	Final Report, Final Presentation

Figure 1: Schedule of Deliverables

ideas to other students before the preliminary proposal is due. You may use the class mailing list (6.375-students@mit.edu) or piazza for this purpose.

Projects should consist of complex digital designs which use an FPGA in some meaningful way. The course website has a list of past years' projects you can use for inspiration in coming up with your project idea.

Experience has shown the best projects are those which are well defined at the start. Having existing reference code, infrastructure, tests or benchmarks you can leverage allows you to quickly focus on the design aspects of the project, which are the most interesting. For example, a project based on the SMIPs processor used in the labs comes with a compiler toolchain, assembly tests, benchmarks, and working infrastructure for running them.

A project to implement an architecture for a personally conceived functional assembly language may not be such a good idea, because you will have to invest a massive amount of work defining the language, implementing a compiler, assembler, coming up with and writing your own tests and benchmarks, and ultimately you may find a flaw, not in the design of your implementation, but in the definition of the system itself. There will be plenty of opportunity to exercise your creativity in the design of the implementation of your project without having to fight such issues.

For domain specific projects you will need to be familiar with the domain and specific application. If you are not already familiar with the domain, you should be prepared to learn it. You must have a solid understanding of the application by the first week of the project.

Project Idea Presentation

Wednesday, March 20

Give a brief presentation in class of the project idea you described in your preliminary report. This should be no more than 5 minutes in length, and not more than one or two slides. You should email your slide(s) to 6.375-staff@mit.edu before class starts to facilitate smooth transitions between presentations.

We will give feedback on the project ideas as presented in the preliminary proposals and these short presentations during the class period. After all the presentations have been given, we will help to finalize the groups and projects to ensure everyone belongs to a group with an interesting project.

Final Proposal, High-Level Design and Test Plan

Week 1

The day before your weekly meeting a report including your final project proposal and high-level design and test plan is due.

The project proposal should discuss the problem you are trying to solve, any background needed to understand the problem, and the benefit of solving or modeling the problem on an FPGA. This will be an expanded version of your preliminary proposal, and should take into account the feedback we gave on your preliminary proposal.

The high-level design and test plan should give a high level description of the design. This should include how you propose to provide inputs and retrieve outputs from your design and how you can verify the design works as expected. System diagrams will be very helpful.

The final proposal and high-level design and test plan together, with figures, should be around 3-5 pages.

In the meeting we will discuss the high-level design and test plan.

Microarchitectural Description

Week 2

The day before your weekly meeting an updated report including appropriate revisions to your previous report and a microarchitectural description is due.

The microarchitectural description should describe the detailed design of your implementation. Include descriptions of each of the modules you expect to use in your design, including their interfaces and functionality. Also include how your design will interact with the host processor. This should be completed before you begin implementing your design.

In the meeting we will discuss your microarchitecture.

By the end of this week you should have a clear understanding of how everything required by your design can be implemented in hardware.

Implementation Status and Planned Exploration

Week 3

The day before your weekly meeting an updated report including appropriate revisions to your previous report, the current status of your implementation, and planned exploration is due.

The implementation status should include what you have implemented so far, and what problems, if any, you have encountered.

The planned exploration should describe what exploration you plan to perform once you have a working system. What trade-offs are you interested in exploring?

In the meeting we will discuss your implementation progress and design exploration plan.

By the end of this week you should have a substantial portion of your design implemented and working. If you have bits flowing end to end, you are doing well.

First Synthesis Results

Week 4

The day before your weekly meeting an updated report including appropriate revisions to your previous report, the current status of your implementation, and first synthesis results are due.

First synthesis results should include the area and critical path of as much of the design you have implemented so far, even if the design is not yet correct in simulation. While you should debug your design in simulation before trying to get it to work on the FPGA, it is important to try synthesizing before that to learn if you need to redesign your system because something has a long critical path, takes up too much area, or otherwise will not work on the FPGA.

In the meeting we will discuss your implementation progress.

By the end of this week you should have bits flowing end to end in simulation.

Simulation Demonstration

Week 5

The day before your weekly meeting an updated report including appropriate revisions to your previous report and the status of your implementation is due.

Your project should now be functioning correctly in simulation. You should demonstrate your working simulation in the meeting.

In the meeting we will discuss your progress.

If by the end of this week your design does not work in simulation, you are behind, and will need to step up your efforts to getting a working design.

FPGA Demonstration

Week 6

The day before your weekly meeting an updated report including appropriate revisions to your previous report and a status update are due.

Your project should now be functioning correctly on the FPGA. You must schedule a time sometime this week to demonstrate the working design on the FPGA to the TA.

In this meeting we will discuss design explorations to be undertaken.

Final Report

Wednesday, Week 7

The final report is the final version of your weekly reports. It should include the following elements, most of which have already been described.

- Project Objective
- High-Level Design and Test Plan
- Microarchitectural Description
- Implementation Evaluation, Performance
- Design Exploration

The implementation evaluation and performance should include reports on the area, critical path, and performance of your design. Does the performance of your design meet your requirements? What is the limiting factor in the performance?

The final report should be between 10 and 20 pages in length. If you put a reasonable amount of effort into the weekly reports, it should be fairly easy to produce the final report from them.

Final Presentation

Wednesday, Week 7

In addition to the final report, you must prepare and present a final presentation of your project. We will all meet Wednesday, May 15th tentatively from 2:30-6pm and listen to the presentations.

The presentations will be 15 minutes each. Your presentations should clearly convey the problem you were trying to solve, how you solved it, what challenges you faced, and the results of your project.