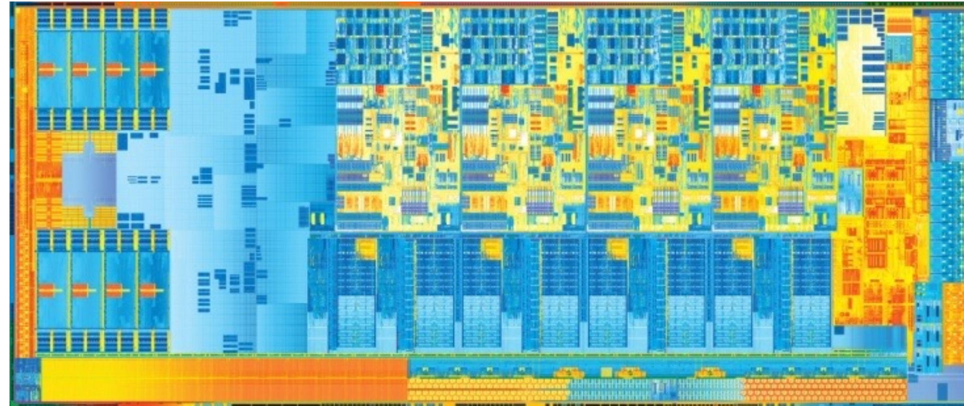
6.5900 Computer System Architecture

Instructors: *Daniel Sanchez*
Mengjia Yan

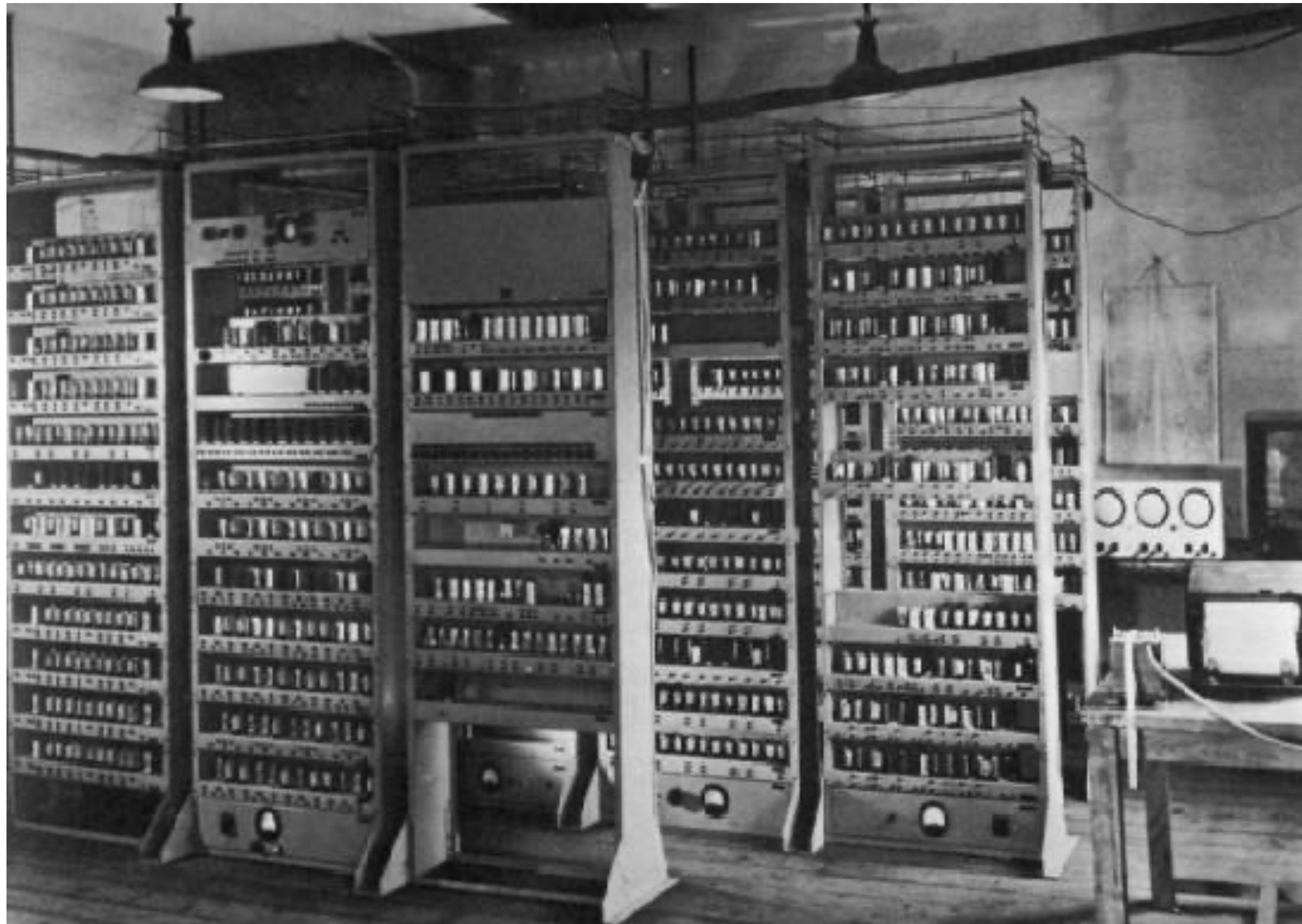
TAs: *Hyung Ryong (Ryan) Lee*
Nikola Samardzic

The processor you built in 6.1910

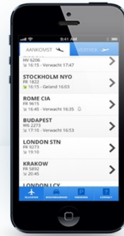


What you'll understand after taking 6.5900

Computing devices then…



Computing devices now



A journey through this space

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- Illustrate via historical examples
  - Early days: ENIAC, EDVAC, and EDSAC
  - Arrival of IBM 650 and then IBM 360
  - Seymour Cray – CDC 6600, Cray 1
  - Microprocessors and PCs
  - Multicores
  - Cell phones

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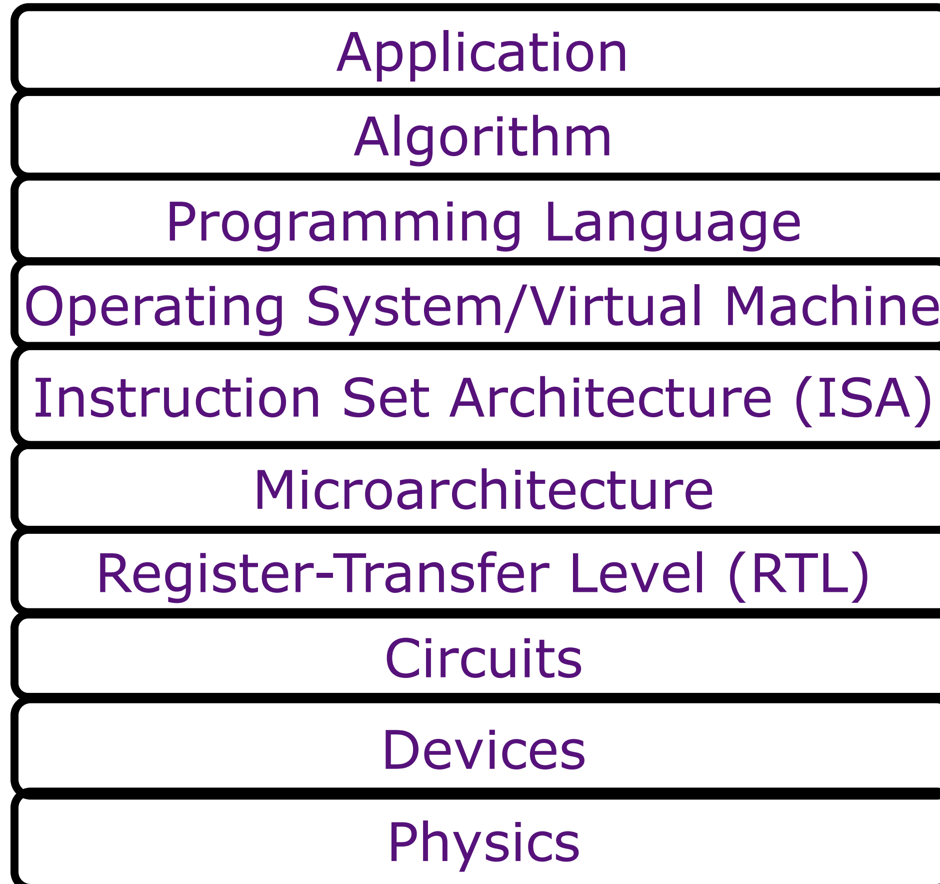
- Focus on ideas, mechanisms, and principles, especially those that have withstood the test of time

Abstraction layers



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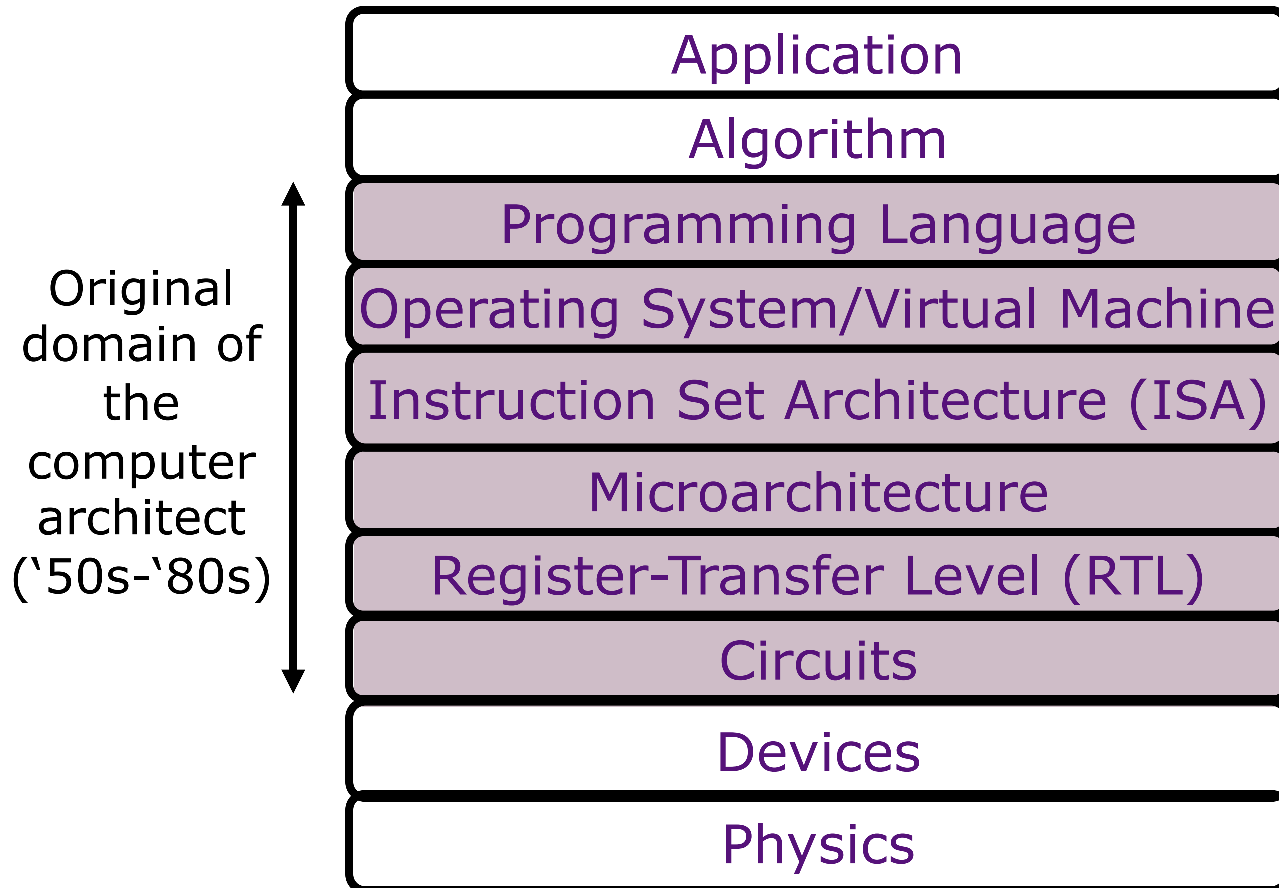

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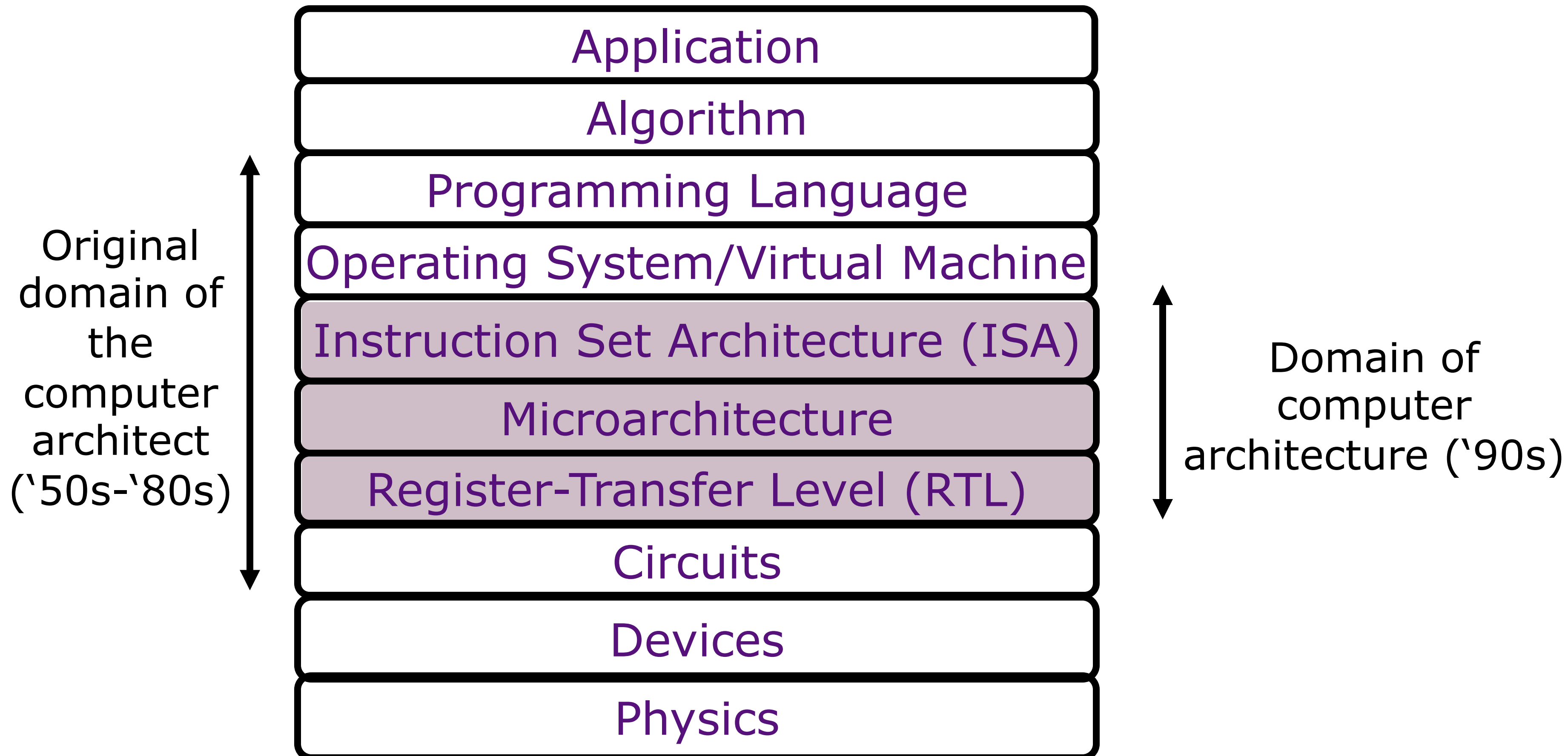

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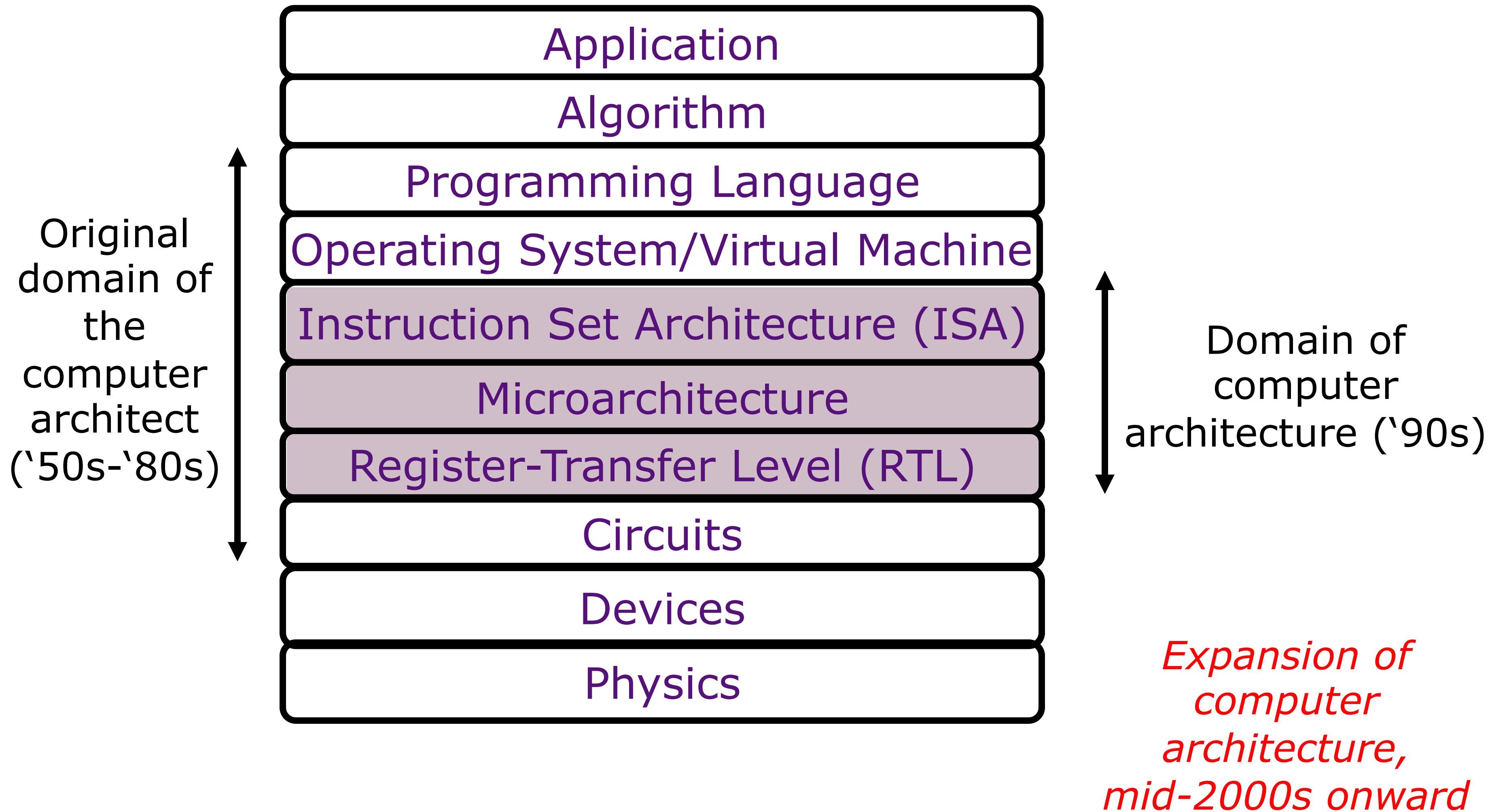

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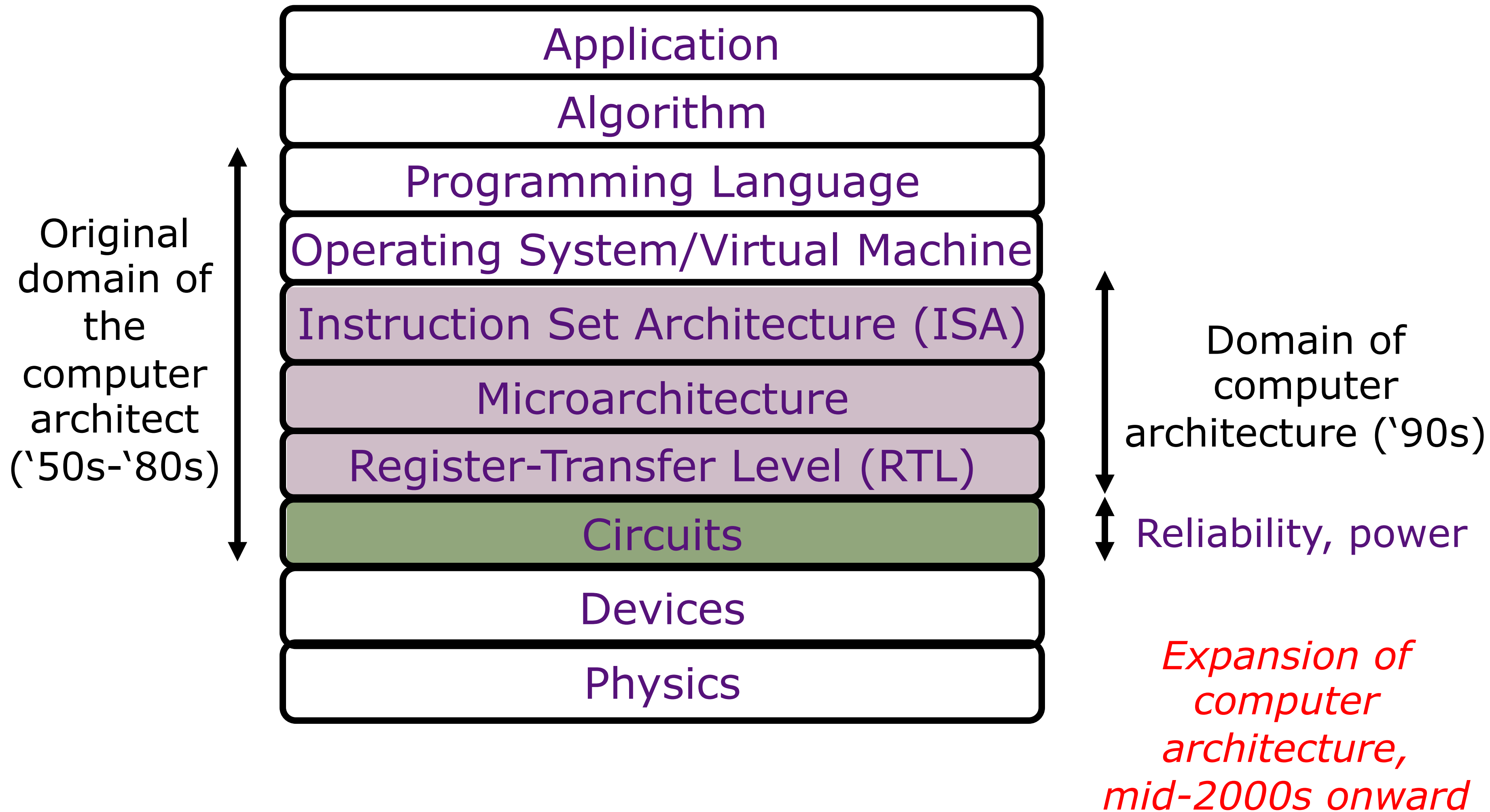

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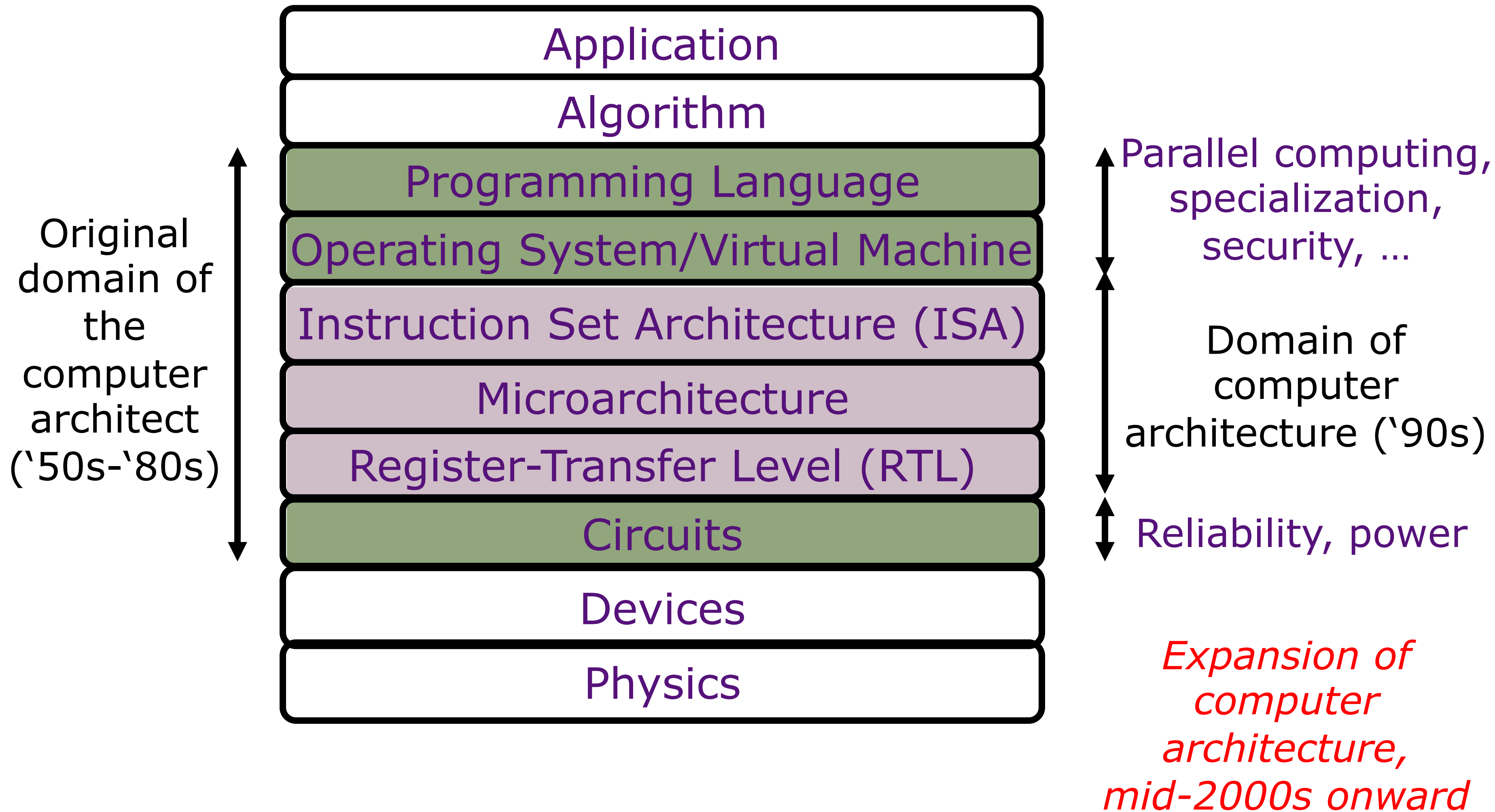

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  - Consistency across a large number of units

- What are the consequences?
  - *Encouragement to create reusable foundations:*
    - *Toolchains, operating systems, libraries*
  - Enticement for application innovation

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Transistors
Integrated circuits
VLSI (initially)
Flash memories, …

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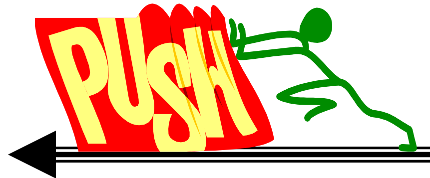
Computers

Technology

Core memories
Magnetic tapes
Disks



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Computers

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- *Magnetic tapes*
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Computers

Technology
- *ROMs, RAMs*
- *VLSI*
- *Packaging*
- *Low Power*

Computers

But Software…

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As people write programs and use computers, our understanding of *programming* and *program behavior* improves.

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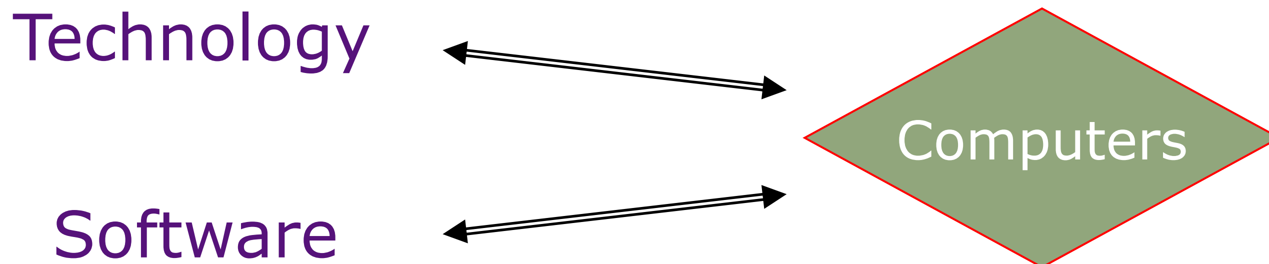

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At different times, and for different applications at the same point in time, the relative balance of these factors can result in widely varying architectural choices

Course Information

All info kept up to date on the website:

http://csg.csail.mit.edu/6.5900

Contact times

- Lectures on Monday and Wednesday
  - 1:00pm to 2:30pm in room 32-141
- Tutorial on Friday
  - 1:00pm to 2:00pm in room 32-141
  - Attendance is optional
  - Additional tutorials will be held in evenings before quizzes
- Quizzes on Friday *(except last quiz)*
  - 1:00pm to 2:30pm in room 32-141
  - Attendance is NOT optional
- Instructor office hours
  - After class or by email appointment
- TA office hours
  - Wednesday 4:00-5:30 pm @ Stata 7th floor lounge

Online resources

- We use Piazza extensively
  - Fastest way to get your questions answered
  - All course announcements are made on Piazza

The course has three modules

Module 1
- ISA and Simple In-Order Pipelines
- Caches and Virtual Memory
- Complex Pipelining and Out-of-Order Execution
- Branch Prediction and Speculative Execution

Module 2
- Multithreading and Multiprocessors
- Coherence and consistency
- On-chip networks

Module 3
- Microcoding and VLIW
- Vector machines and GPUs
- Hardware accelerators
- Hardware security

Textbook and readings

- "Computer Architecture: A Quantitative Approach", Hennessy & Patterson, 6th ed.
  - 5th edition available online through MIT Libraries
  - Recommended, but not necessary
  - NOTE: 6th edition (and 6.5900) uses RISC-V as the main ISA; prior editions (and 6.5900/6.86 offerings) use MIPS

- Course website lists H&P reading material for each lecture, and optional readings that provide more in-depth coverage

Grading

- Grades are not assigned based on a predetermined curve
  - Most of you are capable of getting an A
- 75% of the grade is based on three closed book 1.5 hour quizzes
  - The first two quizzes will be held during the tutorials; the last one during the last lecture (dates on web syllabus)
  - We'll have makeups if needed
- 25% of the grade is based on four laboratory exercises
- No final exam
- No final project

Problem sets & labs

- Problem sets
  - One problem set per module, not graded
  - Intended for private study and for tutorials to help prepare for quizzes
  - Quizzes assume you are very familiar with the content of problem sets
- Labs
  - Four graded labs
  - Based on widely-used PIN tool
  - Labs 2 and 4 are open-ended challenges
- You must complete labs & quizzes individually
  - Please review the collaboration & academic honesty policy

Self evaluation take-home quiz

- Goal is to help you judge for yourself whether you have prerequisites for this class, and to help refresh your memory
- We assume that you understand digital logic, a simple 5-stage pipeline, and simple caches
- Please work by yourself on this quiz – not in groups
- Remember to complete self-evaluation section at end of the quiz
- Due by Friday (on recitation or send answers to TA mailing list)

Please contact us if you have concerns about your ability to take the class

Early Developments: From ENIAC to the mid 50's

Prehistory

- 1800s: Charles Babbage
  - Difference Engine (conceived in 1823, first implemented in 1855 by Scheutz)
  - Analytic Engine, the first conception of a general-purpose computer (1833, never implemented)
- 1890: Tabulating machines
- Early 1900s: Analog computers
- 1930s: Early electronic (fixed-function) digital computers

Electronic Numerical Integrator and Computer (ENIAC)

- Designed and built by Eckert and Mauchly at the University of Pennsylvania during 1943-45
- The first, completely digital, electronic, operational, general-purpose analytical calculator!
  - 30 tons, 72 square meters, 200KW
- Performance
  - Read in 120 cards per minute
  - Addition took 200 μs, Division 6 ms
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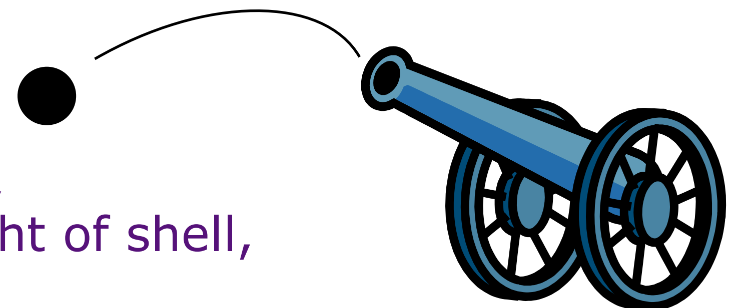
WW-2 Effort

Application: Ballistic calculations



angle = f (location, tail wind, cross wind,
air density, temperature, weight of shell,
propellant charge, ...)

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- *First Draft of a report on EDVAC* was published in 1945, but just had von Neumann's signature!
  - Without a doubt the most influential paper in computer architecture

Stored Program Computer

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plug board	ENIAC 1946
read-only memory	ENIAC 1948
read-write memory	EDVAC 1947 *(concept)*

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EDSAC	1950	Maurice Wilkes

The Spread of Ideas

ENIAC & EDVAC had immediate impact

brilliant engineering: Eckert & Mauchly
lucid paper: Burks, Goldstine & von Neumann

IAS	Princeton	46-52	Bigelow
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Alan Turing's direct influence on these developments is often debated by historians.

Dominant Technology Issue: *Reliability*

ENIAC	⇒	EDVAC
18,000 tubes		4,000 tubes
20 10-digit numbers		2000 word storage
		mercury delay lines

Mean time between failures (MTBF)

MIT's Whirlwind with an MTBF of 20 min. was perhaps the most reliable machine!

Reasons for unreliability:

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2. Storage medium
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CORE J. Forrester 1954

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- Programmer's view of the machine was inseparable from the actual hardware implementation

Accumulator-based computing

Photo: *Joel Emer*

- *Single Accumulator*
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STORE	x	$M[x] \leftarrow (AC)$
ADD	x	$AC \leftarrow (AC) + M[x]$
SUB	x	
MUL	x	Involved a quotient register
DIV	x	
SHIFT LEFT		$AC \leftarrow 2 \times (AC)$
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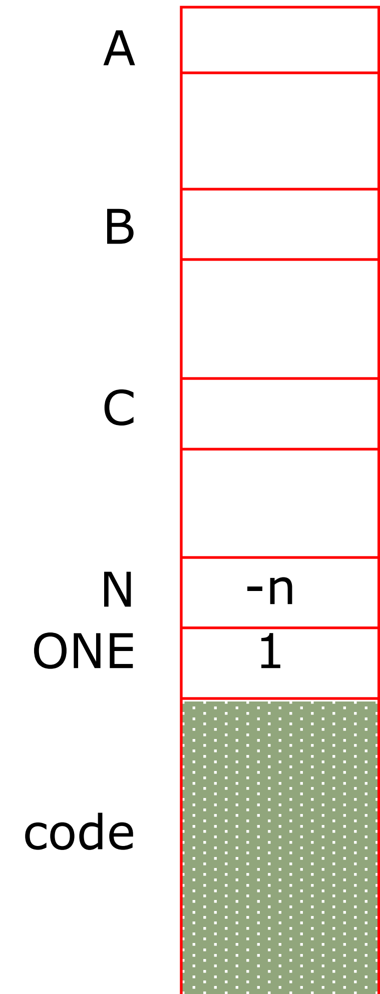
Typically less than 2 dozen instructions!

Programming: Single Accumulator Machine

$C_i \leftarrow A_i + B_i, \quad 1 \leq i \leq n$



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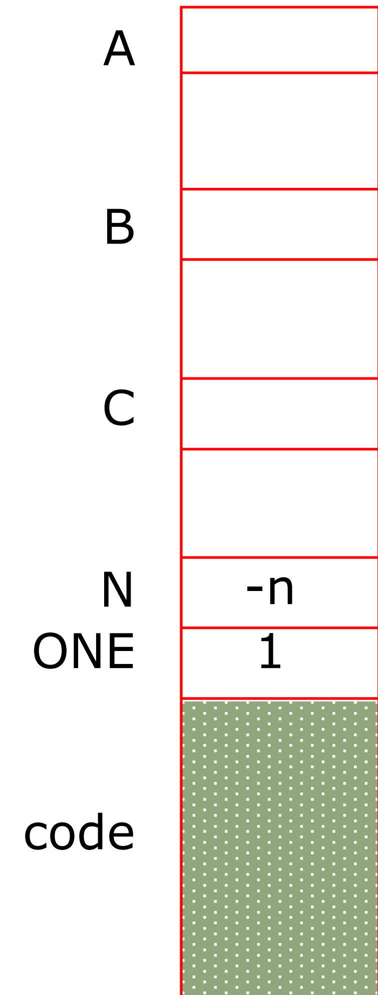
        STORE   N
F1:     LOAD    A
F2:     ADD     B
F3:     STORE   C
        JUMP    LOOP
DONE:   HLT
```



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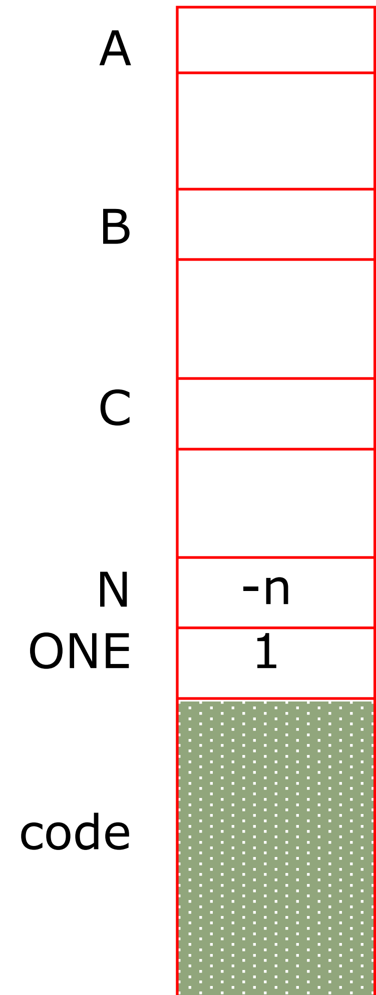

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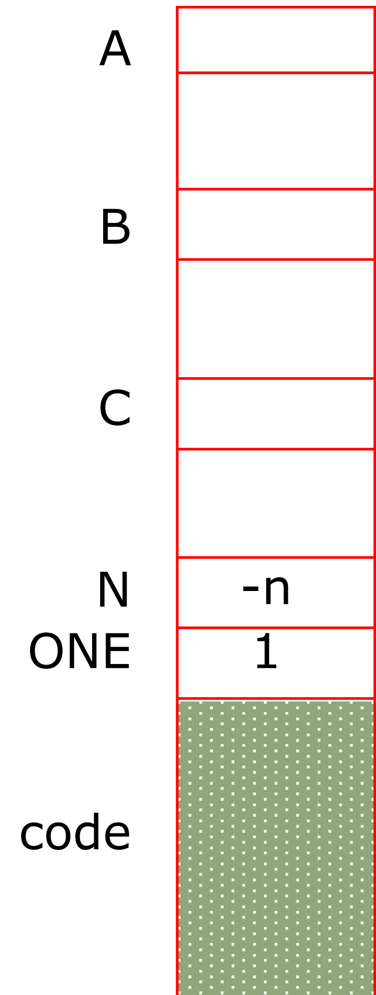

Problem?

How to modify the addresses A, B and C ?

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Each iteration involves

	total	*book-keeping*
instruction fetches		
operand fetches		
stores		

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       ADD         ONE
       STORE ADR   F1
       LOAD ADR    F2
       ADD         ONE
       STORE ADR   F2
       LOAD ADR    F3
       ADD         ONE
       STORE ADR   F3
       JUMP        LOOP
DONE   HLT
```

modify the program for the next iteration

Each iteration involves

	total	*book-keeping*
instruction fetches	*17*	
operand fetches		
stores		

Self-Modifying Code

$C_i \leftarrow A_i + B_i, \quad 1 \leq i \leq n$

```
LOOP    LOAD          N
        JGE           DONE
        ADD           ONE
        STORE         N
F1      LOAD          A
F2      ADD           B
F3      STORE         C
        LOAD ADR      F1
        ADD           ONE
        STORE ADR     F1
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modify the program for the next iteration

Each iteration involves

	total	*book-keeping*
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modify the program for the next iteration

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Each iteration involves

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modify the program for the next iteration

Each iteration involves

	total	*book-keeping*
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Most of the executed instructions are for bookkeeping!

Index Registers

Tom Kilburn, Manchester University, mid 50's

One or more specialized registers to simplify address calculation

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Modify existing instructions

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Add new instructions to manipulate *index registers*

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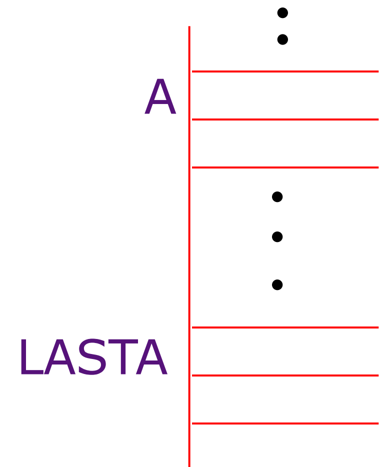
Index registers have accumulator-like characteristics

Using Index Registers

$$C_i \leftarrow A_i + B_i, \quad 1 \leq i \leq n$$

```
        LOADi   N, IX
LOOP    JZi     DONE, IX
        LOAD    LASTA, IX
        ADD     LASTB, IX
        STORE   LASTC, IX
        JUMP    LOOP
DONE    HALT
```

N starts with -n



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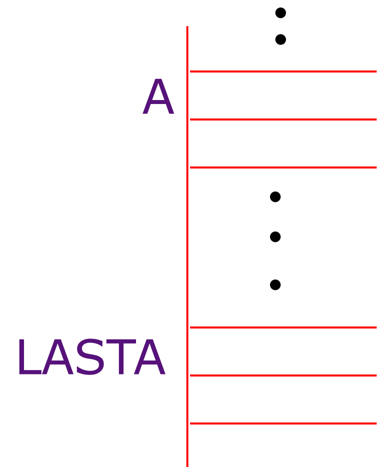

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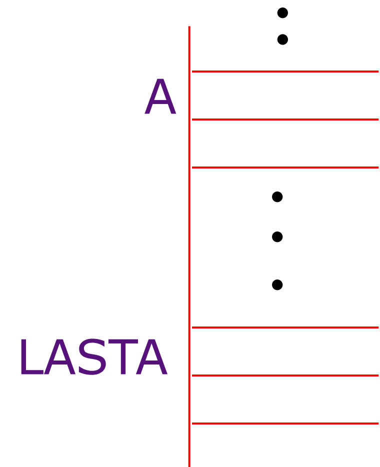

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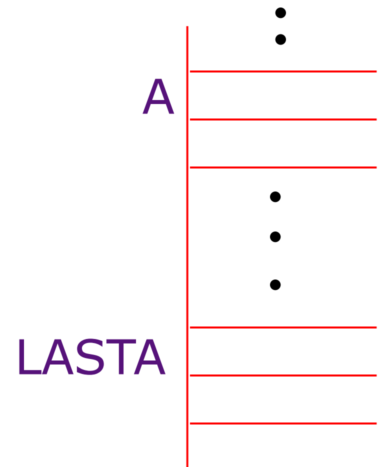

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	with index regs	without index regs
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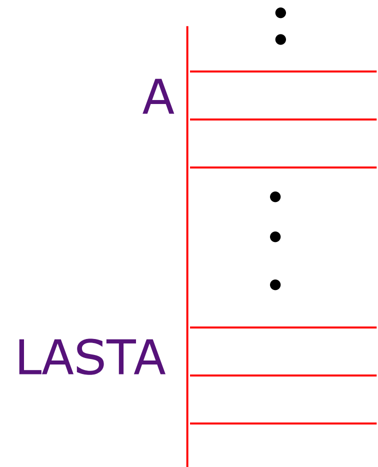

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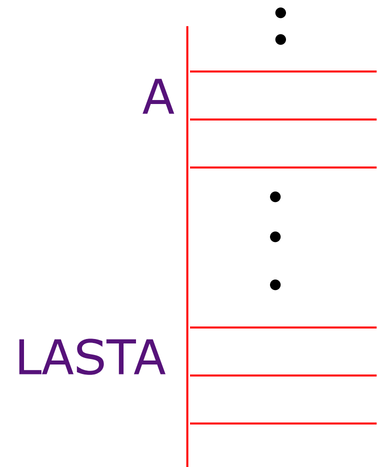

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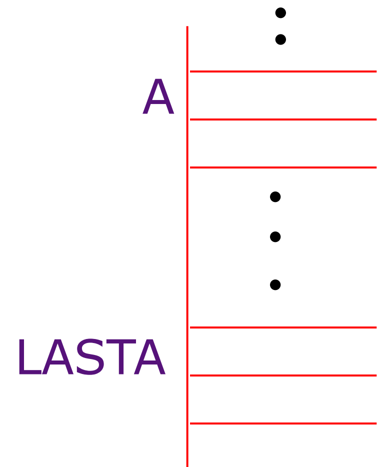

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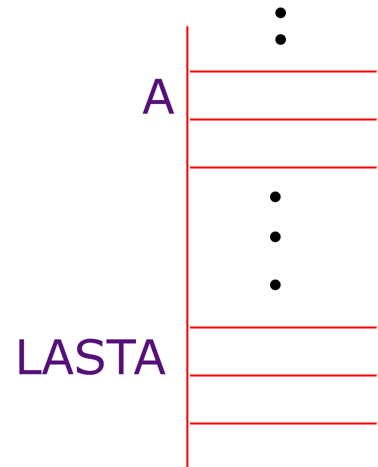

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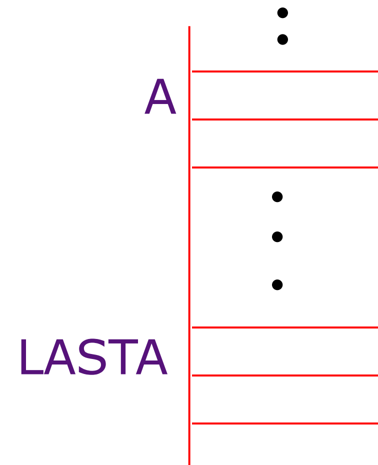

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instruction fetch	5(2)	17 (14)
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- *Costs?*
  - *Complex control*
  - Index register computations (ALU-like circuitry)
  - Instructions 1 to 2 bits longer

Operations on Index Registers

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To increment index register by k

AC ← (IX)	*new instruction*
AC ← (AC) + k	
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INCi k, IX IX ← (IX) + k

More instructions to manipulate index register

STOREi x, IX M[x] ← (IX) (extended to fit a word)
...

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More instructions to manipulate index register

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...		

IX begins to look like an accumulator

⇒ several index registers
several accumulators
⇒ *General Purpose Registers*

Evolution of Addressing Modes

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1. Single accumulator, absolute address

LOAD x

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4. Multiple accumulators, index registers, indirection

    LOAD R, IX, x

    or LOAD R, IX, (x)

the meaning?

$R \leftarrow M[M[x] + (IX)]$

or $R \leftarrow M[M[x + (IX)]]$

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5. Indirect through registers

    LOAD R_I, (R_J)

6. The works

    LOAD R_I, R_J, (R_K) R_J = index, R_K = base addr

Variety of Instruction Formats

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- *Three address formats:* One destination and up to two operand sources per instruction

(Reg op Reg) to Reg	$R_I \leftarrow (R_J)$ op (R_K)
(Reg op Mem) to Reg	$R_I \leftarrow (R_J)$ op M[x]

  - x can be specified directly or via a register
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- *Two address formats:* the destination is same as one of the operand sources

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  load $M[sp] \leftarrow M[M[sp]]$

  - Stack can be in registers or in memory
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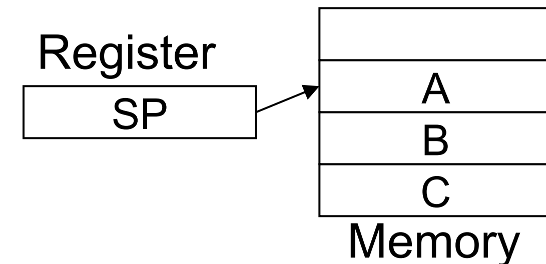

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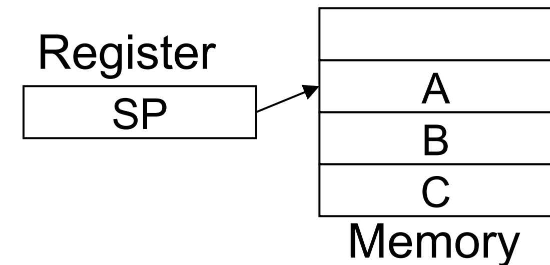

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Many different formats are possible!

Instruction sets in the mid 50's

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- Programmer's view of the machine was inseparable from the actual hardware implementation!

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Next Lecture:

Instruction Set Architectures

and Caches