Complex Pipelining

Daniel Sanchez
Computer Science and Artificial Intelligence Laboratory
M.I.T.
Complex Pipelining: Motivation

Instruction pipelining becomes complex when we want high performance in the presence of

- Multi-cycle operations, for example:
  - Full or partially pipelined floating-point units, or
  - Long-latency operations, e.g., divides

- Variable-latency operations, for example:
  - Memory systems with variable access time

- Replicated functional units, for example:
  - Multiple floating-point or memory units
CDC 6600
Seymour Cray, 1963

- A fast pipelined machine with 60-bit words
  - 128 Kword main memory capacity, 32 banks
- Ten functional units (parallel, unpipelined)
  - Floating Point: adder, 2 multipliers, divider
  - Integer: adder, 2 incrementers, ...
- Hardwired control
- Dynamic scheduling of instructions using a scoreboard
- Ten Peripheral Processors for Input/Output
  - A fast multi-threaded 12-bit integer ALU
- Very fast clock, 10 MHz (FP add in 4 clocks)
- >400,000 transistors, 750 sq. ft., 5 tons, 150 kW, new freon-based cooling technology
- Fastest machine in world for 5 years (until CDC 7600)
  - Over 100 sold ($7-10M each)
CDC 6600: Datapath

- Address Regs: 8 x 18-bit
- Index Regs: 8 x 18-bit
- Operand Regs: 8 x 60-bit
- Inst. Stack: 8 x 60-bit
- IR
- 10 Functional Units

Flow:
- Central Memory
- Operand
- Result
- Address Regs
- Index Regs
- 10 Functional Units
- IR
- Inst. Stack
CDC 6600: A Load/Store Architecture

- Separate instructions to manipulate three types of registers
  - 8 60-bit data registers (X)
  - 8 18-bit address registers (A)
  - 8 18-bit index registers (B)

- All arithmetic and logic instructions are reg-to-reg

<table>
<thead>
<tr>
<th>opcode</th>
<th>i</th>
<th>j</th>
<th>k</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

  \[ \text{Ri} \leftarrow (\text{Rj}) \text{ op } (\text{Rk}) \]

- Only Load and Store instructions refer to memory!

<table>
<thead>
<tr>
<th>opcode</th>
<th>i</th>
<th>j</th>
<th>disp</th>
</tr>
</thead>
<tbody>
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</tr>
</tbody>
</table>

  \[ \text{Ri} \leftarrow \text{M}[(\text{Rj}) + \text{disp}] \]

- Touching address registers 1 to 5 initiates a load
  - 6 to 7 initiates a store
  - very useful for vector operations
CDC6600: Vector Addition

B1 ← - n  
loop:  JZE B1, exit
A1 ← B1 + a1  \textit{load into X1}
A2 ← B1 + b1  \textit{load into X2}
X6 ← X1 + X2
A6 ← B1 + c1  \textit{store X6}
B1 ← B1 + 1
jump loop

Ai = address register
Bi = index register
Xi = data register

\textit{more on vector processing later...}
We will present complex pipelining issues more abstractly ...
Interaction between the Floating point datapath and the Integer datapath is determined largely by the ISA

RISC-V ISA (with F/D extensions)
- separate register files for FP and Integer instructions
  *the only interaction is via a set of move instructions (some ISAs don’t even permit this)*
- separate load/store for FPRs and GPRs, but both use GPRs for address calculation
- branches only take GPRs as sources; FP compare instructions write result to a GPR, which can then be used in a branch
Floating Point Unit

Much more hardware than an integer unit

Single-cycle floating point unit is a bad idea - why?

• it is common to have several floating point units

• it is common to have different types of FPUs \( Fadd, Fmul, Fdiv, \ldots \)

• an FPU may be pipelined, partially pipelined or not pipelined

To operate several FPUs concurrently, the register file needs to have more read and write ports
Functional Unit Characteristics

**fully pipelined**

Functional units have internal pipeline registers

⇒ operands are latched when an instruction enters a functional unit
⇒ inputs to a functional unit (e.g., register file) can change during a long latency operation
Realistic Memory Systems

Latency of access to the main memory is usually much higher than one cycle and often unpredictable.

*Solving this problem is a central issue in computer architecture*

Common approaches to improving memory performance:

- separate instruction and data memory ports
  ⇒ *no self-modifying code*
- caches
  single cycle except in case of a miss ⇒ stall
- interleaved memory
  multiple memory accesses ⇒ bank conflicts
- split-phase memory operations
  ⇒ *out-of-order responses*
Complex Pipeline Structure
Complex Pipeline Control Issues

• Structural hazards at the execution stage if some FPU or memory unit is not pipelined and takes more than one cycle

• Structural hazards at the write-back stage due to variable latencies of different function units

• Out-of-order write hazards due to variable latencies of different function units

• How to handle exceptions?
Complex In-Order Pipeline

- Delay writeback so all operations have same latency to W stage
  - Write ports never oversubscribed (one inst. in & one inst. out every cycle)

How to prevent increased writeback latency from slowing down single-cycle integer operations?
How should we handle data hazards for long-latency operations?

Exceptions?
Superscalar In-Order Pipeline

- Fetch two instructions per cycle; issue both simultaneously if one is integer/memory and other is floating-point
- Inexpensive way of increasing throughput
- Can be extended to wider issue but register file ports and bypassing costs grow quickly
  - E.g., 4-issue UltraSPARC
Dependence Analysis

Needed to Exploit Instruction-level Parallelism
Types of Data Hazards

Consider executing a sequence of
\[ r_k \leftarrow (r_i) \text{ op } (r_j) \]

of instructions

**Data-dependence**
\[
\begin{align*}
r_3 &\leftarrow (r_1) \text{ op } (r_2) \\
\text{Read-after-Write} \\

r_5 &\leftarrow (r_3) \text{ op } (r_4) \\
\text{(RAW) hazard}
\end{align*}
\]

**Anti-dependence**
\[
\begin{align*}
r_3 &\leftarrow (r_1) \text{ op } (r_2) \\
\text{Write-after-Read} \\

r_1 &\leftarrow (r_4) \text{ op } (r_5) \\
\text{(WAR) hazard}
\end{align*}
\]

**Output-dependence**
\[
\begin{align*}
r_3 &\leftarrow (r_1) \text{ op } (r_2) \\
\text{Write-after-Write} \\

r_3 &\leftarrow (r_6) \text{ op } (r_7) \\
\text{(WAW) hazard}
\end{align*}
\]
Detecting Data Hazards

Range and Domain of instruction $i$

$R(i)$ = Registers (or other storage) modified by instruction $i$

$D(i)$ = Registers (or other storage) read by instruction $i$

Suppose instruction $j$ follows instruction $i$ in the program order. Executing instruction $j$ before the effect of instruction $i$ has taken place can cause a

$RAW$ hazard if $R(i) \cap D(j) \neq \emptyset$

$WAR$ hazard if $D(i) \cap R(j) \neq \emptyset$

$WAW$ hazard if $R(i) \cap R(j) \neq \emptyset$
Register vs. Memory Data Dependences

- Data hazards due to register operands can be determined at the decode stage *but*

- Data hazards due to memory operands can be determined only after computing the effective address

\[
\text{store} \quad M[(a1) + \text{offset1}] \leftarrow (a2) \\
\text{load} \quad a3 \leftarrow M[(a4) + \text{offset2}] \\
\]

*Does (a1) + offset1 == (a4) + offset2?*

In lecture 10, we’ll see how to handle memory dependencies. For now, we focus only on register dependencies.
Data Hazards: An Example

\[ I_1 \quad FDIV.D \quad f6, \ f6, \ f4 \]
\[ I_2 \quad FLD \quad f2, \ 45(r3) \]
\[ I_3 \quad FMUL.D \quad f0, \ f2, \ f4 \]
\[ I_4 \quad FDIV.D \quad f8, \ f6, \ f2 \]
\[ I_5 \quad FSUB.D \quad f10, \ f0, \ f6 \]
\[ I_6 \quad FADD.D \quad f6, \ f8, \ f2 \]

RAW Hazards
WAR Hazards
WAW Hazards
Instruction Scheduling

Valid orderings:
in-order  $I_1$  $I_2$  $I_3$  $I_4$  $I_5$  $I_6$

out-of-order  $I_2$  $I_1$  $I_3$  $I_4$  $I_5$  $I_6$

out-of-order  $I_1$  $I_2$  $I_3$  $I_5$  $I_4$  $I_6$
# Out-of-order Completion

## In-order Issue

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Instruction</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FDIV.D</td>
<td>f6,</td>
<td>f6,</td>
<td>f4</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>FLD</td>
<td>f2,</td>
<td>45(r3)</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>FMUL.D</td>
<td>f0,</td>
<td>f2,</td>
<td>f4</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>FDIV.D</td>
<td>f8,</td>
<td>f6,</td>
<td>f2</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>FADD.D</td>
<td>f6,</td>
<td>f8,</td>
<td>f2</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

### What problems can out-of-order comp cause?

- Out-of-order completion can lead to latency issues due to the non-sequential execution of instructions.
- It requires complex hardware to handle the out-of-order execution correctly.
- Compensatory changes in the instruction sequence can be costly in terms of performance.

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*September 25, 2023*
Scoreboard: A Hardware Data Structure to Detect Hazards Dynamically
Can we solve write hazards without equalizing all pipeline depths and without bypassing?
When is it Safe to Issue an Instruction?

• Approach: Stall issue until sure that issuing will cause no dependence problems...

• Suppose a data structure keeps track of all the instructions in all the functional units

• The following checks need to be made before the Issue stage can dispatch an instruction
  – Is the required function unit available?
  – Is the input data available? \(\Rightarrow\) RAW?
  – Is it safe to write the destination? \(\Rightarrow\) WAR? WAW?
  – Is there a structural conflict at the WB stage?
The instruction $i$ at the Issue stage consults this table:

<table>
<thead>
<tr>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Dest</th>
<th>Src1</th>
<th>Src2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Int</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mem</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mult2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Div</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

FU available?
RAW?
WAR?
WAW?

An entry is added to the table if no hazard is detected; An entry is removed from the table after Write-Back.
Simplifying the Data Structure Assuming In-order Issue

• Suppose the instruction is not dispatched by the Issue stage
  • If a RAW hazard exists
  • or if the required FU is busy

• Suppose operands are latched by the functional unit on issue

Can the dispatched instruction cause a

WAR hazard?
WAW hazard?

<table>
<thead>
<tr>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Dest</th>
<th>Src1</th>
<th>Src2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Int</td>
<td></td>
<td></td>
<td>Write Pending</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mem</td>
<td></td>
<td></td>
<td>No read is pending after issue</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>.....</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Simplifying the Data Structure

- No WAR hazard
  ⇒ no need to keep \( src1 \) and \( src2 \)

- The Issue stage does not dispatch an instruction in case of a WAW hazard
  ⇒ a register name can occur at most once in the \( dest \) column
  Can be encoded as a bit vector

<table>
<thead>
<tr>
<th>Name</th>
<th>Busy</th>
<th>Op</th>
<th>Dest</th>
<th>Src1</th>
<th>Src2</th>
</tr>
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<tbody>
<tr>
<td>Int</td>
<td></td>
<td></td>
<td>Write Pending</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mem</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>......</td>
<td></td>
<td></td>
<td>No read is pending after issue</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Scoreboard for In-order Issues

**Busy[FU#]** : a bit-vector to indicate FU’s availability. 
(FU = Int, Add, Mult, Div)
These bits are hardwired to FU’s.

**WP[reg#]** : a bit-vector to record the registers for which writes are pending.
These bits are set to true by the Issue stage and set to false by the WB stage

Issue checks the instruction (opcode dest src1 src2) against the scoreboard (Busy & WP) to dispatch

- FU available?
- RAW?
- WAR?
- WAW?
### Scoreboard Dynamics

<table>
<thead>
<tr>
<th>Issue time</th>
<th>Functional Unit Status</th>
<th>Registers Reserved for Writes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Int(1) Add(1) Mult(3)</td>
<td></td>
</tr>
<tr>
<td>t0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t1</td>
<td>f2</td>
<td>f6, f2</td>
</tr>
<tr>
<td>t2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t3</td>
<td>f0</td>
<td>f6, f0</td>
</tr>
<tr>
<td>t4</td>
<td>f0</td>
<td>f6, f0</td>
</tr>
<tr>
<td>t5</td>
<td>f0 8</td>
<td>f0, f8</td>
</tr>
<tr>
<td>t6</td>
<td>f8</td>
<td>f0, f8</td>
</tr>
<tr>
<td>t7</td>
<td>f10</td>
<td>f8, f10</td>
</tr>
<tr>
<td>t8</td>
<td>f8</td>
<td>f8, f10</td>
</tr>
<tr>
<td>t9</td>
<td>f8</td>
<td>f8</td>
</tr>
<tr>
<td>t10</td>
<td>f6</td>
<td>f6</td>
</tr>
<tr>
<td>t11</td>
<td>f6</td>
<td>f6</td>
</tr>
</tbody>
</table>

**Instructions:**
- $I_1$: FDIV.D
- $I_2$: FLD
- $I_3$: FMUL.D
- $I_4$: FDIV.D
- $I_5$: FSUB.D
- $I_6$: FADD.D

**Check Busy[Fu#]**
- Check WP[src1, src2]
- Check WP[dest]
Preview: Anatomy of a Modern Out-of-Order Superscalar Core

- L06 (Today): Complex pipes w/in-order issue
- L07: Out-of-order exec & renaming
- L08: Branch prediction
- L09: Speculative execution and recovery
- L10: Advanced Memory Ops