Microcoded and VLIW Processors

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Hardwired vs Microcoded Processors

• All processors we have seen so far are *hardwired*: The microarchitecture directly implements all the instructions in the ISA

• *Microcoded processors* add a layer of interpretation: Each ISA instruction is executed as a sequence of simpler *microinstructions*
  – *Simpler implementation*
  – *Lower performance than hardwired (CPI > 1)*

• Microcoding common until the 80s, still in use today (e.g., complex x86 instructions are decoded into multiple “micro-ops”)

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Embed the control logic state table in a read-only memory array

op code conditional flip-flop

\[ \mu \text{ address} \]

Decoder

Matrix A

Matrix B

Control lines to ALU, MUXs, Registers

Next state
Microcmeded Microarchitecture

µcontroller (ROM)

Datapath

Memory (RAM)

holds user program written in macrocode instructions (e.g., MIPS, x86, RISC-V, etc.)

busy?
zero?
opcode

hColds fixed microcode instructions

enMem
MemWrt
A Bus-based Datapath for RISC-V

Microinstruction: register to register transfer (17 control signals)

MA ← PC means RegSel = PC; enReg=yes; IdMA = yes
B ← Reg[rs1] means RegSel = rs1; enReg=yes; IdB = yes
Memory Module

- Assumption: Memory operates asynchronously and is slow compared to Reg-to-Reg transfers
Microcode Controller

\[ \mu \text{JumpType} = \begin{array}{c} \text{next} \mid \text{spin} \\ \text{fetch} \mid \text{dispatch} \\ \text{f eqz} \mid \text{fnez} \end{array} \]

Control Signals (17)
Jump Logic

<table>
<thead>
<tr>
<th>µPCSrc = Case</th>
<th>µJumpTypes</th>
</tr>
</thead>
<tbody>
<tr>
<td>next</td>
<td>µPC+1</td>
</tr>
<tr>
<td>spin</td>
<td>if (busy) then µPC else µPC+1</td>
</tr>
<tr>
<td>fetch</td>
<td>absolute</td>
</tr>
<tr>
<td>dispatch</td>
<td>op-group</td>
</tr>
<tr>
<td>feqz</td>
<td>if (zero) then absolute else µPC+1</td>
</tr>
<tr>
<td>fnez</td>
<td>if (zero) then µPC+1 else absolute</td>
</tr>
</tbody>
</table>
Execution of a RISC-V instruction involves

1. instruction fetch
2. decode and register fetch
3. ALU operation
4. memory operation (optional)
5. write back to register file (optional)
   + the computation of the *next instruction* address
## Instruction Fetch

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>fetch₀</td>
<td>MA ← PC</td>
<td>next</td>
</tr>
<tr>
<td>fetch₁</td>
<td>IR ← Memory</td>
<td>spin</td>
</tr>
<tr>
<td>fetch₂</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>fetch₃</td>
<td>PC ← A + 4</td>
<td>dispatch</td>
</tr>
</tbody>
</table>

...  

| ALU₀     | A ← Reg[rs₁]            | next       |
| ALU₁     | B ← Reg[rs₂]            | next       |
| ALU₂     | Reg[rd] ← func(A,B)     | fetch      |

| ALUi₀    | A ← Reg[rs]             | next       |
| ALUi₁    | B ← sExt(Imm)           | next       |
| ALUi₂    | Reg[rd] ← Op(A,B)       | fetch      |

![Instruction Fetch Diagram](image-url)
## Load & Store

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>LW&lt;sub&gt;0&lt;/sub&gt;</td>
<td>A ← Reg[rs1]</td>
<td>next</td>
</tr>
<tr>
<td>LW&lt;sub&gt;1&lt;/sub&gt;</td>
<td>B ← sExt(Imm)</td>
<td>next</td>
</tr>
<tr>
<td>LW&lt;sub&gt;2&lt;/sub&gt;</td>
<td>MA ← A+B</td>
<td>next</td>
</tr>
<tr>
<td>LW&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Reg[rd] ← Memory</td>
<td>spin</td>
</tr>
<tr>
<td>LW&lt;sub&gt;4&lt;/sub&gt;</td>
<td>fetch</td>
<td></td>
</tr>
<tr>
<td>SW&lt;sub&gt;0&lt;/sub&gt;</td>
<td>A ← Reg[rs1]</td>
<td>next</td>
</tr>
<tr>
<td>SW&lt;sub&gt;1&lt;/sub&gt;</td>
<td>B ← sExt(Imm)</td>
<td>next</td>
</tr>
<tr>
<td>SW&lt;sub&gt;2&lt;/sub&gt;</td>
<td>MA ← A+B</td>
<td>next</td>
</tr>
<tr>
<td>SW&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Memory ← Reg[rs2]</td>
<td>spin</td>
</tr>
<tr>
<td>SW&lt;sub&gt;4&lt;/sub&gt;</td>
<td>fetch</td>
<td></td>
</tr>
</tbody>
</table>
## Branches

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEQ₀</td>
<td>A ← Reg[rs1]</td>
<td>next</td>
</tr>
<tr>
<td>BEQ₁</td>
<td>B ← Reg[rs2]</td>
<td>next</td>
</tr>
<tr>
<td>BEQ₂</td>
<td>A ← A - B</td>
<td>next</td>
</tr>
<tr>
<td>BEQ₃</td>
<td></td>
<td>fnez</td>
</tr>
<tr>
<td>BEQ₄</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>BEQ₅</td>
<td>B ← sExt(Imm&lt;&lt;1)</td>
<td>next</td>
</tr>
<tr>
<td>BEQ₆</td>
<td>PC ← A+B</td>
<td>fetch</td>
</tr>
<tr>
<td>BNE₀</td>
<td>A ← Reg[rs1]</td>
<td>next</td>
</tr>
<tr>
<td>BNE₁</td>
<td>B ← Reg[rs2]</td>
<td>next</td>
</tr>
<tr>
<td>BNE₂</td>
<td>A ← A - B</td>
<td>next</td>
</tr>
<tr>
<td>BNE₃</td>
<td></td>
<td>feqz</td>
</tr>
<tr>
<td>BNE₄</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>BNE₅</td>
<td>B ← sExt(Imm&lt;&lt;1)</td>
<td>next</td>
</tr>
<tr>
<td>BNE₆</td>
<td>PC ← A+B</td>
<td>fetch</td>
</tr>
</tbody>
</table>
## Branches

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLT₀</td>
<td>A ← Reg[rs1]</td>
<td>next</td>
</tr>
<tr>
<td>BLT₁</td>
<td>B ← Reg[rs2]</td>
<td>next</td>
</tr>
<tr>
<td>BLT₂</td>
<td>A ← slt(A, B)</td>
<td>next</td>
</tr>
<tr>
<td>BLT₃</td>
<td></td>
<td>feqz</td>
</tr>
<tr>
<td>BLT₄</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>BLT₅</td>
<td>B ← sExt(Imm&lt;&lt;1)</td>
<td>next</td>
</tr>
<tr>
<td>BLT₆</td>
<td>PC ← A+B</td>
<td>fetch</td>
</tr>
</tbody>
</table>

Similar sequences for BGE, BLTU, BGEU
### Jumps

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>JAL₀</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>JAL₁</td>
<td>Reg[rd] ← A</td>
<td>next</td>
</tr>
<tr>
<td>JAL₂</td>
<td>B ← IR</td>
<td>next</td>
</tr>
<tr>
<td>JAL₃</td>
<td>PC ← JumpTarg(A,B)</td>
<td>fetch</td>
</tr>
<tr>
<td>JALR₀</td>
<td>A ← Reg[rs1]</td>
<td>next</td>
</tr>
<tr>
<td>JALR₁</td>
<td>B ← PC</td>
<td>next</td>
</tr>
<tr>
<td>JALR₂</td>
<td>Reg[rd] ← B</td>
<td>next</td>
</tr>
<tr>
<td>JALR₃</td>
<td>B ← IR</td>
<td>next</td>
</tr>
<tr>
<td>JALR₄</td>
<td>PC ← JumpTarg(A,B)</td>
<td>fetch</td>
</tr>
</tbody>
</table>
VAX 11-780 Microcode (1978)
Very Long Instruction Word (VLIW) Processors
Sequential ISA Bottleneck

Sequential source code

```plaintext
a = foo(b);
for (i=0, i<
```

Superscalar compiler

- Find independent operations
- Schedule operations

Sequential machine code

Superscalar processor

- Check instruction dependencies
- Schedule execution
VLIW: Very Long Instruction Word

- Multiple operations packed into one instruction
- Each operation slot is for a fixed function
- Constant operation latencies are specified
VLIW Design Principles

The architecture:

- Allows operation parallelism within an instruction
  - No cross-operation RAW check
- Provides deterministic latency for all operations
  - Latency measured in ‘instructions’
  - No data use allowed before specified latency with no data interlocks

The compiler:

- Schedules (reorders) to maximize parallel execution
- Guarantees intra-instruction parallelism
- Schedules to avoid data hazards (no interlocks)
  - Typically separates operations with explicit NOPs
Early VLIW Machines

- **FPS AP120B (1976)**
  - scientific attached array processor
  - first commercial wide instruction machine
  - hand-coded vector math libraries using software pipelining and loop unrolling

- **Multiflow Trace (1987)**
  - commercialization of ideas from Fisher’s Yale group including “trace scheduling”
  - available in configurations with 7, 14, or 28 operations/instruction
  - 28 operations packed into a 1024-bit instruction word

- **Cydrome Cydra-5 (1987)**
  - 7 operations encoded in 256-bit instruction word
  - rotating register file

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Loop Execution

for (i=0; i<N; i++)

Compile

loop:  fld f1, 0(x1)
       add x1, 8
       fadd.d f2, f0, f1
       fsd f2, 0(x2)
       add x2, 8
       bne x1, x3, loop

Schedule

loop:  add x1  fld  
       fadd.d  
       add x2  bne  fsd

How many FP ops/cycle?

1 fadd / 8 cycles = 0.125
Loop Unrolling

Unroll inner loop to perform 4 iterations at once

for (i=0; i<N; i++)

Is this code always correct?

No, need to handle values of N that are not multiples of unrolling factor with final cleanup loop

for (i=0; i<N; i+=4)
{
}
### Scheduling Loop Unrolled Code

**Unroll 4 ways**

```plaintext
loop:  fld f1, 0(x1)
       fld f2, 8(x1)
       fld f3, 16(x1)
       fld f4, 24(x1)
       add x1, 32
       fadd.d f5, f0, f1
       fadd.d f6, f0, f2
       fadd.d f7, f0, f3
       fadd.d f8, f0, f4
       fsd f5, 0(x2)
       fsd f6, 8(x2)
       fsd f7, 16(x2)
       fsd f8, 24(x2)
       add x2, 32
       bne x1, x3, loop
```

**Schedule**

<table>
<thead>
<tr>
<th>Int1</th>
<th>Int 2</th>
<th>M1</th>
<th>M2</th>
<th>FP+</th>
<th>FPx</th>
</tr>
</thead>
<tbody>
<tr>
<td>fld f1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fld f2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fld f3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fld f4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>add x1</td>
<td>fadd.d f5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fadd.d f6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fadd.d f7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fadd.d f8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bne x1, x3, loop</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**How many FLOPS/cycle?**

4 fadds / 11 cycles = 0.36
Software Pipelining

Unroll 4 ways first

How many FLOPS/cycle?
4 fadds / 4 cycles = 1
Software Pipelining vs. Unrolling

Software pipelining pays startup/wind-down costs only once per loop, not once per iteration.
What if there are no loops?

- Branches limit basic block size in control-flow intensive irregular code
- Difficult to find ILP in individual basic blocks
Trace Scheduling
[Fisher, Ellis]

- Pick string of basic blocks, a trace, that represents most frequent branch path
- Schedule whole “trace” at once
- Add fixup code to cope with branches jumping out of trace

How do we know which trace to pick?

Use profiling feedback or compiler heuristics to find common branch paths
Problems with “Classic” VLIW

- Knowing branch probabilities
  - Profiling requires an significant extra step in build process

- Scheduling for statically unpredictable branches
  - Optimal schedule varies with branch path

- Object code size
  - Instruction padding wastes instruction memory/cache
  - Loop unrolling/software pipelining replicates code

- Scheduling memory operations
  - Caches and/or memory bank conflicts impose statically unpredictable variability
  - Uncertainty about addresses limit code reordering

- Object-code compatibility
  - Have to recompile all code for every machine, even for two machines in same generation
VLIW Instruction Encoding

- Schemes to reduce effect of unused fields
  - Compressed format in memory, expand on I-cache refill
    - used in Multiflow Trace
    - introduces instruction addressing challenge
  - Provide a single-op VLIW instruction
    - Cydra-5 UniOp instructions
  - Mark parallel groups
    - used in TMS320C6x DSPs, Intel IA-64
Cydra-5: Memory Latency Register (MLR)

- Problem: Loads have variable latency
- Solution: Let software choose desired memory latency

- Compiler schedules code for maximum load-use distance

- Software sets MLR to latency that matches code schedule

- Hardware ensures that loads take exactly MLR cycles to return values into processor pipeline
  - Hardware buffers loads that return early
  - Hardware stalls processor if loads return late
IA-64 Predicated Execution

Problem: Mispredicted branches limit ILP
Solution: Eliminate hard-to-predict branches with predicated execution
- Almost all IA-64 instructions can be executed conditionally under predicate
- Instruction becomes NOP if predicate register false

Mahlke et al, ISCA95: On average >50% branches removed
Where does predication fit in?
**IA-64 Speculative Execution**

**Problem:** Branches restrict compiler code motion

**Solution:** Speculative operations that don’t cause exceptions

Can’t move load above branch because might cause spurious exception

Particularly useful for scheduling long latency loads early
IA-64 Data Speculation

Problem: Possible memory hazards limit code scheduling
Solution: Instruction-based speculation with hardware monitor to check for pointer hazards

Can’t move load above store because store might be to same address

Requires associative hardware in address check table
Clustered VLIW

- Divide machine into clusters of local register files and local functional units.
- Lower bandwidth/higher latency interconnect between clusters.
- Software responsible for mapping computations to minimize communication overhead.
- Common in commercial embedded processors, examples include TI C6x series DSPs, and HP Lx processor.
- Exists in some superscalar processors, e.g., Alpha 21264.
Limits of Static Scheduling

- Unpredictable branches
- Unpredictable memory behavior (cache misses and dependencies)
- Code size explosion
- Compiler complexity

Question:

How applicable are VLIW-inspired techniques to traditional RISC/CISC processor architectures?
Thank you!

Next Lecture: Vector Processors