Security

Mengjia Yan
Computer Science & Artificial Intelligence Lab
M.I.T.

Security and Information Leakage

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- So implementation details and timing behaviors (e.g., microarchitectural state, power, etc.) have been exploited to breach security mechanisms.
- In specific, they have been used as channels to leak information!

Standard Communication Model

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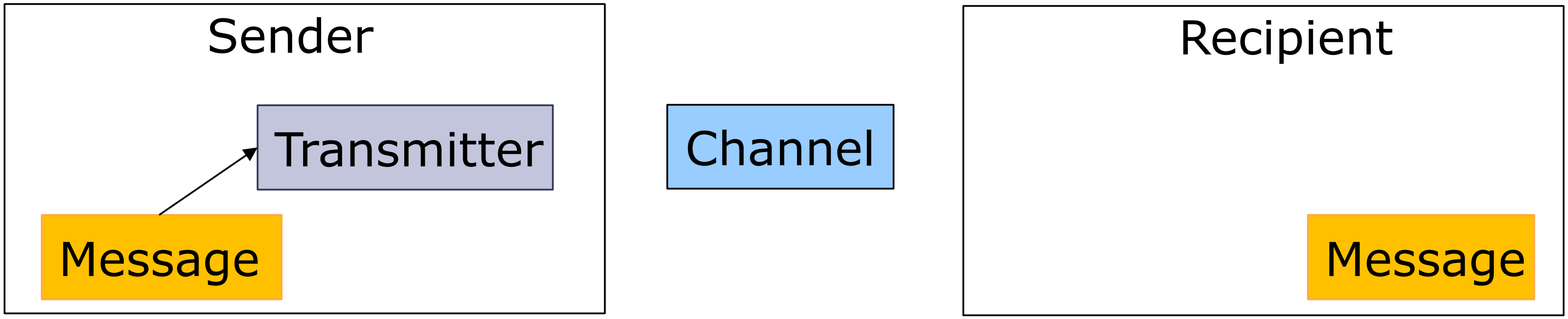
1. Transmitter gets a message

Standard Communication Model



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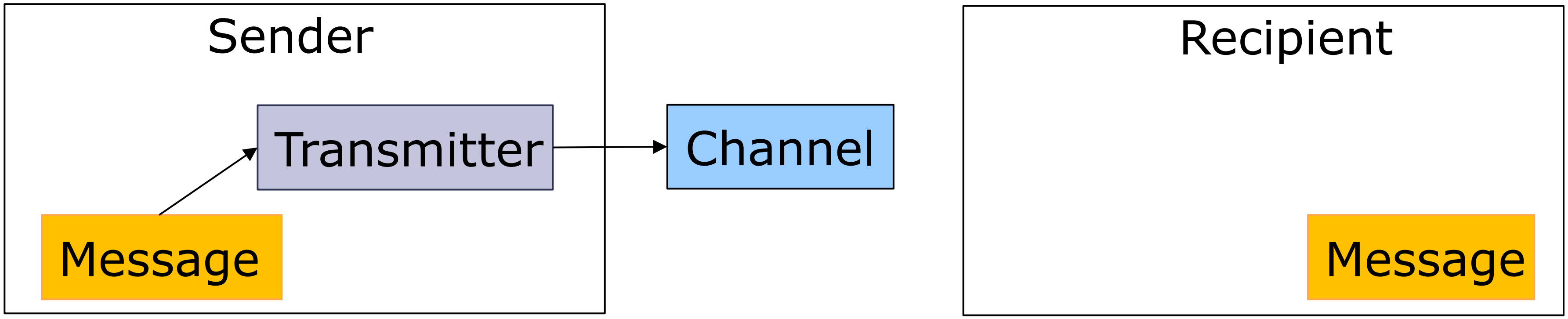
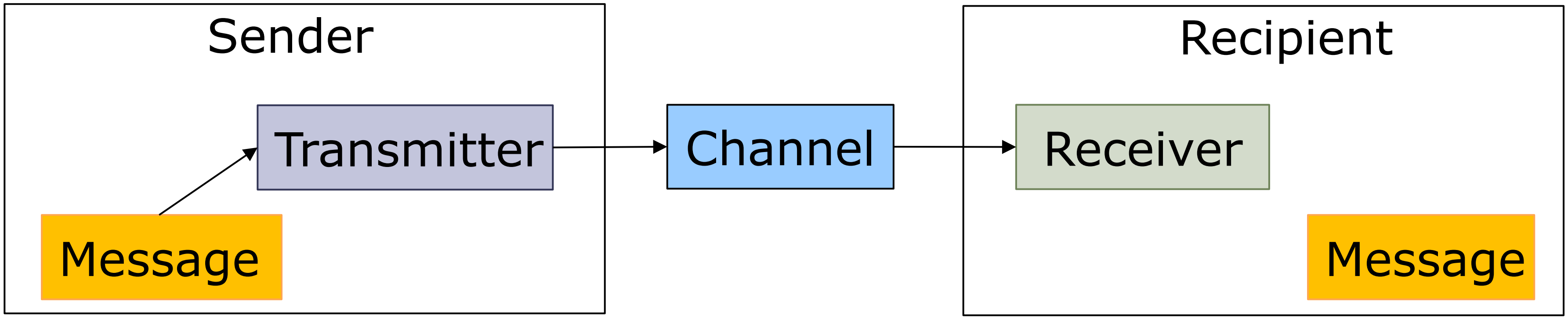


1. Transmitter gets a message
2. Transmitter modulates channel

Standard Communication Model



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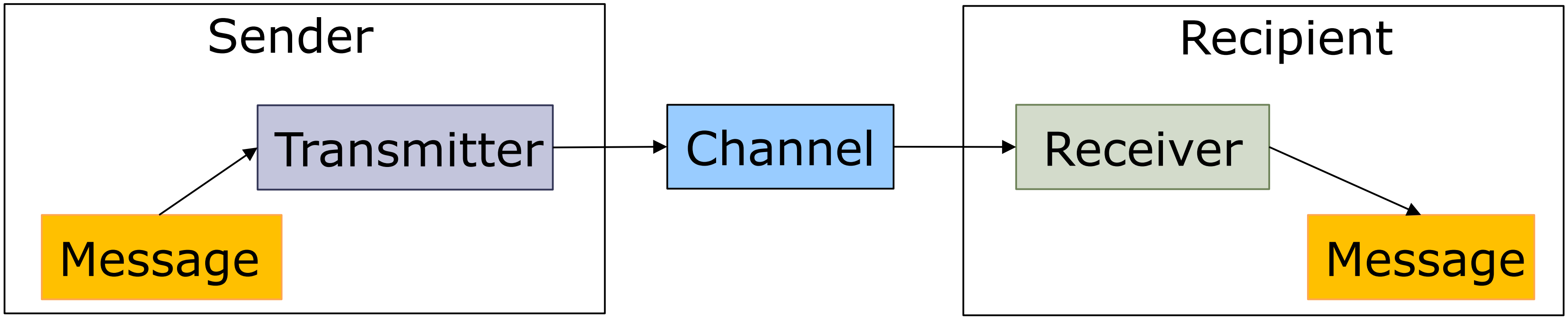

1. Transmitter gets a message
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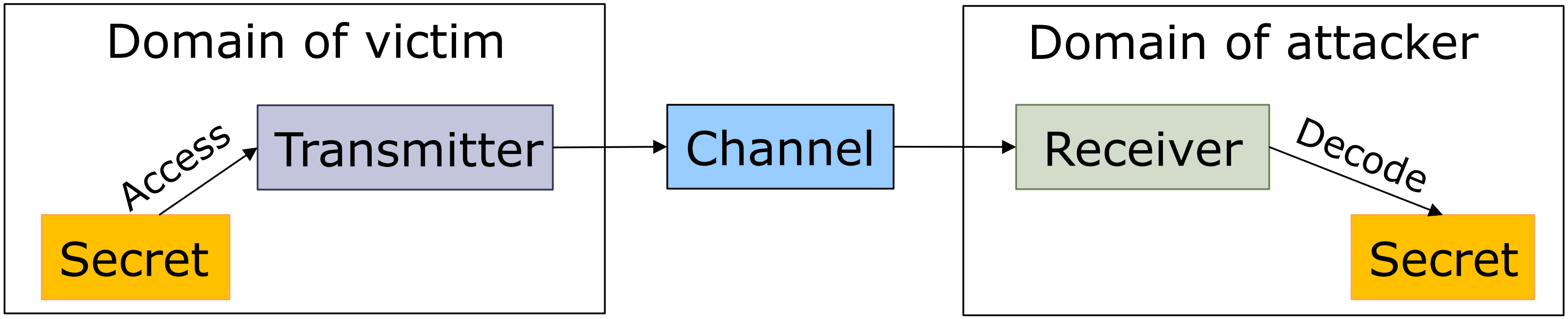
3. Receiver detects modulation on channel
4. Receiver decodes modulation as message

Communication Model of Attacks
[Belay, Devadas, Emer]



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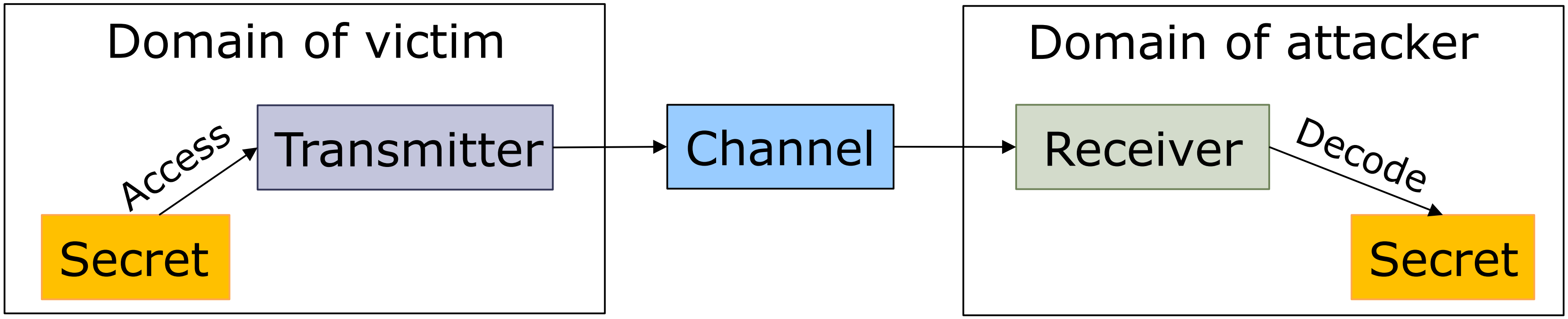

- Domains – Distinct architectural domains in which architectural state is not shared.
- Secret – the "message" that is transmitted on the channel and detected by the receiver
- Channel – some "state" that can be changed, i.e., modulated, by the "transmitter" and whose modulation can be detected by the "receiver".

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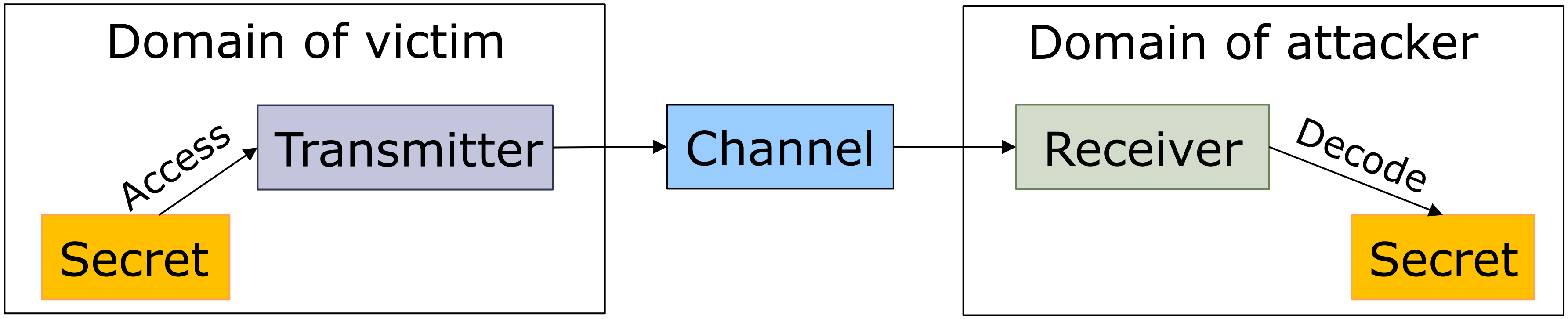

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Because channel is not a "direct" communication channel, it is often referred to as a "side channel"

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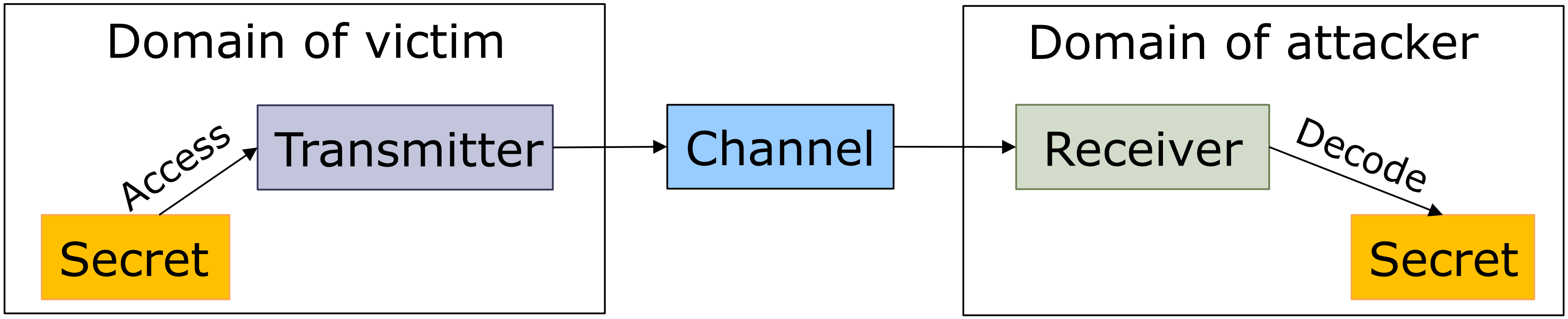
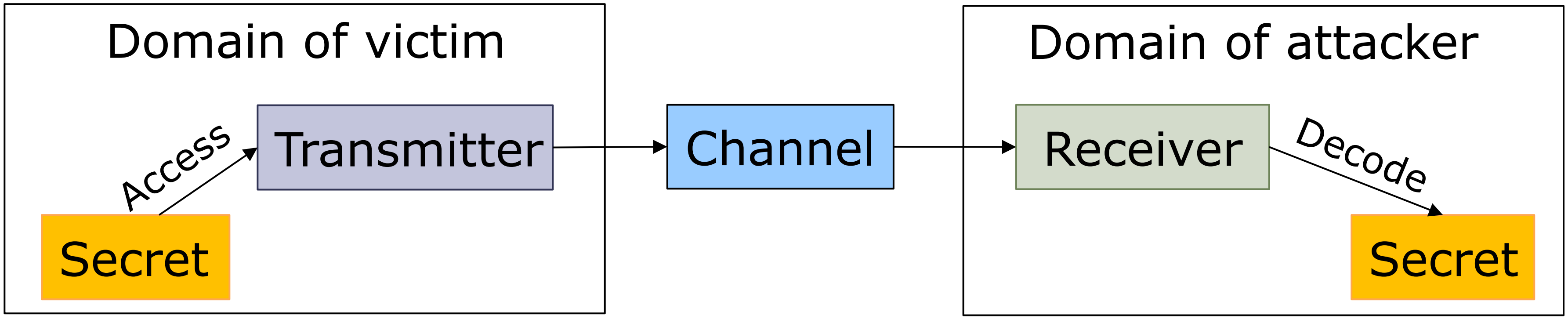


1. Transmitter “accesses” secret
2. Transmitter modulates channel *(microarchitectural state)* with a message based on secret
3. Receiver detects modulation on channel
4. Receiver decodes modulation as a message containing the secret

ATM Acoustic Channels



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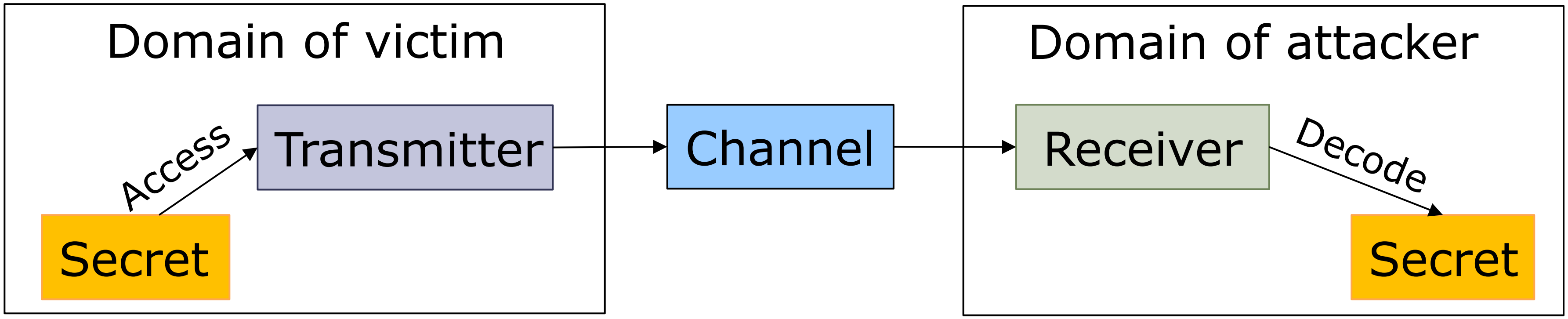

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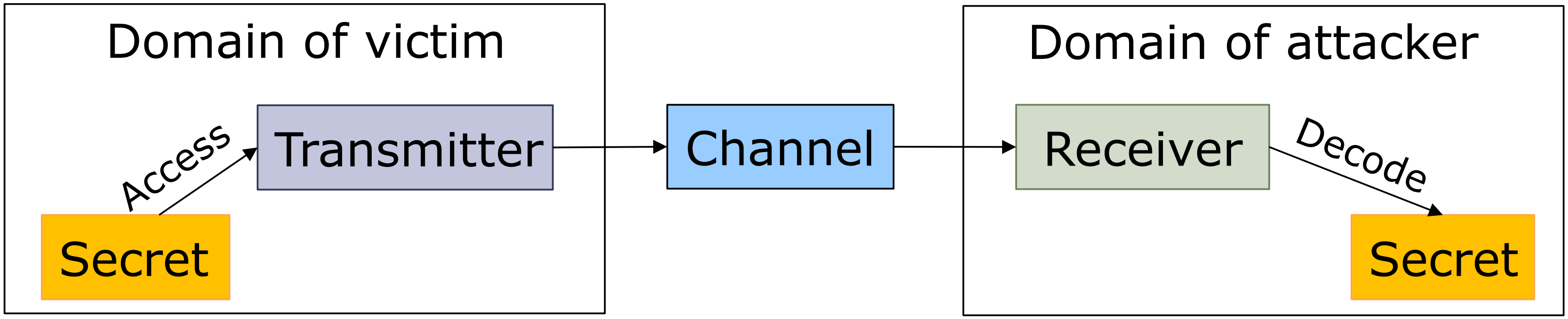

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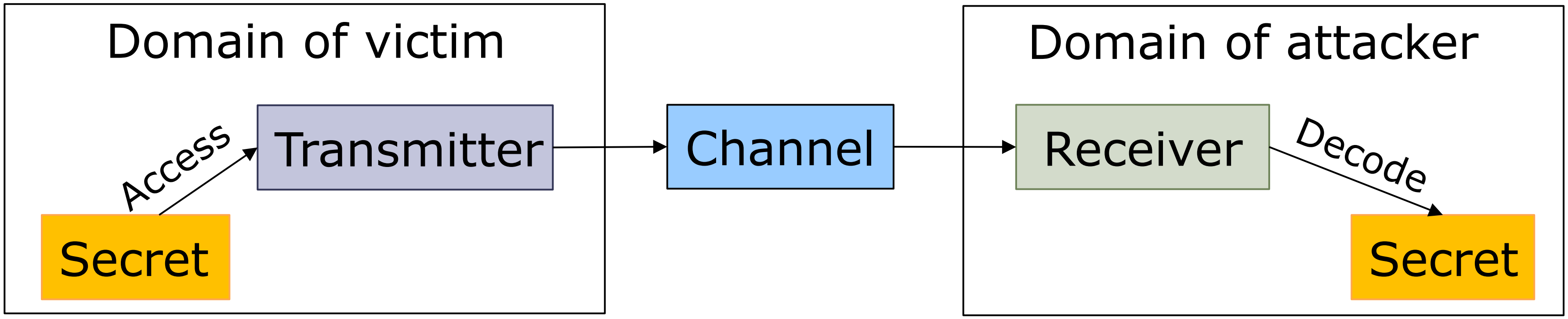

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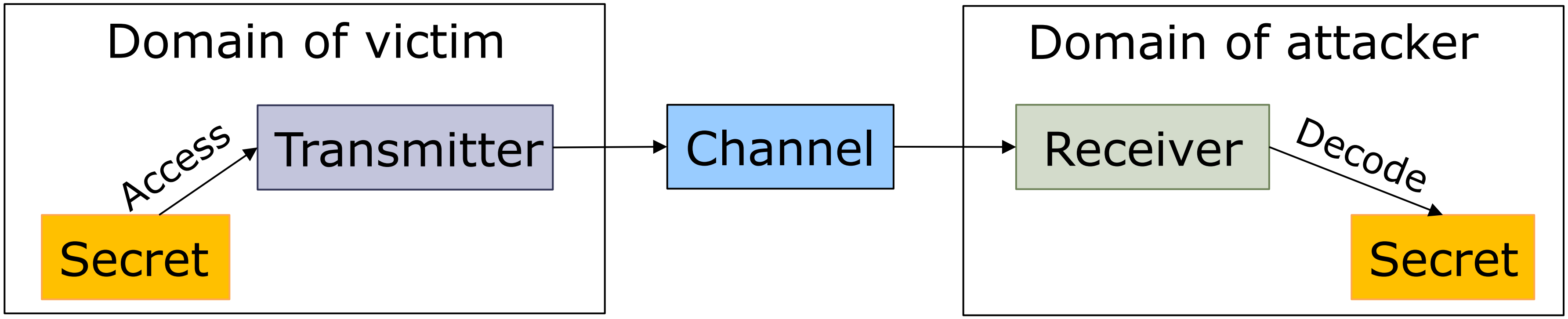

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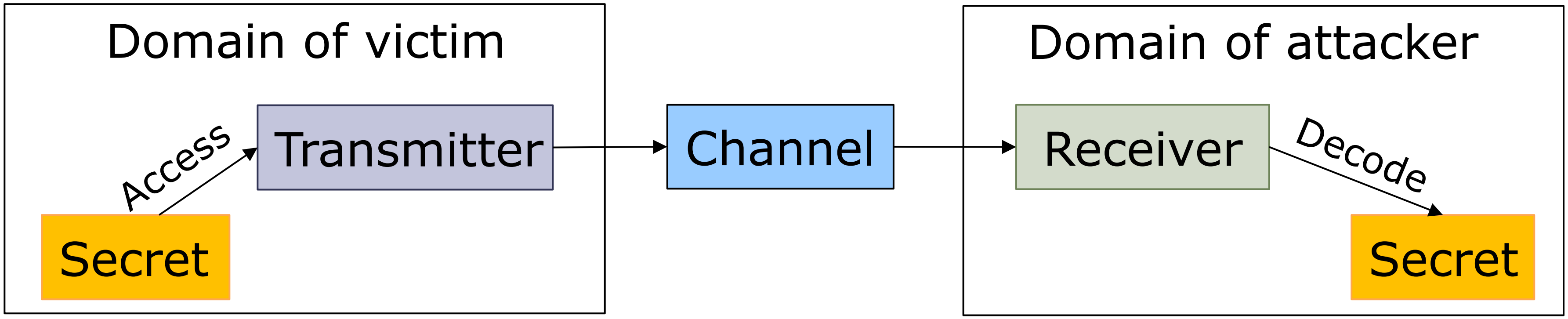

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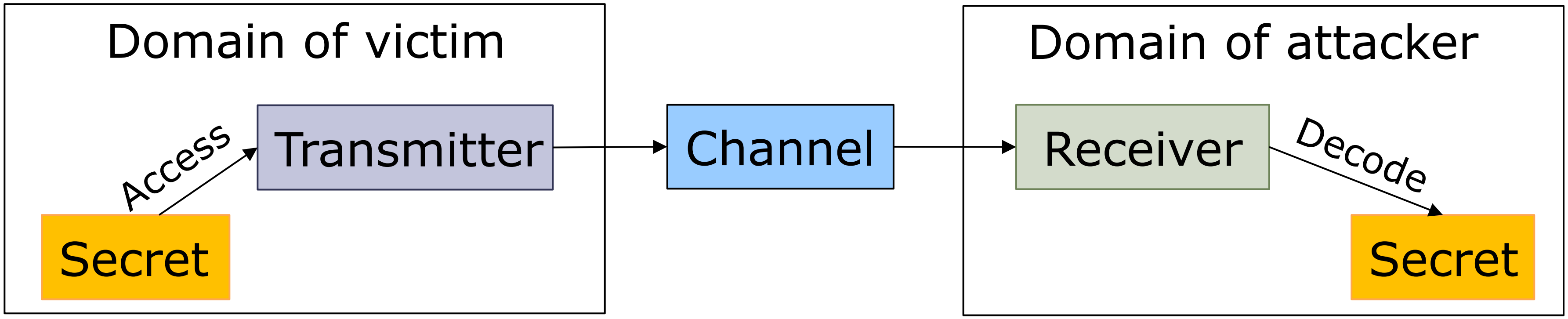

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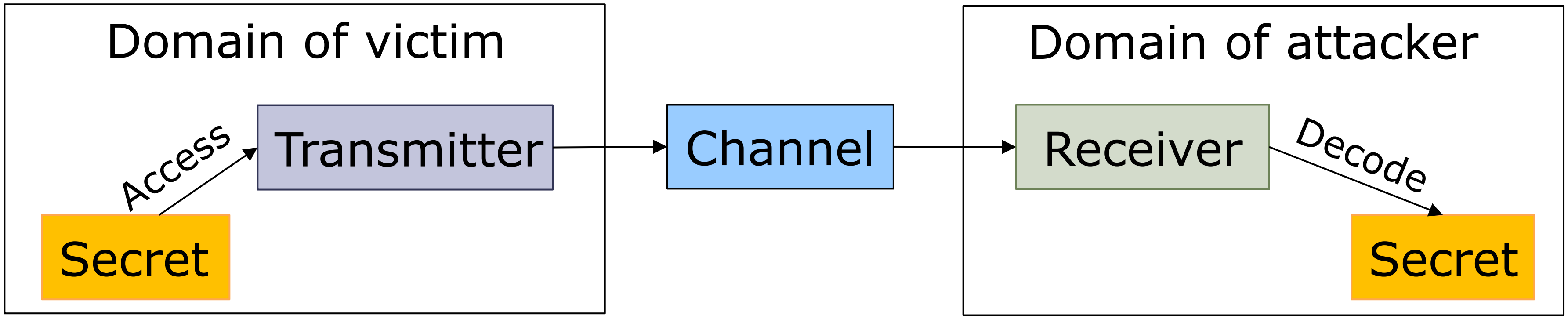

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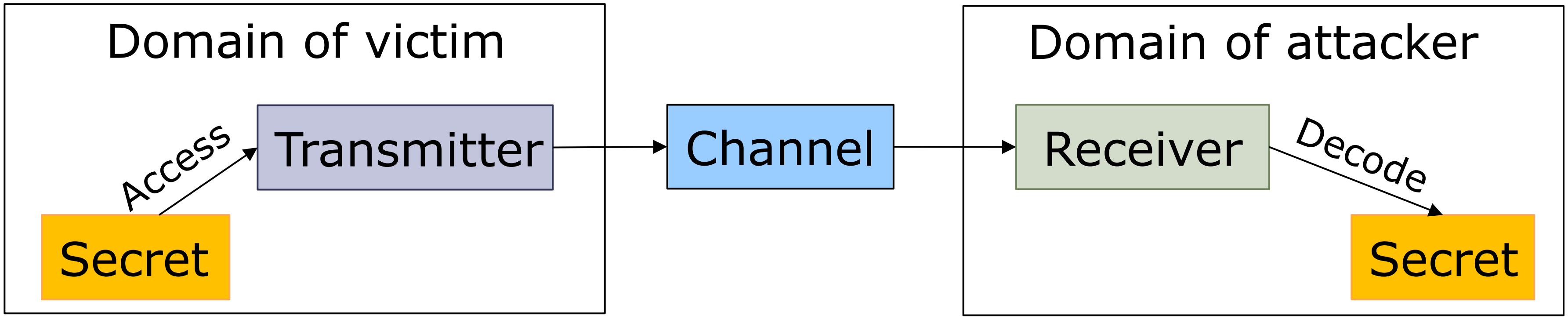

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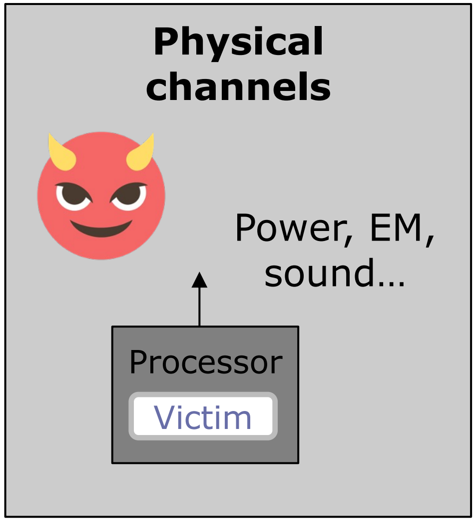
Physical vs Timing vs uArch Channel

- Types of channels



Attacker requires measurement equipment → physical access

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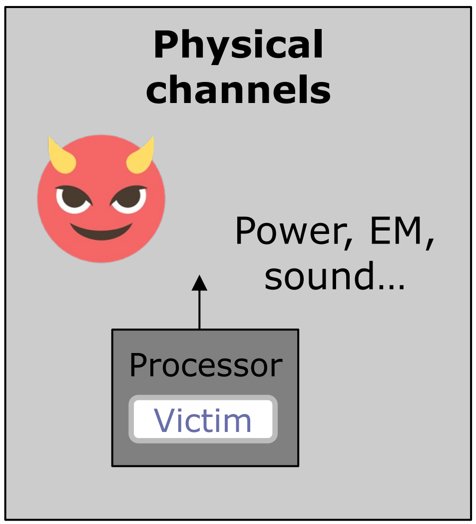

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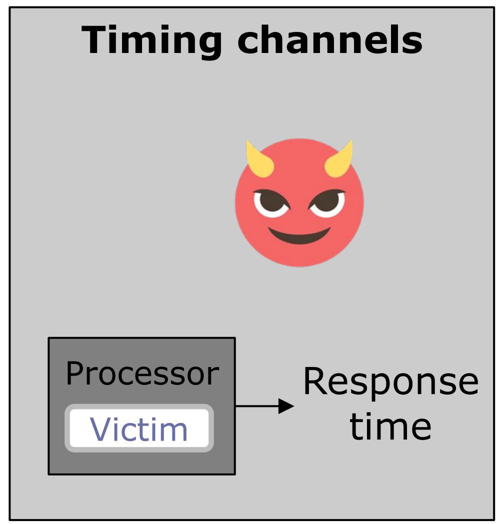

Attacker may be remote (e.g., over an internet connection)

Timing Channel Example

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def check(input):

  size = len(passwd); //passwd contains 8 digits
  for i in range(0,size):
    if (input [i] != password[i]):
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  return (“success”)
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Blind guess needs to maximally try: 10^8

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The execution time is dependent on how many characters match between the input and the correct password. Attacker can brute-force each character. Maximally try 10*8 times.

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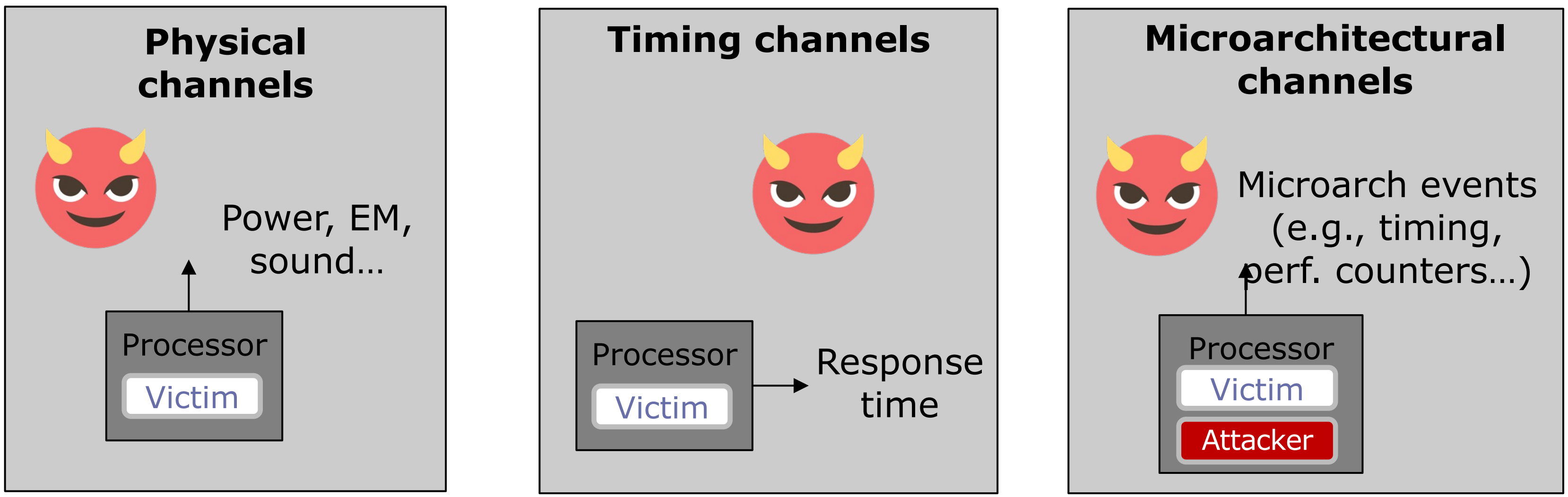

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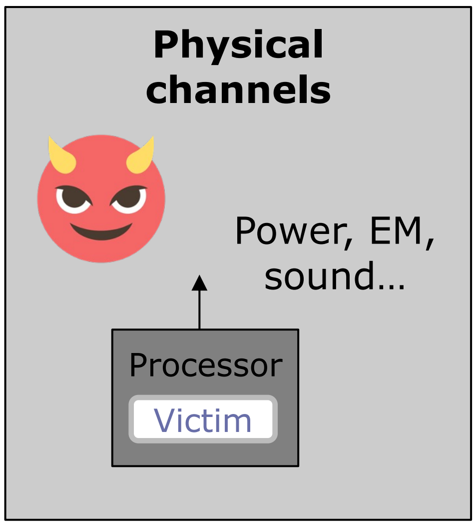

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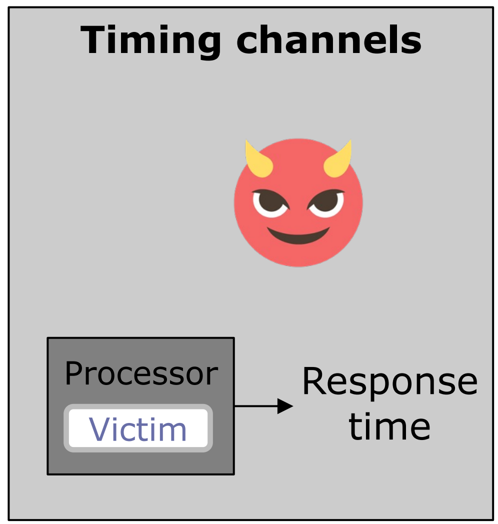

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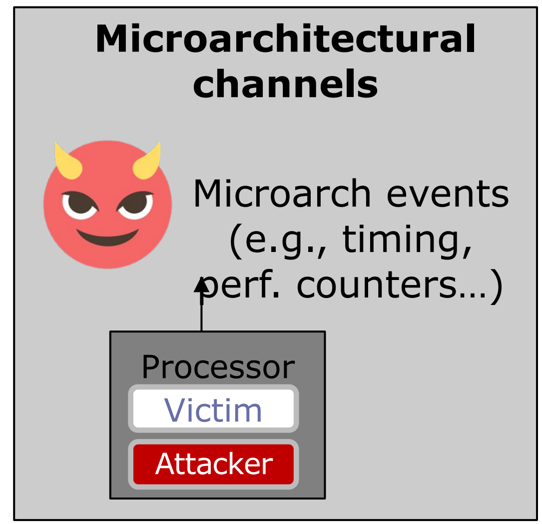

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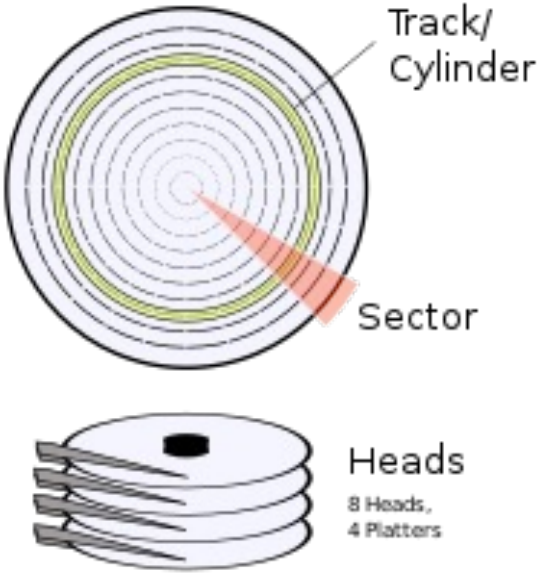
Side Channel Attacks in 1977

- A side channel due to disk arm optimization
  - Enqueues requests by ascending cylinder number and dequeues (executes) them by the "elevator algorithm."



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  1. Receiver issues a request to 55
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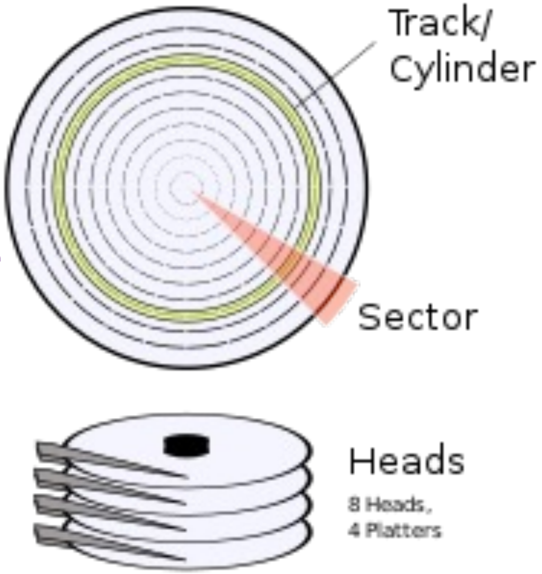

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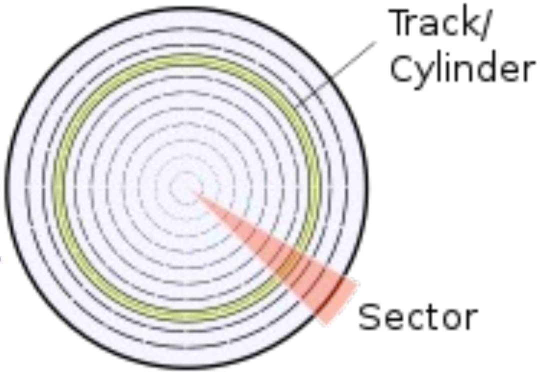

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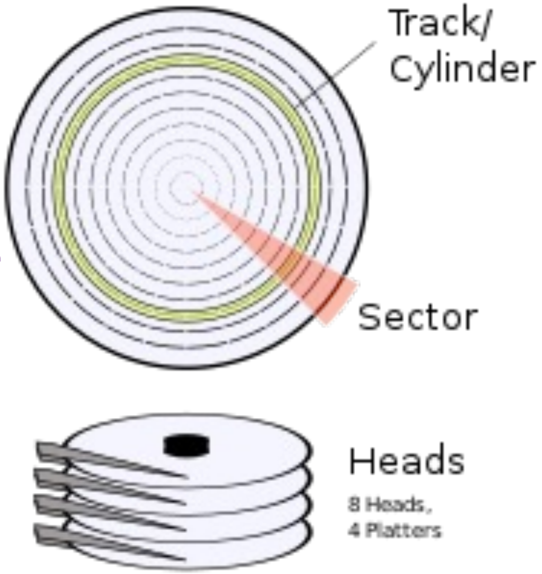

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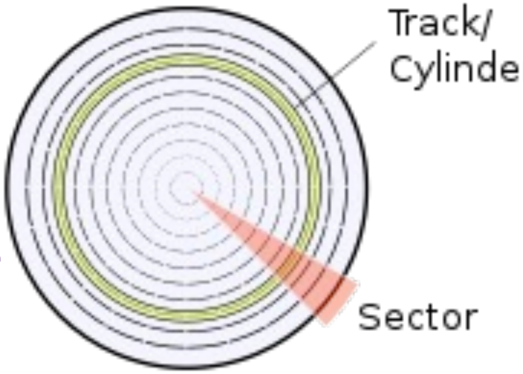

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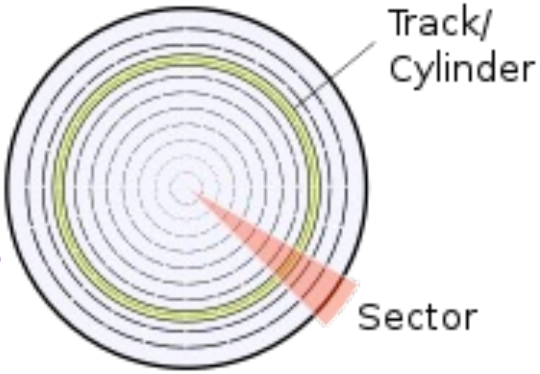

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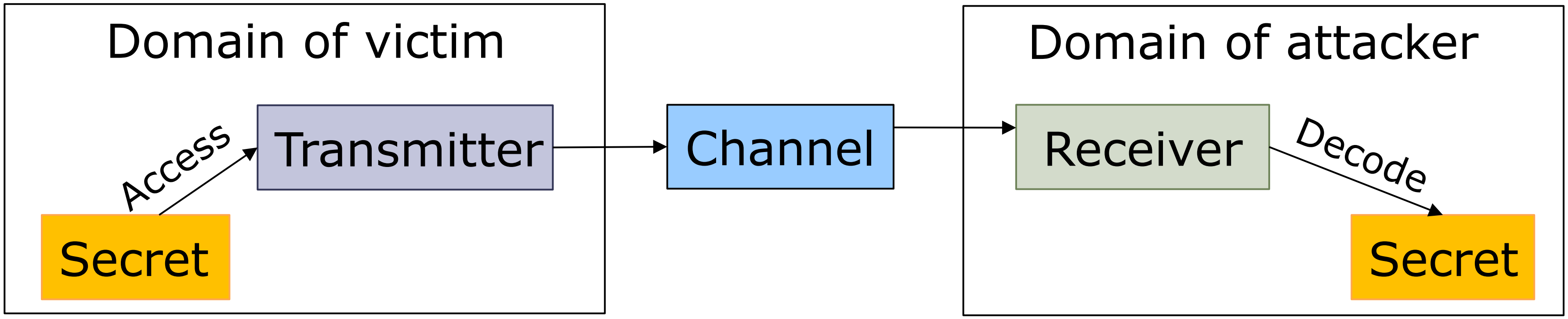
Note this requires an "active" receiver that preconditions the channel

Communication w/ Active Receiver



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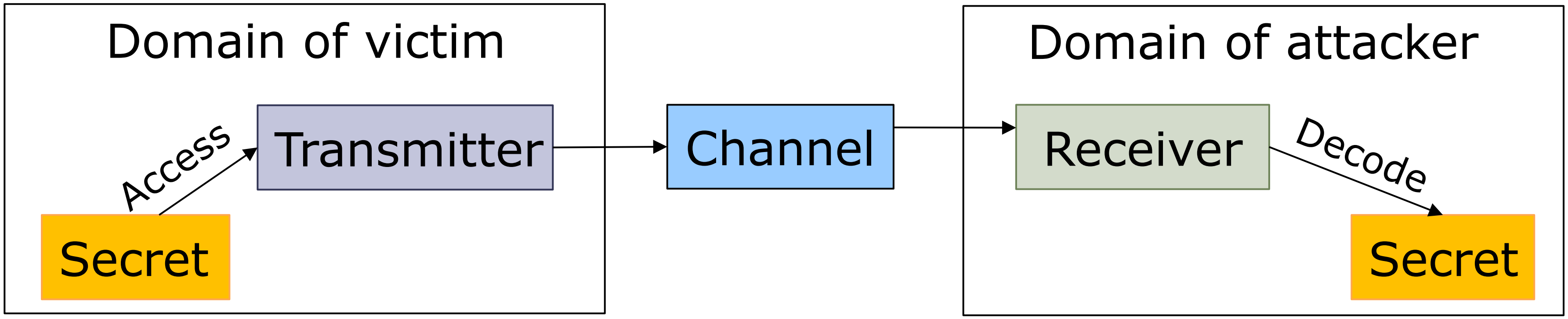

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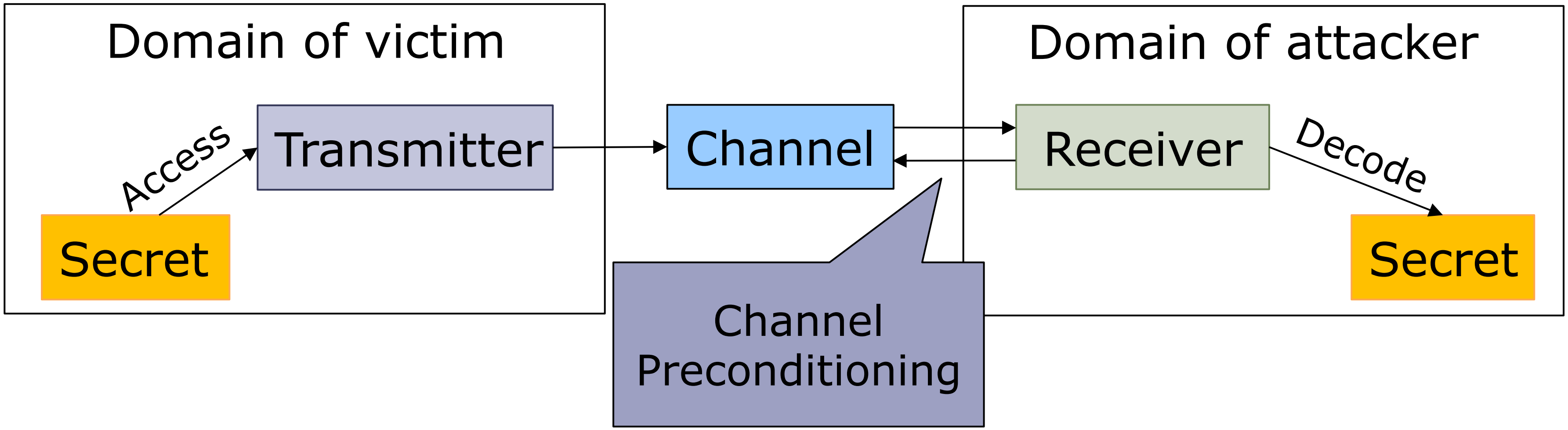

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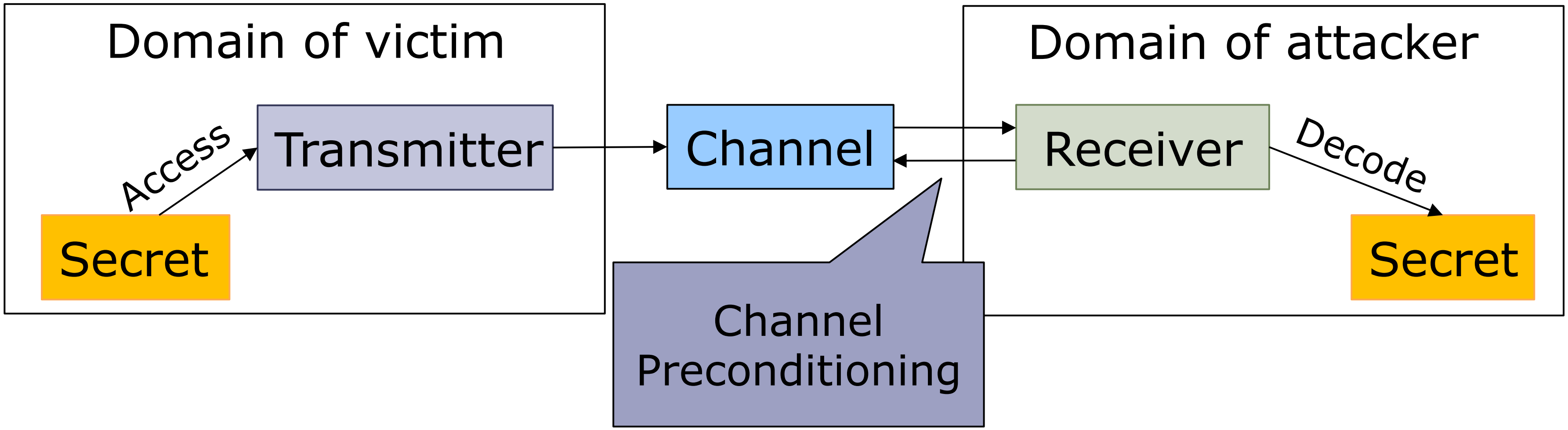

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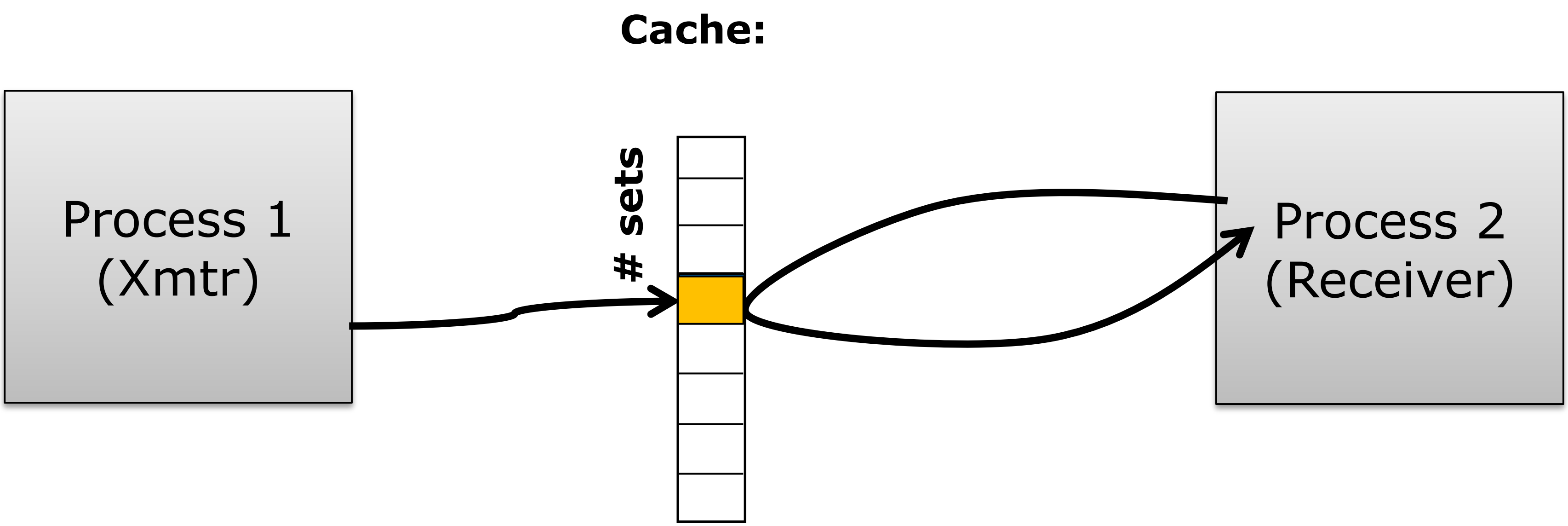
- An active receiver also needs to deal with synchronization of transmission (modulation) activity with reception (demodulation) activity.

A Cache-based Channel



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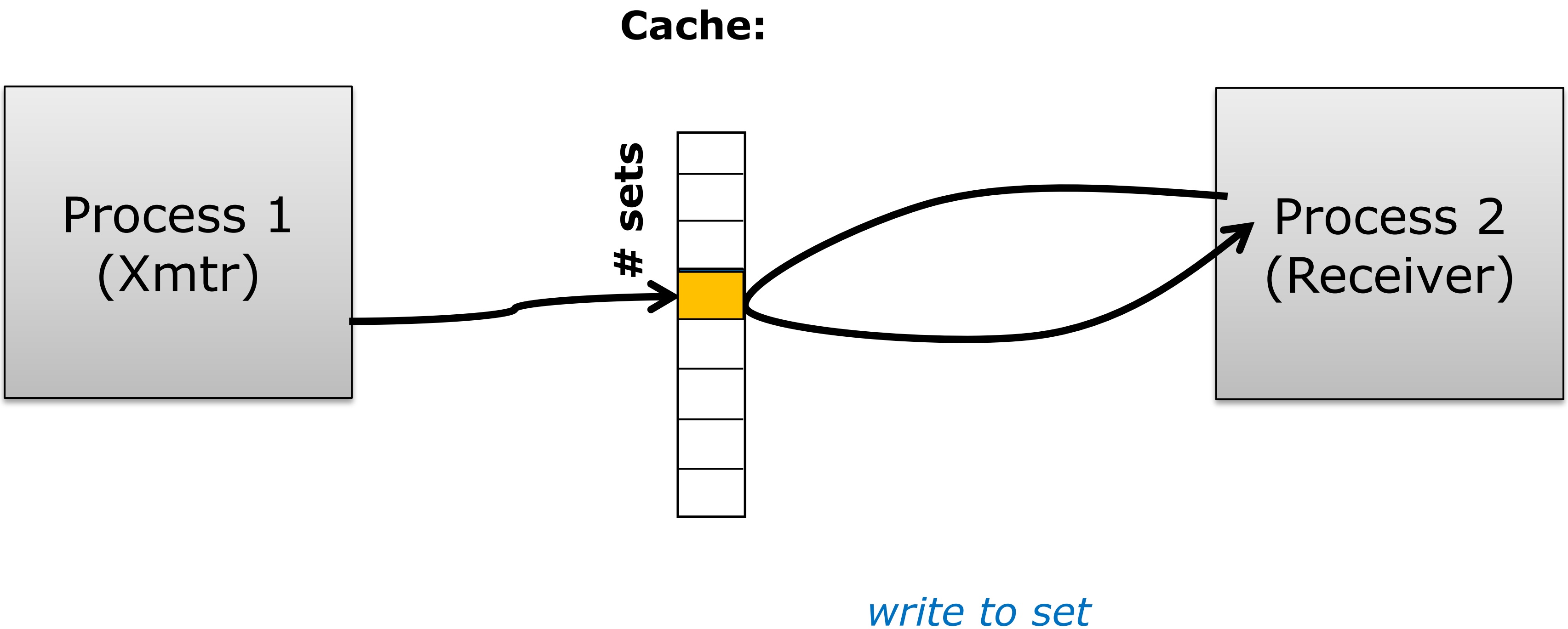

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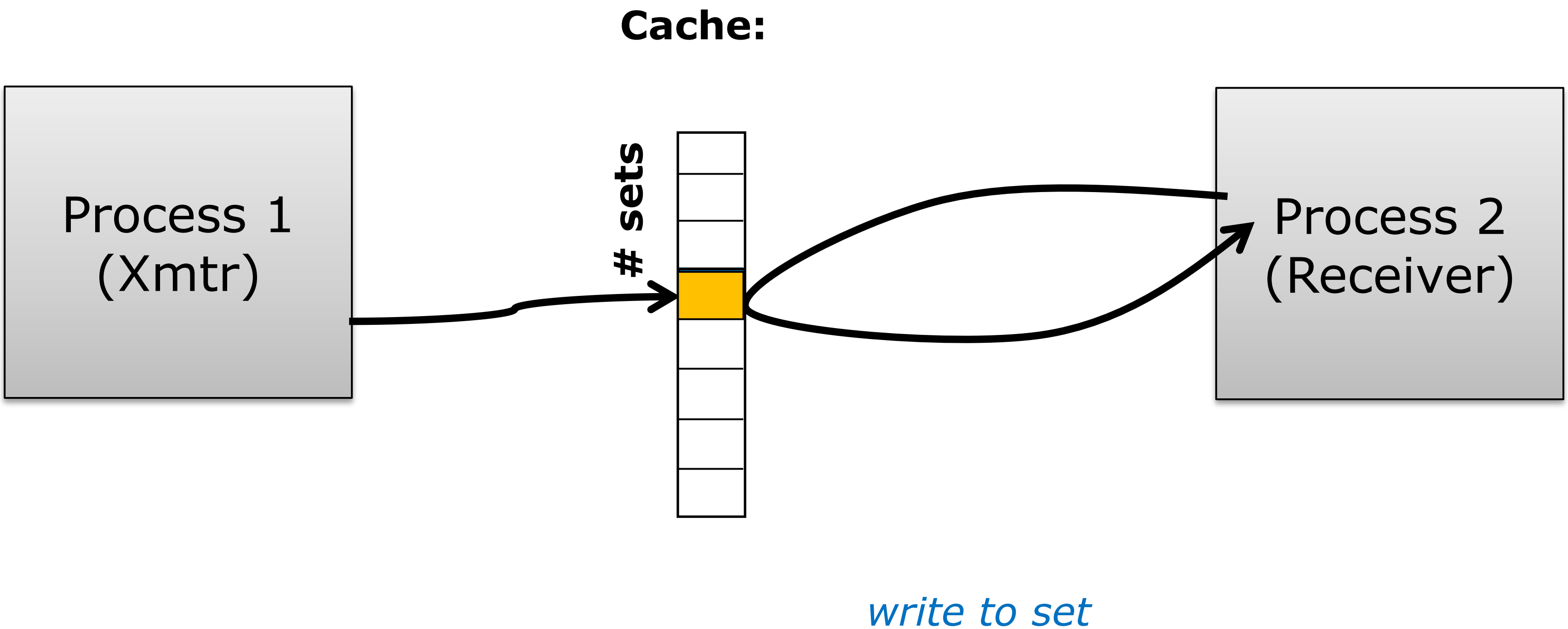

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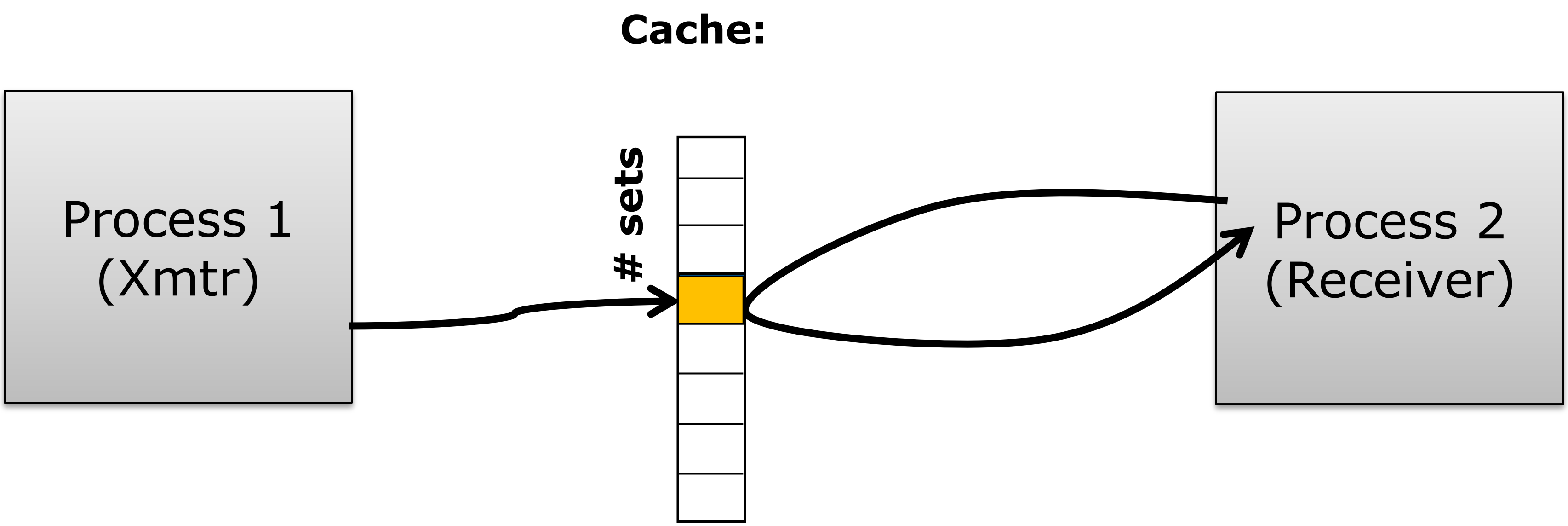

if (**send ‘0’**)
  idle
else
  write to a set

write to set

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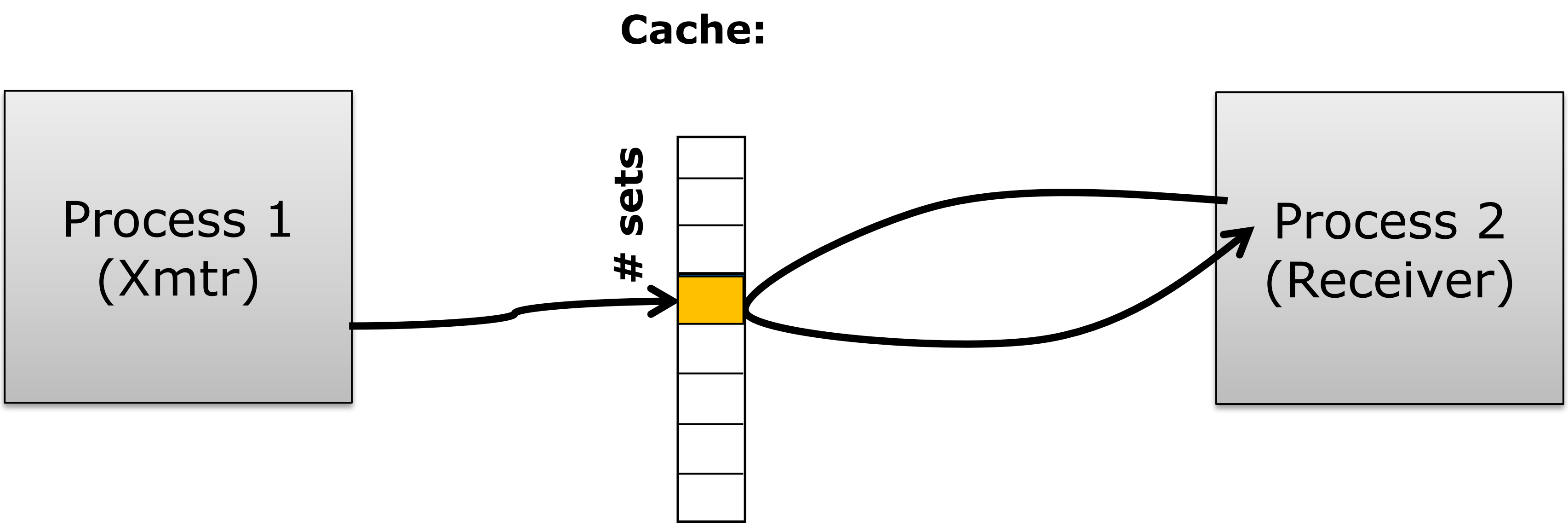

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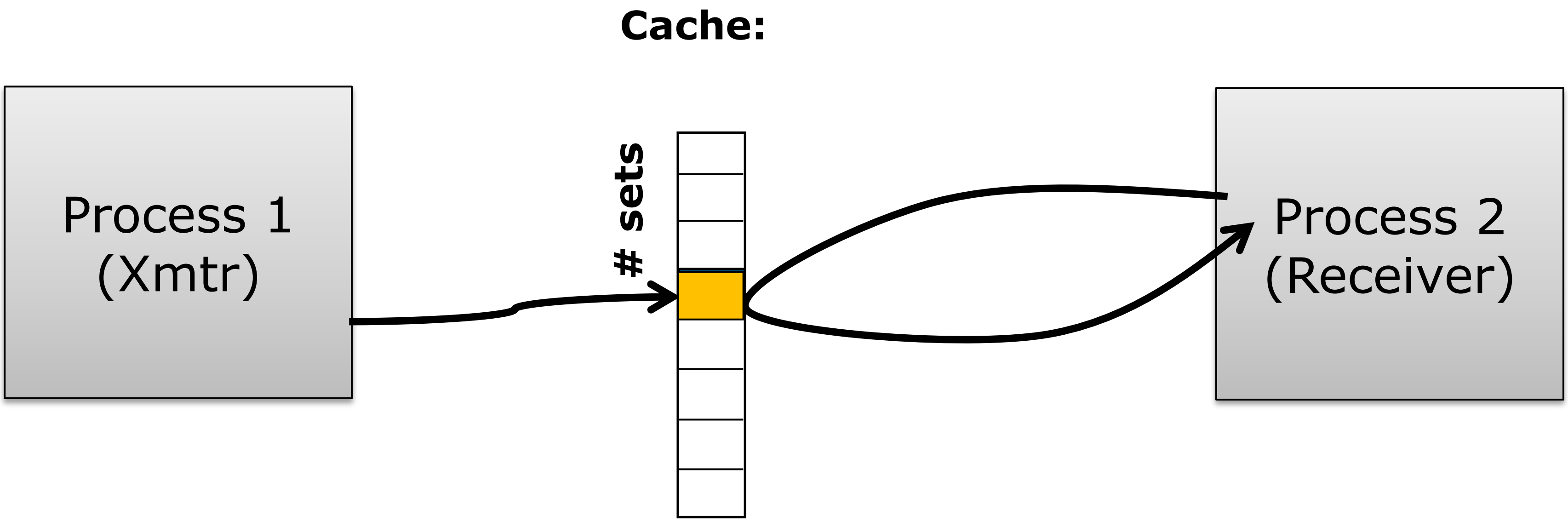

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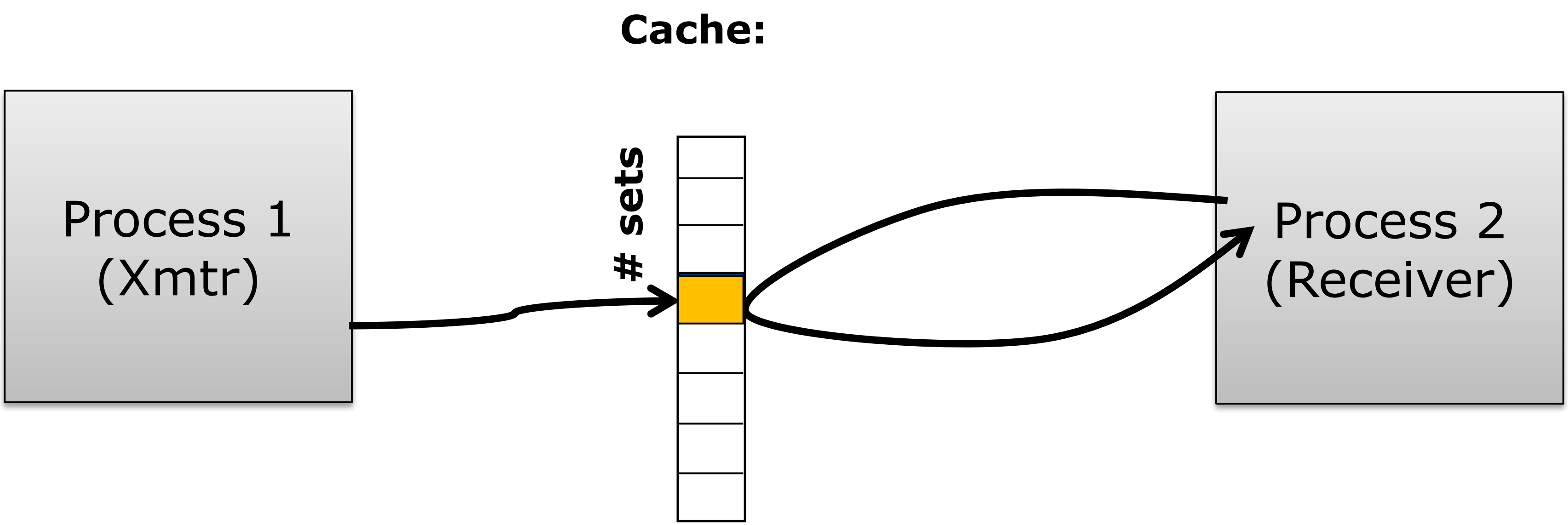

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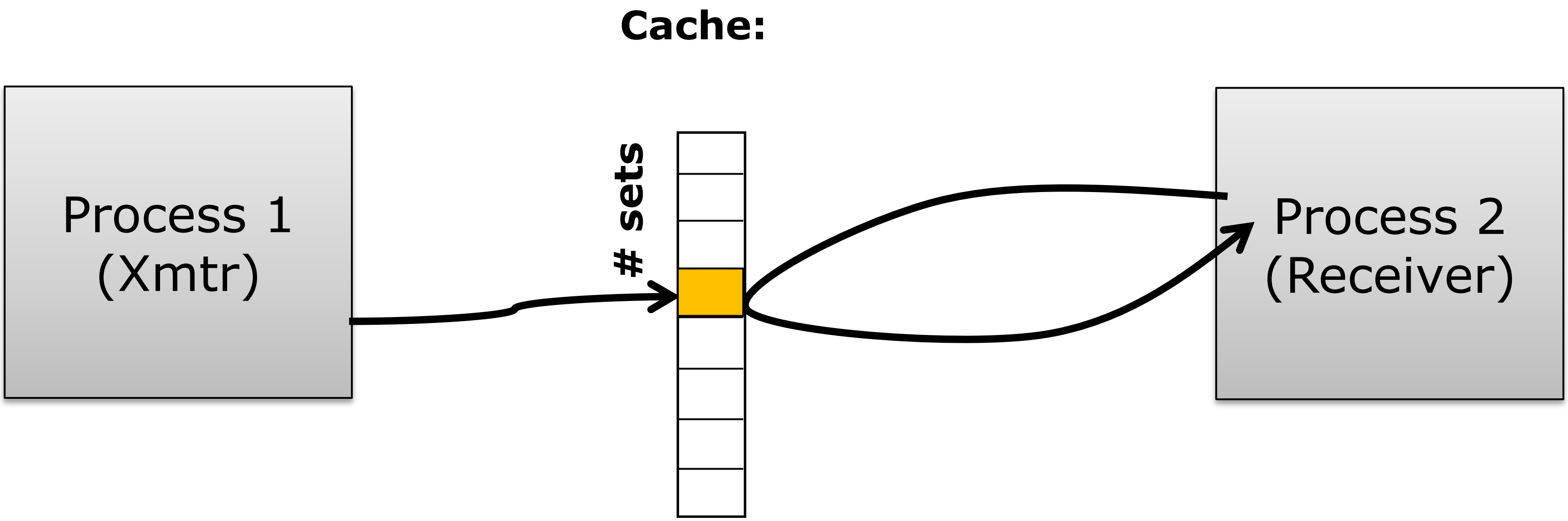

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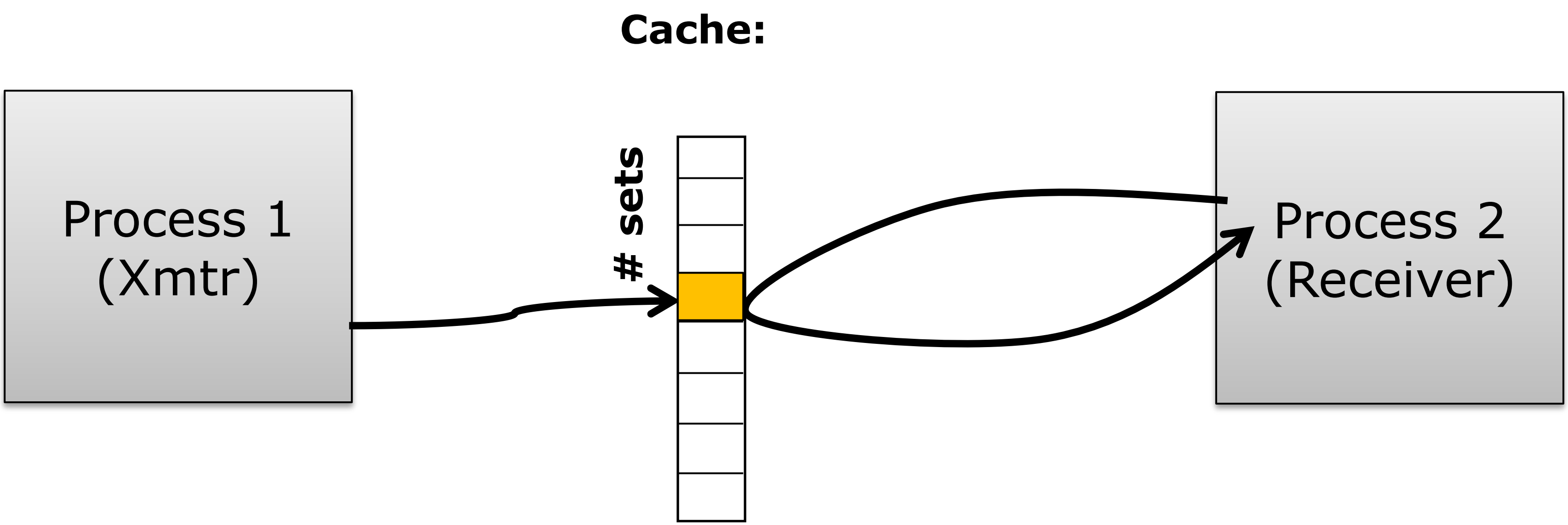

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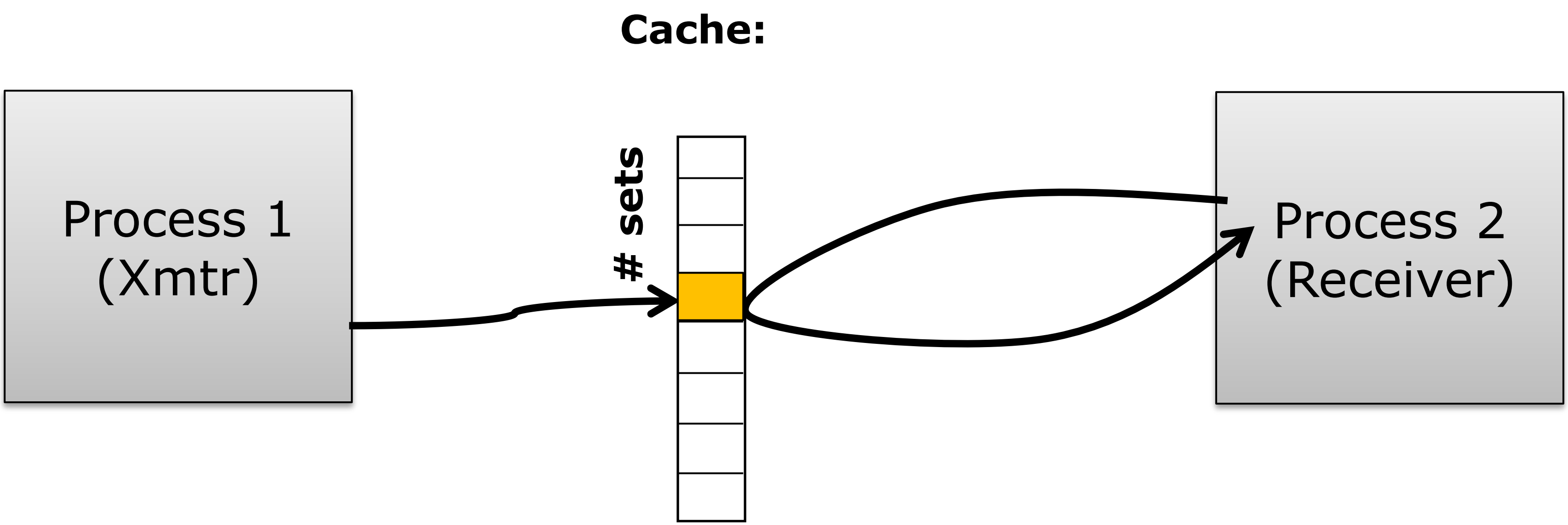

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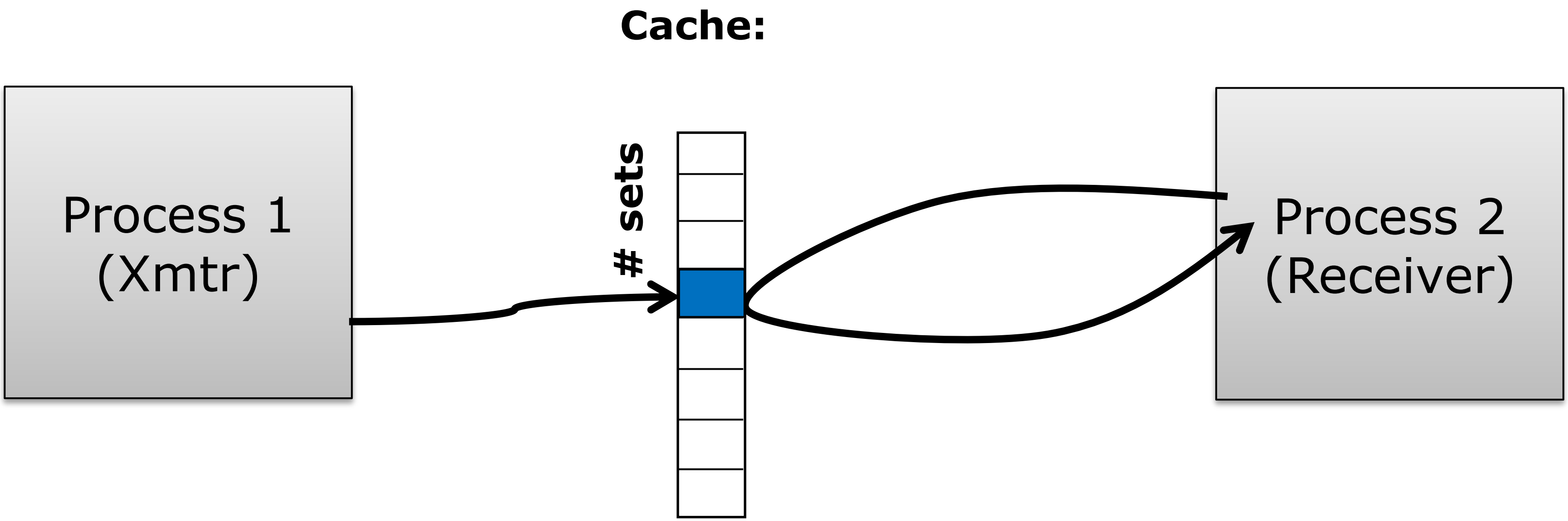

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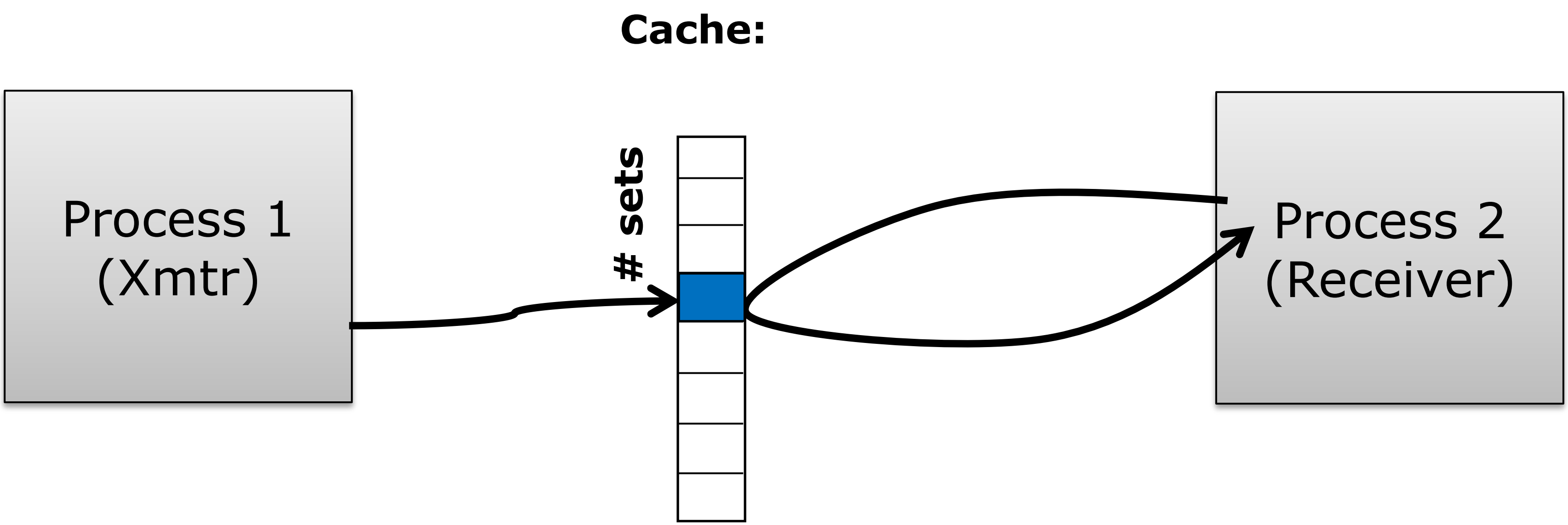

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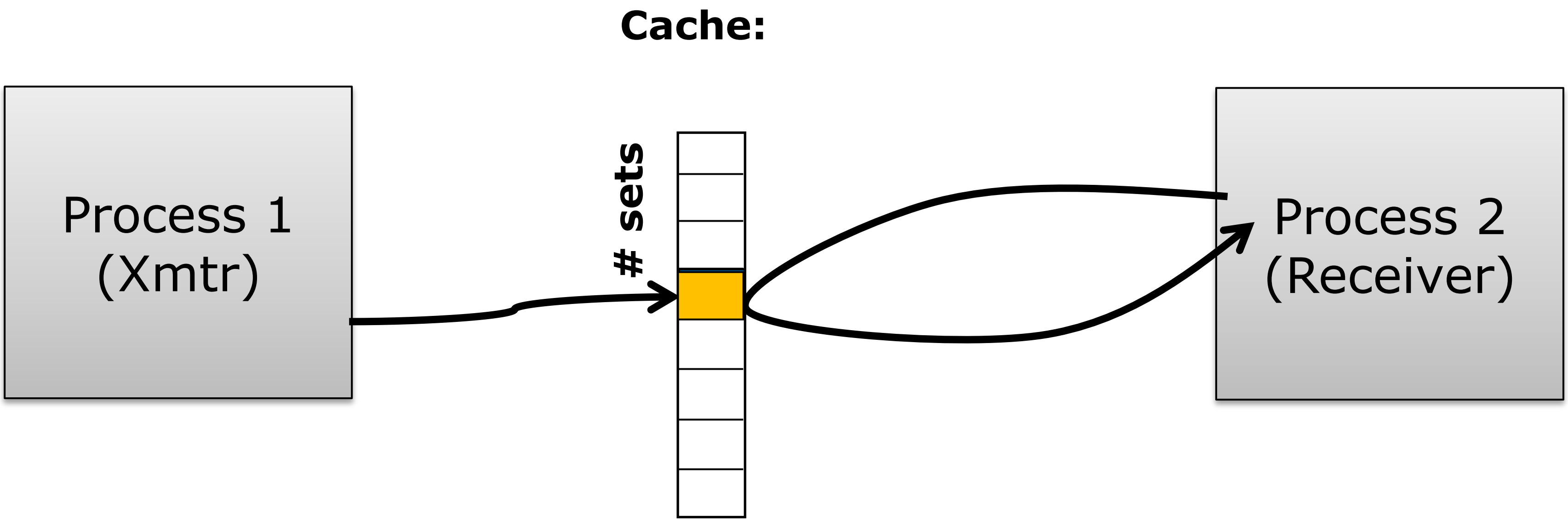

if (**send ‘0’**)
    idle
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write to set

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Transmitter in RSA [Percival 2005]

- Square-and-multiply based exponentiation

Input : base b, modulo m,
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Output: $b^e \bmod m$
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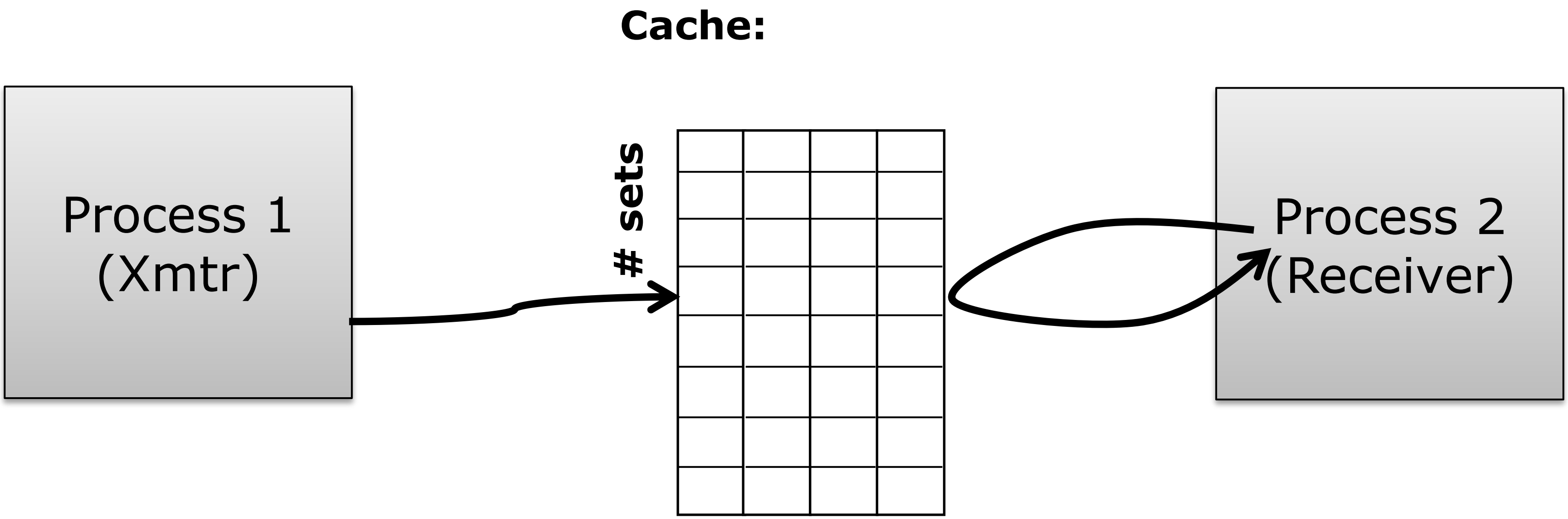
Secret-dependent memory access → transmitter

A Multi-way Cache-based Channel



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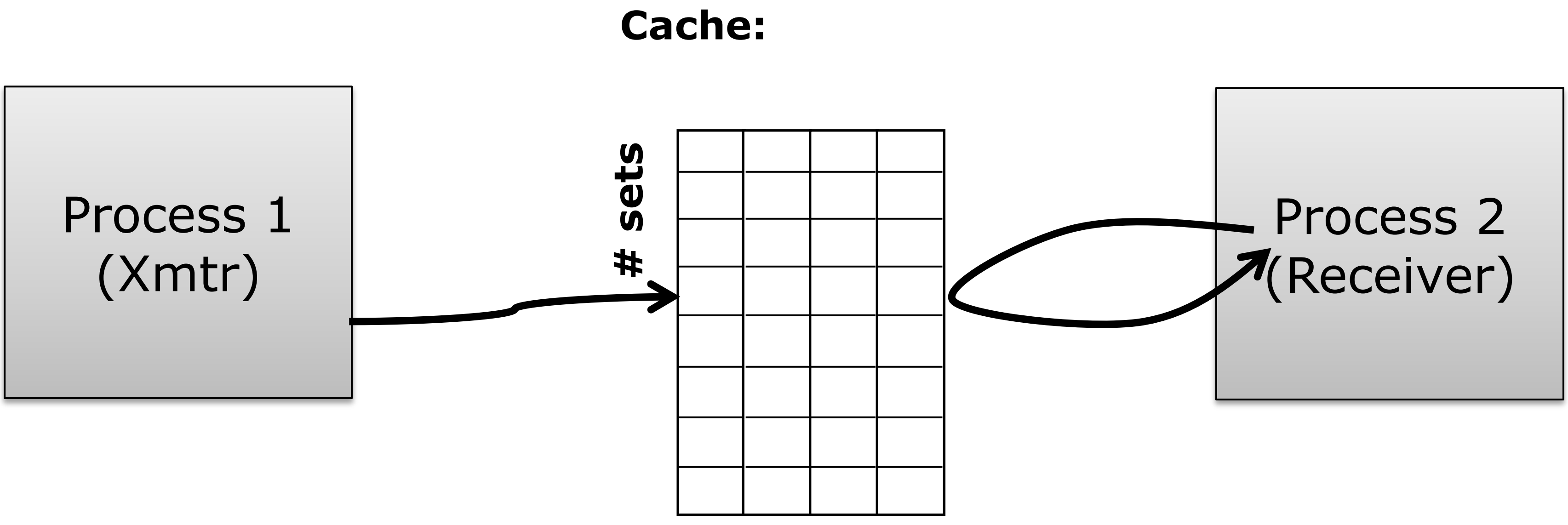

fill a set

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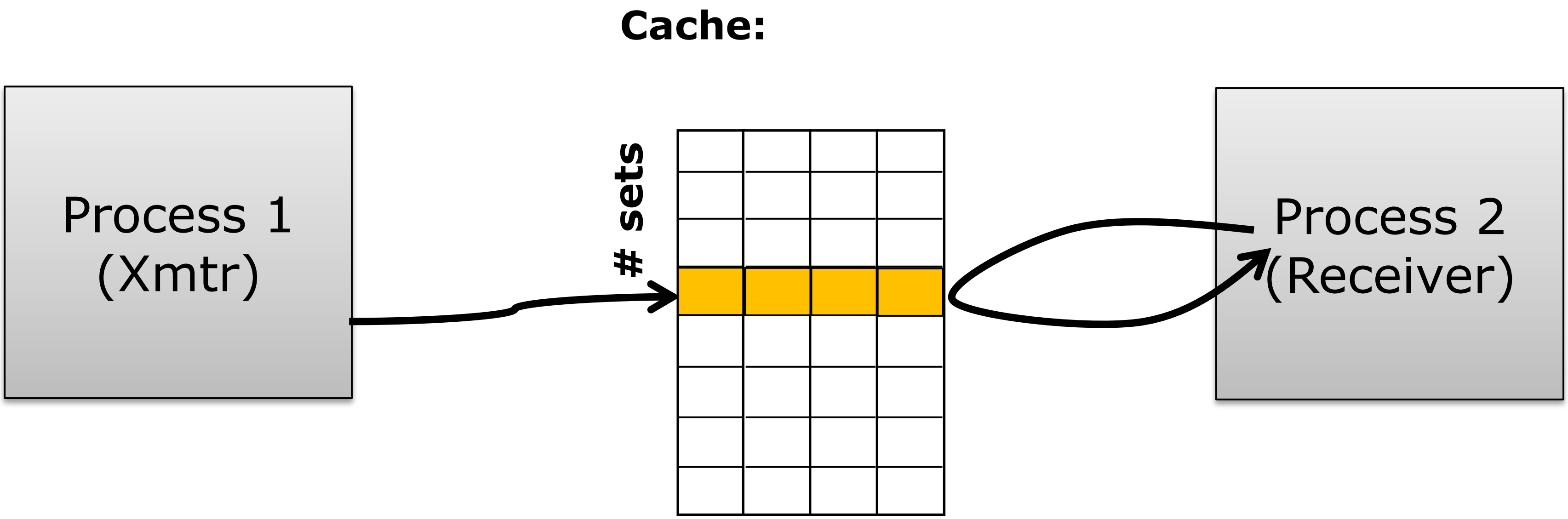

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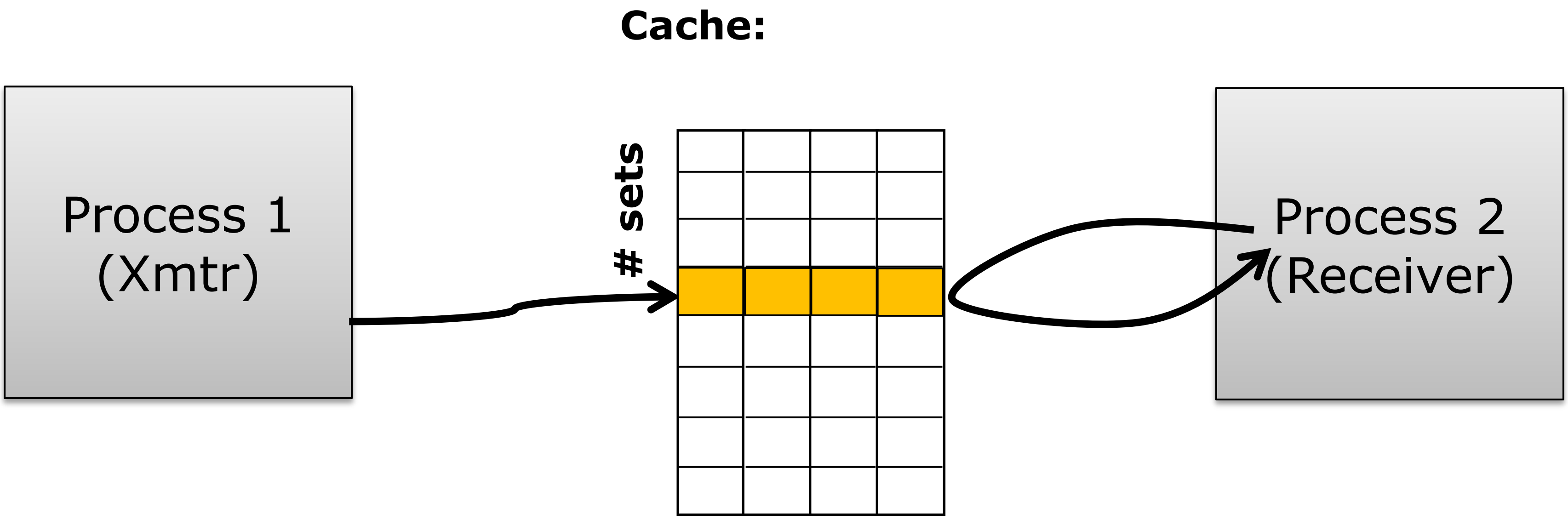

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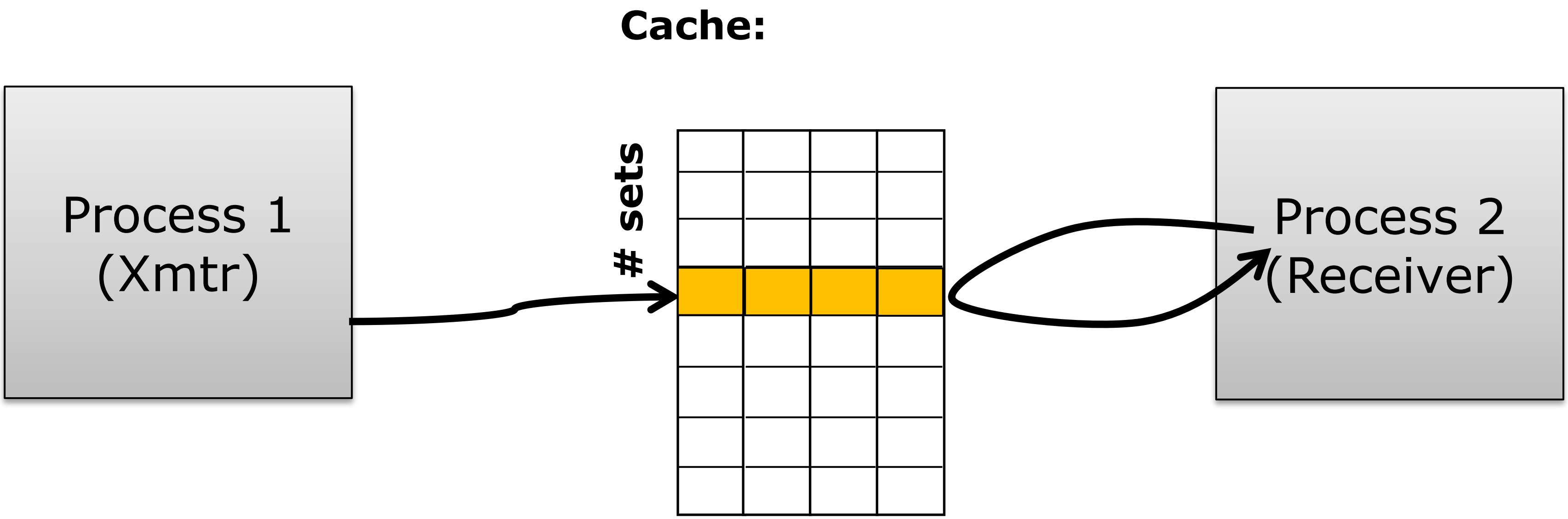

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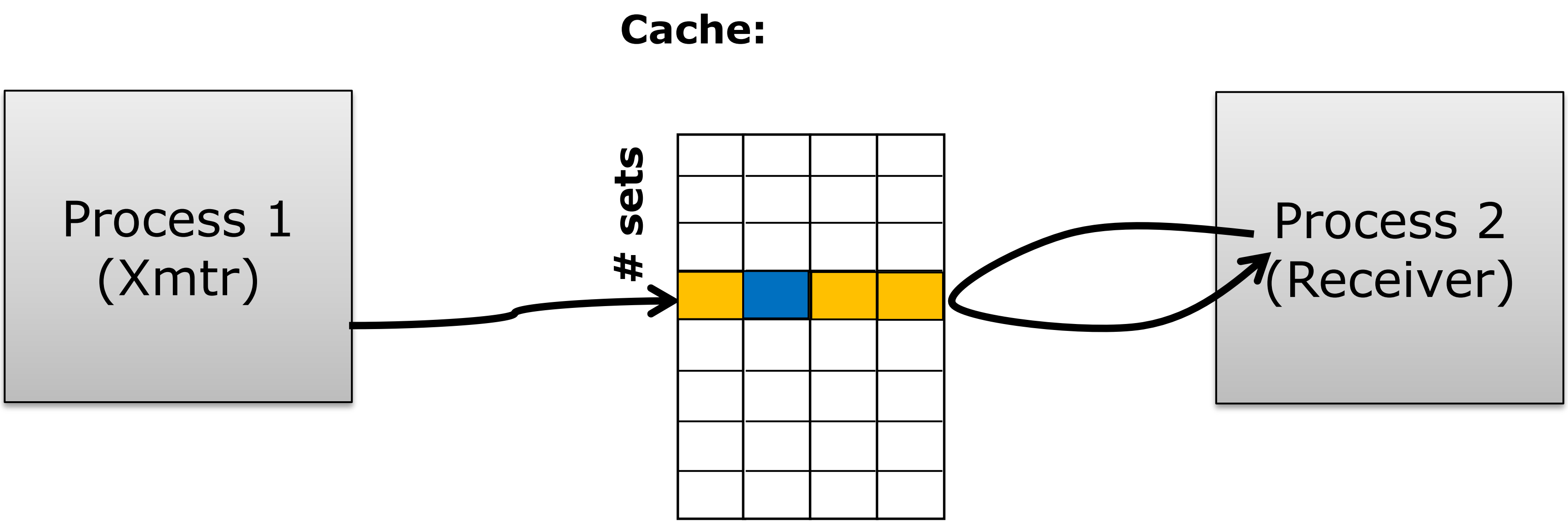

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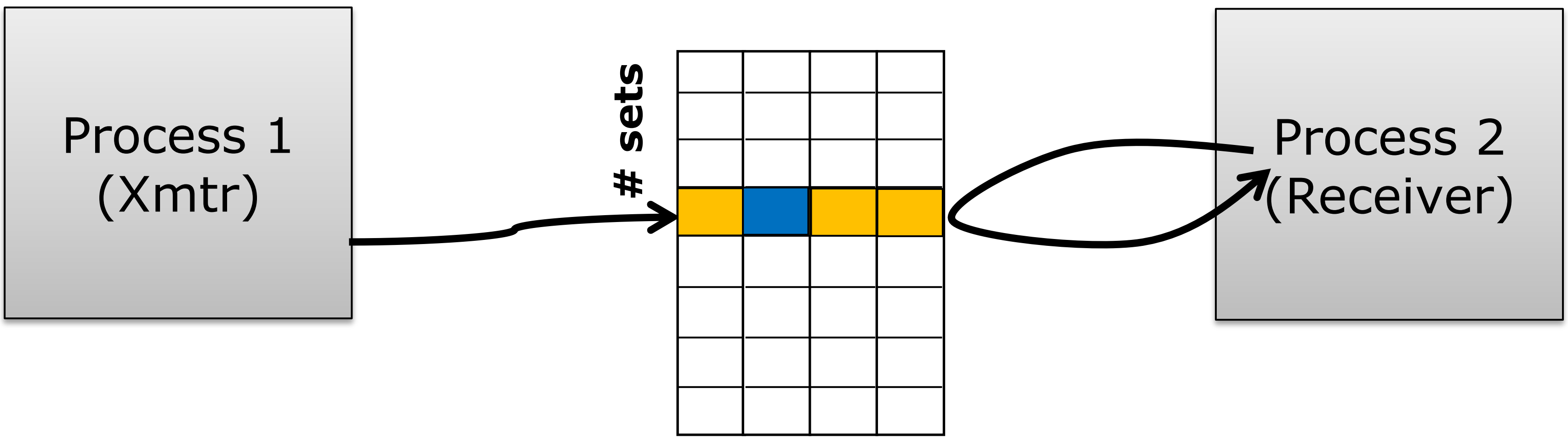

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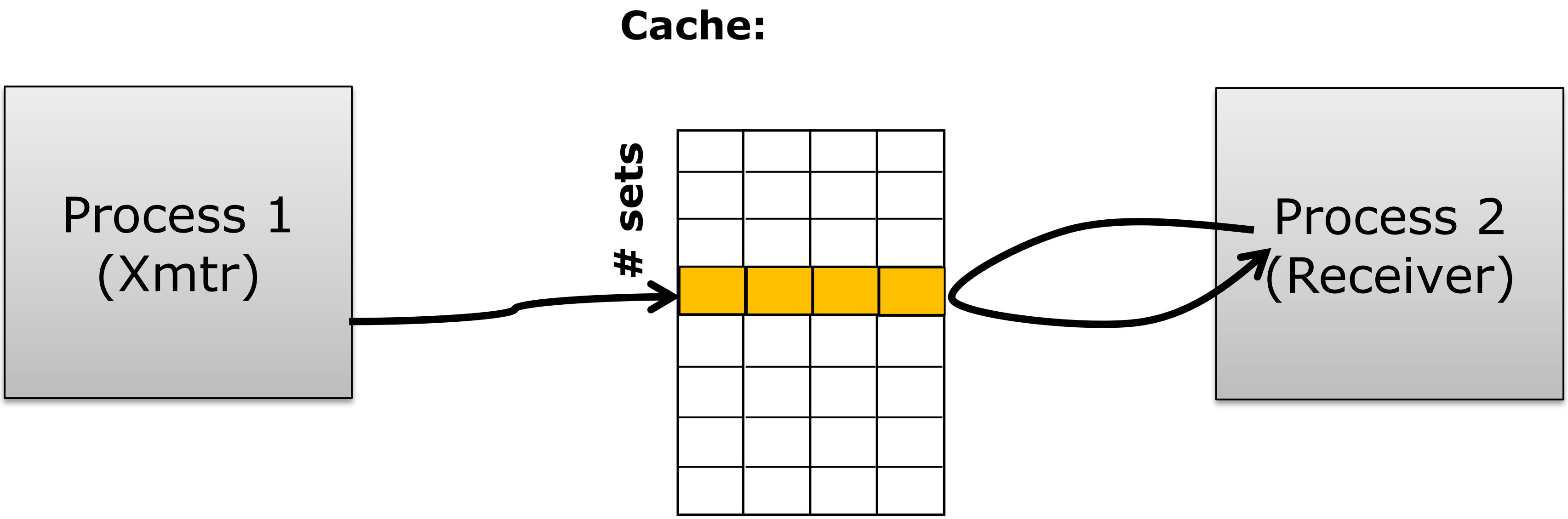

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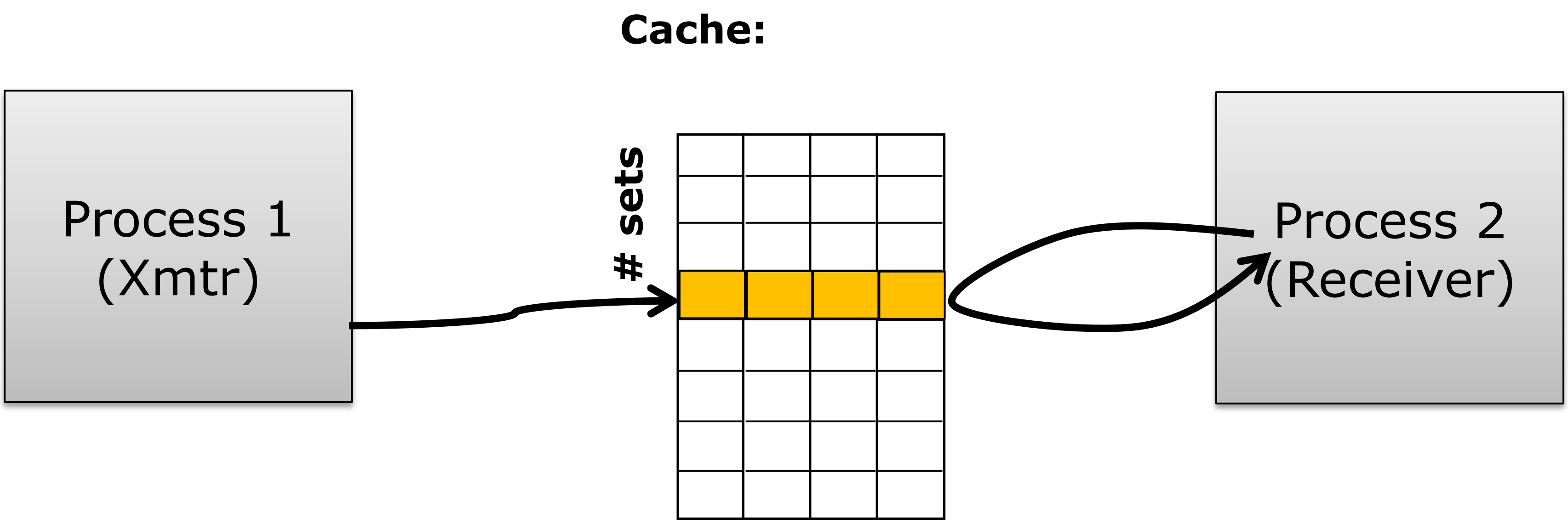

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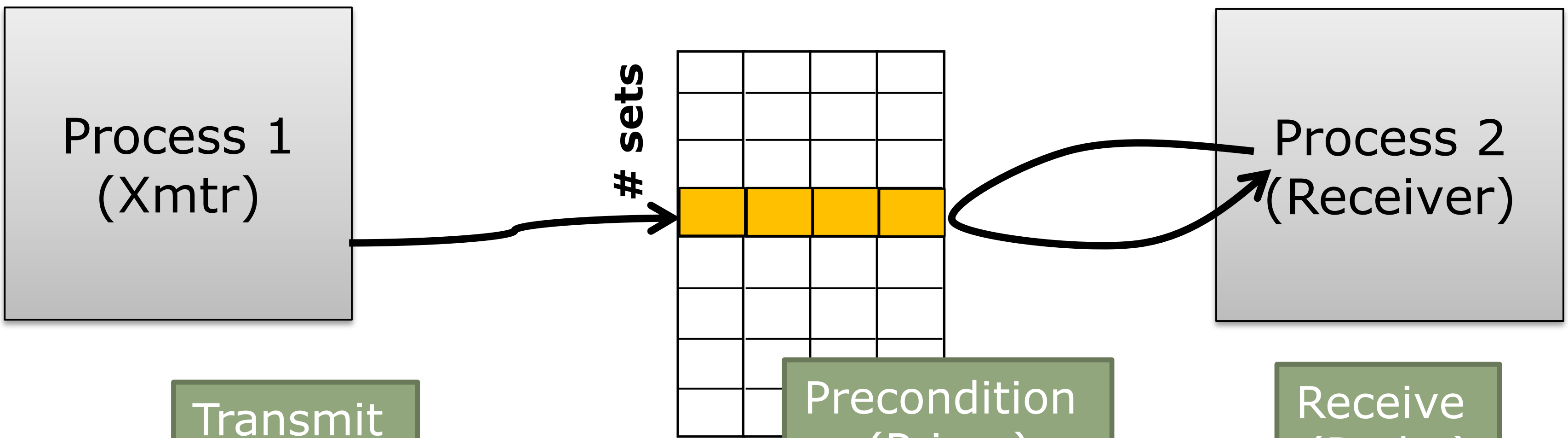

Transmit

if (**send '0'**)
    idle
else
    write to a set

Precondition (Prime)

fill a set

Receive (Probe)

t1 = rdtsc()
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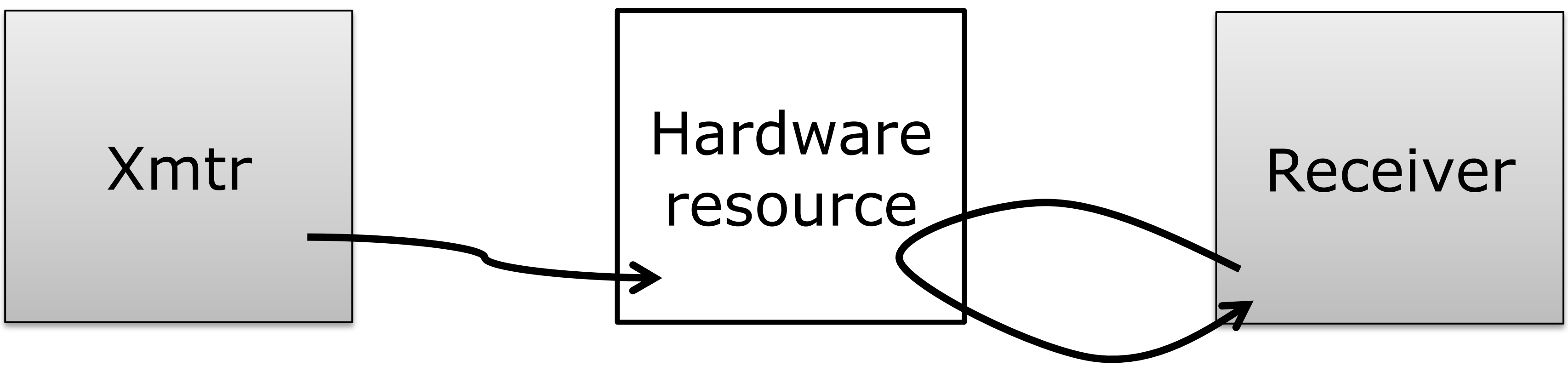
Decode

Generalizes to Other Resources



if (send ‘1’)
  Use resource
else
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t1 = rdtsc()
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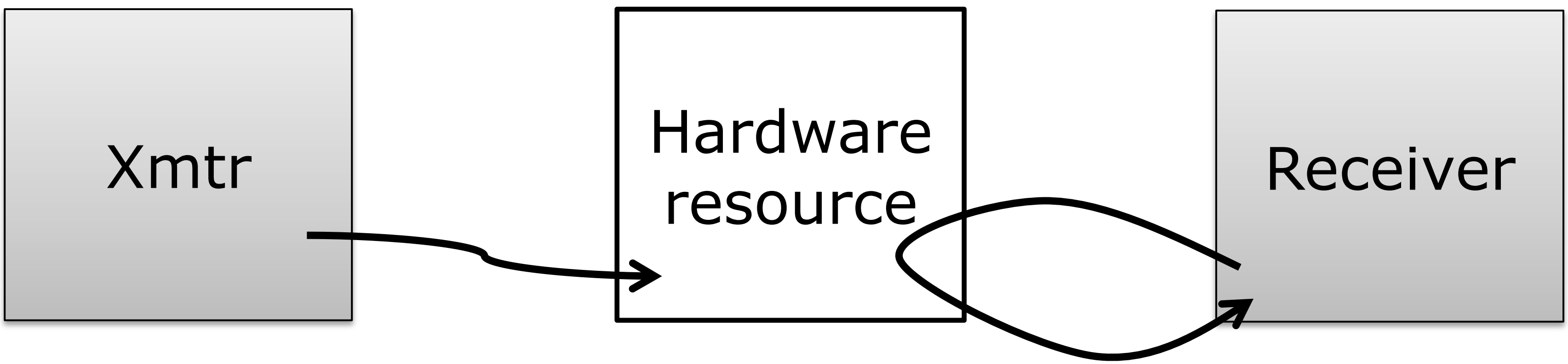

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    read '1'
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    read '0'

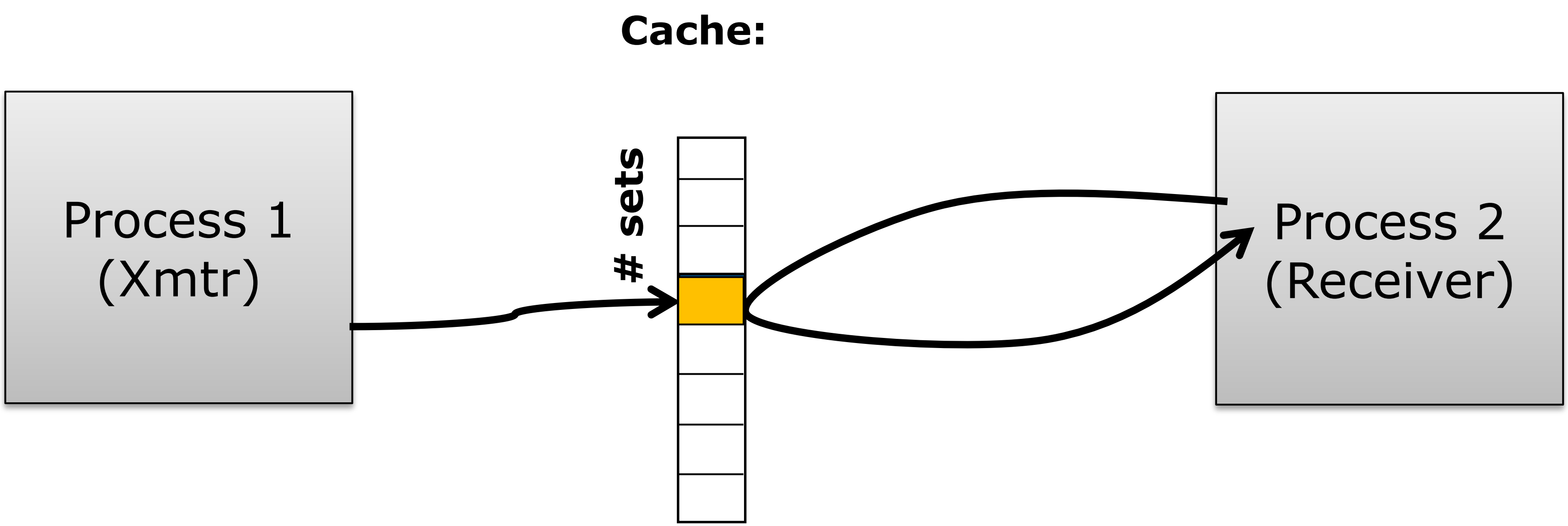
Any other exploitable structures?

Channel Examples

Resource	Shared by
Private cache (L1, L2)	Intra-core
Shared cache (LLC)	On-socket cross core
Cache directory	Cross socket
DRAM row buffer	Cross socket
TLB (private/shared)	Intra-core/Inter-core
Branch Predictor	Intra-core
Network-on-chip	On-socket cross core
…	…

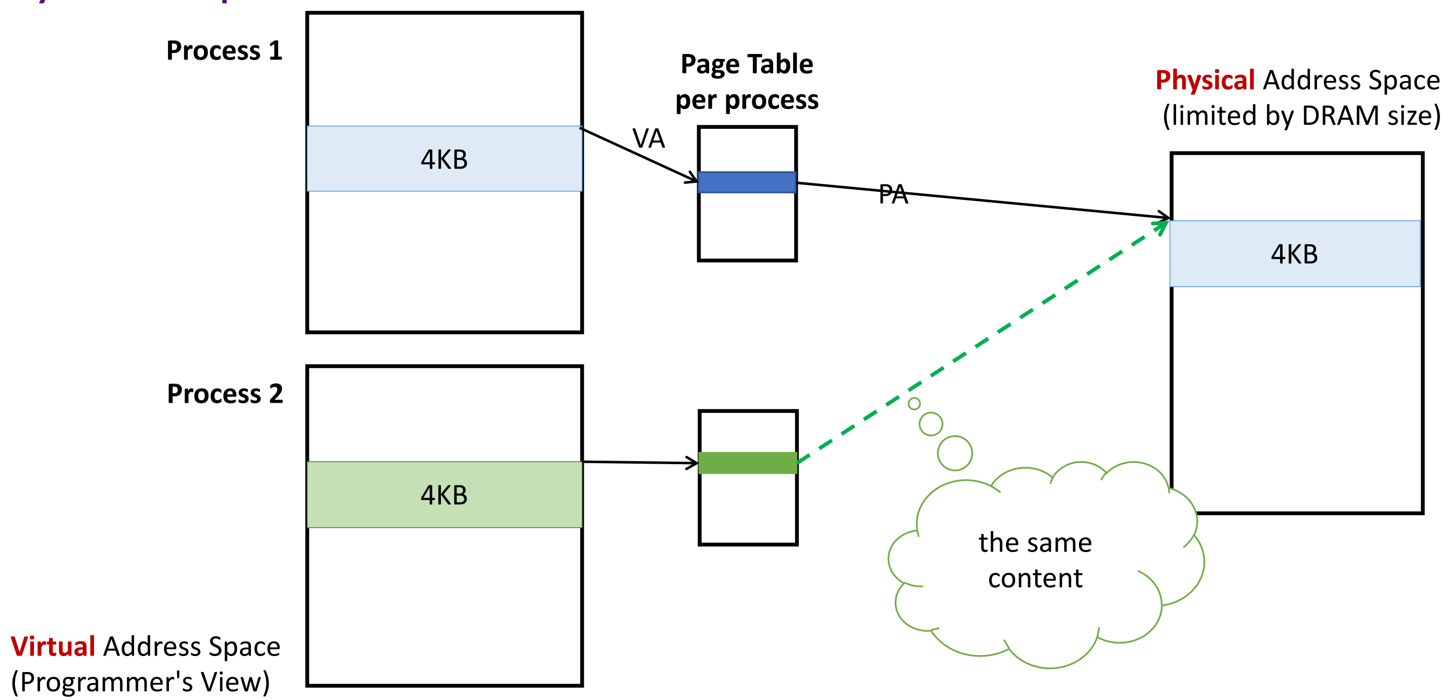
See Attack in Action: Flush+Reload

- The conceptual version
  - The sender and receiver shares addresses in a page
  - Sender repeated accesses address A or B
  - Receiver repeats:
    - flush A and B; using "clflush" -> precondition
    - wait for a few cycles; (sender does something) -> modulation
    - time how long it takes to reload A and B -> receive+decode



See Attack in Action: Page Sharing

- Virtual addresses in different processes map to the same physical address. When?
  - Lazy page allocation
  - Shared library
  - Memory de-duplication



See Attack in Action: Pseudocode

Sender:

```
buffer = mmap(4KB);
secret = getinput();

while (true){
    load buffer[secret*64];
}
```

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Why *64?

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buffer = mmap(4KB);
secret = getinput();

while (true){
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}
```

Why *64?

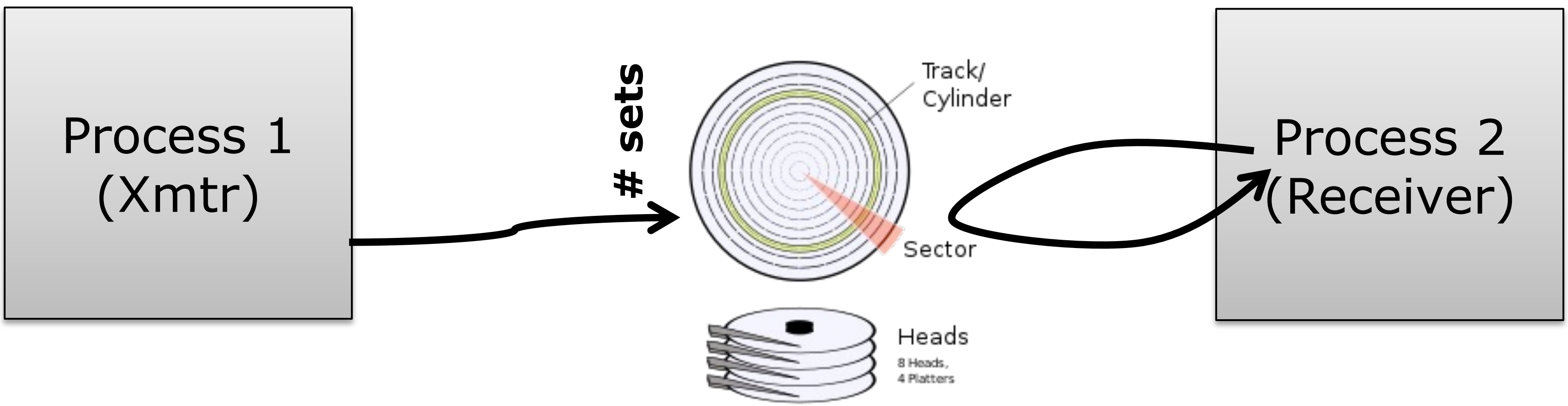
Receiver:

```
buffer = mmap(4KB);
hit_count [MAX] = 0;

for i in range(0,MAX){
    t1 = rdtsc();
    load buffer[i*64];
    t2 = rdtsc();
    if (t2-t1 > threshold){
        hit_count[i] ++;
    }
}
```

Disrupting Communication

Cache:



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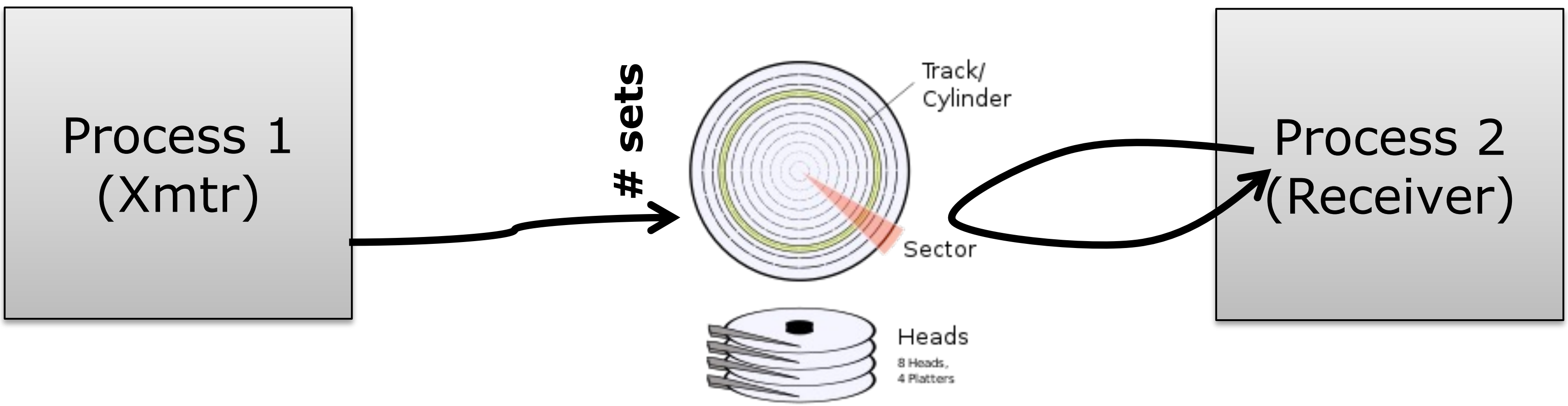
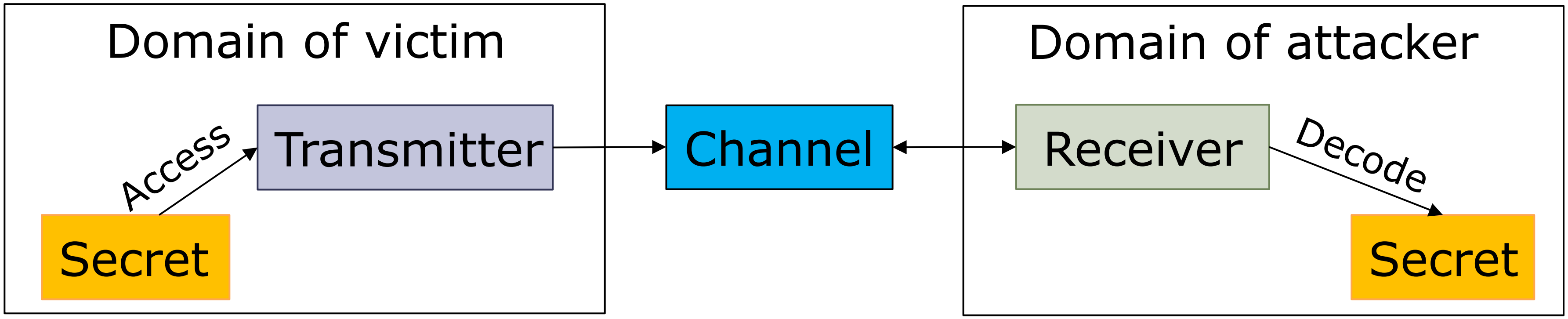


"We found that identifying all of the sources of accurate clocks was much **easier** than finding all of the possible timing channels in the system.
… If we could make the clocks less accurate, then the effective bandwidth of all timing channels in the system would be **lowered**." *(1991)*

Secret-independent Channel Modulation



- Different from conventional communication, this is a side channel (*unintended* communication).

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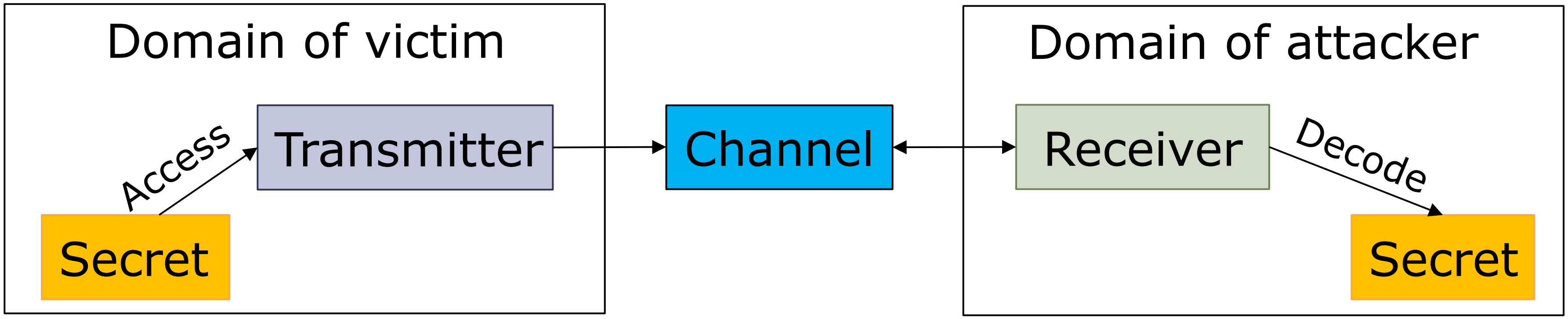

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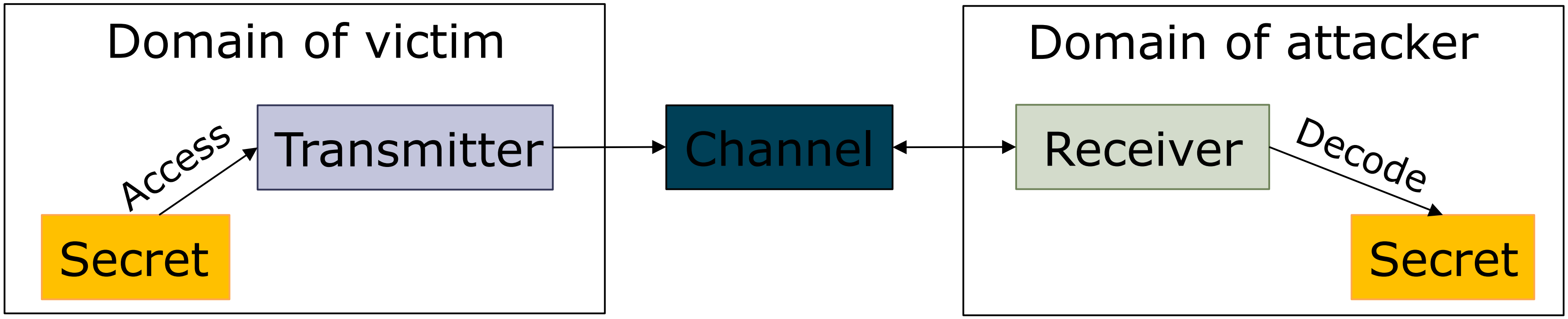

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-> ”data-oblivious execution” or “constant-time programming”.

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Output: $b^e \bmod m$
$r = 1$
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    if $\boldsymbol{e_i}$ **== 1 then**
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end
return r

How to make the code execution independent of the secret?

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No secret-dependent branches, memory accesses, floating point operations

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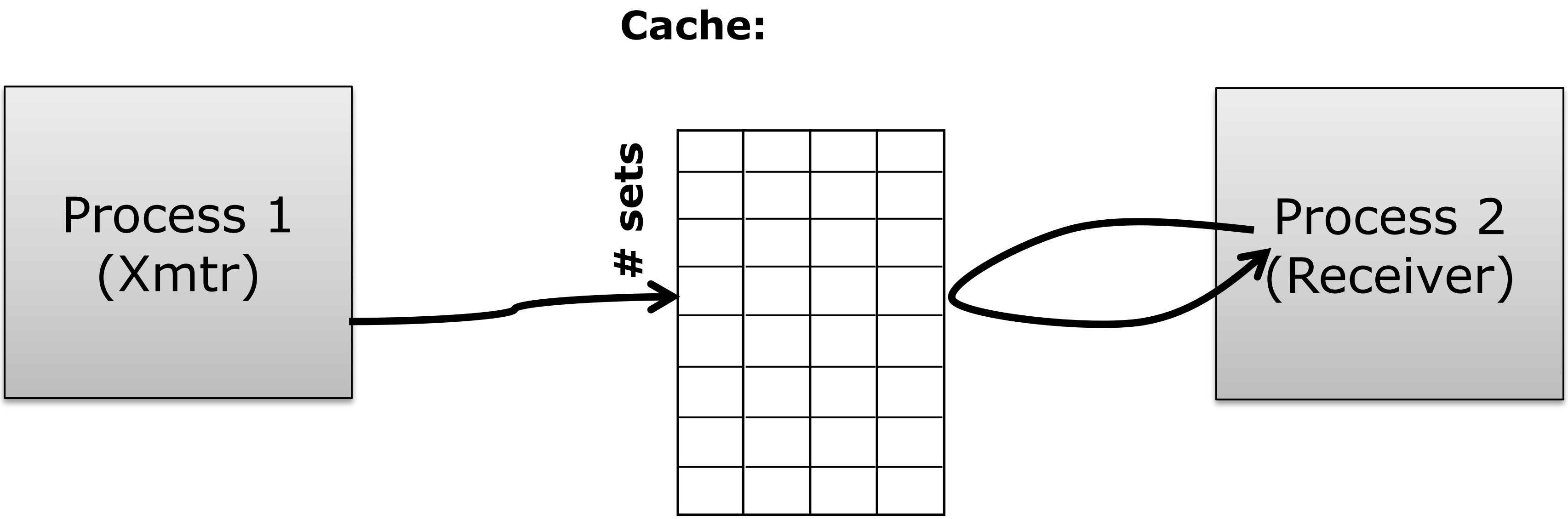
Constant-time programming is hard

Disrupting Communication



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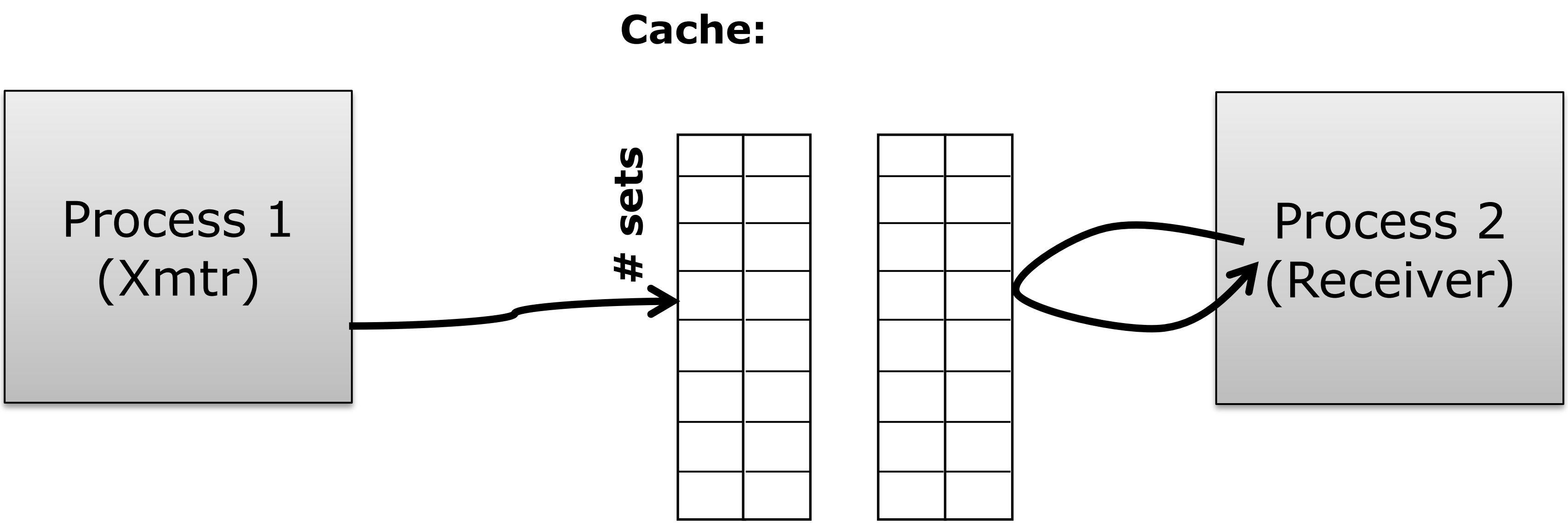

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Kirianski et. al. Dawg, Micro'18

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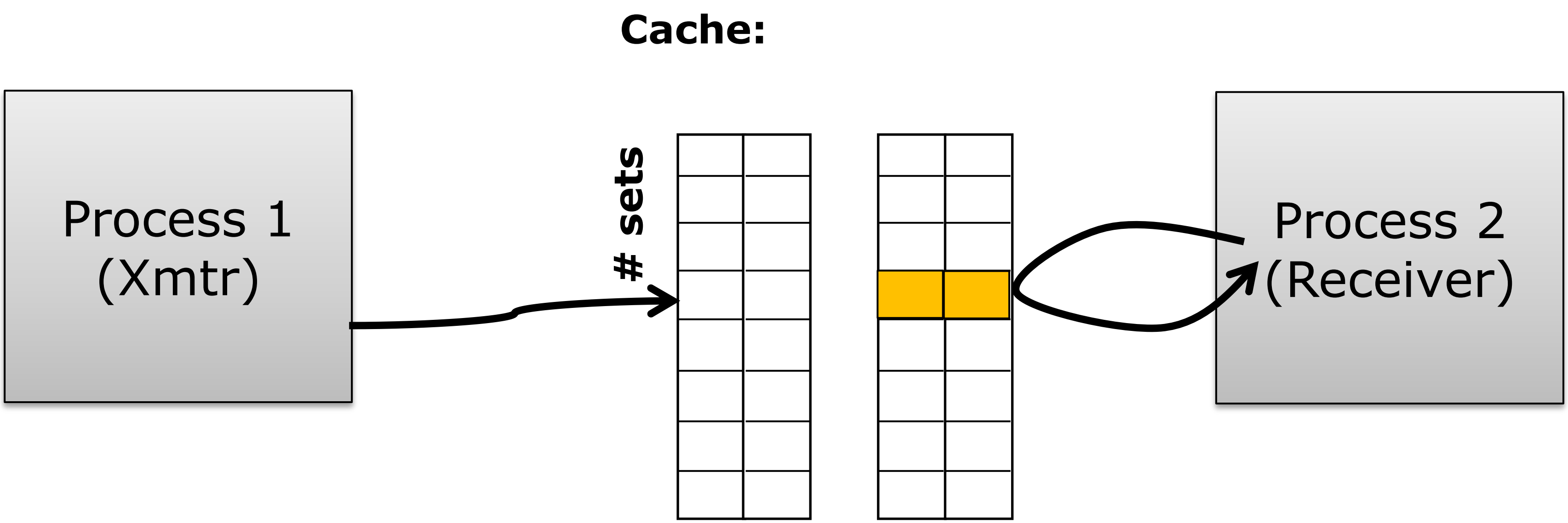

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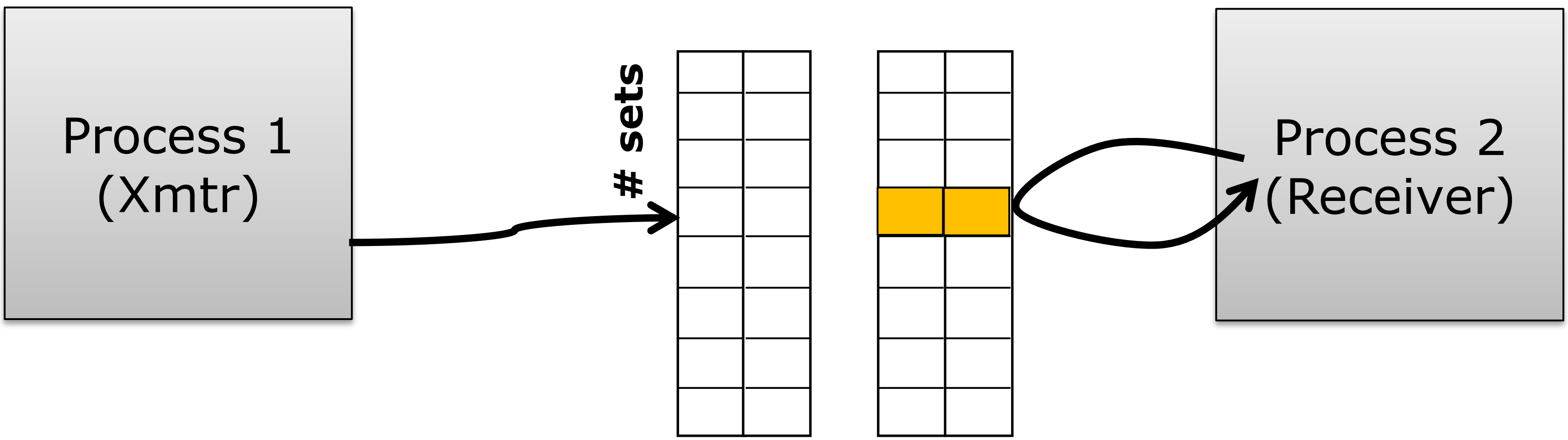

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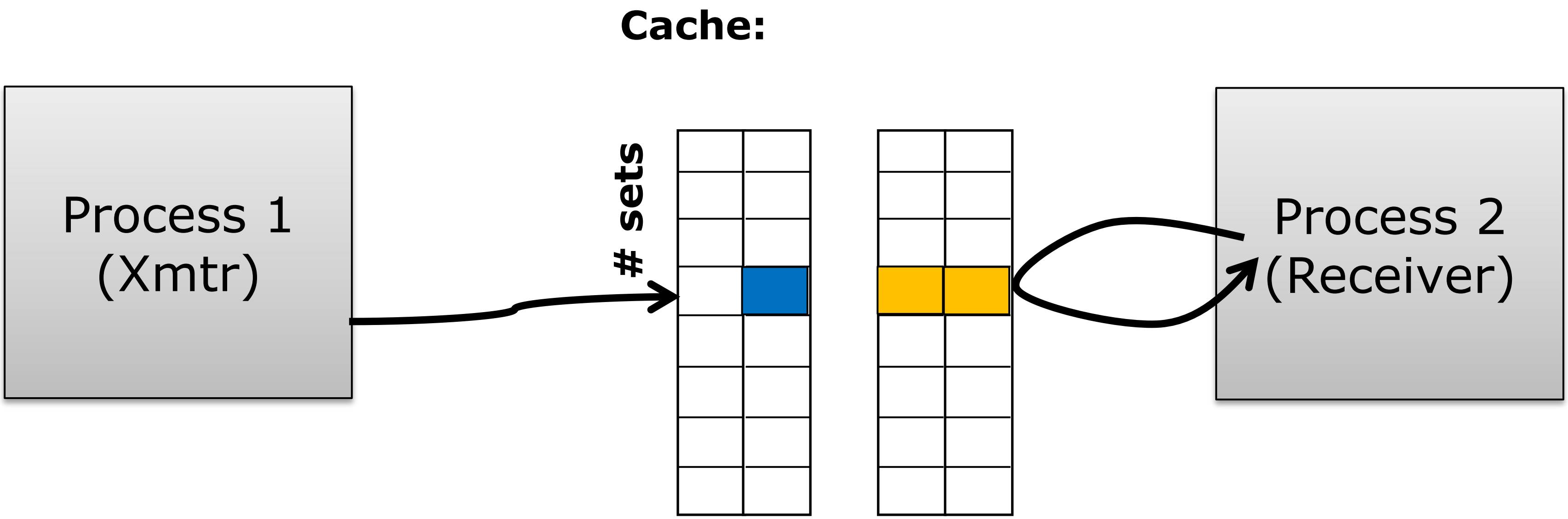

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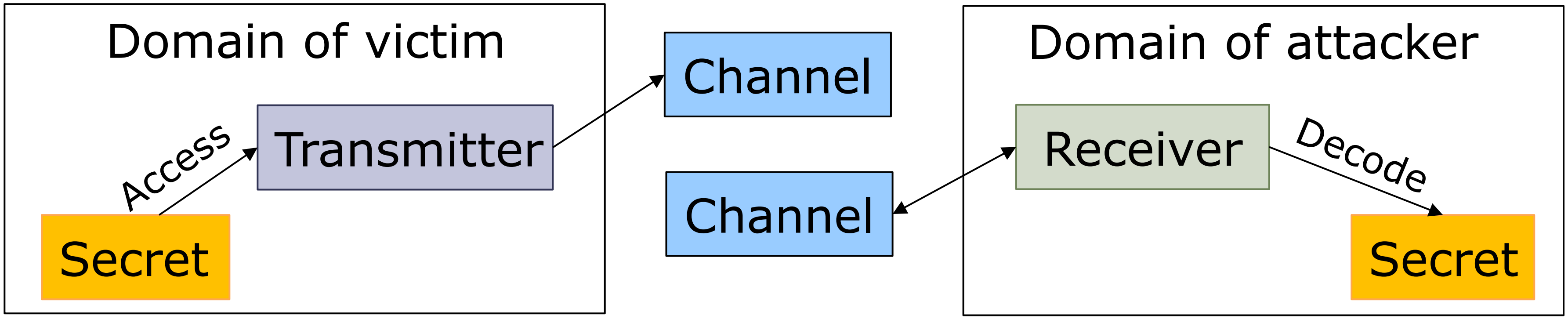
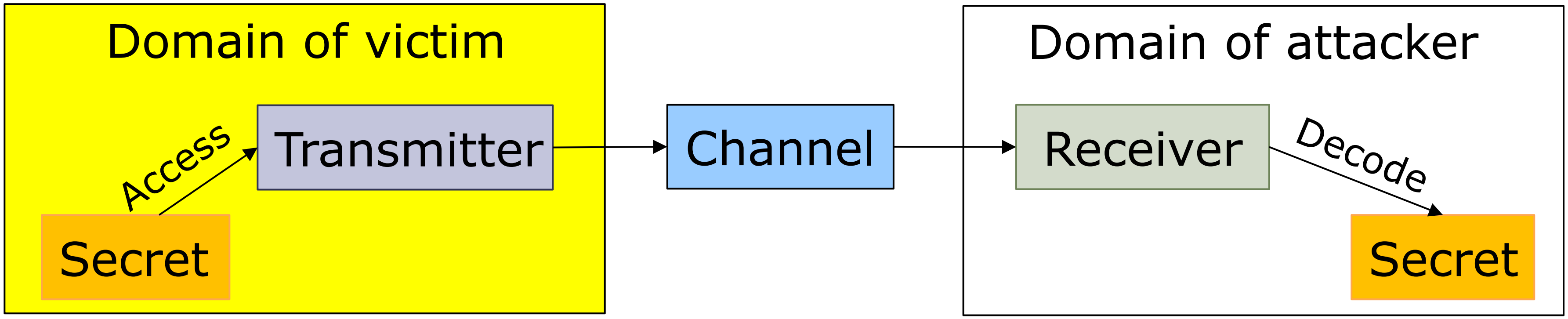
Disjoint Channels



- Making disjoint channels makes communication impossible.

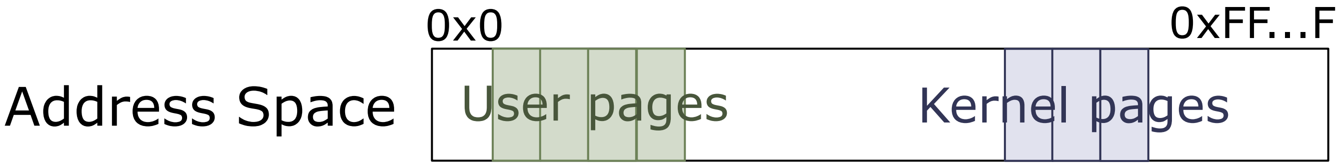
- Channel can be allocated by “domain” and will need to be “cleaned” as processes enter and leave running state, so next process cannot see any “modulation” on the channel.

Types of Transmitters



- Types of transmitter:
  1. Pre-existing so victim itself leaks secret, (e.g., RSA keys)
  2. Programmed and invoked by attacker (e.g., Meltdown)

Reminder: Speculative Execution



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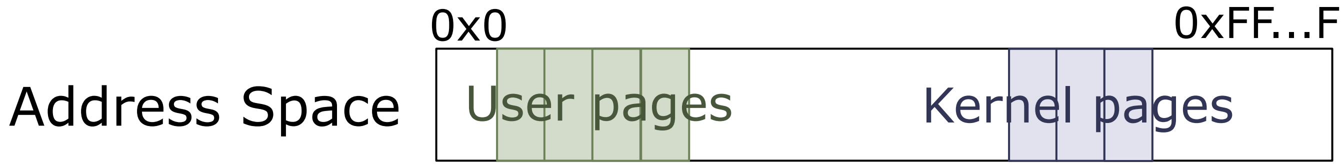

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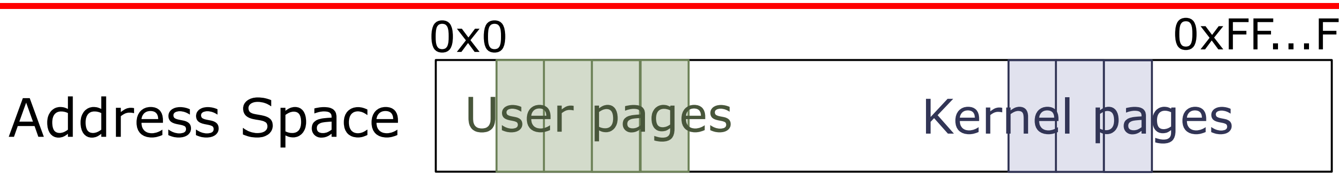

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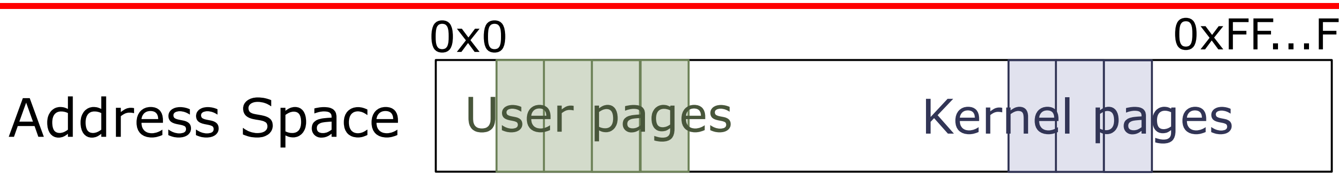

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- So what does the following code do when run in user mode do?

```
val = *kernel_address;
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- Causes a protection fault, but data at “kernel_address” is speculatively read and loaded into val.

Meltdown [Lipp et al. 2018]

1. Preconditioning: Receiver allocates an array `subchannels[256]` and flushes all its cache lines

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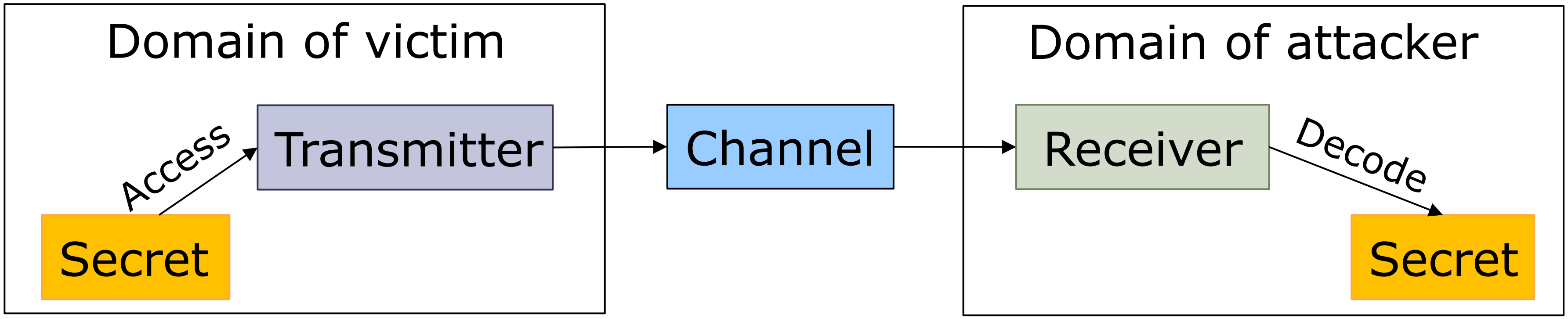
    Return zero upon permission check failure (supporting precise exception)

Types of Transmitters



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Conditional branch misprediction

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[Kocher et al. 2018]

- Consider the following kernel code, e.g., in a system call

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if (x < array1_size)
  y = array2[array1[x] * 4096];
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4. Receive: Attacker probes cache to infer which line of `array2` was fetched, learns data at kernel address

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[Kocher et al. 2018]

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training_branch

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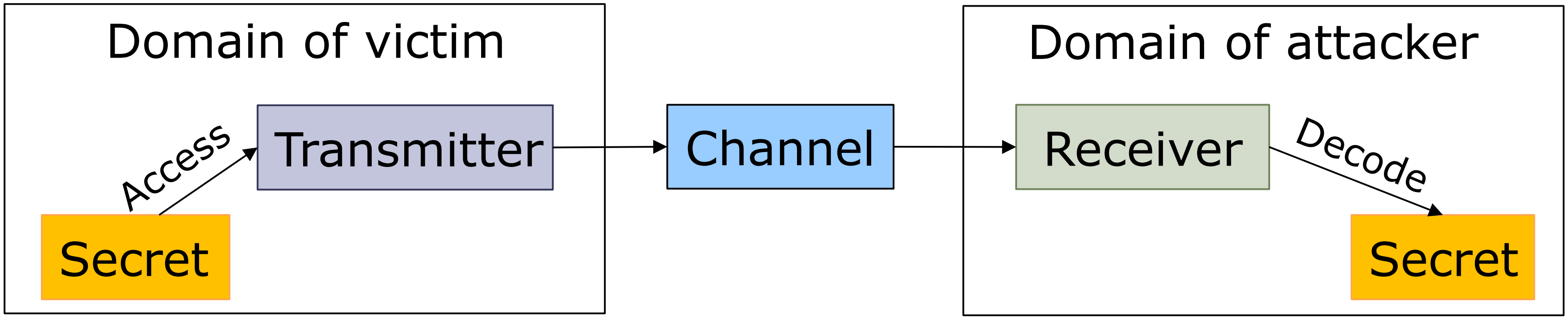
1. Train: trigger `victim_branch -> xmit` many times
2. Transmit: '`victim_branch`' and '`training_branch`' alias in BTB, so we can speculatively trigger `victim_branch -> xmit`
3. Receive: similar to Spectre v1

Types of Transmitters



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- Long-term mitigations:
  - Disabling speculation?
  - Closing side channels?

Summary

- ISA is a timing-independent interface, and
  - Specify *what* should happen, not *when*
- ISA only specifies architectural updates
  - *Micro-architectural changes are left unspecified*
- Implementation details (e.g., speculative execution) and timing behaviors (e.g., microarchitectural state, power, etc.) have been exploited to breach security mechanisms.
- ISA, as a software-hardware contract, is insufficient for reasoning about microarchitectural security

Coming Spring 2024: Secure Hardware Design 6.5950/1

Learn to attack processors…

Side channel attacks

Spectre, Meltdown, Foreshadow

Row-hammer attacks

Intel SGX

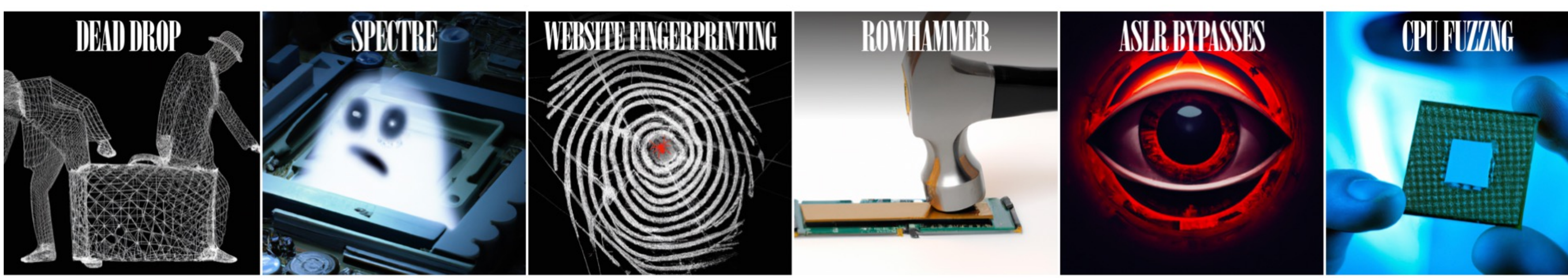
ARM TrustZone

Hardware mitigations for ROP/ JOP

And how to defend them!

Secure Hardware Design @ MIT

Making Computer Architecture Fun!



https://shd.mit.edu

Old number: 6.S983, 6.888

Thank you!