Cache Organization

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CPU-Memory Bottleneck

Performance of high-speed computers is usually limited by memory *bandwidth* & *latency*

- **Latency** (time for a single access)
  - Memory access time $>>$ Processor cycle time

- **Bandwidth** (number of accesses per unit time)
  - if fraction $m$ of instructions access memory,
    - $\Rightarrow 1+m$ memory references / instruction
    - $\Rightarrow$ CPI = 1 requires $1+m$ memory refs / cycle
Memory Technology

- Early machines used a variety of memory technologies
  - Manchester Mark I used CRT Memory Storage
  - EDVAC used a mercury delay line

- Core memory was first large scale reliable main memory
  - Invented by Forrester in late 40s at MIT for Whirlwind project
  - Bits stored as magnetization polarity on small ferrite cores threaded onto 2 dimensional grid of wires
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• Flash memory
  – Slower, but denser than DRAM. Also non-volatile, but with wearout issues

• Phase change memory (PCM, 3D XPoint)
  – Slightly slower, but much denser than DRAM and non-volatile
Bits stored in 2-dimensional arrays on chip
Modern chips have around 8 logical banks on each chip
- each logical bank physically implemented as many smaller arrays
DRAM timing

DRAM Spec:
CL, tRCD, tRP, tRAS, e.g., 9-9-9-24
Processor-DRAM Gap (latency)

The diagram shows the performance gap between processor and memory across different years from 1980 to 2010. The processor curve is consistently higher than the memory curve, indicating the increasing latency gap over time.
Processor-DRAM Gap (latency)

Four-issue 2GHz superscalar accessing 100ns DRAM could execute 800 instructions during time for one memory access!
**Little’s Law**

\[ \text{Throughput (T)} = \frac{\text{Number in Flight (N)}}{\text{Latency (L)}} \]

**Example:**

--- Assume infinite-bandwidth memory
--- 100 cycles / memory reference
--- 1 + 0.2 memory references / instruction

\[ \Rightarrow \text{Table size} = 1.2 \times 100 = 120 \text{ entries} \]

120 independent memory operations in flight!
Basic Static RAM Cell

6-Transistor SRAM Cell

- Write:
  1. Drive bit lines (bit=1, \( \overline{\text{bit}} = 0 \))
  2. Select word line

- Read:
  1. Precharge bit and \( \overline{\text{bit}} \) to Vdd
  2. Select word line
  3. Cell pulls one bit line low
  4. Column sense amp detects difference between bit & \( \overline{\text{bit}} \)
Multilevel Memory

Strategy: Reduce average latency using small, fast memories called caches.

Caches are a mechanism to reduce memory latency based on the empirical observation that the patterns of memory references made by a processor are often highly predictable:

```
...                         PC
96

loop:  add  r2, r1, r1     100
       subi r3, r3, #1      104
       bnez r3, loop       108
...                         112
```
Typical Memory Reference Patterns
Typical Memory Reference Patterns

Address

Instruction fetches

Time
Typical Memory Reference Patterns

Address

Instruction fetches

Time
Typical Memory Reference Patterns

Address

Instruction fetches

n loop iterations

Time
Typical Memory Reference Patterns

Address

Instruction fetches

Stack accesses

n loop iterations

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n loop iterations

subroutine call
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Time
Typical Memory Reference Patterns

- Instruction fetches
- Stack accesses

- Address
- Time

- n loop iterations
- subroutine call
- subroutine return
- argument access
Typical Memory Reference Patterns

- Instruction fetches
- Stack accesses
- Data accesses

Address

Time

n loop iterations

subroutine call

argument access

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Typical Memory Reference Patterns

- Instruction fetches
- Stack accesses
- Data accesses

Address vs. Time

- n loop iterations
- Subroutine call
- Argument access
- Subroutine return
Typical Memory Reference Patterns

Address

Instruction fetches

Stack accesses

Data accesses

Time

n loop iterations

subroutine call

argument access

subroutine return

vector access
Typical Memory Reference Patterns

- Instruction fetches
- Stack accesses
- Data accesses

Address

Time

n loop iterations

subroutine call

argument access

subroutine return

vector access

scalar accesses
Common Predictable Patterns

Two predictable properties of memory references:

– **Temporal Locality**: If a location is referenced it is likely to be referenced again in the near future.

– **Spatial Locality**: If a location is referenced it is likely that locations near it will be referenced in the near future.
Memory Hierarchy

- **size**: Register $<<$ SRAM $<<$ DRAM  
  - why?
- **latency**: Register $<<$ SRAM $<<$ DRAM  
  - why?
- **bandwidth**: on-chip $>>$ off-chip  
  - why?

On a data access:

- *hit* (data $\in$ fast memory) $\Rightarrow$ low latency access
- *miss* (data $\notin$ fast memory) $\Rightarrow$ long latency access *(DRAM)*
Management of Memory Hierarchy

- **Small/fast storage, e.g., registers**
  - Address usually specified in instruction
  - Generally implemented directly as a register file
    - but hardware might do things behind software’s back, e.g., stack management, register renaming

- **Large/slower storage, e.g., memory**
  - Address usually computed from values in register
  - Generally implemented as a cache hierarchy
    - hardware decides what is kept in fast memory
    - but software may provide “hints”, e.g., don’t cache or prefetch
Inside a Cache

Q: How many bits needed in tag? ___________________________
Inside a Cache

Q: How many bits needed in tag? **Enough to uniquely identify block**
Cache Algorithm (Read)

Look at Processor Address, search cache tags to find match. Then either
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  a.k.a. HIT

- Return copy of data from cache
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  - Wait ...
  - Return data to processor and update cache
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Which line do we replace?
Direct-Mapped Cache

Q: What is a bad reference pattern? ____________________
Q: What is a bad reference pattern?  **Strided at size of cache**
Direct Map Address Selection
higher-order vs. lower-order address bits

Index | Tag | Offset

HIT

2^k lines

Q: Why might this be undesirable? ________________________
Direct Map Address Selection
higher-order vs. lower-order address bits

Q: Why might this be undesirable? ________________

Spatially local blocks conflict
Q: What are the tradeoffs of hashing?
Hashed Address Mapping

Q: What are the tradeoffs of hashing?

Good: Regular strides don’t conflict
Bad: Hash adds latency
Tag is larger
2-Way Set-Associative Cache

- Tag
- Index
- Block Offset

Block Offset

V Tag Data Block

V Tag Data Block

HIT

Data Word or Byte

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MIT 6.823 Spring 2019
Fully Associative Cache

Diagram showing the interaction between the tag, data block, block offset, and data word or byte, leading to a hit signal.
Placement Policy

Set Number

Cache

Block Number

Memory

Direct Mapped

block 12 can be placed only into block 4 \((12 \mod 8)\)

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Placement Policy

Block Number

Memory

Set Number

Cache

Direct Mapped

(2-way) Set Associative

block 12 can be placed only into block 4 
(12 mod 8)

anywhere in set 0 
(12 mod 4)

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Placement Policy

Block Number

Memory

Set Number

Cache

block 12 can be placed

Direct Mapped only into block 4

(12 mod 8)

(2-way) Set Associative anywhere in set 0

(12 mod 4)

Fully Associative anywhere

block 12

(12 mod 8)
Improving Cache Performance

Average memory access time = Hit time + Miss rate \times Miss penalty

To improve performance:
- reduce the hit time
- reduce the miss rate (e.g., larger, better policy)
- reduce the miss penalty (e.g., L2 cache)

What is the simplest design strategy?
Improving Cache Performance

Average memory access time = 
Hit time + Miss rate x Miss penalty

To improve performance:
• reduce the hit time
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What is the simplest design strategy?

Biggest cache that doesn’t increase hit time past 1-2 cycles
(approx. 16-64KB in modern technology)
[design issues more complex with out-of-order superscalar processors]
Causes for Cache Misses

• **Compulsory:**
  First reference to a block *a.k.a.* cold start misses
  - misses that would occur even with infinite cache

• **Capacity:**
  cache is too small to hold all data the program needs
  - misses that would occur even under perfect placement & replacement policy

• **Conflict:**
  misses from collisions due to block-placement strategy
  - misses that would not occur with full associativity
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<td>&lt;</td>
<td>?</td>
</tr>
<tr>
<td>Hit latency</td>
<td>&gt;</td>
<td>&gt;</td>
<td>=</td>
</tr>
<tr>
<td>Miss latency</td>
<td>=</td>
<td>=</td>
<td>↑↓</td>
</tr>
</tbody>
</table>

* Assume substantial spatial locality
Block-level Optimizations

- Tags are too large, i.e., too much overhead
  - Simple solution: Larger blocks, but miss penalty could be large.
- Sub-block placement (aka sector cache)
  - A valid bit added to units smaller than the full block, called sub-blocks
  - Only read a sub-block on a miss
  - *If a tag matches, is the sub-block in the cache?*

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>300</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>204</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Replacement Policy

Which block from a set should be evicted?

- Random
- Least Recently Used (LRU)
  - LRU cache state must be updated on every access
  - true implementation only feasible for small sets (2-way)
  - pseudo-LRU binary tree was often used for 4-8 way
- First In, First Out (FIFO) a.k.a. Round-Robin
  - used in highly associative caches
- Not Least Recently Used (NLRU)
  - FIFO with exception for most recently used block or blocks
- One-bit LRU
  - Each way represented by a bit. Set on use, replace first unused.
Replacement Policy

Which block from a set should be evicted?

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Multiple replacement policies

Use the best replacement policy for a program

Cache

Sets

Miss

0: Policy A
1: Policy B
Multiple replacement policies

Use the best replacement policy for a program

How do we decide which policy to use?

Cache

Sets

Miss

0: Policy A
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Multiple replacement policies

Use the best replacement policy for a program

Cache

Sets

0: Policy A Missed
1: Policy B Missed

How do we decide which policy to use?

Miss

Counter

0: Policy A
1: Policy B

>0

+1 -1
Multiple replacement policies

Use the best replacement policy for a program

How do we decide which policy to use?

0: Policy A Missed
1: Policy B Missed

Sets

Policy A

Cache

Miss

0 > 0

Counter

+1

-1

0: Policy A
1: Policy B
Multiple replacement policies

Use the best replacement policy for a program

How do we decide which policy to use?

How do we decide which policy to use?

Cache

Sets

Policy A
Policy B

0: Policy A Missed
1: Policy B Missed

Counter

Miss

0: Policy A
1: Policy B

>0

+1
-1
Multilevel Caches

- A memory cannot be large and fast
- Add level of cache to reduce miss penalty
  - Each level can have longer latency than level above
  - So, increase sizes of cache at each level

Metrics:

Local miss rate = misses in cache / accesses to cache
Global miss rate = misses in cache / CPU memory accesses
Misses per instruction = misses in cache / number of instructions
Inclusion Policy

• **Inclusive multilevel cache:**
  – Inner cache holds copies of data in outer cache
  – External access need only check outer cache
  – Most common case

• *Exclusive* multilevel caches:
  – Inner cache may hold data not in outer cache
  – Swap lines between inner/outer caches on miss
  – Used in AMD Athlon with 64KB primary and 256KB secondary cache

Why choose one type or the other?
Victim Caches (HP 7200)

Victim cache is a small associative back up cache, added to a direct mapped cache, which holds recently evicted lines

- First look up in direct mapped cache
- If miss, look in victim cache
- If hit in victim cache, swap hit line with line now evicted from L1
- If miss in victim cache, L1 victim -> VC, VC victim->?

Fast hit time of direct mapped but with reduced conflict misses
Typical memory hierarchies

(a) Memory hierarchy for a server

- CPU
  - Registers
  - Level 1 Cache
    - Register reference
    - Size: 1000 bytes
    - Speed: 300 ps
  - Level 2 Cache
    - Level 1 Cache reference
    - Size: 64 KB
    - Speed: 1 ns
  - Level 3 Cache
    - Level 2 Cache reference
    - Size: 2–4 MB
    - Speed: 10–20 ns
  - Memory bus
  - Memory
    - Level 3 Cache reference
    - Size: 4–16 GB
    - Speed: 50–100 ns
  - I/O bus
  - Disk storage
    - Disk memory reference
    - Size: 4–16 TB
    - Speed: 5–10 ms

(b) Memory hierarchy for a personal mobile device

- CPU
  - Registers
  - Level 1 Cache
    - Register reference
    - Size: 500 bytes
    - Speed: 500 ps
  - Level 2 Cache
    - Level 1 Cache reference
    - Size: 64 KB
    - Speed: 2 ns
  - Level 2 Cache reference
    - Size: 256 KB
    - Speed: 10–20 ns
  - Memory bus
  - Memory
    - Memory reference
    - Size: 256–512 MB
    - Speed: 50–100 ns
  - Storage
    - FLASH memory reference
    - Size: 4–8 GB
    - Speed: 25–50 us
HBM DRAM or MCDRAM

Source: AMD
Mixed technology caching (Intel Knights Landing)
Thank you!

Next lecture:
Virtual memory