**Table: Control Data 6400/6500/6600/6700**

**Central Processor Instructions**

<table>
<thead>
<tr>
<th>Branch Unit</th>
<th>Multiply Unit</th>
<th>Divide Unit</th>
<th>Increment Unit</th>
<th>Booleans Unit</th>
<th>Shift Unit</th>
<th>Add Unit</th>
<th>Long Add Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 PS</td>
<td>40 FXI Xj * Xk Floating Product</td>
<td>44 FXI Xj/Xk Floating Divide</td>
<td>50 SAI Bj * K Sum of Aj &amp; K to Xi</td>
<td>10 HXI Xj</td>
<td>20 LXI jk</td>
<td>30 FXI Xj * Xk Floating Sum</td>
<td></td>
</tr>
<tr>
<td>01 JS</td>
<td>41 RXI Xj * Xk Round Floating Product</td>
<td>45 HXI Xj/Xk Round Floating Divide</td>
<td>51 SAI Bj * K Sum of Aj &amp; K to Bi</td>
<td>11 HXI Xj + Xk Logical Product</td>
<td>21 AXI jk</td>
<td>31 FXI Xj * Xx Floating Diff</td>
<td></td>
</tr>
<tr>
<td>02 JP</td>
<td>42 DXI Xj * Xk Floating DP Product</td>
<td>46 NO</td>
<td>52 SAI Xj * K Sum of Xj &amp; K to Ai</td>
<td>12 HXI Xj * Xx Logical Sum</td>
<td>22 AXI Bj Xk</td>
<td>32 DXI Xj * Xx Floating DP Sum</td>
<td></td>
</tr>
<tr>
<td>03 ZR</td>
<td>43 RXI Xj + Xk Sum of ones in Xj to Xk</td>
<td>47 CXI Xk</td>
<td>53 SAI Xj * K Sum of Xj &amp; K to Bi</td>
<td>13 HXI Xj * Xx Logical Difference</td>
<td>23 AXI Bj Xx</td>
<td>33 DXI Xj + Xx Floating DP Sum</td>
<td></td>
</tr>
<tr>
<td>04 PL</td>
<td>44 RXI Xj * Xk Round Floating Product</td>
<td>48 HXI Xj/Xk Round Floating Divide</td>
<td>54 SAI Xj * K Sum of Xj &amp; K to Bi</td>
<td>14 HXI Xx * Xj Log Prod Xj &amp; Xx comp to Xi</td>
<td>24 NIXI Xj Bj Normalizes Xx to Xi &amp; Bj</td>
<td>34 HXI Xj + Xx Floating DP Diff</td>
<td></td>
</tr>
<tr>
<td>05 NE</td>
<td>45 RXI Xj + Xk Sum of ones in Xj to Xk</td>
<td>49 CXI Xk</td>
<td>55 SAI Xj * K Sum of Xj &amp; K to Bi</td>
<td>15 HXI Xx + Xj Log Sum Xj &amp; Xx comp</td>
<td>25 ZXI Bj Xx</td>
<td>35 HXI Xj + Xx Round Floating Sum</td>
<td></td>
</tr>
<tr>
<td>06 GE</td>
<td>46 RXI Xj + Xk Sum of ones in Xj to Xk</td>
<td>50 SAI Xj * K Sum of Xj &amp; K to Bi</td>
<td>56 SAI Bj * K Sum of Bj &amp; K to Ai</td>
<td>16 HXI Xx + Xj Log Diff Xj &amp; Xx comp</td>
<td>26 UXI Bj Xx</td>
<td>36 HXI Xj + Xx Round Floating Diff</td>
<td></td>
</tr>
<tr>
<td>07 LT</td>
<td>47 CXI Xk</td>
<td>57 SAI Bj * K Sum of Bj &amp; K to Bi</td>
<td>58 SXI Xj * K Sum of Xj &amp; K to Bi</td>
<td>17 HXI Xx + Xx Log Diff Xj &amp; Xx comp</td>
<td>27 FXI Bj Xx</td>
<td>37 HXI Xj + Xx Integer Sum</td>
<td></td>
</tr>
</tbody>
</table>

**Extended Core Storage**

- Bit 0: Address out of range
- Bit 1: Operand out of range (Infinite)
- Bit 2: Indeterminate operand

**Symbols**

- Comp = Complement
- DP = Double Precision
- Xmit = Transmit

---

**CDC Programming Card**

March 8, 2017
Complex Pipelining: Out-of-Order Execution, Register Renaming, and Exceptions

Joel Emer
Computer Science and Artificial Intelligence Laboratory
M.I.T.
CDC 6600-style Scoreboard

Instructions are issued in order. An instruction is issued only if
- It cannot cause a RAW hazard
- It cannot cause a WAW hazard

\[ \Rightarrow \text{There can be at most one instruction in the execute phase that can write in a particular register} \]

WAR hazards are not possible
- Due to in-order issue + operands read immediately

Scoreboard:
Two bit-vectors

Busy[FU\#]: Indicates FU's availability
- These bits are hardwired to FU's.

WP[reg\#]: Records if a write is pending for a register
- Set to true by the Issue stage and set to false by the WB stage
### Scoreboard Dynamics

<table>
<thead>
<tr>
<th>Issue time</th>
<th>Functional Unit Status</th>
<th>Registers Reserved for Writes (WP)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Int(1) Add(1) Mult(3) Div(4) WB</td>
<td></td>
</tr>
<tr>
<td>t0</td>
<td></td>
<td>f6</td>
</tr>
<tr>
<td>t1</td>
<td>I_1</td>
<td>f6</td>
</tr>
<tr>
<td>t2</td>
<td>f2</td>
<td>f6</td>
</tr>
<tr>
<td>t3</td>
<td>I_3</td>
<td>f6</td>
</tr>
<tr>
<td>t4</td>
<td>f0</td>
<td>f6</td>
</tr>
<tr>
<td>t5</td>
<td>I_4</td>
<td>f6</td>
</tr>
<tr>
<td>t6</td>
<td>f0 f8</td>
<td>f6</td>
</tr>
<tr>
<td>t7</td>
<td>I_5</td>
<td>f6</td>
</tr>
<tr>
<td>t8</td>
<td>f8 f10</td>
<td>f6</td>
</tr>
<tr>
<td>t9</td>
<td>f8</td>
<td>f6</td>
</tr>
<tr>
<td>t10</td>
<td>I_6</td>
<td>f6</td>
</tr>
<tr>
<td>t11</td>
<td></td>
<td>f6</td>
</tr>
</tbody>
</table>

- **I_1** DIVD f6, f6, f4
- **I_2** LD f2, 45(r3)
- **I_3** MULTD f0, f2, f4
- **I_4** DIVD f8, f6, f2
- **I_5** SUBD f10, f0, f6
- **I_6** ADDD f6, f8, f2

September 27, 2021  MIT 6.823 Fall 2021
In-Order Issue Limitations
An example

In-order: 1 (2,1) ... ... 2 3 4 4 3 5 ... 5 6 6

In-order restriction prevents instruction 4 from being dispatched
Out-of-Order Issue

How can we address the delay caused by a RAW dependence associated with the next in-order instruction?

- Issue stage buffer holds multiple instructions waiting to issue.
- Decode adds next instruction to buffer if there is space and the instruction does not cause a WAR or WAW hazard.
- Can issue any instruction in buffer whose RAW hazards are satisfied (for now at most one dispatch per cycle).

*Note:* A writeback (WB) may enable more instructions.
In-Order Issue Limitations

An example

<table>
<thead>
<tr>
<th></th>
<th>Instruction</th>
<th>Sources</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LD F2, 34(R2)</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>LD F4, 45(R3)</td>
<td></td>
<td>long</td>
</tr>
<tr>
<td>3</td>
<td>MULTD F6, F4, F2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SUBD F8, F2, F2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DIVD F4, F2, F8</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>ADDD F10, F6, F4</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

In-order: 1 (2,1) . . . . . . 2 3 4 4 3 5 . . . 5 6 6
Out-of-order: 1 (2,1) 4 4 . . . . 2 3 5 . 3 . 5 6 6

WAR/WAW hazards prevent instruction 5 from being dispatched

Out-of-order execution did not produce a significant improvement!
How many Instructions can be in the pipeline

Throughput is limited by number of instructions in flight, but which feature of an ISA limits the number of instructions in the pipeline?

**Number of Registers**

Out-of-order dispatch by itself does not provide a significant performance improvement!

How can we better understand the impact of number of registers on throughput?
Little’s Law

*Throughput (\( \bar{T} \)) = Number in Flight (\( \bar{N} \)) / Latency (\( \bar{L} \))*

Example:

4 floating point registers
8 cycles per floating point operation

\[ \Rightarrow \frac{1}{2} \text{ issues per cycle!} \]
Overcoming the Lack of Register Names

Floating Point pipelines often cannot be kept filled with small number of registers.
IBM 360 had only 4 Floating Point Registers

Can a microarchitecture use more registers than specified by the ISA without loss of ISA compatibility?

Yes, Robert Tomasulo of IBM suggested an ingenious solution in 1967 based on on-the-fly register renaming.
Instruction-level Parallelism via *Renaming*

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LD</td>
<td>F2,</td>
<td>34(R2)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>LD</td>
<td>F4,</td>
<td>45(R3)</td>
<td>long</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>MULTD</td>
<td>F6,</td>
<td>F4,</td>
<td>F2</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>SUBD</td>
<td>F8,</td>
<td>F2,</td>
<td>F2</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>DIVD</td>
<td>F4’,</td>
<td>F2,</td>
<td>F8</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>ADDD</td>
<td>F10,</td>
<td>F6,</td>
<td>F4’</td>
<td>1</td>
</tr>
</tbody>
</table>

In-order: 1 (2,1) 2 3 4 4 3 5 6 6
Out-of-order: 1 (2,1) 4 4 5 2 (5,2) 3 3 6 6

*Renaming eliminates WAR and WAW hazards (renaming ⇒ additional storage)*
Handling register dependencies

- Decode does register renaming, providing a new spot for each register write
  - Renaming eliminates WAR and WAW hazards by allowing use of more storage space

- Renamed instructions added to an issue stage structure, called the reorder buffer (ROB). Any instruction in the ROB whose RAW hazards have been satisfied can be dispatched
  - Out-of-order or dataflow execution handles RAW hazards
Instruction slot is candidate for execution when:
- It holds a valid instruction ("use" bit is set)
- It has not already started execution ("exec" bit is clear)
- Both operands are available ("present" bits p1 and p2 are set)

Is it obvious where an architectural register value is? \textit{No}
Renaming & Out-of-order Issue

- When are names in sources replaced by data?
- Whenever an FU produces data
- When can a name be reused?
- Whenever an instruction completes
Renaming & Out-of-order Issue
An example

Renaming table & reg file

<table>
<thead>
<tr>
<th>p</th>
<th>data</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1</td>
<td></td>
</tr>
<tr>
<td>F2</td>
<td>0</td>
</tr>
<tr>
<td>F3</td>
<td></td>
</tr>
<tr>
<td>F4</td>
<td>0</td>
</tr>
<tr>
<td>F5</td>
<td></td>
</tr>
<tr>
<td>F6</td>
<td>0</td>
</tr>
<tr>
<td>F7</td>
<td></td>
</tr>
<tr>
<td>F8</td>
<td>0</td>
</tr>
</tbody>
</table>

data (v_i) / tag(t_i)

Reorder buffer

<table>
<thead>
<tr>
<th>Ins#</th>
<th>use</th>
<th>exec</th>
<th>op</th>
<th>p1</th>
<th>src1</th>
<th>p2</th>
<th>src2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>LD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>LD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>MUL</td>
<td>0</td>
<td>t2</td>
<td>1</td>
<td>v1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>SUB</td>
<td>1</td>
<td>v1</td>
<td>1</td>
<td>v1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>DIV</td>
<td>1</td>
<td>v1</td>
<td>0</td>
<td>t4</td>
</tr>
</tbody>
</table>

- Insert instruction in ROB
- Issue instruction from ROB
- Complete instruction
- Empty ROB entry

1  LD  F2,  34(R2)
2  LD  F4,  45(R3)
3  MULTD  F6,  F4,  F2
4  SUBD  F8,  F2,  F2
5  DIVD  F4,  F2,  F8
6  ADDD  F10,  F6,  F4
Simplifying Allocation/Deallocation

Instruction buffer is managed circularly
- Set “exec” bit when instruction begins execution
- When an instruction completes its “use” bit is marked free
- Increment ptr\textsubscript{2} only if the “use” bit is marked free

<table>
<thead>
<tr>
<th>Ins#</th>
<th>use</th>
<th>exec</th>
<th>op</th>
<th>p1</th>
<th>src1</th>
<th>p2</th>
<th>src2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reorder buffer

ptr\textsubscript{2} next to deallocate
ptr\textsubscript{1} next available
Data-Driven Execution

Renaming table & reg file

Reorder buffer

Replacing the tag by its value is an expensive operation

- Instruction template (i.e., tag $t$) is allocated by the Decode stage, which also stores the tag in the reg file
- When an instruction completes, its tag is deallocated
IBM 360/91 Floating Point Unit
R. M. Tomasulo, 1967

Common bus ensures that data is made available immediately to all the instructions waiting for it.
Effectiveness?

Renaming and Out-of-order execution was first implemented in 1969 in IBM 360/91 but was effective only on a very small class of problems and thus did not show up in the subsequent models until mid-nineties. *Why?*

1. Did not address the memory latency problem which turned out be a much bigger issue than FU latency

2. Made exceptions imprecise

*One more problem needed to be solved*

*Branch/jump penalties*

*More on this in the next lecture*
Exceptions are relatively unlikely events that need special processing, but where adding explicit control flow instructions is not desired, e.g., divide by 0, page fault

Exceptions can be viewed as an implicit conditional subroutine call that is inserted between two instructions.

Therefore, it must appear as if the exception is taken between two instructions (say $I_i$ and $I_{i+1}$)

- the effect of all instructions up to and including $I_i$ is complete
- no effect of any instruction after $I_i$ has taken place

The handler either aborts the program or restarts it at $I_{i+1}$.
### Effect on Exceptions

#### Out-of-order Completion

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_1$</td>
<td>DIVD</td>
<td>f6, f6, f4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_2$</td>
<td>LD</td>
<td>f2, 45(r3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_3$</td>
<td>MULTD</td>
<td>f0, f2, f4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_4$</td>
<td>DIVD</td>
<td>f8, f6, f2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_5$</td>
<td>SUBD</td>
<td>f10, f0, f6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_6$</td>
<td>ADDD</td>
<td>f6, f8, f2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Consider exceptions on “DIVD”s

- Precise exceptions are difficult to implement at high speed
- Want to start execution of later instructions before exception checks finished on earlier instructions

**out-of-order comp**

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>5</td>
<td>5</td>
<td>4</td>
<td>6</td>
</tr>
</tbody>
</table>

**restore f2**

**restore f10**
Exceptions

• Exceptions create a dependence on the value of the next PC

• Options for handling this dependence:
  • Stall  No
  • Bypass  No
  • Find something else to do  No
  • Change the architecture  Sometimes: Alpha, Multiflow
  • Speculate!  Most common approach!

• How can we handle rollback on mis-speculation?
  Delay state update until commit on speculated instructions

• Note: earlier exceptions must override later ones
Reminder: Exception Handling (In-Order Five-Stage Pipeline)

Hold exception flags in pipeline until commit point (M stage)

- If exception at commit:
  - update Cause/EPC registers
  - kill all stages
  - fetch at handler PC

Inject external interrupts at commit point
Phases of Instruction Execution

- **Fetch**: Instruction bits retrieved from cache.
- **Decode**: Instructions placed in appropriate issue (aka “dispatch”) stage buffer.
- **Execute**: Instructions and operands sent to execution units. When execution completes, all results and exception flags are available.
- **Commit**: Instruction irrevocably updates architectural state (aka “graduation” or “completion”).
In-Order Commit for Precise Exceptions

- Instructions fetched and decoded into instruction reorder buffer in-order
- Execution is out-of-order (⇒ out-of-order completion)
- Commit (write-back to architectural state, i.e., regfile & memory) is in-order

Temporary storage needed to hold results before commit (shadow registers and store buffers)
## Extensions for Precise Exceptions

### Reorder buffer

- **ptr\textsubscript{2}** next to commit
- **ptr\textsubscript{1}** next available

<table>
<thead>
<tr>
<th>Inst#</th>
<th>use</th>
<th>exec</th>
<th>op</th>
<th>p1</th>
<th>src1</th>
<th>p2</th>
<th>src2</th>
<th>pd</th>
<th>dest</th>
<th>data</th>
<th>cause</th>
</tr>
</thead>
</table>

- add \(<pd, \text{dest}, \text{data}, \text{cause}\)> fields in the instruction template
- commit instructions to reg file and memory in program order \(\Rightarrow\) buffers can be maintained circularly
- on exception, clear reorder buffer by resetting \(\text{ptr}_{1}=\text{ptr}_{2}\)
  \(\text{(stores must wait for commit before updating memory)}\)
Rollback and Renaming

Register file does not contain renaming tags any more.

How does the decode stage find the tag of a source register?

Search the “dest” field in the reorder buffer
Renaming table is a cache to speed up register name lookup. It needs to be cleared after each exception taken. When else are valid bits cleared? Control transfers.
Physical Register Files

- Reorder buffers are space inefficient – a data value may be stored in multiple places in the reorder buffer
- Idea: Keep all data values in a physical register file
  - Tag represents the name of the data value and name of the physical register that holds it
  - Reorder buffer contains only tags

Thus, 64-bit data values may be replaced by 8-bit tags for a 256-element physical register file

More on this in later lectures ...
Branch Penalty

How many instructions need to be killed on a misprediction?

Modern processors may have > 10 pipeline stages between nextPC calculation and branch resolution!

Next lecture: Branch prediction & Speculative execution

How many instructions need to be killed on a misprediction?