Branch Prediction

Joel Emer
Computer Science and Artificial Intelligence Laboratory
M.I.T.
Modern processors may have > 10 pipeline stages between next PC calculation and branch resolution!
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How much work is lost if pipeline doesn’t follow correct instruction flow?
Control Flow Penalty

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~ Loop length x pipeline width
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\~ \text{Loop length} \times \text{pipeline width}
Average Run-Length between Branches

Average dynamic instruction mix of SPEC CPU 2017 [Limaye and Adegbiya, ISPASS’18]:

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<td>Branches</td>
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SPECInt17: perlbench, gcc, mcf, omnetpp, xalancbmk, x264, deepsjeng, leela, exchange2, xz
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What is the average run length between branches?

Roughly 5-10 instructions
MIPS Branches and Jumps

Each instruction fetch depends on one or two pieces of information from the preceding instruction:

1) Is the preceding instruction a taken branch?
2) If so, what is the target address?

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*After Inst. Decode*
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Example Branch Penalties

UltraSPARC-III instruction fetch pipeline stages
(in-order issue, 4-way superscalar, 750MHz, 2000)

A | PC Generation/Mux
P | Instruction Fetch Stage 1
F | Instruction Fetch Stage 2
B | Branch Address Calc/Begin Decode
I | Complete Decode
J | Steer Instructions to Functional units
R | Register File Read
E | Integer Execute

... Remainder of execute pipeline
(+ another 6 stages)
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</tr>
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<td>Instruction Fetch Stage 1</td>
</tr>
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</table>

<table>
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<th>Branch Direction &amp; Jump Register Target Known</th>
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<tr>
<td>R E</td>
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PC Generation/Mux
Instruction Fetch Stage 1
Instruction Fetch Stage 2
Branch Address Calc/Begin Decode
Complete Decode
Steer Instructions to Functional units
Register File Read
Integer Execute

Remainder of execute pipeline (+ another 6 stages)
Reducing Control Flow Penalty

- Software solutions
- Hardware solutions
Reducing Control Flow Penalty

• Software solutions
  – *Eliminate branches – loop unrolling*
    Increases run length between branches

• Hardware solutions
Reducing Control Flow Penalty

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  – *Eliminate branches – loop unrolling*
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  – *Reduce resolution time – instruction scheduling*
    Compute the branch condition as early as possible
    (of limited value)

• Hardware solutions
Reducing Control Flow Penalty

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  - Bypass – usually results are used immediately
Reducing Control Flow Penalty

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- **Hardware solutions**
  
  - Bypass – usually results are used immediately
  
  - Change architecture – find something else to do
    
    *Delay slots* – replace pipeline bubbles with useful work
    (requires software cooperation)
Reducing Control Flow Penalty

- **Software solutions**
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- **Hardware solutions**
  - Bypass – usually results are used immediately
  - Change architecture – find something else to do
    *Delay slots* – replace pipeline bubbles with useful work
    (requires software cooperation)
  - Speculate – branch prediction
    *Speculative execution* of instructions beyond the branch
Branch Prediction

Motivation:
Branch penalties limit performance of deeply pipelined processors

Modern branch predictors have high accuracy (>95%) and can reduce branch penalties significantly

Required hardware support:
Prediction structures:
• Branch history tables, branch target buffers, etc.

Mispredict recovery mechanisms:
• Keep result computation separate from commit
• Kill instructions following branch in pipeline
• Restore state to state following branch
Static Branch Prediction

Overall probability a branch is taken is ~60-70% but:

- backward 90%
- forward 50%
Static Branch Prediction

Overall probability a branch is taken is ~60-70% but:

\[ \text{backward} \quad 90\% \quad \text{forward} \quad 50\% \]

ISA can attach preferred direction semantics to branches, e.g., Motorola MC88110

- bne0 (*preferred taken*)
- beq0 (*not taken*)
Overall probability a branch is taken is $\sim$60-70% but:

**Static Branch Prediction**

ISA can attach preferred direction semantics to branches, e.g., Motorola MC88110
- bne0 (*preferred taken*)
- beq0 (*not taken*)

ISA can allow arbitrary choice of statically predicted direction, e.g., HP PA-RISC, Intel IA-64
- typically reported as $\sim$80% accurate
Dynamic Prediction

Prediction as a feedback control process

Input

Predictor

Truth/Feedback

Prediction

Operations
- Predict
- Update
Dynamic Branch Prediction

Learning based on past behavior

Temporal correlation
The way a branch resolves may be a good predictor of the way it will resolve at the next execution

Spatial correlation
Several branches may resolve in a highly correlated manner (a preferred path of execution)
Predictor Primitive
Emer & Gloy, 1997

- Indexed table holding values

- Operations
  - Predict
  - Update

- Algebraic notation

Prediction = P[Width, Depth](Index; Update)
One-bit Predictor
aka Branch History Table (BHT)

Simple temporal prediction

1 bit

PC

A21064(PC; T) = P[ 1, 2K ](PC; T)

What happens on loop branches?
One-bit Predictor
aka Branch History Table (BHT)

Simple temporal prediction

1 bit

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A21064(PC; T) = P[ 1, 2K ](PC; T)

What happens on loop branches?
At best, mispredicts twice for every use of loop
Two-bit Predictor
Smith, 1981

- Use two bits per entry instead of one bit
- Manage them as a saturating counter:

<table>
<thead>
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<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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- Direction prediction changes only after two wrong predictions
Two-bit Predictor

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<td>1</td>
<td>1</td>
<td>Strongly taken</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Weakly taken</td>
</tr>
<tr>
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How many mispredictions per loop? ___
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- Direction prediction changes only after two wrong predictions

How many mispredictions per loop? 1
Two-bit Predictor

Smith, 1981

Counter\[W,D\](I; T) = P[W, D](I; if T then P+1 else P-1)

A21164(PC; T) = MSB(Counter[2, 2K](PC; T))
## Branch History Table

<table>
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<tr>
<th>Fetch PC</th>
<th>0</th>
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Branch History Table

Fetch PC

I-Cache

Instruction

Opcode offset
Branch History Table

**Fetch PC**

**I-Cache**

**Instruction**

**Opcode**

**offset**

**Branch?**

**Target PC**

0 0
Branch History Table

Fetch PC

I-Cache

Instruction

Opcode

offset

Branch?

Target PC

2^k-entry BHT, 2 bits/entry

Taken/¬Taken?
Branch History Table

4K-entry BHT, 2 bits/entry, ~80-90% correct predictions
if (x[i] < 7) then
    y += 1;
if (x[i] < 5) then
    c -= 4;

If first condition false, second condition also false
Exploiting Spatial Correlation
Yeh and Patt, 1992

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If first condition false, second condition also false

*History register* records the direction of the last N branches executed by the processor
History Registers
aka Pattern History Table (PHT)

History(PC; T) = P(PC; P || T)
Global-History Predictor

\[
\text{GHist}(;T) = \text{MSB}(\text{Counter(History}(0, T); T))
\]
Global-History Predictor

\[ \text{GHist}(;T) = \text{MSB}(\text{Counter}(\text{History}(0, T); T)) \]

Can we take advantage of a pattern at a particular PC?
Local-History Predictor

\[ \text{LHist}(PC; T) = \text{MSB}(\text{Counter}(\text{History}(PC; T); T)) \]
Local-History Predictor

Can we take advantage of the global pattern at a particular PC?

\[ LHist(PC; T) = \text{MSB}(\text{Counter}(\text{History}(PC; T); T)) \]
Global-History Predictor with Per-PC Counters

\[ \text{GHistPA}(\text{PC}; T) = \text{MSB}(\text{Counter}(\text{History}(0; T)||\text{PC}; T)) \]
Two-Level Branch Predictor
(Pentium Pro, 1995)

Pentium Pro uses the result from the last two branches to select one of the four sets of BHT bits (~95% correct)

Shift in Taken/¬Taken results of each branch

2-bit global branch history shift register

Fetch PC

0 0
Choosing Predictors

LHist → Prediction

GHist → LHist

Chooser → GHist

Chooser → Prediction
Choosing Predictors

Chooser = MSB(P(PC; P + (A==T) - (B==T)))

or

Chooser = MSB(P(GHist(PC; T); P + (A==T) - (B==T)))
Tournament Branch Predictor
(Alpha 21264, 1996)

- Choice predictor learns whether best to use local or global branch history in predicting next branch
- Global history is speculatively updated but restored on mispredict
- Claim 90-100% success on range of applications
TAGE predictor
Seznec & Michaud, 2006

PC

Bimodal

TAGE[L1]

TAGE[L2]

TAGE[L3]

My guess

Use me?

Final Prediction
\[
TAGE_{\text{TREE}}[L1, L2, L3](PC; T) = \\
TAGE[L3](PC, \\
TAGE[L2](PC, \\
TAGE[L1](PC, \text{Bimodal}(PC; T) \\
; T)) ; T) ; T)
\]
TAGE component

Next Predictor

Counter

Useful

Tag

Prediction

My guess

Use me?

GHist

PC
TAGE predictor component
TAGE predictor component

TAGE[L](PC, NEXT; T) =

\[
\begin{align*}
\text{idx} &= \text{hash}(PC, \text{GHIST}[L](;T)) \\
\text{tag} &= \text{hash'}(PC, \text{GHIST}[L](;T))
\end{align*}
\]

TAGE.U = \text{SA}(\text{idx}, \text{tag}; ((\text{TAGE} == \text{T}) && (\text{NEXT} != \text{T}))?1:\text{SA})
TAGE.Counter = \text{SA}(\text{idx}, \text{tag}; \text{T}\?\text{SA}+1:\text{SA}-1)

use_me = \text{TAGE.U} \&\& \text{isStrong(TAGE.Counter)}
TAGE = use_me?\text{MSB(TAGE.Counter)}:\text{NEXT}

Notes:

- SA is a set-associative structure
- SA allocation occurs on mispredict (not shown)
- TAGE.U cleared on global counter saturation
Limitations of branch predictors

Only predicts branch direction. Therefore, cannot redirect fetch stream until after branch target is determined.

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Remainder of execute pipeline (+ another 6 stages)

*UltraSPARC-III fetch pipeline*
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Correctly predicted taken branch penalty

UltraSPARC-III fetch pipeline

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Correctly predicted taken branch penalty

Jump Register penalty

UltraSPARC-III fetch pipeline
Branch Target Buffer (untagged)

BP bits are stored with the predicted target address.

**IF stage:**  *If (BP=taken) then nPC=target else nPC=PC+4*

**later:**  *check prediction, if wrong then kill the instruction and update BTB & BPb, else update BPb*
Address Collisions

Assume a 128-entry BTB

What will be fetched after the instruction at 1028?

BTB prediction =
Correct target =

⇒
What will be fetched after the instruction at 1028?

BTB prediction = 236
Correct target =

⇒

Assume a 128-entry BTB

Jump 100
Add ....
Instruction Memory
Address Collisions

Assume a 128-entry BTB

What will be fetched after the instruction at 1028?

- BTB prediction = 236
- Correct target = 1032

⇒
Address Collisions

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What will be fetched after the instruction at 1028?

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- Correct target = 1032

⇒ *kill* PC=236 and *fetch* PC=1032
Address Collisions

What will be fetched after the instruction at 1028?

- BTB prediction = 236
- Correct target = 1032

⇒ *kill* PC=236 and *fetch* PC=1032

*Is this a common occurrence?*
Address Collisions

Assume a 128-entry BTB

What will be fetched after the instruction at 1028?

BTB prediction = 236
Correct target = 1032

⇒ kill PC=236 and fetch PC=1032

Is this a common occurrence? Can we avoid these mispredictions?
BTB is only for Control Instructions

BTB contains useful information for branch and jump instructions only
   \[ \Rightarrow \] Do not update it for other instructions

For all other instructions the next PC is (PC)+4 !

*How to achieve this effect without decoding the instruction?*
Branch Target Buffer (tagged)

- Keep both the branch PC and target PC in the BTB
- PC+4 is fetched if match fails
- Only *taken* branches and jumps held in BTB
- Next PC determined *before* branch fetched and decoded
Consulting BTB Before Decoding

- The match for PC=1028 fails and 1028+4 is fetched
  ⇒ eliminates false predictions after ALU instructions

- BTB contains entries only for control transfer instructions
  ⇒ more room to store branch targets
Combining BTB and BHT

- BTB entries are considerably more expensive than BHT, but can redirect fetches at earlier stage in pipeline and can accelerate indirect branches (JR)
- BHT can hold many more entries and is more accurate
Combining BTB and BHT

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<table>
<thead>
<tr>
<th>A</th>
<th>PC Generation/Mux</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>Instruction Fetch Stage 1</td>
</tr>
<tr>
<td>F</td>
<td>Instruction Fetch Stage 2</td>
</tr>
<tr>
<td>B</td>
<td>Branch Address Calc/Begin Decode</td>
</tr>
<tr>
<td>I</td>
<td>Complete Decode</td>
</tr>
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<td>Steer Instructions to Functional units</td>
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BHT in later pipeline stage corrects when BTB misses a predicted taken branch

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| F | Instruction Fetch Stage 1 |
| B | Instruction Fetch Stage 2 |
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BTB/BHT only updated after branch resolves in E stage

Diagram:
- BTB
- BHT
- A: PC Generation/Mux
- P: Instruction Fetch Stage 1
- F: Instruction Fetch Stage 2
- B: Branch Address Calc/Begin Decode
- I: Complete Decode
- J: Steer Instructions to Functional units
- R: Register File Read
- E: Integer Execute

BHT in later pipeline stage corrects when BTB misses a predicted taken branch
Uses of Jump Register (JR)

• Switch statements (jump to address of matching case)

• Dynamic function call (jump to run-time function address)

• Subroutine returns (jump to return address)
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How well does BTB work for each of these cases?
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  BTB works well if same function usually called, (e.g., in C++ programming, when objects have same type in virtual function call)

- Subroutine returns (jump to return address)
  
  BTB works well if usually return to the same place
  ⇒ Often one function called from many distinct call sites!

How well does BTB work for each of these cases?
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.
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Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

```c
fa() { fb(); }
fb() { fc(); }
fc() { fd(); }
```
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

```c
fa() { fb(); }

fb() { fc(); }

fc() { fd(); }
```

```

k entries
(typically k=8-16)
```
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

```c
fa() { fb(); }  
fb() { fc(); }  
fc() { fd(); }
```

Push call address when function call executed

$k$ entries

(typically $k=8-16$)
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

```c
fa() { fb(); }
fb() { fc(); }
fcc() { fd(); }
```

*Push call address when function call executed*

- 4-8 entries (typically k=8-16)
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

\begin{verbatim}
fa() { fb(); }
fb() { fc(); }
fc() { fd(); }
\end{verbatim}

*Push call address when function call executed*

\[k\text{ entries (typically } k=8-16)\]
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

```c
fa() { fb(); }
fb() { fc(); }
fc() { fd(); }
```

*Push call address when function call executed*

```
&fd()
&fc()
&fb()
```

$k$ entries (typically $k=8-16$)
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

\[
\begin{align*}
\text{fa}() & \{ \text{fb}(); \} \\
\text{fb}() & \{ \text{fc}(); \} \\
\text{fc}() & \{ \text{fd}(); \}
\end{align*}
\]

Push call address when function call executed

Pop return address when subroutine return decoded

\[k \text{ entries} \] (typically \( k=8-16 \))
Line Prediction
(Alpha 21[234]64)

- For superscalar, useful to predict next cache line(s) to fetch

- Line Predictor predicts line to fetch each cycle (tight loop)
  - Untagged BTB structure - Why?
  - 21464 was to predict 2 lines per cycle

- Icache fetches block, and predictors improve target prediction

- PC Calc checks accuracy of line prediction(s)
Overview of Branch Prediction
Overview of Branch Prediction

PC \quad \cdots \quad \text{Decode}
Overview of Branch Prediction

![Diagram showing the pipeline stages: PC, Decode, Reg Read.](image)
Overview of Branch Prediction
Overview of Branch Prediction

Instr type, PC relative targets available
Overview of Branch Prediction

Instr type, PC relative targets available
Overview of Branch Prediction

Instr type, PC relative targets available

Simple conditions, register targets available

Execute
Overview of Branch Prediction

- **PC**: Decode
  - Instr type, PC relative targets available
- **Reg Read**: Simple conditions, register targets available
- **Execute**
Overview of Branch Prediction

- **Decode**
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- **Reg Read**
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- **Execute**
  - Complex conditions and exceptions available
Overview of Branch Prediction

- **Decode**: Instr type, PC relative targets available
- **Reg Read**: Simple conditions, register targets available
- **Execute**: Complex conditions and exceptions available
Overview of Branch Prediction

- PC
  - Need next PC immediately
- Decode
  - Instr type, PC relative targets available
- Reg Read
  - Simple conditions, register targets available
- Execute
  - Complex conditions and exceptions available
Overview of Branch Prediction

- Need next PC immediately
- Decode: Instr type, PC relative targets available
- Reg Read: Simple conditions, register targets available
- Execute: Complex conditions and exceptions available
Overview of Branch Prediction

- PC
- BTB
- Decode
- Reg Read
- Execute

Tight loop

Need next PC immediately

Instr type, PC relative targets available

Simple conditions, register targets available

Complex conditions and exceptions available
Overview of Branch Prediction

Need next PC immediately

Tight loop

Loose loop

Instr type, PC relative targets available

Simple conditions, register targets available

Complex conditions and exceptions available

BTB
Overview of Branch Prediction

- **PC**
- **BTB**

Need next PC immediately

- **Tight loop**

Instr type, PC relative targets available

- **Loose loop**

Simple conditions, register targets available

- **Loose loop**

Complex conditions and exceptions available

- **Loose loop**
Overview of Branch Prediction

- Need next PC immediately
- Instr type, PC relative targets available
- Simple conditions, register targets available
- Complex conditions and exceptions available

Tight loop  Loose loop  Loose loop  Loose loop

Must speculation check always be correct?
Overview of Branch Prediction

Must speculation check always be correct? No...
Overview of Branch Prediction

Must speculation check always be correct?  No...

Tight loop

Loose loop

Loose loop

Loose loop

Need next PC immediately

Instr type, PC relative targets available

Simple conditions, register targets available

Complex conditions and exceptions available

PC

BTB

Decode

Reg Read

Execute

BP, JMP, Ret
Overview of Branch Prediction

- **PC**
- **BTB**
- **Decoding**
- **Register Read**
- **Execute**

**Overview**

- Needs next PC immediately
- Instr type, PC relative targets available
- Simple conditions, register targets available
- Complex conditions and exceptions available
- Best predictors reflect program behavior

**Loose loop**

- Tight loop
- Loose loop
- Loose loop
- Loose loop

**Question:** Must speculation check always be correct?

**Answer:** No...
Next Lecture:
Speculative Execution
& Value Management