Cache Coherence

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M.I.T.
The Shift to Multicore

- Since 2005, improvements in system performance mainly due to increasing cores per chip
- Why?

[https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/]
Multicore Performance

Cost/perf curve of possible core designs

- High-perf, expensive core

Cost (area, energy...)

Performance
Multicore Performance

Cost/perf curve of possible core designs

High-perf, expensive core

Moderate perf, efficient core
Multicore Performance

Cost/perf curve of possible core designs

- High-perf, expensive core
- Moderate perf, efficient core

Performance

Cost (area, energy...)

2 cores
Multicore Performance

Cost/perf curve of possible core designs:
- High-perf, expensive core
- Moderate perf, efficient core

Performance vs. Cost (area, energy...): 2 cores to 4 cores
Multicore Performance

Cost/perf curve of possible core designs

- High-perf, expensive core
- Moderate perf, efficient core

What factors may limit multicore performance?
Amdahl’s Law

- Speedup = \( \frac{t_{\text{without enhancement}}}{t_{\text{with enhancement}}} \)
- Suppose an enhancement speeds up a fraction \( f \) of a task by a factor of \( S \)

\[
\begin{align*}
    t_{\text{new}} &= t_{\text{old}} \cdot ((1-f) + \frac{f}{S}) \\
    S_{\text{overall}} &= \frac{1}{((1-f) + \frac{f}{S})}
\end{align*}
\]

Corollary: Make the common case fast
Amdahl’s Law and Parallelism

- Say you write a program that can do 90% of the work in parallel, but the other 10% is sequential.
- What is the maximum speedup you can get by running on a multicore machine?

\[ S_{\text{overall}} = \frac{1}{(1-f) + \frac{f}{S}} \]

\[ f = 0.9, \ S=\infty \rightarrow S_{\text{overall}} = 10 \]

What \( f \) do you need to use a 1000-core machine well?
Communication Models

• Shared memory:
  – Single address space
  – Implicit communication by reading/writing memory
    • Data
    • Control (semaphores, locks, barriers, ...)
  – Low-level programming model: threads

• Message passing:
  – Separate address spaces
  – Explicit communication by send/rcv messages
    • Data
    • Control (blocking msgs, barriers, ...)
  – Low-level programming model: processes + inter-process communication (e.g., MPI)

• Pros/cons of each model?
Coherence and Consistency

• Shared memory systems:
  – Have multiple private caches for performance reasons
  – Need to provide the illusion of a single shared memory

• Intuition: A read should return the most recently written value
  – What is “most recent”?

• Formally:
  – Coherence: What values can a read return?
    • Concerns reads/writes to a single memory location
  – Consistency: When do writes become visible to reads?
    • Concerns reads/writes to multiple memory locations
Cache Coherence Avoids Stale Data

![Diagram showing a system with main memory and multiple cores and caches.](image-url)
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
Cache Coherence Avoids Stale Data

1. LD $0xA \rightarrow 2$

Diagram:
- Main Memory
- Cache [0xA] = 2
- Core 0
- Core 1
- Core 2
- Core 3
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
3. LD 0xA → 2 (stale!)
Cache Coherence Avoids Stale Data

- A cache coherence protocol controls cache contents to avoid stale cache lines.

**Diagram:**

1. LD 0xA → 2
2. ST 3 → 0xA
3. LD 0xA → 2 (stale!)

A cache coherence protocol controls cache contents to avoid stale cache lines.
Implementing Cache Coherence

• Coherence protocols must enforce two rules:
  – *Write propagation*: Writes eventually become visible to all processors
  – *Write serialization*: Writes to the same location are serialized (all processors see them in the same order)

• How to ensure write propagation?
  – *Write-invalidate protocols*: Invalidate all other cached copies before performing the write
  – *Write-update protocols*: Update all other cached copies after performing the write

• How to track sharing state of cached data and serialize requests to the same address?
  – *Snooping-based protocols*: All caches observe each other’s actions through a shared bus (bus is the serialization point)
  – *Directory-based protocols*: A coherence directory tracks contents of private caches and serializes requests (directory is the serialization point)
Caches watch (snoop on) bus to keep all processors’ view of memory coherent
Snooping-Based Coherence

- Bus provides serialization point
  - Broadcast, totally ordered
Snooping-Based Coherence

- **Bus provides serialization point**
  - Broadcast, totally **ordered**

- **Controller**
  - One cache controller for each core “snoops” all bus transactions
  - Controller
    - Responds to requests from core and the bus
    - Changes state of the selected cache block
    - Generates bus transactions to access data or invalidate

![Diagram of processor, cache, and snooping](image-url)
Snooping-Based Coherence

• Bus provides serialization point
  – Broadcast, totally ordered

• Controller
  – One cache controller for each core “snoops” all bus transactions
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    • generates bus transactions to access data or invalidate

• Snoopy protocol (FSM)
  – State-transition diagram
  – Actions

---

[Diagram of processor and cache with state, tag, and data fields, and a snoop (observed bus transaction) marked.]
Snooping-Based Coherence

- Bus provides serialization point
  - Broadcast, totally ordered

- Controller
  - One cache controller for each core “snoops” all bus transactions
  - Controller
    - Responds to requests from core and the bus
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    - Generates bus transactions to access data or invalidate

- Snoopy protocol (FSM)
  - State-transition diagram
  - Actions

- Handling writes:
  - Write-invalidate
  - Write-update
A Simple Protocol: Valid/Invalid (VI)

- Assume write-through caches
- Transition nomenclature: *triggering action / taken action(s)*

### Actions

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Read (PrRd)</td>
<td></td>
</tr>
<tr>
<td>Processor Write (PrWr)</td>
<td></td>
</tr>
<tr>
<td>Bus Read (BusRd)</td>
<td></td>
</tr>
<tr>
<td>Bus Write (BusWr)</td>
<td></td>
</tr>
</tbody>
</table>

October 19, 2022
Valid/Invalid Example

Main Memory

Cache

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
</table>

Core 0

Cache

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
</table>

Core 1
Valid/Invalid Example

1. LD 0xA
Valid/Invalid Example

```plaintext
\begin{figure}
\centering
\begin{tikzpicture}
% Diagram code...
\end{tikzpicture}
\end{figure}
```

- BusRd 0xA
- Core 0
- Core 1
- LD 0xA
Valid/Invalid Example

Main Memory

BusRd 0xA

Cache

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

Core 0

Core 1

LD 0xA
Valid/Invalid Example

![Diagram of memory hierarchy with caches]

1. LD 0xA
Valid/Invalid Example

1. LD 0xA

2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
Valid/Invalid Example

1. LD 0xA

2. LD 0xA

Additional loads satisfied locally, without BusRd
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

BusWr 0xA, 3

1. LD 0xA

2. LD 0xA

3. ST 0xA
Valid/Invalid Example

**Diagram Description:**
- **Main Memory:**
- **Cache:**
  - **Core 0:** 
    - Tag: 0xA
    - State: V
    - Data: 2
  - **Core 1:** 
    - Tag: 0xA
    - State: V
    - Data: 2
- **BusWrite (BusWr):** 0xA, 3
- **Instructions:**
  1. **LD 0xA**
  2. **LD 0xA**
  3. **ST 0xA**
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

BusWr 0xA, 3

Core 0
1. LD 0xA
2. ST 0xA
3. ST 0xA

Core 1
2. LD 0xA

Main Memory

Cache
<table>
<thead>
<tr>
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<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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</tr>
</tbody>
</table>

Cache
<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>2</td>
</tr>
</tbody>
</table>
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA

VI Problems?
Modified/Shared/Invalid (MSI) Protocol

- Allows writeback caches + satisfying writes locally

**Actions**

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</thead>
<tbody>
<tr>
<td>Processor Write (PrWr)</td>
</tr>
<tr>
<td>Bus Read (BusRd)</td>
</tr>
<tr>
<td>Bus Read Exclusive (BusRdX)</td>
</tr>
<tr>
<td>Bus Writeback (BusWB)</td>
</tr>
</tbody>
</table>
MSI Example

Main Memory

<table>
<thead>
<tr>
<th>Cache</th>
<th>Cache</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tag</td>
<td>State</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Core 0

Core 1
MSI Example

1. LD 0xA
MSI Example

```
1. LD 0xA
```

```
BusRd 0xA
```

```
Main Memory
```

```
Core 0
```

```
Core 1
```

```
Cache
```

```
<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
</table>
```

```
Cache
```

```
<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
</table>
```
MSI Example

![Diagram showing main memory, cache, and cores with data structures](image-url)

1. LD 0xA

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>S</td>
<td>2</td>
</tr>
</tbody>
</table>

Core 0

Core 1
MSI Example

1. LD 0xA
MSI Example

1. LD 0xA

2. LD 0xA
MSI Example

1. LD 0xA
2. LD 0xA
MSI Example

1. LD 0xA

2. LD 0xA
Additional loads satisfied locally, without BusRd (like in VI)
MSI Example

1. LD 0xA
2. LD 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

Additional loads *and stores* from core 0 satisfied locally, without bus transactions (unlike in VI)
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>M</td>
<td>3</td>
</tr>
<tr>
<td>0xA</td>
<td>I</td>
<td>2</td>
</tr>
</tbody>
</table>
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
Cache interventions

- MSI allows caches to serve writes without updating memory, so main memory can have stale data
  - Core 0’s cache needs to supply data
  - But main memory may also respond!
- Cache must override response from main memory
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
 MSI Example

Main Memory

Core 0
1. LD 0xA
3. ST 0xA
5. LD 0xA

Core 1
2. LD 0xA
4. ST 0xA
### MSI Example

The diagram illustrates the memory access process in a multiprocessor system with two cores, Core 0 and Core 1, each having a cache. The main memory is connected to the cores through the bus. The actions performed are:

<table>
<thead>
<tr>
<th>Core 0</th>
<th>Core 1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1</strong> LD 0xA</td>
<td><strong>2</strong> LD 0xA</td>
</tr>
<tr>
<td><strong>3</strong> ST 0xA</td>
<td></td>
</tr>
<tr>
<td><strong>5</strong> LD 0xA</td>
<td><strong>4</strong> ST 0xA</td>
</tr>
</tbody>
</table>

#### Cache Tables

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
<tr>
<td>0xA</td>
<td>M</td>
<td>10</td>
</tr>
</tbody>
</table>

The diagram shows the process of accessing memory locations and the state of the cache entries.
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA
MSI Example

Main Memory

BusRd 0xA

Cache

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 0

1. LD 0xA
3. ST 0xA
5. LD 0xA

BusWB 0xA, 10

Cache

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>S</td>
<td>10</td>
</tr>
</tbody>
</table>

Core 1

2. LD 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA
MSI Optimizations: Exclusive State

• Observation: Doing read-modify-write sequences on private data is common
  – What’s the problem with MSI?

• Solution: E state (exclusive, clean)
  – If no other sharers, a read acquires line in E instead of S
  – Writes silently cause E\(\rightarrow\)M (exclusive, dirty)
MESI: An Enhanced MSI protocol
increased performance for private read-write data

M: Modified Exclusive
E: Exclusive, unmodified
S: Shared
I: Invalid

```
PrWr / --
PrRd /--
BusRd / BusWB
PrWr/ BusRdX
```

```
BusRdX / --
```

```
PrWr/ BusRdX
```

```
PrRd /--
BusRd / --
```
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PrWr / --
PrRd /--
BusRd / BusWB
PrWr/ BusRdX
PrRd /--
PrWr /--
BusRdX/ BusWB
BusRdX / --
PrRd /--
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PrWr / --
PrRd /--

BusRd / BusWB
PrWr/ BusRdX

PrRd / BusRd
if other sharers
PrRd / BusRdX
BusRdX/ BusWB
PrRd / BusRd
if no other sharers

PrRd / --
PrRd / BusRd
if other sharers
PrRd /--
Mesity: An Enhanced MSI protocol
increased performance for private read-write data

M: Modified Exclusive
E: Exclusive, unmodified
S: Shared
I: Invalid

- **M**: PrWr / --, PrRd / --
- **E**: PrRd / --
  - PrRd / BusRd if no other sharers
- **S**: PrRd / --
  - BusRd / BusWB
  - PrWr / BusRdX
- **I**: BusRdX / --
  - PrRd / BusRd if other sharers
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PrWr / BusRdX / --
PrRd / --
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PrWr / BusRdX
BusRdX / --
PrRd / BusRd if no other sharers
PrRd / BusRd if other sharers

PrRd / --
PrWr / --
BusRdX / --
PrWr / --
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M: Modified Exclusive
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S: Shared
I: Invalid

BusRd / BusWB
PrWr / BusRdX
PrRd /--
PrWr /--
PrRd /--

PrRd / BusRd if no other sharers
PrRd / BusRd if other sharers

PrRd /--
PrRd /--
PrRd / BusRdX
PrRd / BusRdX
MESI: An Enhanced MSI protocol
increased performance for private read-write data

Each cache line has a tag

- **M**: Modified Exclusive
- **E**: Exclusive, unmodified
- **S**: Shared
- **I**: Invalid

<table>
<thead>
<tr>
<th>State bits</th>
<th>Address tag</th>
</tr>
</thead>
<tbody>
<tr>
<td>PrWr / --</td>
<td>M</td>
</tr>
<tr>
<td>PrRd / --</td>
<td>E</td>
</tr>
<tr>
<td>BusRd / --</td>
<td>S</td>
</tr>
<tr>
<td>BusWB</td>
<td>I</td>
</tr>
</tbody>
</table>

**Transition Rules**

- **M** to **E**: BusRdX
- **E** to **M**: PrWr / --, BusRd / --
- **E** to **S**: PrRd / BusRdX, BusRdX / --
- **S** to **E**: PrRd / BusRdX, BusRdX / --
- **E** to **I**: PrRd / BusRd
- **S** to **I**: PrRd / BusRd

BusRdX: BusRd if no other sharers

PrRd / BusRd if other sharers
MSI Optimizations: Owner State

- Observation: On M→S transitions, must write back line!
  - What happens with frequent read-write sharing?
  - Can we defer the write after S?

- Solution: O state (Owner)
  - O = S + responsibility to write back
  - On M→S transition, one sharer (typically the one who had the line in M) retains the line in O instead of S
  - On eviction, O writes back line (or another sharer does S→O)

- MSI, MESI, MOSI, MOESI...
  - Typically E if private read-write >> shared read-only (common)
  - Typically O only if writebacks are expensive (main mem vs L3)
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

- Supports multiple simultaneous transactions
  - Higher throughput
  - Responses may arrive out of order

- Often implemented as multiple buses (req+resp)

Split-Transaction Bus

Simple, but low throughput!

- Supports multiple simultaneous transactions
  - Higher throughput
  - Responses may arrive out of order

- Often implemented as multiple buses (req+resp)
Non-Atomicity → Transient States

- Protocol must handle lack of atomicity
- Two types of states
  - Stable (e.g. MSI)
  - Transient
- Split + race transitions
- More complex

<table>
<thead>
<tr>
<th>Actions</th>
</tr>
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<tbody>
<tr>
<td>Bus Request</td>
</tr>
<tr>
<td>(BusReq)</td>
</tr>
<tr>
<td>Bus Grant</td>
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<tr>
<td>(BusGnt)</td>
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Non-Atomicity $\rightarrow$ Transient States

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</table>

\[ \begin{array}{c|c} 
\text{Actions} & \text{Words} \\
\hline 
\text{Bus Request} & (BusReq) \\
\text{Bus Grant} & (BusGnt) \\
\end{array} \]
Non-Atomicity \rightarrow Transient States

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- Bus Grant (BusGnt)
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</table>
Scaling Cache Coherence

- Can implement ordered interconnects that scale better than buses...

- ... but broadcast is fundamentally unscalable
  - Bandwidth, energy of transactions with 100s of cache snoops?

Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors.
Directory-Based Coherence

- Route all coherence transactions through a directory
  - Tracks contents of private caches → No broadcasts
  - Serves as ordering point for conflicting requests → Unordered networks

(more on next lecture)
Coherence and False Sharing
Performance Issue #1

A cache block contains more than one word and cache coherence is done at the block-level and not word-level.

Suppose $P_1$ writes $\text{word}_i$ and $P_2$ writes $\text{word}_k$ and both words have the same block address.

What can happen?

How to address this problem?
Coherence and Synchronization

Performance Issue #2

Processor 1

R ← 1
L: swap (mutex), R;
if <R> then goto L;
<critical section>
M[mutex] ← 0;

cache

Processor 2

R ← 1
L: swap (mutex), R;
if <R> then goto L;
<critical section>
M[mutex] ← 0;

cache

Processor 3

R ← 1
L: swap (mutex), R;
if <R> then goto L;
<critical section>
M[mutex] ← 0;

mutex=1

CPU-Memory Bus
Coherence and Synchronization

Performance Issue #2

Cache coherence protocols will cause mutex to ping-pong between P1’s and P2’s caches.
Coherence and Synchronization
Performance Issue #2

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Cache coherence protocols will cause *mutex* to ping-pong between P1’s and P2’s caches.

Ping-ponging can be reduced by first reading the *mutex* location (*non-atomically*) and executing a swap only if it is found to be zero (*test&test&set*).
Coherence and Bus Occupancy
Performance Issue #3

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  ⇒ expensive for simple buses
  ⇒ *very expensive* for split-transaction buses
Coherence and Bus Occupancy
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• In a multiprocessor setting, bus needs to be locked for the entire duration of the atomic read and write operation:
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• Modern processors use:
  *load-reserve*
  *store-conditional*
Load-reserve & Store-conditional

Special register(s) to hold reservation flag and address, and the outcome of store-conditional

Load-reserve R, (a):
<flag, adr> ← <1, a>;
R ← M[a];

Store-conditional (a), R:
if <flag, adr> == <1, a>
    then cancel other procs’ reservation on a;
        M[a] ← <R>;
        status ← succeed;
else status ← fail;

If the snooper sees a store transaction to the address in the reserve register, the reserve bit is set to 0
  • Several processors may reserve ‘a’ simultaneously
  • These instructions are like ordinary loads and stores with respect to the bus traffic
The total number of memory (bus) transactions is not necessarily reduced, but splitting an atomic instruction into load-reserve & store-conditional:

- *increases bus utilization* (and reduces processor stall time), especially in split-transaction buses

- *reduces cache ping-pong effect* because processors trying to acquire a mutex do not have to perform stores each time
Thank you!

Next lecture: Directory-based Cache Coherence