Advanced Memory Operations

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M.I.T.
Reminder: Direct-Mapped Cache

- Tag
- Index
- Block Offset

- Tag
- Data Block

Data Word or Byte

2^k lines
Write Performance

How does write timing compare to read timing?
Write Performance

How does write timing compare to read timing?

Completely serial!
Reducing Write Hit Time

Problem: Writes take two cycles in memory stage, one cycle for tag check plus one cycle for data write if hit
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View: Treat as data dependence on micro-architectural value ‘hit/miss’
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Solutions:
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- Wait – delivering data as fast as possible:
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- **Wait** – delivering data as fast as possible:
  - Fully associative (CAM Tag) caches: Word line only enabled if hit

- **Speculate predicting hit with greedy data update**:
  - Design data RAM that can perform read and write in one cycle
  - Restore old value after tag miss (abort)
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  – Fully associative (CAM Tag) caches: Word line only enabled if hit

• Speculate predicting hit with greedy data update:
  – Design data RAM that can perform read and write in one cycle
  – Restore old value after tag miss (abort)

• Speculate predicting miss with lazy data update:
  – Hold write data for store in single buffer ahead of cache
  – Write cache data during next idle data access cycle (commit)
Pipelined/Delayed Write Timing

Problem: Need to commit lazily saved write data
Pipelined/Delayed Write Timing

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Solution: Write data during idle data cycle of next store’s tag check

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LD₀, ST₁, ST₂, LD₃, ST₄, LD₅
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LD0, ST1, ST2, LD3, ST4, LD5
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- **LD**₀
- **ST**₁
- **ST**₂
- **LD**₃
- **ST**₄
- **LD**₅

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- LD₀: Load 0
- ST₁: Store 1
- ST₂: Store 2
- LD₃: Load 3
- ST₄: Store 4
- LD₅: Load 5
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- LD₀: Load 0
- ST₁: Store 1
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- LD₅: Load 5

Diagram: Dive into timing cycles showing the pipelined operations and how data and tag are managed.
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- LD₀: Load Data 0
- ST₁: Store Tag 1
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- ST₄: Store Tag 4
- LD₅: Load Data 5
## Pipelined/Delayed Write Timing

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**Solution:** Write data during idle data cycle of next store’s tag check

### Diagram

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### Diagram Legend
- LD₀: Load 0
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Diagram showing the timing of load (LD) and store (ST) operations, indicating the timing of data and tag operations for the next store.
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Buffer:
- ST₁
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![Diagram showing pipelined/delayed write timing]

- **Time**: The timeline for the operations.
- **Tag**: Operations include `LD_0`, `ST_1`, `ST_2`, `LD_3`, and `ST_4`.
- **Data**: Operations include `LD_0`, `ST_1`, `LD_3`, and `ST_2`.
- **Buffer**: Operations include `ST_1`, `ST_2`, `ST_2`, and `ST_4`.

Arrows indicate the direction of data flow or operation sequence.
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```

- LD₀: Load data
- ST₁, ST₂, ST₄, ST₅: Store data
- LD₃: Load data
Pipelining Cache Writes

What if instruction needs data in delayed write buffer?
Pipelining Cache Writes

What if instruction needs data in delayed write buffer? Bypass
Pipelining Cache Writes

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Pipelining Cache Writes

What if instruction needs data in delayed write buffer?

Bypass

Address and Store Data From CPU

Tag | Index | Delayed Write Addr. | Delayed Write Data | Load Data to CPU

Tags

Load/Store

Hit?
Write Policy Choices

• Cache hit:
  – *Write-through*: write both cache & memory
    • generally higher traffic but simplifies multi-processor design
  – *Write-back*: write cache only
    (memory is written only when the entry is evicted)
    • a dirty bit per block can further reduce the traffic

• Cache miss:
  – *No-write-allocate*: only write to main memory
  – *Write-allocate* (*aka* fetch on write): fetch into cache

• Common combinations:
  – write-through and no-write-allocate
  – write-back with write-allocate
Reducing Read Miss Penalty

Problem: Write buffer may hold updated value of location needed by a read miss – RAW data hazard
Reducing Read Miss Penalty

**Problem:** Write buffer may hold updated value of location needed by a read miss – RAW data hazard

**Stall:** On a read miss, wait for the write buffer to go empty
Reducing Read Miss Penalty

**Problem:** Write buffer may hold updated value of location needed by a read miss – RAW data hazard

**Stall:** On a read miss, wait for the write buffer to go empty

**Bypass:** Check write buffer addresses against read miss addresses, if no match, allow read miss to go ahead of writes, else, return value in write buffer

Evicted dirty lines for writeback cache

OR

All writes in writethrough cache
We’ve handled the register dependencies, but what about memory operations?
Speculative Loads / Stores

- Problem: Just like register updates, stores should not permanently change the architectural memory state until after the instruction is committed

- Choice: Data update policy: greedy or lazy?
Speculative Loads / Stores

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Lazy: Add a speculative store buffer, a structure to lazily hold speculative store data.
Speculative Loads / Stores

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• Choice: Data update policy: greedy or lazy?
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• Choice: Handling of store-to-load data hazards: stall, bypass, speculate...?
Speculative Loads / Stores

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• Choice: Handling of store-to-load data hazards: stall, bypass, speculate...?
  
  Bypass: ...
Store Buffer Responsibilities
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- **Lazy store of data**: Buffer new data values for stores
Store Buffer Responsibilities

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- **Commit/abort:** The data from the oldest instructions must either be committed to memory or forgotten
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*Commits are generally done in order – why?*
Store Buffer Responsibilities

- **Lazy store of data:** Buffer new data values for stores

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Commits are generally done in order – why? WAW Hazards
Store Buffer Responsibilities

- **Lazy store of data:** Buffer new data values for stores

- **Commit/abort:** The data from the oldest instructions must either be committed to memory or forgotten

- **Bypass:** Data from older instructions must be provided (or forwarded) to younger instructions before the older instruction is committed

*Commits are generally done in order – why?*

WAW Hazards
Store Buffer – Lazy data management

- On store execute:

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<th>Inum</th>
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Speculative Store Buffer

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Store Address

L1 Data Cache

Tags

Data

Store Commit Path

Load Data
**Store Buffer – Lazy data management**

- On store execute:
  - mark valid and speculative; save tag, data, and instruction number

![Diagram of Store Buffer and L1 Data Cache with speculative store buffer, store address, and load data pathways.](image-url)
Store Buffer – Lazy data management

- On store execute:
  - mark valid and speculative; save tag, data, and instruction number
- On store commit:
Store Buffer – Lazy data management

- On store execute:
  - mark valid and speculative; save tag, data, and instruction number
- On store commit:
  - clear speculative bit and eventually move data to cache
Store Buffer – Lazy data management

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- On store execute:
  - mark valid and speculative; save tag, data, and instruction number
- On store commit:
  - clear speculative bit and eventually move data to cache
- On store abort:
**Store Buffer – Lazy data management**

- **On store execute:**
  - mark valid and speculative; save tag, data, and instruction number
- **On store commit:**
  - clear speculative bit and eventually move data to cache
- **On store abort:**
  - clear valid bit
Store Buffer - Bypassing

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Load Address
Store Buffer - Bypassing

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Store Buffer - Bypassing

What fields must be examined for bypassing?

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• Calculating entry needed in the store buffer can be considered a dependence on the index needed to access the store buffer. So store buffer bypassing can be managed speculatively by building a simple predictor that guesses that the specific entry in the store buffer the load needs. So what happens if we guessed the wrong entry?
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  Declare a mis-speculation and abort.
Memory Dependencies

For registers, we used tags or physical register numbers to determine dependencies. What about memory operations?

```plaintext
st r1, (r2)
ld r3, (r4)
```

*When is the load dependent on the store?*
Memory Dependencies

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*Does our ROB know this at issue time?*
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When is the load dependent on the store?

When \( r2 = r4 \)

Does our ROB know this at issue time? No
In-Order Memory Queue

\[
\text{st } r1, (r2) \\
\text{ld } r3, (r4)
\]

Stall naively:

- Execute all loads and stores in program order

=> Load and store cannot start execution until all previous loads and stores have completed execution

- Can still execute loads and stores speculatively, and out-of-order with respect to other instructions
Conservative O-o-O Load Execution

\begin{verbatim}
st r1, (r2)
ld r3, (r4)
\end{verbatim}

Stall intelligently:

- Split execution of store instruction into two phases: address calculation and data write
- Can execute load before store, if addresses known and r4 \(!=\) r2
- Each load address compared with addresses of all previous uncommitted stores \textit{(can use partial conservative check, e.g., bottom 12 bits of address)}
- Don’t execute load if any previous store address not known

\textit{(MIPS R10K, 16 entry address queue)}
Address Speculation

\begin{align*}
&\text{st } r1, (r2) \\
&\text{ld } r3, (r4)
\end{align*}
Address Speculation

\[
\text{st r1, (r2)} \\
\text{ld r3, (r4)}
\]

1. Guess that \( r4 \neq r2 \), and execute load before store address known
Address Speculation

\[\text{st } r1, (r2)\]
\[\text{ld } r3, (r4)\]

1. Guess that \(r4 \neq r2\), and execute load before store address known
2. If \(r4 \neq r2\) commit...
Address Speculation

\[
\begin{align*}
st & \ r1, \ (r2) \\
ld & \ r3, \ (r4)
\end{align*}
\]

1. Guess that r4 != r2, and execute load before store address known

2. If r4 != r2 commit...

3. But if r4==r2, squash load and all following instructions
   - To support squash we need to hold all completed but uncommitted load/store addresses/data in program order
Address Speculation

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*How do we resolve the speculation, i.e., detect when we need to squash?*
Address Speculation

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2. If r4 != r2 commit...
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   - To support squash we need to hold all completed but uncommitted load/store addresses/data in program order

How do we resolve the speculation, i.e., detect when we need to squash?

Watch for stores that arrive after load that needed its data
Speculative Load Buffer

**Speculation check:**
Detect if a load has executed before an earlier store to the same address – missed RAW hazard

- On load execute:
**Speculative Load Buffer**

**Speculation check:** Detect if a load has executed before an earlier store to the same address – missed RAW hazard.

- On load execute:
  - mark entry valid, and instruction number and tag of data.
Speculative Load Buffer

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```
Load Address

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Speculative Load Buffer
Speculative Load Buffer

**Speculation check:**
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- **On load execute:**
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Speculative Load Buffer

- If data in load buffer with instruction younger than store:
Speculative Load Buffer

- If data in load buffer with instruction younger than store:
  - Speculative violation – abort!

![Speculative Load Buffer Diagram]

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April 1, 2021
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=> Large penalty for inaccurate address speculation
Speculative Load Buffer

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Does tag match have to be perfect?
Speculative Load Buffer

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*Does tag match have to be perfect?* No!
Memory Dependence Prediction
(Alpha 21264)

```
st r1, (r2)
ld r3, (r4)
```

1. Guess that r4 != r2 and execute load before store

2. If later find r4==r2, squash load and all following instructions, but mark load instruction as *store-wait*

- Subsequent executions of the same load instruction will wait for all previous stores to complete

- Periodically clear *store-wait* bits

April 1, 2021
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- Periodically clear \textit{store-wait} bits

Notice the general problem of predictors that learn something but can’t unlearn it
Store Sets
(Alpha 21464)

Multiple Readers
- multiple code paths
- multiple components of a single location

Multiple Writers

Program Order

PC

0 Store
4 Store
8 Store
12 Store
28 Load
32 Load
36 Load
40 Load

PC 8

{Empty}

PC 0
PC 12

PC 8

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MIT 6.823 Spring 2021
Memory Dependence Prediction using Store Sets

- A load must wait for any stores in its *store set* that have not yet executed.

- The processor approximates each load’s *store set* by initially allowing naïve speculation and recording memory-order violations.
The Store Set Map Table

- Store/Load Pair causing Memory Order Violation
Store Set Sharing for Multiple Readers

Program Order

- Store/Load Pair causing Memory Order Violation
Store Set Map Table, cont.

- Store/Load Pair causing Memory Order Violation
Prefetching

- Execution of a load ‘depends’ on the data it needs being in the cache...
Prefetching

• Execution of a load ‘depends’ on the data it needs being in the cache...

• Speculate on future instruction and data accesses and fetch them into cache(s)
  – Instruction accesses easier to predict than data accesses
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  Reduce      Increase
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  Reduce      Increase
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- **How does prefetching affect cache misses?**
  
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Issues in Prefetching

- Usefulness – should produce hits
- Timeliness – not late and not too early
- Cache and bandwidth pollution

![Diagram showing CPU, L1 Instruction, L1 Data, Unified L2 Cache, and Prefetched data connections.]

April 1, 2021
Hardware Instruction Prefetching

Instruction prefetch in Alpha AXP 21064

- Fetch two blocks on a miss; the requested block (i) and the next consecutive block (i+1)
- Requested block placed in cache, and next block in instruction stream buffer
- If miss in cache but hit in stream buffer, move stream buffer block into cache and prefetch next block (i+2)
Hardware Data Prefetching

• Prefetch-on-miss:
  – Prefetch $b + 1$ upon miss on $b$

• One Block Lookahead (OBL) scheme
  – Initiate prefetch for block $b + 1$ when block $b$ is accessed
  – *Why is this different from doubling block size?*
  – Can extend to N-block lookahead (called *stream prefetching*)

• Strided prefetch
  – If observe sequence of accesses to block $b, b+N, b+2N, \ldots$, then prefetch $b+3N$ etc.

**Example:** IBM Power 5 [2003] supports eight independent streams of strided prefetch per processor, prefetching 12 lines ahead of current access
Thank you!

Next lecture: Cache Coherence