Cache Coherence

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M.I.T.
The Shift to Multicore


[https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/]
The Shift to Multicore

- Since 2005, improvements in system performance mainly due to increasing cores per chip

Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
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October 20, 2021
The Shift to Multicore

- Since 2005, improvements in system performance mainly due to increasing cores per chip
- Why? Technology scaling
  Limited instruction-level parallelism

October 20, 2021
MIT 6.823 Fall 2021
Multicore Performance

Cost/perf curve of possible core designs

High-perf, expensive core
Multicore Performance

Cost/perf curve of possible core designs

- High-perf, expensive core
- Moderate perf, efficient core

Cost (area, energy...) vs. Performance
Multicore Performance

Cost/perf curve of possible core designs

- High-perf, expensive core
- Moderate perf, efficient core
- 2 cores
Multicore Performance

Cost/perf curve of possible core designs

High-perf, expensive core

Moderate perf, efficient core

Performance

Cost (area, energy...)

2 cores

4 cores
Multicore Performance

Cost/perf curve of possible core designs

What factors may limit multicore performance?
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- Limited application parallelism
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- Limited application parallelism
- Memory accesses and inter-core communication
Multicore Performance

What factors may limit multicore performance?

- Limited application parallelism
- Memory accesses and inter-core communication
- Programming complexity
Amdahl’s Law

- Speedup = \( \frac{\text{time}_{\text{without enhancement}}}{\text{time}_{\text{with enhancement}}} \)
- Suppose an enhancement speeds up a fraction \( f \) of a task by a factor of \( S \)

\[
\text{time}_{\text{old}} = (1 - f) + f
\]
Amdahl’s Law

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\[
\frac{\text{time}_{old}}{\text{time}_{new}} = \frac{(1 - f)}{\left(1 - \frac{f}{S}\right)}
\]
Amdahl’s Law

- Speedup = \( \frac{\text{time}_{\text{without enhancement}}}{\text{time}_{\text{with enhancement}}} \)
- Suppose an enhancement speeds up a fraction \( f \) of a task by a factor of \( S \)
  \[
  \text{time}_{\text{new}} = \text{time}_{\text{old}} \cdot ( (1-f) + \frac{f}{S} )
  \]
Amdahl’s Law

- Speedup = \( \frac{\text{time}_{\text{without enhancement}}}{\text{time}_{\text{with enhancement}}} \)
- Suppose an enhancement speeds up a fraction \( f \) of a task by a factor of \( S \)
  
  \[
  \text{time}_{\text{new}} = \text{time}_{\text{old}} \cdot \left( (1-f) + \frac{f}{S} \right)
  \]
  
  \[
  S_{\text{overall}} = \frac{1}{(1-f) + \frac{f}{S}}
  \]
Amdahl’s Law

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\[
\begin{align*}
\text{time}_{\text{new}} &= \text{time}_{\text{old}} \cdot (1 - f) + \frac{f}{S} \\
S_{\text{overall}} &= \frac{1}{(1 - f) + \frac{f}{S}}
\end{align*}
\]

Corollary: Make the common case fast
Amdahl’s Law and Parallelism

- Say you write a program that can do 90% of the work in parallel, but the other 10% is sequential.
- What is the maximum speedup you can get by running on a multicore machine?
Amdahl’s Law and Parallelism

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\[ S_{overall} = \frac{1}{(1-f) + \frac{f}{S}} \]

\[ f = 0.9, \ S=\infty \rightarrow S_{overall} = 10 \]
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What \( f \) do you need to use a 1000-core machine well?
Communication Models

• Shared memory:
  – Single address space
  – Implicit communication by reading/writing memory
    • Data
    • Control (semaphores, locks, barriers, ...)
  – Low-level programming model: threads
Communication Models

• **Shared memory:**
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• **Message passing:**
  - Separate address spaces
  - Explicit communication by send/rcv messages
    • Data
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  - Low-level programming model: processes + inter-process communication (e.g., MPI)
Communication Models

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- **Pros/cons of each model?**
Coherence and Consistency

- Shared memory systems:
  - Have multiple private caches for performance reasons
Coherence and Consistency

• Shared memory systems:
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Coherence and Consistency

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• Intuition: A read should return the most recently written value
  – What is “most recent”? 
Coherence and Consistency

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• Formally:
  – Coherence: What values can a read return?
    • Concerns reads/writes to a single memory location
  – Consistency: When do writes become visible to reads?
    • Concerns reads/writes to multiple memory locations
Coherence and Consistency

- **Shared memory systems:**
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Cache Coherence Avoids Stale Data
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
3. LD 0xA → 2 (stale!)
Cache Coherence Avoids Stale Data

- A cache coherence protocol controls cache contents to avoid stale cache lines.
Implementing Cache Coherence

• Coherence protocols must enforce two rules:
  – *Write propagation*: Writes eventually become visible to all processors
  – *Write serialization*: Writes to the same location are serialized (all processors see them in the same order)
Implementing Cache Coherence

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• How to ensure write propagation?
  – *Write-invalidate protocols*: Invalidate all other cached copies before performing the write
  – *Write-update protocols*: Update all other cached copies after performing the write
Implementing Cache Coherence

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- How to ensure write propagation?
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  - *Write-update protocols*: Update all other cached copies after performing the write

- How to track sharing state of cached data and serialize requests to the same address?
  - *Snooping-based protocols*: All caches observe each other’s actions through a shared bus (bus is the serialization point)
  - *Directory-based protocols*: A coherence directory tracks contents of private caches and serializes requests (directory is the serialization point)
Snooping-Based Coherence  
(*Goodman, 1983*)

Caches watch (snoop on) bus to keep all processors’ view of memory coherent
Snooping-Based Coherence

- Bus provides serialization point
  - Broadcast, totally ordered
Snooping-Based Coherence

- Bus provides serialization point
  - Broadcast, totally ordered

- Controller
  - One cache controller for each core “snoops” all bus transactions
  - Controller
    - Responds to requests from core and the bus
    - changes state of the selected cache block
    - generates bus transactions to access data or invalidate
Snooping-Based Coherence

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- Snoopy protocol (FSM)
  - State-transition diagram
  - Actions

![Diagram of processor and cache with state, tag, and data fields, and a note on snooping observed bus transaction]
Snooping-Based Coherence

• Bus provides serialization point
  – Broadcast, totally ordered

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  – One cache controller for each core “snoops” all bus transactions
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    • Responds to requests from core and the bus
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• Snoopy protocol (FSM)
  – State-transition diagram
  – Actions

• Handling writes:
  – Write-invalidate
  – Write-update

\[\text{Snoop (observed bus transaction)}\]
A Simple Protocol: Valid/Invalid (VI)

• Assume write-through caches
• Transition nomenclature:
  "triggering action / taken action(s)"

### Actions

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Read</td>
<td>Processor Write</td>
</tr>
<tr>
<td>PrRd / BusRd</td>
<td>PrWr / BusWr</td>
</tr>
<tr>
<td>PrRd / --</td>
<td>PrWr / --</td>
</tr>
<tr>
<td>BusWr / --</td>
<td>PrWr / BusWr</td>
</tr>
<tr>
<td>PrRd / BusRd</td>
<td>PrRd / --</td>
</tr>
<tr>
<td>BusRd / --</td>
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</tr>
<tr>
<td>PrWr / --</td>
<td>PrWr / --</td>
</tr>
<tr>
<td>BusWr / --</td>
<td>BusWr / --</td>
</tr>
</tbody>
</table>
Valid/Invalid Example

![Diagram showing the relationship between main memory, cores, and caches.](image-url)
Valid/Invalid Example

1. LD 0xA
Valid/Invalid Example

Main Memory

BusRd 0xA

Core 0

1

LD 0xA

Core 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
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Valid/Invalid Example

Main Memory

BusRd 0xA

Cache

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</thead>
<tbody>
<tr>
<td>0xA</td>
<td>V</td>
<td>2</td>
</tr>
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</table>

Core 0

1 LD 0xA

Core 1
Valid/Invalid Example

1. LD 0xA

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</table>
Valid/Invalid Example

1. LD 0xA

2. LD 0xA
Valid/Invalid Example

Core 0

1. LD 0xA

Core 1

2. LD 0xA

Cache

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<tr>
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Main Memory

BusRd 0xA
Valid/Invalid Example

1. LD 0xA

2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA

Additional loads satisfied locally, without BusRd
Valid/Invalid Example

1. LD 0xA

2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA

BusWr 0xA, 3
Valid/Invalid Example

BusWr 0xA, 3

<table>
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<tbody>
<tr>
<td>1</td>
<td>0xA</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

Core 0

1. LD 0xA
2. ST 0xA

Core 1

2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

Core 0
1. LD 0x0A
2. ST 0x0A
3. LD 0x0A

Core 1

Cache
<table>
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<tr>
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<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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Cache
<table>
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<tr>
<th>Tag</th>
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<tbody>
<tr>
<td>0xA</td>
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Main Memory

BusWr 0x0A, 3
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA

Main Memory

BusRd 0xA

Core 0

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<thead>
<tr>
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<tbody>
<tr>
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Cache

Core 1

<table>
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<tr>
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Cache
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA
Valid/Invalid Example

Main Memory

BusRd 0xA

Cache

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Core 0

1. LD 0xA
2. ST 0xA
3. LD 0xA
4. LD 0xA

VI Problems?
Valid/Invalid Example

VI Problems? Every write updates main memory
Every write requires broadcast & snoop

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA

Core 0
Cache
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<tbody>
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Core 1
Cache
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BusRd 0xA
Main Memory
Modified/Shared/Invalid (MSI) Protocol

- Allows writeback caches + satisfying writes locally

### Actions

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<tr>
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<tr>
<td>Processor Write (PrWr)</td>
</tr>
<tr>
<td>Bus Read (BusRd)</td>
</tr>
<tr>
<td>Bus Read Exclusive (BusRdX)</td>
</tr>
<tr>
<td>Bus Writeback (BusWB)</td>
</tr>
</tbody>
</table>
 MSI Example

Main Memory

Cache

Tag | State | Data
--- | --- | ---

Core 0

Cache

Tag | State | Data
--- | --- | ---

Core 1
MSI Example

Main Memory

Cache

<table>
<thead>
<tr>
<th>Tag</th>
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</table>

Core 0

Core 1

1. LD 0xA
MSI Example

Main Memory

BusRd 0xA

Cache

Tag | State | Data
---|---|---

Core 0

Core 1

LD 0xA
MSI Example

![Diagram of Main Memory, Cache, and Cores]

1. LD 0xA

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<thead>
<tr>
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<tbody>
<tr>
<td>0xA</td>
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BusRd 0xA
MSI Example

1. LD 0xA

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Main Memory

Core 0

Core 1
MSI Example

1. LD 0xA
2. LD 0xA
MSI Example

1. LD 0xA
2. LD 0xA
MSI Example

1. LD 0xA

2. LD 0xA
MSI Example

1. LD 0xA
2. LD 0xA

Additional loads satisfied locally, without BusRd (like in VI)
MSI Example

1. LD 0xA

2. LD 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA

BusRdX 0xA

Core 0: 0xA → S → 2

Core 1: 0xA → I → 2

Main Memory

L12-20
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA

Additional loads *and stores* from core 0 satisfied locally, without bus transactions (unlike in VI)
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

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MSI Example

1. LD 0xA
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3. ST 0xA
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MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
Cache interventions

- MSI allows caches to serve writes without updating memory, so main memory can have stale data
  - Core 0’s cache needs to supply data
  - But main memory may also respond!
- Cache must override response from main memory
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA

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<tbody>
<tr>
<td>0xA</td>
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MSI Example

Core 0

1. LD 0xA
2. ST 0xA
3. LD 0xA

Core 1

4. ST 0xA
5. LD 0xA

Cache

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Main Memory

BusRd 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA
MSI Example

1. BusRd 0xA
2. BusWB 0xA, 10
3. Core 0
   - LD 0xA
   - ST 0xA
   - LD 0xA
4. Core 1
   - LD 0xA
   - ST 0xA

---

Main Memory

Cache

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MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA
MSI Optimizations: Exclusive State

• Observation: Doing read-modify-write sequences on private data is common
  – What’s the problem with MSI?
MSI Optimizations: Exclusive State

• Observation: Doing read-modify-write sequences on private data is common
  – What’s the problem with MSI?

• Solution: E state (exclusive, clean)
  – If no other sharers, a read acquires line in E instead of S
  – Writes silently cause E→M (exclusive, dirty)
MESI: An Enhanced MSI protocol
increased performance for private read-write data

**M**: Modified Exclusive
**E**: Exclusive, unmodified
**S**: Shared
**I**: Invalid

```
M: PrWr / --
PrRd /--

S: BusRd / BusWB
PrWr/ BusRdX
PrRd /--

I: BusRdX / --
```

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Diagram:

- M (Modified Exclusive)
  - PrWr / --
  - PrRd / --
  - BusRd / BusWB

- E (Exclusive, unmodified)
  - PrWr / --
  - PrRd / --
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MESI: An Enhanced MSI protocol
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Each cache line has a tag

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### State Diagram

- **M**: Modified Exclusive
- **E**: Exclusive, unmodified
- **S**: Shared
- **I**: Invalid

**State Bits**
- **PrWr**: Write
- **PrRd**: Read

**Bus Signals**
- **BusRd**: Read
- **BusWB**: Write Back
- **BusRdX**: Read-Exclusive

**State Transitions**
- **M**:
  - **PrWr** / --
  - **PrRd** / --
- **E**:
  - **PrWr** / --
  - **BusRd / BusRdX**
  - **BusRd / BusWB**
  - **PrRd / BusRd** if no other sharers
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MSI Optimizations: Owner State

- Observation: On M→S transitions, must write back line!
  - What happens with frequent read-write sharing?
  - Can we defer the write after S?
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• Solution: O state (Owner)
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- MSI, MESI, MOSI, MOESI...
  - Typically E if private read-write >> shared read-only (common)
  - Typically O only if writebacks are expensive (main mem vs L3)
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

Req → Delay → Response

Simple, but low throughput!
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

Req

Delay

Response

Simple, but low throughput!

Split-Transaction Bus

Req1

Req2

Req3

Resp1

Resp3
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

- Supports multiple simultaneous transactions

Simple, but low throughput!

Split-Transaction Bus

- Supports multiple simultaneous transactions
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

[Diagram showing a single request and response with delay]

Simple, but low throughput!

Split-Transaction Bus

[Diagram showing multiple requests and responses simultaneously]

- Supports multiple simultaneous transactions
  - Higher throughput
  - Responses may arrive out of order
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

- **Supports multiple simultaneous transactions**
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- Often implemented as multiple buses (req+resp)

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Non-Atomicity → Transient States

- Protocol must handle lack of atomicity
- Two types of states
  - Stable (e.g. MSI)
  - Transient
- Split + race transitions
- More complex

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Scaling Cache Coherence

• Can implement ordered interconnects that scale better than buses...

Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors.
Scaling Cache Coherence

- Can implement ordered interconnects that scale better than buses...

Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors.

- ... but broadcast is fundamentally unscalable
  - Bandwidth, energy of transactions with 100s of cache snoops?
Directory-Based Coherence

- Route all coherence transactions through a directory
  - Tracks contents of private caches \(\rightarrow\) No broadcasts
  - Serves as ordering point for conflicting requests \(\rightarrow\) Unordered networks

*(more on next lecture)*
## Coherence and False Sharing

### Performance Issue #1

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<tr>
<th>state</th>
<th>blk addr</th>
<th>data0</th>
<th>data1</th>
<th>...</th>
<th>dataN</th>
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A cache block contains more than one word and cache coherence is done at the block-level and not word-level.
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**What can happen?** The block may be invalidated (ping-pong) many times unnecessarily because addresses are in the same block.
Coherence and False Sharing

Performance Issue #1

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**What can happen?** The block may be invalidated (ping-pong) many times unnecessarily because addresses are in the same block.

**How to address this problem?**
Coherence and Synchronization
Performance Issue #2

Processor 1
R ← 1
L: swap (mutex), R;
if <R> then goto L;
<critical section>
M[mutex] ← 0;

Processor 2
R ← 1
L: swap (mutex), R;
if <R> then goto L;
<critical section>
M[mutex] ← 0;

Processor 3
R ← 1
L: swap (mutex), R;
if <R> then goto L;
<critical section>
M[mutex] ← 0;

CPU-Memory Bus
Cache coherence protocols will cause `mutex` to ping-pong between P1’s and P2’s caches.
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Ping-ponging can be reduced by first reading the mutex location (non-atomically) and executing a swap only if it is found to be zero (test&test&set).
Coherence and Bus Occupancy
Performance Issue #3

• In general, an *atomic read-modify-write* instruction requires two memory (bus) operations without intervening memory operations by other processors.
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• In a multiprocessor setting, bus needs to be locked for the entire duration of the atomic read and write operation.
  ⇒ expensive for simple buses
  ⇒ *very expensive* for split-transaction buses
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  ⇒ expensive for simple buses
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• modern processors use
  
  *load-reserve*
  
  *store-conditional*
Load-reserve & Store-conditional

Special register(s) to hold reservation flag and address, and the outcome of store-conditional

Load-reserve R, (a):
<flag, adr> ← <1, a>;
R ← M[a];

Store-conditional (a), R:
if <flag, adr> == <1, a>
then cancel other procs’ reservation on a;
M[a] ← <R>;
status ← succeed;
else status ← fail;

If the snooper sees a store transaction to the address in the reserve register, the reserve bit is set to 0

- Several processors may reserve ‘a’ simultaneously
- These instructions are like ordinary loads and stores with respect to the bus traffic
The total number of memory (bus) transactions is not necessarily reduced, but splitting an atomic instruction into load-reserve & store-conditional:

- *increases bus utilization* (and reduces processor stall time), especially in split-transaction buses

- *reduces cache ping-pong effect* because processors trying to acquire a mutex do not have to perform stores each time
Thank you!

Next lecture: Directory-based Cache Coherence