Directory-Based Cache Coherence

Mengjia Yan
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M.I.T.
Maintaining Cache Coherence

It is sufficient to have hardware such that

- Only one processor at a time has write permission for a location
- No processor can load a stale copy of the location after a write
Maintaining Cache Coherence

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• Only one processor at a time has write permission for a location
• No processor can load a stale copy of the location after a write

⇒ A correct approach could be:
Maintaining Cache Coherence

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⇒ A correct approach could be:

write request:
The address is *invalidated* in all other caches *before* the write is performed
Maintaining Cache Coherence

It is sufficient to have hardware such that

• Only one processor at a time has write permission for a location
• No processor can load a stale copy of the location after a write

⇒ A correct approach could be:

write request:
   The address is *invalidated* in all other caches *before* the write is performed

read request:
   If a dirty copy is found in some cache, a write-back is performed before the memory is read
Directory-Based Coherence
[Censier and Feautrier, 1978]

Snoopy Protocols

- Snoopy schemes broadcast requests over memory bus
- Difficult to scale to large numbers of processors
- Requires additional bandwidth to cache tags for snoop requests
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Directory-Based Coherence
[Censier and Feautrier, 1978]

- Snoopy schemes broadcast requests over memory bus
- Difficult to scale to large numbers of processors
- Requires additional bandwidth to cache tags for snoop requests

- Directory schemes send messages to only those caches that might have the line
- Can scale to large numbers of processors
- Requires extra directory storage to track possible sharers
An MSI Directory Protocol

- Cache states: Modified (M) / Shared (S) / Invalid (I)

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
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<tbody>
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Cache 0

<table>
<thead>
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Core 0

<table>
<thead>
<tr>
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<tbody>
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Cache N

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</tbody>
</table>

Core N

...
An MSI Directory Protocol

- Cache states: Modified (M) / Shared (S) / Invalid (I)
- Directory states:
  - Uncached (Un): No sharers
  - Shared (Sh): One or more sharers with read permission (S)
  - Exclusive (Ex): A single sharer with read & write permissions (M)
An MSI Directory Protocol

- Cache states: Modified (M) / Shared (S) / Invalid (I)
- Directory states:
  - Uncached (Un): No sharers
  - Shared (Sh): One or more sharers with read permission (S)
  - Exclusive (Ex): A single sharer with read & write permissions (M)

- Transient states not drawn for clarity; for now, assume no racing requests
MSI Protocol: Caches (1/3)

Transitions initiated by processor accesses:

- M
- S
- I

<table>
<thead>
<tr>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Read (PrRd)</td>
</tr>
<tr>
<td>Processor Write (PrWr)</td>
</tr>
<tr>
<td>Shared Request (ShReq)</td>
</tr>
<tr>
<td>Exclusive Request (ExReq)</td>
</tr>
</tbody>
</table>
Transitions initiated by processor accesses:

- Processor Read (PrRd)
- Processor Write (PrWr)
- Shared Request (ShReq)
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MSI Protocol: Caches (1/3)

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MSI Protocol: Caches (1/3)

Transitions initiated by processor accesses:

- Processor Read (PrRd)
- Processor Write (PrWr)
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MSI Protocol: Caches (1/3)

Transitions initiated by processor accesses:

- Processor Write (PrWr) / Exclusive Request (ExReq)
- PrRd / --
- PrRd / Shared Request (ShReq)

Actions

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Transitions initiated by processor accesses:

- Processor Read (PrRd)
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- Shared Request (ShReq)
- Exclusive Request (ExReq)
MSI Protocol: Caches (2/3)

Transitions initiated by directory requests:

- M
- S
- I

<table>
<thead>
<tr>
<th>Actions</th>
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<tbody>
<tr>
<td>Invalidation Request (InvReq)</td>
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<tr>
<td>Downgrade Request (DownReq)</td>
</tr>
<tr>
<td>Invalidation Response (InvResp)</td>
</tr>
<tr>
<td>Downgrade Response (DownResp)</td>
</tr>
</tbody>
</table>
Transitions initiated by directory requests:

- Invalidation Request (InvReq)
- Downgrade Request (DownReq)
- Invalidation Response (InvResp)
- Downgrade Response (DownResp)
MSI Protocol: Caches (2/3)

Transitions initiated by directory requests:

M

↓

S

↓

I

InvReq / InvResp (with data)

DownReq / DownResp (with data)

<table>
<thead>
<tr>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalidation Request (InvReq)</td>
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<tr>
<td>Downgrade Request (DownReq)</td>
</tr>
<tr>
<td>Invalidation Response (InvResp)</td>
</tr>
<tr>
<td>Downgrade Response (DownResp)</td>
</tr>
</tbody>
</table>
MSI Protocol: Caches (2/3)

Transitions initiated by directory requests:

- DownReq / DownResp (with data)
- InvReq / InvResp (with data)
- InvReq / InvResp (without data)

Actions:

- Invalidation Request (InvReq)
- Downgrade Request (DownReq)
- Invalidation Response (InvResp)
- Downgrade Response (DownResp)
Transitions initiated by evictions:

- **M**
- **S**
- **I**

<table>
<thead>
<tr>
<th>Actions</th>
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</thead>
<tbody>
<tr>
<td>Writeback Request (WbReq)</td>
</tr>
</tbody>
</table>
Transitions initiated by evictions:

- **M** to **S**: Eviction / WbReq (with data)
- **S** to **I**: Writeback Request (WbReq)
MSI Protocol: Caches (3/3)

Transitions initiated by evictions:

- Eviction / WbReq (with data)
- Eviction / WbReq (without data)

Actions

- Writeback Request (WbReq)
MSI Protocol: Caches

Transitions initiated by processor accesses
Transitions initiated by directory requests
Transitions initiated by evictions
MSI Protocol: Directory (1/2)

Transitions initiated by data requests:

- Ex
- Sh
- Un
Transitions initiated by data requests:

- $\text{Ex}$
- $\text{Sh}$
  - $\text{ShReq} / \text{Sharers} = \text{Sharers} + \{P\}; \text{ShResp}$
  - $\text{ShReq} / \text{Sharers} = \{P\}; \text{ShResp}$
- $\text{Un}$
**Transitions initiated by data requests:**

- **ExReq** / **Sharers** = \{P\};  **ExResp**

  ![Diagram](image)

  - **Ex**
    - **Sh**
      - **ShReq** / **Sharers** = **Sharers** + \{P\};  **ShResp**
      - **ShReq** / **Sharers** = \{P\};  **ShResp**
    - **Un**
Transitions initiated by data requests:

ExReq / Sharers = \{P\}; ExResp

ExReq / Inv(Sharers – \{P\}); Sharers = \{P\}; ExResp

ShReq / Sharers = Sharers + \{P\}; ShResp

ShReq / Sharers = \{P\}; ShResp
Transitions initiated by data requests:

ExReq / Sharers = \{P\}; ExResp

ExReq / Inv(Sharers), Sharers=\{P\}; ExResp

ExReq / Inv(Sharers – \{P\}); Sharers = \{P\}; ExResp

ShReq / Sharers = Sharers + \{P\}; ShResp

ShReq / Sharers = \{P\}; ShResp
Transitions initiated by data requests:

ExReq / Sharers = {P}; ExResp

Ex

ExReq / Inv(Sharers), Sharers={P}; ExResp

Sh

ShReq / Down(Sharer); Sharers = Sharer + {P}; ShResp

Un

ShReq / Sharers = Sharers + {P}; ShResp

ShReq / Sharers = {P}; ShResp
MSI Protocol: Directory (2/2)

Transitions initiated by writeback requests:

- Ex
- Sh
- Un
Transitions initiated by writeback requests:

\[ \text{WbReq / Sharers} = \{\}; \text{WbResp} \]
Transitions initiated by writeback requests:

Ex

WbReq / Sharers = {}; WbResp

Sh

WbReq && |Sharers| > 1 /
Sharers = Sharers - {P}; WbResp

Un
Transitions initiated by writeback requests:

- **Ex**
  - WbReq / Sharers = {}; WbResp

- **Sh**
  - WbReq && |Sharers| > 1 /
    - Sharers = Sharers - {P}; WbResp

- **Un**
  - WbReq && |Sharers| == 1 /
    - Sharers = {}; WbResp
MSI Directory Protocol Example

Main Memory

Directory

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<thead>
<tr>
<th>Tag</th>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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</tr>
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</table>

Core 0

Cache 0

<table>
<thead>
<tr>
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<tbody>
<tr>
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Core 1

Cache 1

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td></td>
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<td></td>
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</table>

Core 2

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tbody>
</table>

L13-11
MSI Directory Protocol Example

1. LD 0xA
MSI Directory Protocol Example

1. LD 0xA
MSI Directory Protocol Example

1. LD 0xA

2. ShReq 0xA
MSI Directory Protocol Example

2 ShReq 0xA

1 LD 0xA
MSI Directory Protocol Example

1. LD 0xA

2. ShReq 0xA

3. Mem[0xA] = 3
MSI Directory Protocol Example

1. LD 0xA

2. ShReq 0xA

3. Mem[0xA] = 3

4. ShResp 0xA, data=3
MSI Directory Protocol Example

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MSI Directory Protocol Example

Main Memory

Directory

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<tbody>
<tr>
<td>0xA</td>
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<td>{0}</td>
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Cache 0

<table>
<thead>
<tr>
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</tr>
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<tbody>
<tr>
<td>0xA</td>
<td>S</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 0

Cache 1

<table>
<thead>
<tr>
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</tr>
</thead>
</table>

Core 1

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
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</tr>
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</table>

Core 2
MSI Directory Protocol Example

Main Memory

Directory

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<thead>
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<tbody>
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Cache 0

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<tbody>
<tr>
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<td>3</td>
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</tbody>
</table>

Cache 1

Cache 2

Core 0

Core 1

Core 2

1 LD 0xA
MSI Directory Protocol Example

Core 0
- Cache 0
  - Tag: 0xA
  - State: S
  - Data: 3

Core 1
- Cache 1
  - Tag: 0xA
  - State: I->S

Core 2
- Cache 2
  - Tag: 0xA
  - State: I->S

Directory

<table>
<thead>
<tr>
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</tr>
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<tbody>
<tr>
<td>0xA</td>
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<td>{0}</td>
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</tbody>
</table>

1. LD 0xA
MSI Directory Protocol Example

1. LD 0xA
2. ShReq 0xA
MSI Directory Protocol Example

Core 0

Cache 0

Tag | State | Data
---|------|----
0xA | S    | 3

Directory

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>0xA</td>
<td>Sh</td>
<td>{0,2}</td>
</tr>
</tbody>
</table>

Core 1

Cache 1

Tag | State | Data
---|------|----
0xA |      |    

Core 2

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I-&gt;S</td>
<td></td>
</tr>
</tbody>
</table>

1. LD 0xA
2. ShReq 0xA
MSI Directory Protocol Example

1. **LD 0xA**
   - Core 0
   - Cache 0: Tag 0xA, State S, Data 3

2. **ShReq 0xA**
   - Directory
   - Tag 0xA, State Sh, Sharers {0, 2}

3. **Mem[0xA] = 3**
   - Main Memory

Core 0

Core 1

Core 2
### MSI Directory Protocol Example

#### Core 0
- **Cache 0**
  - Tag: 0xA
  - State: S
  - Data: 3

#### Core 1
- **Cache 1**
  - Tag: 0xA
  - State: I\(\rightarrow\)S
  - Data: 0xA

#### Core 2
- **Cache 2**
  - Tag: 0xA
  - State: I\(\rightarrow\)S
  - Data: 0xA

#### Directory
- **Tag**: 0xA
- **State**: Sh
- **Sharers**: \{0,2\}

#### Main Memory
- **Mem[0xA]** = 3

#### Timeline:
1. **LD 0xA**
2. **ShReq 0xA**
3. **Mem[0xA] = 3**
4. **ShResp 0xA, data=3**
MSI Directory Protocol Example

1. LD 0xA
2. ShReq 0xA
3. Mem[0xA] = 3
4. ShResp 0xA, data=3
# MSI Directory Protocol Example

## Main Memory

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<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Sh</td>
<td>{0,2}</td>
</tr>
</tbody>
</table>

## Directory

### Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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<td>3</td>
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</table>

### Cache 1

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>0xA</td>
<td>I-&gt;M</td>
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### Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
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<th>Data</th>
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</thead>
<tbody>
<tr>
<td>0xA</td>
<td>S</td>
<td>3</td>
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</table>

1. **ST 0xA**
MSI Directory Protocol Example

1. ST 0xA

2. ExReq 0xA

<table>
<thead>
<tr>
<th>Directory</th>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0xA</td>
<td>Sh</td>
<td>{0,2}</td>
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</table>

<table>
<thead>
<tr>
<th>Cache 0</th>
<th>Tag</th>
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<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td>3</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Cache 1</th>
<th>Tag</th>
<th>State</th>
<th>Data</th>
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</thead>
<tbody>
<tr>
<td></td>
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<td>I-&gt;M</td>
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<tr>
<td></td>
<td>0xA</td>
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</table>
MSI Directory Protocol Example

1. ST 0xA
2. ExReq 0xA
3. InvReq 0xA
3. InvReq 0xA

Directory

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<tr>
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<tbody>
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<td>0xA</td>
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Main Memory

Cache 0

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Cache 1

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<tbody>
<tr>
<td>0xA</td>
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Cache 2

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MSI Directory Protocol Example

Main Memory

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<tbody>
<tr>
<td>0xA</td>
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Core 0

Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
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<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 1

Cache 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
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<tbody>
<tr>
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<tr>
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Core 2

Cache 2

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1. ST 0xA
2. ExReq 0xA
3. InvReq 0xA
### MSI Directory Protocol Example

#### Main Memory

#### Directory

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#### Core 0

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</table>

- **1** ST 0xA
- **2** ExReq 0xA
- **3** InvReq 0xA
- **4** InvResp 0xA
- **3** InvReq 0xA
- **4** InvResp 0xA
MSI Directory Protocol Example

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Ex</td>
<td>{1}</td>
</tr>
</tbody>
</table>

Main Memory

Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Cache 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I-&gt;M</td>
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</tbody>
</table>

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 0

Core 1

Core 2

1. ST 0xA
2. ExReq 0xA
3. InvReq 0xA
4. InvResp 0xA
3. InvReq 0xA
4. InvResp 0xA

October 24, 2022
MSI Directory Protocol Example

Main Memory

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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<td>{1}</td>
</tr>
</tbody>
</table>

Core 0

Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 1

Cache 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

Core 2

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

ST 0xA

ExReq 0xA

InvReq 0xA

InvResp 0xA

Mem[0xA] = 3
MSI Directory Protocol Example

Main Memory

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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<td>{1}</td>
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</tbody>
</table>

Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
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<td>3</td>
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</tbody>
</table>

Cache 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
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Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

ST 0xA

ExReq 0xA

Mem[0xA] = 3

InvReq 0xA

ExResp 0xA
data = 3

InvResp 0xA

InvResp 0xA

InvResp 0xA
MSI Directory Protocol Example

Main Memory

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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<td>{1}</td>
</tr>
</tbody>
</table>

Core 0

Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 1

Cache 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
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</table>

Core 2

Cache 2

<table>
<thead>
<tr>
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<th>State</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

1. ST 0xA
2. ExReq 0xA
3. InvReq 0xA
4. InvResp 0xA
5. Mem[0xA] = 3
6. ExResp 0xA data = 3
MSI Directory Protocol Example

Main Memory

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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Cache 0

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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
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</tr>
</tbody>
</table>

Cache 1

<table>
<thead>
<tr>
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<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
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<td>M-&gt;I</td>
<td>5</td>
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</tbody>
</table>

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 0

Core 1

ST 0xB

Core 2
MSI Directory Protocol Example

1. ST 0x8B

2. WbReq 0x8A, data=5
MSI Directory Protocol Example

1. ST 0xB

2. WbReq 0xA, data=5

3. Mem[0xA] = 5
MSI Directory Protocol Example

1. ST 0xB

2. WbReq 0xA, data=5

3. Mem[0xA] = 5

<table>
<thead>
<tr>
<th>Core 0</th>
<th>Cache 0</th>
<th>Cache 1</th>
<th>Cache 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tag</td>
<td>State</td>
<td>Data</td>
<td>Tag</td>
</tr>
<tr>
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<td>I</td>
<td>3</td>
<td>0xA</td>
</tr>
</tbody>
</table>

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Un</td>
<td>{}</td>
</tr>
</tbody>
</table>

Main Memory

Mem[0xA] = 5
MSI Directory Protocol Example

1. ST 0xB
2. WbReq 0xA, data=5
3. Mem[0xA] = 5
4. WbResp 0xA
MSI Directory Protocol Example

1. ST 0xB
2. WbReq 0xA, data=5
3. Mem[0xA] = 5
4. WbResp 0xA
MSI Directory Protocol Example

1. **ST 0xB**

2. **WbReq 0xA, data=5**

3. **Mem[0xA] = 5**

4. **WbResp 0xA**

5. **ExReq 0xB**
MSI Directory Protocol Example

1. ST 0xB

2. WbReq 0xA, data=5

3. Mem[0xA] = 5

4. WbResp 0xA

5. ExReq 0xB
MSI Directory Protocol Example

1. ST 0xB
2. WbReq 0xA, data=5
3. Mem[0xA] = 5
4. WbResp 0xA
5. ExReq 0xB
6. Mem[0xB] = 10
MSI Directory Protocol Example

1. ST 0xB
2. WbReq 0xA, data=5
3. Mem[0xA] = 5
4. WbResp 0xA
5. ExReq 0xB
6. Mem[0xB] = 10
7. ExResp 0xB, data=10
MSI Directory Protocol Example

1. ST 0xB

2. WbReq 0xA, data=5

3. Mem[0xA] = 5

4. WbResp 0xA

5. ExReq 0xB

6. Mem[0xB] = 10

7. ExResp 0xB, data=10
Why are 0xA’s wb and 0xB’s req serialized?
Why are 0xA’s wb and 0xB’s req serialized?

Structural dependence
### MSI Directory Protocol Example

**Core 0**
- **Cache 0**
  - **Tag**: 0xA
  - **State**: I
  - **Data**: 3

**Core 1**
- **Cache 1**
  - **Tag**: 0xB
  - **State**: M
  - **Data**: 10

**Core 2**
- **Cache 2**
  - **Tag**: 0xA
  - **State**: I
  - **Data**: 3

#### Why are 0xA’s wb and 0xB’s req serialized?

**Structural dependence**

#### Possible solutions?

---

**October 24, 2022**

MIT 6.5900 (ne 6.823) Fall 2022
Why are 0xA’s wb and 0xB’s req serialized?  
Structural dependence
Possible solutions?  Buffer outside of cache to hold write data
Miss Status Holding Register

MSHR – Holds load misses and writes outside of cache

MSHR entry

| V | X | Addr | Data |

• On eviction/writeback
  – No free MSHR entry: stall
  – Allocate new MSHR entry
  – When channel available send WBReq and data
  – Deallocate entry on WBResp
Miss Status Holding Register

MSHR – Holds load misses and writes outside of cache

<table>
<thead>
<tr>
<th>MSHR entry</th>
<th>per ld/st slots</th>
</tr>
</thead>
<tbody>
<tr>
<td>V</td>
<td>X</td>
</tr>
</tbody>
</table>

- **On cache load miss**
  - No free MSHR entry: stall
  - Allocate new MSHR entry
  - Send ShReq (or ExReq)
  - On *Resp forward data to CPU and cache
  - Deallocate MSHR
Miss Status Holding Register

MSHR – Holds load misses and writes outside of cache

<table>
<thead>
<tr>
<th>MSHR entry</th>
<th>per ld/st slots</th>
</tr>
</thead>
<tbody>
<tr>
<td>V</td>
<td>X</td>
</tr>
</tbody>
</table>

L13-17
Miss Status Holding Register

MSHR – Holds load misses and writes outside of cache

Per ld/st slots allow servicing multiple requests with one entry
Miss Status Holding Register

MSHR – Holds load misses and writes outside of cache

- On cache load miss
  - Look for matching address in MSHRs
    - If not found
      - If no free MSHR entry: stall
      - Allocate new MSHR entry and fill in
    - If found, just fill in per ld/st slot
  - Send ShReq (or ExReq)
  - On *Resp forward data to CPU and cache
  - Deallocate MSHR

Per ld/st slots allow servicing multiple requests with one entry
Directory Organization

• Requirement: Directory needs to keep track of all the cores that are sharing a cache block

• Challenge: For each block, the space needed to hold the list of sharers grows with number of possible sharers...
Flat, Memory-based Directories

- Dedicate a few bits of main memory to store the state and sharers of every line
- Encode sharers using a bit-vector

Main Memory

- 64 bytes
- 10 bits

State

Sharer Set

Sh: 0 1 0 0 1 1 0 0
Flat, Memory-based Directories

- Dedicate a few bits of main memory to store the state and sharers of every line
- Encode sharers using a bit-vector

![Diagram of main memory with state and sharer set]

- Simple
- Slow
- Very inefficient with many processors (~P bits/line)
Sparse Full-Map Directories

- Not every line in the system needs to be tracked – only those in private caches!
- Idea: Organize directory as a cache

Diagram showing directory entry format with line address 0xF00, state Sh, and sharer set 0 1 0 1 1 0 0.
Sparse Full-Map Directories

- Not every line in the system needs to be tracked – only those in private caches!
- Idea: Organize directory as a cache

Directory Entry Format

- Low latency, energy-efficient
- Bit-vectors grow with # cores → Area scales poorly
- Limited associativity → Directory-induced invalidations
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

![Diagram of memory and cache structures]

```
<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Sh</td>
<td>{0}</td>
<td>0xF</td>
<td>Ex</td>
<td>{1}</td>
</tr>
</tbody>
</table>
```

- Core 0:
  - Cache 0: Tag 0xA, State S, Data 3

- Core 1:
  - Cache 1: Tag 0xF, State M, Data 1

- Core 2:
  - Cache 2: Empty

- Core 1 executes LD 0xB
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
<th>Tag</th>
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</tr>
</thead>
<tbody>
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<td>Sh</td>
<td>{0}</td>
<td>0xF</td>
<td>Ex</td>
<td>{1}</td>
</tr>
</tbody>
</table>

Main Memory

Cache 0
- 0xA S 3

Cache 1
- 0xF M 1

Cache 2
- 0xB I->S

Core 0
-Core 1
-Core 2

LD 0xB
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address.
- Example: 2-way set-associative sparse directory.

### Main Memory

#### Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
<th>Tag</th>
<th>State</th>
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<tbody>
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<td>Sh</td>
<td>{0}</td>
<td>0xF</td>
<td>Ex</td>
<td>{1}</td>
</tr>
</tbody>
</table>

### Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>S</td>
<td>3</td>
</tr>
</tbody>
</table>

### Cache 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
<td>M</td>
<td>1</td>
</tr>
</tbody>
</table>

### Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xB</td>
<td>I-&gt;S</td>
<td></td>
</tr>
</tbody>
</table>

#### Core 0

1. LD 0xB

#### Core 1

2. ShReq 0xB
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

<table>
<thead>
<tr>
<th>Main Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Directory</td>
</tr>
<tr>
<td>Tag</td>
</tr>
<tr>
<td>------</td>
</tr>
<tr>
<td>0xA</td>
</tr>
</tbody>
</table>

1. LD 0xB
2. ShReq 0xB
3. InvReq 0xA
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Sh</td>
<td>{0}</td>
<td>0xF</td>
<td>Ex</td>
<td>{1}</td>
</tr>
</tbody>
</table>

1. LD 0xB
2. ShReq 0xB
3. InvReq 0xA
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

```
Main Memory

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
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<table>
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<tr>
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<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
<td>Ex</td>
<td>{1}</td>
</tr>
</tbody>
</table>

Core 0

Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 1

Cache 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
<td>M</td>
<td>1</td>
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</tbody>
</table>

Core 2

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xB</td>
<td>I-&gt;S</td>
<td></td>
</tr>
</tbody>
</table>
```

1. LD 0xB
2. ShReq 0xB
3. InvReq 0xA
4. InvResp 0xA
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

---

**Main Memory**

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xB</td>
<td>Sh</td>
<td>{2}</td>
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</tbody>
</table>

**Directory**

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
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</table>

**Cache 0**

<table>
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<tr>
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</tr>
</thead>
<tbody>
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</table>

**Cache 1**

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
<td>M</td>
<td>1</td>
</tr>
</tbody>
</table>

**Cache 2**

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xB</td>
<td>I-&gt;S</td>
<td></td>
</tr>
</tbody>
</table>

**Core 0**

**Core 1**

**Core 2**

**Core 0**

**Core 1**

**Core 2**

- **1** LD 0xB
- **2** ShReq 0xB
- **3** InvReq 0xA
- **4** InvResp 0xA
- **5** Mem[0xB] = 5
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

```
<table>
<thead>
<tr>
<th>Tag</th>
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<tbody>
<tr>
<td>0xB</td>
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</tbody>
</table>
```

---

1. LD 0xB
2. ShReq 0xB
3. InvReq 0xA
4. InvResp 0xA
5. Mem[0xB] = 5
6. ShResp 0xB, data=5
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

```
<table>
<thead>
<tr>
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<tbody>
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```

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<tbody>
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<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
<td>M</td>
<td>1</td>
</tr>
</tbody>
</table>

```

```
Core 0
```

```
Core 1
```

```
Core 2
```

```
Mem[0xB] = 5
```

```
InvReq 0xA
```

```
InvResp 0xA
```

```
ShReq 0xB
```

```
ShResp 0xB, data=5
```

```
LD 0xB
```
Directory-Induced Invalidations

- To retain inclusion, must invalidate all sharers of an entry before reusing it for another address
- Example: 2-way set-associative sparse directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xB</td>
<td>Sh</td>
<td>{2}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
<td>Ex</td>
<td>{1}</td>
</tr>
</tbody>
</table>

```
Core 0
```
```
Cache 0
```
```
Tag | State | Data |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>
```
```
Core 1
```
```
Cache 1
```
```
Tag | State | Data |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF</td>
<td>M</td>
<td>1</td>
</tr>
</tbody>
</table>
```
```
Core 2
```
```
Cache 2
```
```
Tag | State | Data |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0xB</td>
<td>S</td>
<td>5</td>
</tr>
</tbody>
</table>
```

```
LD 0xB
```
```
InvReq 0xA
```
```
InvResp 0xA
```
```
ShReq 0xB
```
```
Mem[0xB] = 5
```
```
ShResp 0xB, data=5
```
```
How many entries should the directory have?
```
Inexact Representations of Sharer Sets

- Coarse-grain bit-vectors (e.g., 1 bit per 4 cores)

<table>
<thead>
<tr>
<th>Sharer Set</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4-7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8-11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12-15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16-19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20-23</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Limited pointers: Maintain a few sharer pointers, on overflow mark ‘all’ and broadcast (or invalidate another sharer)

<table>
<thead>
<tr>
<th>Sharer Set</th>
<th>0</th>
<th>8</th>
<th>14</th>
<th>33</th>
</tr>
</thead>
<tbody>
<tr>
<td>all</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>sharer 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>sharer 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>sharer 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Allow false positives (e.g., Bloom filters)
Inexact Representations of Sharer Sets

- **Coarse-grain bit-vectors (e.g., 1 bit per 4 cores)**

  Sharer Set

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0-3</td>
<td>4-7</td>
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<td>12-15</td>
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<td>20-23</td>
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- **Limited pointers**: Maintain a few sharer pointers, on overflow mark ‘all’ and broadcast (or invalidate another sharer)

  Sharer Set

<p>| | | | |</p>
<table>
<thead>
<tr>
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<td>33</td>
</tr>
<tr>
<td>all</td>
<td>sharer 1</td>
<td>sharer 2</td>
<td>sharer 3</td>
</tr>
</tbody>
</table>

- **Allow false positives (e.g., Bloom filters)**

  ✓ Reduced area & energy
  ✗ Overheads still not scalable (these techniques simply play with constant factors)
  ✗ Inexact sharers → Broadcasts, invalidations or spurious invalidations and downgrades
In-Cache Directories

- **Common multicore memory hierarchy:**
  - 1+ levels of private caches
  - A shared last-level cache
  - Need to enforce coherence among private caches

- **Idea:** Embed the directory information in shared cache tags
  - Shared cache must be inclusive
In-Cache Directories

- **Common multicore memory hierarchy:**
  - 1+ levels of private caches
  - A shared last-level cache
  - Need to enforce coherence among private caches

- **Idea:** Embed the directory information in shared cache tags
  - Shared cache must be inclusive

✅ Avoids tag overheads & separate lookups
❌ Can be inefficient if shared cache size >> sum(private cache sizes)
Extra Hops and 3-Hop Protocols
Reducing Protocol Latency

- Problem: Data in another cache needs to pass through the directory, adding latency
- Optimization: Forward data to requester directly

<table>
<thead>
<tr>
<th>Main Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Directory</td>
</tr>
<tr>
<td>Tag</td>
</tr>
<tr>
<td>------</td>
</tr>
<tr>
<td>0xA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Core 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache 0</td>
</tr>
<tr>
<td>Tag</td>
</tr>
<tr>
<td>-----</td>
</tr>
<tr>
<td>0xA</td>
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</tbody>
</table>

<table>
<thead>
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</tr>
</thead>
<tbody>
<tr>
<td>Cache 1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Core 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache 2</td>
</tr>
</tbody>
</table>
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**Main Memory**

<table>
<thead>
<tr>
<th>Directory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tag</strong></td>
</tr>
<tr>
<td>0xA</td>
</tr>
</tbody>
</table>

**Cache 0**

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>M</td>
<td>3</td>
</tr>
</tbody>
</table>

**Cache 1**

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
</table>

**Cache 2**

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
</table>

**Core 0**

**Core 1**

**Core 2**

1. ST 0xA
Extra Hops and 3-Hop Protocols
Reducing Protocol Latency

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<table>
<thead>
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<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Ex</td>
<td>{0}</td>
</tr>
</tbody>
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**Main Memory**

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<tr>
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<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Ex</td>
<td>{0}</td>
</tr>
</tbody>
</table>

---

**Cache 0**

- **Core 0**
  - Tag: 0xA
  - State: M
  - Data: 3

**Cache 1**

- **Core 1**
  - Tag: 0xA
  - State: Ex
  - Data: M

**Cache 2**

- **Core 2**
  - Tag: 0xA
  - State: I->M
  - Data: }

1. ST 0xA
2. ExReq 0xA
Extra Hops and 3-Hop Protocols
Reducing Protocol Latency

- Problem: Data in another cache needs to pass through the directory, adding latency
- Optimization: Forward data to requester directly

![Diagram](attachment:image.png)
Extra Hops and 3-Hop Protocols
Reducing Protocol Latency

- Problem: Data in another cache needs to pass through the directory, adding latency
- Optimization: Forward data to requester directly

![Diagram of cache memory hierarchy and directory]

1. **ST 0xA**
2. **ExReq 0xA**
3. **ExFwd 0xA, req=2**
Extra Hops and 3-Hop Protocols
Reducing Protocol Latency

- Problem: Data in another cache needs to pass through the directory, adding latency
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3. ExFwd 0xA, req=2
Extra Hops and 3-Hop Protocols
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- Problem: Data in another cache needs to pass through the directory, adding latency
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### Diagram

- **Main Memory**
  - Directory
    - | Tag | State | Sharers |
    - |-----|-------|---------|
    - | 0xA | Ex->Ex | {2}     |

- **Cache 0**
  - | Tag | State | Data |
  - |-----|-------|------|
  - | 0xA | I     | 3    |

- **Cache 1**
  - | Tag | State | Data |
  - |-----|-------|------|
  - | 0xA | I->M  |      |

- **Cache 2**
  - | Tag | State | Data |
  - |-----|-------|------|
  - | 0xA | I->M  |      |

- **Core 0**
- **Core 1**
- **Core 2**

1. ST 0xA
2. ExReq 0xA
3. ExFwd 0xA, req=2
4. ExResp 0xA, data=3
Extra Hops and 3-Hop Protocols
Reducing Protocol Latency

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Main Memory

Directory

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Ex-&gt;Ex</td>
<td>{2}</td>
</tr>
</tbody>
</table>

Core 0

- ExFwd 0xA, req=2

Core 1

- ExReq 0xA

Core 2

- ST 0xA

- ExResp 0xA, data=3

Core 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 1

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>M</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>
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---

Main Memory

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<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Ex-&gt;Ex</td>
<td>{2}</td>
</tr>
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</table>

---

Core 0

Cache 0

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>I</td>
<td>3</td>
</tr>
</tbody>
</table>

Core 1

Cache 1

Core 2

Cache 2

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>M</td>
<td>3</td>
</tr>
</tbody>
</table>

---

1. ST 0xA

2. ExReq 0xA

3. ExFwd 0xA, req=2

4. ExAck 0xA

---

ExResp 0xA, data=3
Extra Hops and 3-Hop Protocols
Reducing Protocol Latency

- Problem: Data in another cache needs to pass through the directory, adding latency
- Optimization: Forward data to requester directly

\[\begin{array}{|c|c|c|}
\hline
\text{Tag} & \text{State} & \text{Sharers} \\
\hline
0xA & \text{Ex} & \{2\} \\
\hline
\end{array}\]
Protocol Races

- Directory serializes multiple requests for the same address
  - Same-address requests are queued or NACKed and retried
- But races still exist due to conflicting requests
- Example: Upgrade race

### Main Memory

<table>
<thead>
<tr>
<th>ReqQ</th>
<th>Directory</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tag</td>
</tr>
<tr>
<td></td>
<td>0xA</td>
</tr>
</tbody>
</table>

### Core 0

<table>
<thead>
<tr>
<th>Cache 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tag</td>
</tr>
<tr>
<td>0xA</td>
</tr>
</tbody>
</table>

### Core 1

<table>
<thead>
<tr>
<th>Cache 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tag</td>
</tr>
<tr>
<td>0xA</td>
</tr>
</tbody>
</table>
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<tr>
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<th>Directory</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tag</td>
</tr>
<tr>
<td></td>
<td>0xA</td>
</tr>
</tbody>
</table>

### Core 0
- Cache 0
  - Tag | State | Data |
  - 0xA | S     | 3    |
- Core 0
  - ST 0xA

### Core 1
- Cache 1
  - Tag | State | Data |
  - 0xA | S     | 3    |
- Core 1
  - ST 0xA
Protocol Races

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Protocol Races

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- Example: Upgrade race

Caches 0 and 1 issue simultaneous ExReqs

1. ST 0xA
2. ExReq 0xA

1’. ST 0xA
2’. ExReq 0xA

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Sharers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>Sh</td>
<td>{0,2}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tag</th>
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<tbody>
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- Directory serializes multiple requests for the same address
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Caches 0 and 1 issue simultaneous ExReqs.
Directory starts serving cache 0’s ExReq, queues cache 1’s
Protocol Races

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  - Same-address requests are queued or NACKed and retried
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Caches 0 and 1 issue simultaneous ExReqs
Directory starts serving cache 0’s ExReq, queues cache 1’s

Cache 1 expected ExResp, but got InvReq!
Protocol Races

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- But races still exist due to conflicting requests
- Example: Upgrade race

Caches 0 and 1 issue simultaneous ExReqs
Directory starts serving cache 0’s ExReq, queues cache 1’s

Cache 1 expected ExResp, but got InvReq!

Cache 1 should transition from S->M to I->M and send InvResp
Avoiding Protocol Deadlock

- Protocols can cause deadlocks even if network is deadlock-free! *(more on this later)*

Example: Both nodes saturate all intermediate buffers with requests to each other, blocking responses from entering the network.
Avoiding Protocol Deadlock

- Protocols can cause deadlocks even if network is deadlock-free! *(more on this later)*

Example: Both nodes saturate all intermediate buffers with requests to each other, blocking responses from entering the network.

- **Solution:** Separate *virtual networks*
  - Different sets of virtual channels and endpoint buffers
  - Same physical routers and links
Avoiding Protocol Deadlock

- Protocols can cause deadlocks even if network is deadlock-free! (*more on this later*)

  Example: Both nodes saturate all intermediate buffers with requests to each other, blocking responses from entering the network.

- Solution: Separate *virtual networks*
  - Different sets of virtual channels and endpoint buffers
  - Same physical routers and links

- Most protocols require at least 2 virtual networks (for requests and replies), often >2 needed
Coherence in Multi-Level Hierarchies

- Can use the same or different protocols to keep coherence across multiple levels
- Key invariant: Ensure sufficient permissions in all intermediate levels
- Example: 8-socket Xeon E7 (8 cores/socket)
A cache block contains more than one word and cache coherence is done at the block-level and not word-level.
Coherence and False Sharing

Performance Issue #1

A cache block contains more than one word and cache coherence is done at the block-level and not word-level.

Suppose $P_1$ writes $\text{word}_i$ and $P_2$ writes $\text{word}_k$ and both words have the same block address.

*What can happen?*
A cache block contains more than one word and cache coherence is done at the block-level and not word-level.

Suppose $P_1$ writes $\text{word}_i$ and $P_2$ writes $\text{word}_k$ and both words have the same block address.

**What can happen?** The block may be invalidated (ping-pong) many times unnecessarily because addresses are in the same block.
Coherence and False Sharing

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What can happen? The block may be invalidated (ping-pong) many times unnecessarily because addresses are in the same block.

How to address this problem?
Coherence and Synchronization

Performance Issue #2

Processor 1

R ← 1
L: swap (R, mutex);
   if <R> then goto L;
   <critical section>
   M[mutex] ← 0;

Processor 2

R ← 1
L: swap (R, mutex);
   if <R> then goto L;
   <critical section>
   M[mutex] ← 0;

Processor 3

R ← 1
L: swap (R, mutex);
   if <R> then goto L;
   <critical section>
   M[mutex] ← 0;

swap (R, mutex):
   R = test&set(mutex)
Coherence and Synchronization
Performance Issue #2

Processor 1
R ← 1
L: swap (R, mutex);
   if <R> then goto L;
   <critical section>
   M[mutex] ← 0;

cache

Processor 2
R ← 1
L: swap (R, mutex);
   if <R> then goto L;
   <critical section>
   M[mutex] ← 0;

cache

Processor 3
R ← 1
L: swap (R, mutex);
   if <R> then goto L;
   <critical section>
   M[mutex] ← 0;

mutex=1

CPU-Memory Bus

swap (R, mutex):
   R = test&set(mutex)

test&set(mutex):
   old_val = M[mutex];
   M[mutex] = 1;
   return old_val;
Our cache coherence protocol will introduce a performance issue here. What is the problem?
Cache coherence protocols will cause `mutex` to *ping-pong* between P1’s and P2’s caches.
Cache coherence protocols will cause `mutex` to ping-pong between P1’s and P2’s caches.

Ping-ponging can be reduced by first reading the `mutex` location (non-atomically) and executing a swap only if it is found to be zero (test&test&set).
In general, an *atomic read-modify-write* instruction requires two memory (bus) operations without intervening memory operations by other processors.

Implementation options:
- *With snoopy coherence, lock the bus* → expensive
- *With directory-based coherence, lock the line in the cache (prevent invalidations or evictions until atomic op finishes)* → complex

```
test&set(mutex):
    old_val = M[mutex];
    M[mutex] = 1;
    return old_val;
```
In general, an atomic read-modify-write instruction requires two memory (bus) operations without intervening memory operations by other processors.

Implementation options:
- With snoopy coherence, lock the bus → expensive
- With directory-based coherence, lock the line in the cache (prevent invalidations or evictions until atomic op finishes) → complex

Modern processors use load-reserve store-conditional.

```c
test&set(mutex):
    old_val = M[mutex];
    M[mutex] = 1;
    return old_val;
```
If the cache receives an invalidation to the address in the reserve register, the reserve bit is set to 0

- Several processors may reserve ‘a’ simultaneously
- These instructions are like ordinary loads and stores with respect to the bus traffic

Load-reserve R, (a):
\[
\text{<flag, adr> } \leftarrow \text{<1, a>};
\]
R \leftarrow \text{M[a]};

Store-conditional (a), R:
\[
\text{if <flag, adr> } == \text{<1, a>}
\]
\[
\text{then } \text{cancel other procs’ reservation on a;}
\]
\[
\text{M[a] } \leftarrow \text{<R>};
\]
\[
\text{status } \leftarrow \text{succeed;}
\]
\[
\text{else } \text{status } \leftarrow \text{fail;}
\]
Load-Reserve/Store-Conditional

Swap implemented with Ld-Reserve/St-Conditional

# Swap(R1, mutex):

L: Ld-Reserve R2, (mutex) 
   St-Conditional (mutex), R1 
   if (status == fail) goto L 
   R1 <- R2
The total number of coherence transactions is not necessarily reduced, but splitting an atomic instruction into load-reserve & store-conditional:

- *increases utilization* (and reduces processor stall time), especially in split-transaction buses and directories

- *reduces cache ping-pong effect* because processors trying to acquire a semaphore do not have to perform stores each time
Thank you!

Next Lecture: Consistency and Relaxed Memory Models