Microcoded and VLIW Processors

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Hardwired vs Microcoded Processors

• All processors we have seen so far are hardwired: The microarchitecture directly implements all the instructions in the ISA

• Microcoded processors add a layer of interpretation: Each ISA instruction is executed as a sequence of simpler microinstructions
  – Simpler implementation
  – Lower performance than hardwired (CPI > 1)

• Microcoding common until the 80s, still in use today (e.g., complex x86 instructions are decoded into multiple “micro-ops”)
Embed the control logic state table in a read-only memory array

- op code
- conditional flip-flop
- \( \mu \) address

Decoder

Matrix A

Matrix B

Control lines to ALU, MUXs, Registers
Microcoded Microarchitecture

μcontroller (ROM)

Datapath

Memory (RAM)

busy?
zero?
opcode

enMem
MemWrt

holds fixed microcode instructions

holds user program written in macrocode instructions (e.g., MIPS, x86, etc.)

Data
Addr
A Bus-based Datapath for MIPS

Microinstruction: register to register transfer (17 control signals)

MA ← PC means RegSel = PC; enReg=yes; IdMA=yes
B ← Reg[rt] means RegSel = rt; enReg=yes; IdB=yes

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Memory Module

- Assumption: Memory operates asynchronously and is slow compared to Reg-to-Reg transfers
Microcode Controller

\[ \mu \text{JumpType} = \text{next} \mid \text{spin} \mid \text{fetch} \mid \text{dispatch} \mid \text{feqz} \mid \text{fnez} \]

Control Signals (17)
## Jump Logic

\[
\mu\text{PCSrc} = \text{Case} \quad \mu\text{JumpTypes}
\]

<table>
<thead>
<tr>
<th>(\text{next})</th>
<th>(\Rightarrow)</th>
<th>(\mu\text{PC}+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\text{spin})</td>
<td>(\Rightarrow)</td>
<td>if (busy) then (\mu\text{PC}) else (\mu\text{PC}+1)</td>
</tr>
<tr>
<td>(\text{fetch})</td>
<td>(\Rightarrow)</td>
<td>absolute</td>
</tr>
<tr>
<td>(\text{dispatch})</td>
<td>(\Rightarrow)</td>
<td>op-group</td>
</tr>
<tr>
<td>(\text{f eqz})</td>
<td>(\Rightarrow)</td>
<td>if (zero) then absolute else (\mu\text{PC}+1)</td>
</tr>
<tr>
<td>(\text{fnez})</td>
<td>(\Rightarrow)</td>
<td>if (zero) then (\mu\text{PC}+1) else absolute</td>
</tr>
</tbody>
</table>
Instruction Execution

Execution of a MIPS instruction involves

1. instruction fetch
2. decode and register fetch
3. ALU operation
4. memory operation (optional)
5. write back to register file (optional)
   + the computation of the
     next instruction address
Instruction Fetch

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>fetch₀</td>
<td>MA ← PC</td>
<td>next</td>
</tr>
<tr>
<td>fetch₁</td>
<td>IR ← Memory</td>
<td>spin</td>
</tr>
<tr>
<td>fetch₂</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>fetch₃</td>
<td>PC ← A + 4</td>
<td>dispatch</td>
</tr>
</tbody>
</table>

... ALU₀ A ← Reg[rs] next
... ALU₁ B ← Reg[rt] next
... ALU₂ Reg[rd] ← func(A,B) fetch

ALUi₀ A ← Reg[rs] next
ALUi₁ B ← sExt₁₆(Imm) next
ALUi₂ Reg[rd] ← Op(A,B) fetch
## Load & Store

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>LW₀</td>
<td>A ← Reg[rs]</td>
<td>next</td>
</tr>
<tr>
<td>LW₁</td>
<td>B ← sExt₁₆(Imm)</td>
<td>next</td>
</tr>
<tr>
<td>LW₂</td>
<td>MA ← A+B</td>
<td>next</td>
</tr>
<tr>
<td>LW₃</td>
<td>Reg[rt] ← Memory</td>
<td>spin</td>
</tr>
<tr>
<td>LW₄</td>
<td></td>
<td>fetch</td>
</tr>
<tr>
<td>SW₀</td>
<td>A ← Reg[rs]</td>
<td>next</td>
</tr>
<tr>
<td>SW₁</td>
<td>B ← sExt₁₆(Imm)</td>
<td>next</td>
</tr>
<tr>
<td>SW₂</td>
<td>MA ← A+B</td>
<td>next</td>
</tr>
<tr>
<td>SW₃</td>
<td>Memory ← Reg[rt]</td>
<td>spin</td>
</tr>
<tr>
<td>SW₄</td>
<td></td>
<td>fetch</td>
</tr>
</tbody>
</table>
# Branches

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEQZ₀</td>
<td>A ← Reg[rs]</td>
<td>next</td>
</tr>
<tr>
<td>BEQZ₁</td>
<td></td>
<td>fnez</td>
</tr>
<tr>
<td>BEQZ₂</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>BEQZ₃</td>
<td>B ← sExt₁₆(Imm&lt;&lt;2)</td>
<td>next</td>
</tr>
<tr>
<td>BEQZ₄</td>
<td>PC ← A+B</td>
<td>fetch</td>
</tr>
<tr>
<td>BNEZ₀</td>
<td>A ← Reg[rs]</td>
<td>next</td>
</tr>
<tr>
<td>BNEZ₁</td>
<td></td>
<td>feqz</td>
</tr>
<tr>
<td>BNEZ₂</td>
<td>A ← PC</td>
<td>next</td>
</tr>
<tr>
<td>BNEZ₃</td>
<td>B ← sExt₁₆(Imm&lt;&lt;2)</td>
<td>next</td>
</tr>
<tr>
<td>BNEZ₄</td>
<td>PC ← A+B</td>
<td>fetch</td>
</tr>
</tbody>
</table>
# Jumps

<table>
<thead>
<tr>
<th>State</th>
<th>Control points</th>
<th>next-state</th>
</tr>
</thead>
<tbody>
<tr>
<td>J₀</td>
<td>$A \leftarrow \text{PC}$</td>
<td>next</td>
</tr>
<tr>
<td>J₁</td>
<td>$B \leftarrow \text{IR}$</td>
<td>next</td>
</tr>
<tr>
<td>J₂</td>
<td>$\text{PC} \leftarrow \text{JumpTarg}(A,B)$</td>
<td>fetch</td>
</tr>
<tr>
<td>JR₀</td>
<td>$A \leftarrow \text{Reg[rs]}$</td>
<td>next</td>
</tr>
<tr>
<td>JR₁</td>
<td>$\text{PC} \leftarrow A$</td>
<td>fetch</td>
</tr>
<tr>
<td>JAL₀</td>
<td>$A \leftarrow \text{PC}$</td>
<td>next</td>
</tr>
<tr>
<td>JAL₁</td>
<td>$\text{Reg[31]} \leftarrow A$</td>
<td>next</td>
</tr>
<tr>
<td>JAL₂</td>
<td>$B \leftarrow \text{IR}$</td>
<td>next</td>
</tr>
<tr>
<td>JAL₃</td>
<td>$\text{PC} \leftarrow \text{JumpTarg}(A,B)$</td>
<td>fetch</td>
</tr>
<tr>
<td>JALR₀</td>
<td>$A \leftarrow \text{PC}$</td>
<td>next</td>
</tr>
<tr>
<td>JALR₁</td>
<td>$B \leftarrow \text{Reg[rs]}$</td>
<td>next</td>
</tr>
<tr>
<td>JALR₂</td>
<td>$\text{Reg[31]} \leftarrow A$</td>
<td>next</td>
</tr>
<tr>
<td>JALR₃</td>
<td>$\text{PC} \leftarrow B$</td>
<td>fetch</td>
</tr>
</tbody>
</table>
VAX 11-780 Microcode (1978)
Very Long Instruction Word (VLIW) Processors
Sequential ISA Bottleneck

Sequential source code

a = foo(b);
for (i=0, i<

Superscalar compiler

Find independent operations

Schedule operations

Sequential machine code

Superscalar processor

Check instruction dependencies

Schedule execution

L19-16
VLIW: Very Long Instruction Word

- Multiple operations packed into one instruction
- Each operation slot is for a fixed function
- Constant operation latencies are specified

Two Integer Units, Single Cycle Latency
Two Load/Store Units, Three Cycle Latency
Two Floating-Point Units, Four Cycle Latency
VLIW Design Principles

The architecture:
• Allows operation parallelism within an instruction
  – No cross-operation RAW check
• Provides deterministic latency for all operations
  – Latency measured in ‘instructions’
  – No data use allowed before specified latency with no data interlocks

The compiler:
• Schedules (reorders) to maximize parallel execution
• Guarantees intra-instruction parallelism
• Schedules to avoid data hazards (no interlocks)
  – Typically separates operations with explicit NOPs
Early VLIW Machines

• FPS AP120B (1976)
  – scientific attached array processor
  – first commercial wide instruction machine
  – hand-coded vector math libraries using software pipelining and loop unrolling

• Multiflow Trace (1987)
  – commercialization of ideas from Fisher’s Yale group including “trace scheduling”
  – available in configurations with 7, 14, or 28 operations/instruction
  – 28 operations packed into a 1024-bit instruction word

• Cydrome Cydra-5 (1987)
  – 7 operations encoded in 256-bit instruction word
  – rotating register file
### Loop Execution

```c
for (i=0; i<N; i++)
```

**Compile**

- `loop: ld f1, 0(r1)`
- `add r1, 8`
- `fadd f2, f0, f1`
- `sd f2, 0(r2)`
- `add r2, 8`
- `bne r1, r3, loop`

**Schedule**

<table>
<thead>
<tr>
<th>Int1</th>
<th>Int 2</th>
<th>M1</th>
<th>M2</th>
<th>FP+</th>
<th>FPx</th>
</tr>
</thead>
<tbody>
<tr>
<td>add r1</td>
<td>ld</td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td>fadd</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>add r2</td>
<td>bne</td>
<td>sd</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

How many FP ops/cycle?

1 fadd / 8 cycles = 0.125
Loop Unrolling

Unroll inner loop to perform 4 iterations at once

Is this code correct?

No, need to handle values of N that are not multiples of unrolling factor with final cleanup loop
Scheduling Loop Unrolled Code

Unroll 4 ways

loop:  ld f1, 0(r1)
   ld f2, 8(r1)
   ld f3, 16(r1)
   ld f4, 24(r1)
   add r1, 32
   fadd f5, f0, f1
   fadd f6, f0, f2
   fadd f7, f0, f3
   fadd f8, f0, f4
   sd f5, 0(r2)
   sd f6, 8(r2)
   sd f7, 16(r2)
   sd f8, 24(r2)
   add r2, 32
   bne r1, r3, loop

Schedule

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<tr>
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<tr>
<td>loop:</td>
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</tr>
<tr>
<td>ld f1</td>
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<td></td>
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<tr>
<td>ld f2</td>
<td></td>
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<tr>
<td>ld f3</td>
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<tr>
<td>ld f4</td>
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<td></td>
</tr>
<tr>
<td>add r1</td>
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<tr>
<td>fadd f5</td>
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<tr>
<td>fadd f6</td>
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<td></td>
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<tr>
<td>fadd f7</td>
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<tr>
<td>fadd f8</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>sd f5</td>
<td></td>
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</tr>
<tr>
<td>sd f6</td>
<td></td>
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<tr>
<td>sd f7</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>add r2</td>
<td></td>
<td></td>
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<tr>
<td>bne</td>
<td></td>
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<tr>
<td>sd f8</td>
<td></td>
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</tr>
</tbody>
</table>

How many FLOPS/cycle?

4 fadds / 11 cycles = 0.36
Software Pipelining

Unroll 4 ways first

loop: ld f1, 0(r1)
    ld f2, 8(r1)
    ld f3, 16(r1)
    ld f4, 24(r1)
    add r1, 32
    fadd f5, f0, f1
    fadd f6, f0, f2
    fadd f7, f0, f3
    fadd f8, f0, f4
    sd f5, 0(r2)
    sd f6, 8(r2)
    sd f7, 16(r2)
    add r2, 32
    sd f8, -8(r2)
    bne r1, r3, loop

prolog

iterate

loop:

add r1

bp

4 fadds / 4 cycles = 1

How many FLOPS/cycle?
Software Pipelining vs. Unrolling

Loop Unrolling

Software Pipelining

Software pipelining pays startup/wind-down costs only once per loop, not once per iteration
What if there are no loops?

- Branches limit basic block size in control-flow intensive irregular code
- Difficult to find ILP in individual basic blocks
Trace Scheduling
[Fisher, Ellis]

- Pick string of basic blocks, a trace, that represents most frequent branch path
- Schedule whole “trace” at once
- Add fixup code to cope with branches jumping out of trace

How do we know which trace to pick?
Use profiling feedback or compiler heuristics to find common branch paths
Problems with “Classic” VLIW

- Knowing branch probabilities
  - Profiling requires an significant extra step in build process

- Scheduling for statically unpredictable branches
  - Optimal schedule varies with branch path

- Object code size
  - Instruction padding wastes instruction memory/cache
  - Loop unrolling/software pipelining replicates code

- Scheduling memory operations
  - Caches and/or memory bank conflicts impose statically unpredictable variability
  - Uncertainty about addresses limit code reordering

- Object-code compatibility
  - Have to recompile all code for every machine, even for two machines in same generation
VLIW Instruction Encoding

- Schemes to reduce effect of unused fields
  - Compressed format in memory, expand on I-cache refill
    - used in Multiflow Trace
    - introduces instruction addressing challenge
  - Provide a single-op VLIW instruction
    - Cydra-5 UniOp instructions
  - Mark parallel groups
    - used in TMS320C6x DSPs, Intel IA-64
Cydra-5: Memory Latency Register (MLR)

- Problem: Loads have variable latency
- Solution: Let software choose desired memory latency

- Compiler schedules code for maximum load-use distance

- Software sets MLR to latency that matches code schedule

- Hardware ensures that loads take exactly MLR cycles to return values into processor pipeline
  - Hardware buffers loads that return early
  - Hardware stalls processor if loads return late
**IA-64 Predicated Execution**

**Problem:** Mispredicted branches limit ILP

**Solution:** Eliminate hard-to-predict branches with predicated execution
- Almost all IA-64 instructions can be executed conditionally under predicate
- Instruction becomes NOP if predicate register false

```plaintext
b0:  Inst 1  if
     Inst 2
     br a==b, b2

b1:  Inst 3  else
     Inst 4
     br b3

b2:  Inst 5  then
     Inst 6

b3:  Inst 7
     Inst 8
```

**Predication**

```plaintext
Inst 1
Inst 2
p1,p2 ← cmp(a==b)
(p1) Inst 3  ||  (p2) Inst 5
(p1) Inst 4  ||  (p2) Inst 6
Inst 7
Inst 8
```

**One basic block**

- Mahlke et al, ISCA95: On average >50% branches removed
Where does predication fit in?
IA-64 Speculative Execution

Problem: Branches restrict compiler code motion
Solution: Speculative operations that don’t cause exceptions

Inst 1
Inst 2
br a==b, b2

Load r1
Use r1
Inst 3

Load.s r1
Inst 1
Inst 2
br a==b, b2

Chk.s r1
Use r1
Inst 3

Speculative load never causes exception, but sets “poison” bit on destination register
Check for exception in original home block jumps to fixup code if exception detected

Can’t move load above branch because might cause spurious exception

Particularly useful for scheduling long latency loads early
IA-64 Data Speculation

Problem: Possible memory hazards limit code scheduling
Solution: Instruction-based speculation with hardware monitor to check for pointer hazards

Can’t move load above store because store might be to same address

Requires associative hardware in address check table
Clustered VLIW

- Divide machine into clusters of local register files and local functional units
- Lower bandwidth/higher latency interconnect between clusters
- Software responsible for mapping computations to minimize communication overhead
- Common in commercial embedded processors, examples include TI C6x series DSPs, and HP Lx processor
- Exists in some superscalar processors, e.g., Alpha 21264
Limits of Static Scheduling

- Unpredictable branches
- Unpredictable memory behavior (cache misses and dependencies)
- Code size explosion
- Compiler complexity

Question:

How applicable are the VLIW-inspired techniques to traditional RISC/CISC processor architectures?
Thank you!

Next Lecture: Vector Processors