Virtualization

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M.I.T.
Abstractions

Devices
Materials
Atoms
Abstractions

Digital design
Combinational and sequential circuits

Devices
Materials
Atoms
Abstractions

Computer architecture
Processors, caches, pipelining

Digital design
Combinational and sequential circuits

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Software

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Devices
Materials
Atoms

Instruction set + memory

Digital circuits

Bits, Logic gates
Abstractions

Computer programs
Virtual machines

Computer systems
Instruction set + memory
Operating systems, virtual memory, I/O

Computer architecture
Digital circuits
Processors, caches, pipelining

Digital design
Bits, Logic gates
Combinational and sequential circuits

Devices
Materials
Atoms
Evolution in Number of Users

IBM 1620
1959

Single User

Runtime
loaded with
program
Evolution in Number of Users

IBM 1620
1959

IBM 360
1960s

Single User  Multiple Users

Runtime loaded with program  OS for sharing resources
Evolution in Number of Users

<table>
<thead>
<tr>
<th>Year</th>
<th>System</th>
<th>Users</th>
<th>OS for Sharing Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>1959</td>
<td>IBM 1620</td>
<td>Single</td>
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</tr>
<tr>
<td>1960s</td>
<td>IBM 360</td>
<td>Multiple</td>
<td>OS for sharing resources</td>
</tr>
<tr>
<td>1980s</td>
<td>IBM PC</td>
<td>Single</td>
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</tbody>
</table>
Evolution in Number of Users

IBM 1620 1959
Single User
Runtime loaded with program

IBM 360 1960s
Multiple Users
OS for sharing resources

IBM PC 1980s
Single User
OS for sharing resources

Cloud Servers 1990s
Multiple Users
Multiple OSs
Single-Program Machine

- Hardware executes a single program and has direct and complete access to all hardware resources.
Single-Program Machine

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- The ISA is the interface between software and hardware:
Single-Program Machine

- Hardware executes a single program and has direct and complete access to all hardware resources
- The ISA is the interface between software and hardware:
  - Program counter
  - General purpose registers
  - Memory
• Runtime library added to save programming effort and provided *an abstraction to create uniform interface to devices.*
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Multi-Program Machine (1st attempt)

- Program
- Program
- Runtime Library
- Hardware

ISA
RTL
API
Multi-Program Machine (1st attempt)

Program  Program

Runtime Library

Hardware

Any problems?
Multi-Program Machine (1st attempt)

Any problems? security
Operating Systems

- Operating System (OS) goals:
Operating Systems

• Operating System (OS) goals:
  – Abstraction: OS hides details of underlying hardware
    • e.g., a process can open and access files instead of issuing raw commands to the disk
Operating Systems

- **Operating System (OS) goals:**
  - **Abstraction:** OS hides details of underlying hardware
    - e.g., a process can open and access files instead of issuing raw commands to the disk
  - **Resource management:** OS controls how processes share hardware (CPU, memory, disk, etc.)
### Operating Systems

#### Operating System (OS) goals:
- **Abstraction**: OS hides details of underlying hardware
  - e.g., a process can open and access files instead of issuing raw commands to the disk
- **Resource management**: OS controls how processes share hardware (CPU, memory, disk, etc.)
- **Protection and privacy**: Processes cannot access each other’s data

<table>
<thead>
<tr>
<th>process$_1$</th>
<th>process$_2$</th>
<th>...</th>
<th>process$_N$</th>
</tr>
</thead>
</table>

Application Binary Interface (ABI)

ISA

Hardware
Operating System Mechanisms

- The OS kernel provides a **private address space** to each process
  - Each process is allocated space in physical memory by the OS
  - A process is not allowed to access the memory of other processes
Operating System Mechanisms

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  - Each process is given a fraction of CPU time
  - A process cannot use more CPU time than allowed
Operating System Mechanisms

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- The OS kernel lets processes invoke system services (e.g., access files or network sockets) via **system calls**
Simple Base and Bound Translation

Load X

Program Address Space

Base Physical Address

Effective Address

Bound Register

Base Register

Segment Length

Bounds Violation?

Physical Address

current segment

Main Memory

Base Physical Address
Simple Base and Bound Translation

Load X

Program Address Space

Bound Register

Effective Address

Base Register

Segment Length

≤

Bounds Violation?

Physical Address

Main Memory

current segment

Base Physical Address

Base Physical Address
Introduce a new privileged mode in which the base and bounds registers are visible/accessible.
Protecting Memory

Page Table Entry

<table>
<thead>
<tr>
<th>Valid&lt;31&gt;</th>
<th>Prot&lt;30:27&gt;</th>
<th>Modified&lt;26&gt;</th>
<th>OS&lt;25:21&gt;</th>
<th>PFN&lt;20:0&gt;</th>
</tr>
</thead>
</table>

L23-11
Protecting Memory

Page Table Entry

| Valid<31> | Prot<30:27> | Modified<26> | OS<25:21> | PFN<20:0> |
Protecting Memory

Page Table Entry

Valid<31>  Prot<30:27>  Modified<26>  OS<25:21>  PFN<20:0>

TLB Entry

Tag  Valid  Prot  PFN
Protecting Memory

Page Table Entry

Valid<31>  Prot<30:27>  Modified<26>  OS<25:21>  PFN<20:0>

TLB Entry

Tag  Valid  Prot  PFN

TLB Fill
Protecting Memory

Page Table Entry

- Valid<31>
- Prot<30:27>
- Modified<26>
- OS<25:21>
- PFN<20:0>

TLB Entry

- Tag
- Valid
- Prot
- PFN

- TLB access checks if protection allows access for current mode
- TLB fills require read/copy page table data -> security sensitive
ISA Extensions to Support OS

- Two modes of execution: user and supervisor
  - OS kernel runs in supervisor mode
  - All other processes run in user mode
ISA Extensions to Support OS

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• Privileged instructions and registers that are only available in supervisor mode
ISA Extensions to Support OS

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- How to transition from user mode to supervisor mode?
ISA Extensions to Support OS

• Two modes of execution: user and supervisor
  – OS kernel runs in supervisor mode
  – All other processes run in user mode
• Privileged instructions and registers that are only available in supervisor mode
• How to transition from user mode to supervisor mode?
  – Traps (exceptions) to safely transition from user to supervisor mode
Process Mode Switching

Trap, e.g., i/o read() or exception

user mode

kernel mode
Process Mode Switching

Trap, e.g., i/o read() or exception

user mode

Switch to kernel mode;
Pass arguments;
Save app state;
Transfer to trap handler

kernel mode
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Trap handler

Must be at fixed addresses
Process Mode Switching

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user mode

Switch to kernel mode;
Pass arguments;
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kernel mode

Trap handler

Must be at fixed addresses

Check arguments;
Find kernel routine addr
Process Mode Switching

- **Trap, e.g., i/o read() or exception**
  - Switch to kernel mode;
  - Pass arguments;
  - Save app state;
  - Transfer to trap handler

- **user mode**
- **kernel mode**

**Trap handler**
- Must be at fixed addresses
- Check arguments;
  - Find kernel routine addr

**Why?**
Process Mode Switching

Trap, e.g., i/o read() or exception

user mode

Switch to kernel mode;
Pass arguments;
Save app state;
Transfer to trap handler

kernel mode

Trap handler

Must be at fixed addresses

Kernel routine

Check arguments;
Find kernel routine addr

Why?
Process Mode Switching

Trap, e.g., i/o read() or exception

Switch to kernel mode; Pass arguments; Save app state; Transfer to trap handler

user mode

kernel mode

Must be at fixed addresses

Kernel routine

Trap handler

Check arguments; Find kernel routine addr

Why?

Restore app state; Return to user
Protection – Single OS

Diagram showing the interaction between OS Kernel, User Process, Trap, and User Process.
Protection – Single OS

Key idea: Provides a strong abstraction that cannot be escaped
Virtual Machines

• The OS gives a Virtual Machine (VM) to each process
  – Each process believes it runs on its own machine...
  – ...but this machine does not exist in physical hardware
Virtual Machines

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**Process1**

- Virtual CPUs
- Virtual Memory
- Events
- Files
- Sockets
- Syscalls

**VM1**

**OS Kernel (specially privileged process)**

**Physical Hardware**

- Processor
- Memory
- Disk
- Network card
- Display
- Keyboard

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December 5, 2022
Virtual Machines

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Virtual Machines

- A Virtual Machine (VM) is an *emulation* of a computer system
  - Very general concept, used beyond operating systems

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**Physical Hardware**

- Processor
- Memory
- Disk
- Network card
- Display
- Keyboard

**Virtual Machines**

- VM1
- OS Kernel (specially privileged process)
- Process1
- ABI
  - Virtual CPUs
  - Virtual Memory
  - Events
  - Files
  - Sockets
  - Syscalls

- Process2
- Process3
- Process4
Virtual Machines Are Everywhere

- Example: Consider a Python program running on a Linux Virtual Machine
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  Python program
  Python interpreter (CPython)
  Python Language
  Implements a Python VM
Virtual Machines Are Everywhere

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- Example: Consider a Python program running on a Linux Virtual Machine

- Python program
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- Linux OS kernel
- VirtualBox

  - Python Language
  - Implements a Python VM
  - Linux ABI
  - Implements a Linux-x86 VM
  - x86 ISA
  - Implements an x86 system VM
Virtual Machines Are Everywhere

Example: Consider a Python program running on a Linux Virtual Machine

Python program
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Linux OS kernel
VirtualBox
OS kernel (Win/Linux/MacOS/...)

Python Language
Implements a Python VM
Linux ABI
Implements a Linux-x86 VM
x86 ISA
Implements an x86 system VM
Win/Linux/MacOS/... ABI
Implements an OS-x86 VM
Virtual Machines Are Everywhere

• Example: Consider a Python program running on a Linux Virtual Machine

  - Python program
  - Python interpreter (CPython)
  - Linux OS kernel
  - VirtualBox
  - OS kernel (Win/Linux/MacOS/…)
  - Hardware (e.g., your laptop)
  - Python Language
  - Implements a Python VM
  - Linux ABI
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  - Implements an x86 system VM
  - Win/Linux/MacOS/… ABI
  - Implements an OS-x86 VM
  - x86 ISA
  - Implements an x86 physical machine
Implementing Virtual Machines

• Virtual machines can be implemented entirely in software, but at a performance cost
  – e.g., Python programs are 10-100x slower than native Linux programs due to Python interpreter overheads
Implementing Virtual Machines

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• We want to support virtual machines with minimal overheads → often need hardware support!
Application-level virtualization

• Programs are usually distributed in a binary format that encodes the program’s instructions and initial values of some data segments. These requirements are called the application binary interface (ABI), which can be virtualized.

• ABI specifications include
  – Which instructions are available (the ISA)
  – What system calls are possible (I/O, or the environment)
  – What state is available at process creation

• Operating system implements the virtual environment
  – At process startup, OS reads the binary program, creates an environment for it, then begins to execute the code, handling traps for I/O calls, emulation, etc.
Full ISA-Level Virtualization
Full ISA-Level Virtualization

Run programs for one ISA on hardware with different ISA
Full ISA-Level Virtualization

Run programs for one ISA on hardware with different ISA

- Run-time Hardware Emulation
  - IBM System 360 had IBM 1401 emulator in microcode
  - Intel Itanium converted x86 to native VLIW (two software-visible ISAs)
  - ARM cores support 64-bit ARM, 32-bit ARM, 16-bit Thumb
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• Emulation (*OS software interprets instructions at run-time*)
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- **Static Binary Translation** *(convert at install time, load time, or offline)*
  - IBM AS/400 to modified PowerPC cores
  - DEC tools for VAX->Alpha and MIPS->Alpha
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- Dynamic Binary Translation (*non-native to native ISA at run time*)
  - Sun’s HotSpot Java JIT (just-in-time) compiler
  - Transmeta Crusoe, x86->VLIW code morphing
Partial ISA-level virtualization

Often good idea to implement part of ISA in software:
Partial ISA-level virtualization

Often good idea to implement part of ISA in software:

- Expensive but rarely used instructions can cause trap to OS emulation routine:
  - e.g., decimal arithmetic in µVax implementation of VAX ISA
Partial ISA-level virtualization

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  - e.g., IEEE floating-point denormals cause traps in almost all floating-point unit implementations
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- Old machine can trap unused opcodes, allows binaries for new ISA to run on old hardware
  - e.g., Sun SPARC v8 added integer multiply instructions, older v7 CPUs trap and emulate
Motivation for Multiple OSs

Some motivations for using multiple operating systems on a single computer:

- Allows use of capabilities of multiple distinct operating systems
Motivation for Multiple OSs

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- Allows different users to share a system while using completely independent software stacks
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• Allows different users to share a system while using completely independent software stacks

• Allows for load balancing and migration across multiple machines

• Allows operating system development without making entire machine unstable or unusable
Supporting Multiple OSs

- process₁ \ldots processₙ
- process₁ \ldots processₘ
- OS Kernel₁ \ldots OS Kernelₖ
- Virtual Machine Monitor (VMM/Hypervisor)
- Hardware
A VMM (aka Hypervisor) provides a system virtual machine to each OS.
Supporting Multiple OSs

- A VMM (aka Hypervisor) provides a system virtual machine to each OS
- VMM can run directly on hardware (as above) or on another OS
  - Precisely, VMM can be implemented against an ISA (as above) or a process-level ABI. Who knows what lays below the interface...
Virtualization Nomenclature

From (Machine we are attempting to execute)
- Guest
- Client
- Foreign ISA

To (Machine that is doing the real execution)
- Host
- Target
- Native ISA
Virtual Machine Requirements
[Popek and Goldberg, 1974]

• Equivalence/Fidelity: A program running on the VMM should exhibit a behavior essentially identical to that demonstrated when running on an equivalent machine directly.

• Resource control/Safety: The VMM must be in complete control of the virtualized resources.

• Efficiency/Performance: A statistically dominant fraction of machine instructions must be executed without VMM intervention.
Classification of instructions into 3 groups:

- Privileged instructions: Instructions that trap if the processor is in user mode and do not trap if it is in a more privileged mode.

- Control-sensitive instructions: Instructions that attempt to change the configuration of resources in the system.

- Behavior-sensitive instructions: Those whose behavior depends on the configuration of resources, e.g., mode

Building an effective VMM for an architecture is possible if the set of sensitive instructions is a subset of the set of privileged instructions.

Run OS code using the trap-and-emulate strategy.
Sensitive instruction handling

Sensitive instruction

Non-VMM mode

Switch to VMM mode; Pass arguments; Save app state

VMM mode

VMM handler

Find handler addr

VMM routine

Restore app state, Return to guest
Protection – Multiple OS
Virtual Memory in VMs

Virtual Address Space of Process-1

Physical Address Space
Virtual Memory in VMs

- App-a
- App-b

Guest OS

Virtual Address Space

Physical Address Space

Virtual Address Space of Process-1

0 1 2 3

1 0 3 2
Virtual Memory in VMs

Virtual Address Space of Process-1

Virtual Address Space of App-a inside VM

Virtual Address Space of App-b inside VM

Physical Address Space
Virtual Memory in VMs

Guest Virtual Address (gVA)

Virtual Address Space of App-a inside VM

Virtual Address Space of App-b inside VM

Virtual Address Space of Process-1

Physical Address Space
Virtual Memory in VMs

Guest Virtual Address (gVA)

Host Virtual Address (hVA) = Guest Physical Address (gPA)

Virtual Address Space of App-a inside VM

Virtual Address Space of App-b inside VM

Virtual Address Space of Process-1

Physical Address Space
Virtual Memory in VMs

Guest Virtual Address (gVA)

Host Virtual Address (hVA)
= Guest Physical Address (gPA)

Host Physical Address (hPA)

Virtual Address Space of App-a inside VM

Virtual Address Space of App-b inside VM

Virtual Address Space of Process-1

Physical Address Space
Nested Page Tables

Guest VA

Guest Page Table Base

Guest Page Table

Guest PA == Host VA

Host Page Table Base

Guest PA

How many accesses do we need?

Host PA

Host PA == Host VA
Nested Page Tables

Guest VA

Index Offset

Guest Page Table Base

Guest PA => hPA

Page Table

PPN Offset

Host Page Table Base

Host PA

Index Offset

gPA => hPA

How many accesses do we need?

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Guest PA => hPA

Page Table

PPN Offset

Host PA

gPA => hPA

Host Page Table Base

Page Table

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gPA => hPA

How many accesses do we need?
Nested Page Tables

Guest VA

Guest Page Table Base

Guest PA == Host VA

How many accesses do we need? \(1 \Rightarrow 3\)
Nested Page Tables (Hierarchical)

Guest VA

Guest Page Table Base

L1 Table

PTP

PTE

L2 Table

PPN

Offset

Index 1

Index 2

Offset

Guest PA == Host VA

Host Page Table Base

L1 Table

PTP

PTE

L2 Table

PPN

Offset

Index 1

Index 2

Offset

How many accesses do we need?
Nested Page Tables (Hierarchical)

Guest VA

- Guest Page Table Base
- Index 1
- Index 2
- Offset
- gPA→hPA
- L1 Table
- PTP
- PTE
- gPA→hPA
- L2 Table
- PPN
- Offset

Host Page Table Base

- L1 Table
- PTP
- PTE

How many accesses do we need?

Guest PA == Host VA

- Index 1
- Index 2
- Offset
- gPA→hPA
- L1 Table
- PTP
- PTE
- L2 Table
- PPN
- Offset

Guest PA

Host PA
Nested Page Tables (Hierarchical)

Guest VA

- Guest Page Table Base
- Index 1
- Index 2
- Offset
- gPA -> hPA
- PTP
- PTE
- L1 Table
- L2 Table
- PPN
- Offset

How many accesses do we need? 2 => 8

Guest PA == Host VA

- Host Page Table Base
- Index 1
- Index 2
- Offset
- gPA -> hPA
- PTP
- PTE
- L1 Table
- L2 Table
- PPN
- Offset

Guest PA

- gPA -> hPA
- L2 Table
- Host PA
Shadow Page Tables

How many accesses do we need?
How many accesses do we need?
How many accesses do we need? \(2 \Rightarrow 2\)
What if guest OS changes the guest page table?
# Nested vs Shadow Paging

<table>
<thead>
<tr>
<th></th>
<th>Native</th>
<th>Nested Paging</th>
<th>Shadow Paging</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TLB Hit</strong></td>
<td>VA-&gt;PA</td>
<td>gVA-&gt;hPA</td>
<td>gVA-&gt;hPA</td>
</tr>
<tr>
<td><strong>TLB Miss (max)</strong></td>
<td>4</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td><strong>PTE Updates</strong></td>
<td>Fast</td>
<td>Fast</td>
<td>Uses VMM</td>
</tr>
</tbody>
</table>

On x86-64
Supporting Multiple Process Groups

- ABI
  - process\(_1\) ... process\(_N\)
  - Container
- ISA
  - OS Kernel
- Hardware

- ABI
  - process\(_1\) ... process\(_M\)
  - Container
Supporting Multiple Process Groups

- A “container” provides a **process group virtual machine** to each set of processes
Supporting Multiple Process Groups

- A “container” provides a process group virtual machine to each set of processes

- Container can run directly on OS, which provides a specific OS ABI to the processes in container
Container Semantics

• Isolation between containers is maintained by the OS, which supports a virtualized set of kernel calls.
  – Therefore, processes in all containers must target the same OS*

• Per Container Resources
  – Set of processes (each with a virtual memory space)
  – Set of filesystems
  – Set of network interfaces and ports
  – Selected devices

*Or closely related variants
Coming Spring 2023 ...

- 6.S984: Datacenter Computing
- Instructor: Christina Delimitrou
- Short description:
  - Datacenter Computing explores the end-to-end stack of modern datacenters, from hardware and OS all the way to resource managers and programming frameworks.
  - The class will also explore cross-cutting issues, such as ML for systems, energy efficiency, availability, security, and reliability.
  - The main deliverable for the course is a semester-long research project on cloud computing, done in groups of 2-3 students. We will provide a list of suggested projects, but students are also encouraged to suggest their own.

- Lecture time: two 1.5-hour meetings per week
Thank you!