Instruction Pipelining and Hazards

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http://www.csg.csail.mit.edu/6.823
Reminder: Harvard-Style Single-Cycle Datapath for MIPS
Princeton challenge

• What problem arises if we use a single memory to hold instructions and data?
Princeton challenge

• What problem arises if we use a single memory to hold instructions and data?

At least the instruction fetch and a Load (or Store) cannot be executed in the same cycle
Princeton challenge

- What problem arises if we use a single memory to hold instructions and data?

At least the instruction fetch and a Load (or Store) cannot be executed in the same cycle

Structural hazard
Princeton Microarchitecture
Datapath & Control

PCen → PCSrc → RegWrite → MemWrite → WBSrc

0x4 → Add → 31

IR → 31 → rs1, rs2, rd1, we, ws, wd, rd2, GPRs

Imm Ext → ALU Control

Add → ALU → ALU Output: wdata, rdata, Data

MemWrite: addr, Data, Memory, wdata

IRen, OpCode, RegDst, ExtSel, OpSel, BSrc, zero?, AddrSrc
Princeton Microarchitecture

Datapath & Control

Fetch phase

PCen → PCSrc → Add (0x4) → IR

clk → IRen → OpCode → RegDst

ExtSel → PCSrc → Add (31) → GPRs

rs1 → rs2 → we → rd1 → ALU

Imm Ext → ALU Control

pled → we → MemWrite

WBSrc → Add → WE (rd2) → wdata

clk → Memory Data wdata
Princeton Microarchitecture
Datapath & Control

Fetch phase

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Datapath & Control

Fetch phase

IRen  OpCode  RegDst  ExtSel  OpSel  BSrc  zero?  AddrSrc  =  PC

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Fetch phase

IRen  OpCode  RegDst  ExtSel  OpSel  BSrc  zero?  AddrSrc = PC

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Datapath & Control

Fetch phase
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Datapath & Control

Fetch phase

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Datapath & Control

Fetch phase

IRen OpCode RegDst
ExtSel OpSel BSrc zero? AddrSrc = PC

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Datapath & Control

Fetch phase

PCen

off

0x4

Add

RegWrite

off

MemWrite

off

WBSrc

IR

clk

RegDst

PCSrc

Add

ExtSel

OpCode

GPRs

rs1

rs2

rd1

ws

wd

rd2

Imm

Ext

ALU

Add

we

clk

MemWrite

Data

addr

rdata

Data Memory

wdata

ALU Control

clk

IR

clk

AddrSrc = PC

Windows

Fetch phase

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Two-State Controller: 
Princeton Architecture

fetch phase

execute phase

A flipflop can be used to remember the phase
Hardwired Controller:
Princeton Architecture

IR → old combinational logic (Harvard) → ExtSel, BSrc, OpSel, WBSrc, RegDest, PCsrc1, PCsrc2

zero? → new combinational logic

1-bit Toggle FF

Fetch / Execute

S → IRen, PCen, AddrSrc
Princeton Microarchitecture
Datapath & Control for 2-cycles-per-instruction
Princeton Microarchitecture (redrawn)

The same (mux not shown)

Only one of the phases is active in any cycle ⇒ a lot of datapath is not in use at any given time
Princeton Microarchitecture
Overlapped execution

fetch phase

execute phase
Princeton Microarchitecture
Overlapped execution

Can we overlap instruction fetch and execute?
Princeton Microarchitecture
Overlapped execution

Can we overlap instruction fetch and execute?

Yes, unless IR contains a Load or Store
Can we overlap instruction fetch and execute?

*Yes, unless IR contains a Load or Store*

Which action should be prioritized?
Princeton Microarchitecture
Overlapped execution

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Which action should be prioritized?  Execute
Princeton Microarchitecture
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What do we do with Fetch?
Princeton Microarchitecture
Overlapped execution

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What do we do with Fetch? Stall it
Princeton Microarchitecture

Overlapped execution

Can we overlap instruction fetch and execute?

Yes, unless IR contains a Load or Store

Which action should be prioritized? Execute

What do we do with Fetch? Stall it

How?
Stalling the instruction fetch

Princeton Microarchitecture

fetch phase

execute phase
Stalling the instruction fetch

Princeton Microarchitecture

When stall condition is indicated

fetch phase

eexecute phase

0x4 Add

V waddr

Memory wdata

IR

V we

rs1

rs2

rd1

ws

wdrd2

GPRs

Imm Ext

ALU

we

addr

we

rdata

Memory wdata
Stalling the instruction fetch
Princeton Microarchitecture

When stall condition is indicated
  • *don’t fetch a new instruction and don’t change the PC*
Stalling the instruction fetch

Princeton Microarchitecture

When stall condition is indicated
- don’t fetch a new instruction and don’t change the PC
Stalling the instruction fetch
Princeton Microarchitecture

When stall condition is indicated
- don’t fetch a new instruction and don’t change the PC
- insert a nop in the IR
Stalling the instruction fetch
Princeton Microarchitecture

When stall condition is indicated
- don’t fetch a new instruction and don’t change the PC
- insert a nop in the IR
- set the Memory Address mux to ALU (not shown)
Stalling the instruction fetch

Princeton Microarchitecture

When stall condition is indicated

- don’t fetch a new instruction and don’t change the PC
- insert a nop in the IR
- set the Memory Address mux to ALU (not shown)

What if IR contains a jump or branch instruction?
Need to stall on branches

Princeton Microarchitecture

fetch phase

execute phase
Need to stall on branches
Princeton Microarchitecture

When IR contains a jump or branch-taken

- no “structural conflict” for the memory
Need to stall on branches

Princeton Microarchitecture

When IR contains a jump or branch-taken

- no “structural conflict” for the memory
- but we do not have the correct PC value in the PC
Need to stall on branches

Princeton Microarchitecture

When IR contains a jump or branch-taken

- no "structural conflict" for the memory
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- memory cannot be used – Address Mux setting is irrelevant
Need to stall on branches

Princeton Microarchitecture

When IR contains a jump or branch-taken:

- No "structural conflict" for the memory
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- insert the nextPC (branch-target) address in the PC
Need to stall on branches
Princeton Microarchitecture

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Pipelined Princeton Microarchitecture

- PCSrc2
- PCSrc
- RegWrite
- MemWrite
- WBSrc
- n0p
- clk
- IR
- IRSrc
- Add
- 0x4
- ExtSel
- OpCode
- Add
- ALU
- ALUControl
- PC
- MAddrSrc
- nop
- stall
- stall
- rdata
- Data
- Memory
- wdata
- Imm
- Ext
- Addr
- we
- rs1
- rs2
- rd1
- ws
- wd
- rd2
- GPRs
- zero?
- MAddrSrc
- OpCode
- RegDst
- ExtSel
- OpSel
- BSrc
- zero?
- MAddrSrc
# Pipelined Princeton: Control Table

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BSrc = Reg / Imm ; WBSrc = ALU / Mem / PC; IRSrc = nop/mem; MAddSrc = pc/ALU
RegDst = rt / rd / R31; PCSrc1 = pc+4 / br / rind / jabs; PCSrc2 = pc/nPC
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<td>no</td>
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<td>*</td>
<td>pc+4</td>
<td>npc</td>
<td>mem</td>
<td>pc</td>
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</table>

BSrc = Reg / Imm  ;  WBSrc = ALU / Mem / PC;  IRSrc = nop/mem;  MAaddr Src = pc/ALU
RegDst = rt / rd / R31;  PCSrc1 = pc+4 / br / rind / jabs;  PCSrc2 = pc/nPC

February 27, 2017  Sanchez & Emer
# Pipelined Princeton: Control Table

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Stall</th>
<th>Ext Sel</th>
<th>B Src</th>
<th>Op Sel</th>
<th>Mem W</th>
<th>Reg W</th>
<th>WB Src</th>
<th>Reg Dst</th>
<th>PC Src1</th>
<th>PC Src2</th>
<th>IR Src</th>
<th>MAaddr Src</th>
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RegDst = rt / rd / R31;  PCSrc1 = pc+4 / br / rind / jabs;  PCSrc2 = pc/nPC

stall & IRSrc columns are identical
Pipelined Princeton Architecture

Clock: \[ t_{C-Princeton} > t_{RF} + t_{ALU} + t_{M} + t_{WB} \]

CPI: \((1 - f) + 2f\) cycles per instruction where \(f\) is the fraction of instructions that cause a stall
Pipelined Princeton Architecture

**Clock:** \( t_{C\text{-Princeton}} > t_{RF} + t_{ALU} + t_M + t_{WB} \)

**CPI:** \((1 - f) + 2f \) cycles per instruction
where \( f \) is the fraction of instructions that cause a stall

What is a likely value of \( f \)?
An Ideal Pipeline

- All objects go through the same stages
- No sharing of resources between any two stages
- Propagation delay through all pipeline stages is equal
- The scheduling of an object entering the pipeline is not affected by the objects in other stages

*These conditions generally hold for industrial assembly lines.*

*But what about an instruction pipeline?*
Pipelined Datapath
Pipelined Datapath

\[ \text{addr} \rightarrow \text{wdata} \rightarrow \text{rdata} \]

\[ \text{ALU} \]

\[ \text{Imm Ext} \]

\[ \text{Memory} \rightarrow \text{GPRs} \]

\[ \text{rs1, rs2, rd1, ws, wd, rd2} \]

\[ \text{we} \]

\[ \text{L06-16} \]
Pipelined Datapath

fetch phase

decode & Reg-fetch phase

execute phase

memory phase

write-back phase
Pipelined Datapath

Clock period can be reduced by dividing the execution of an instruction into multiple cycles

\[ t_C > \max \{ t_{IM}, t_{RF}, t_{ALU}, t_{DM}, t_{RW} \} \ ( = t_{DM} \text{ probably}) \]

However, CPI will increase unless instructions are pipelined
How to divide the datapath into stages

Suppose memory is significantly slower than other stages. In particular, suppose

\[
\begin{align*}
    t_{IM} &= 10 \text{ units} \\
    t_{DM} &= 10 \text{ units} \\
    t_{ALU} &= 5 \text{ units} \\
    t_{RF} &= 1 \text{ unit} \\
    t_{RW} &= 1 \text{ unit}
\end{align*}
\]

Since the slowest stage determines the clock, it may be possible to combine some stages without any loss of performance.
Alternative Pipelining

\[ t_C > \max \{ t_{IM}, t_{RF}, t_{ALU}, t_{DM}, t_{RW} \} = t_{DM} \]
Alternative Pipelining

\[ t_C > \max \{ t_{IM}, t_{RF}, t_{ALU}, t_{DM}, t_{RW} \} = t_{DM} \]
Alternative Pipelining

$$t_C > \max \{t_{IM}, t_{RF} + t_{ALU}, t_{DM}, t_{RW}\} = t_{DM}$$
Alternative Pipelining

Write-back stage takes much less time than other stages. Suppose we combined it with the memory phase.
Alternative Pipelining

$t_C > \max \{t_{IM}, t_{RF} + t_{ALU}, t_{DM}, t_{RW}\} = t_{DM}$

Write-back stage takes much less time than other stages. Suppose we combined it with the memory phase
Alternative Pipelining

\[ t_C > \text{max} \{ t_{IM}, t_{RF}+t_{ALU}, t_{DM}+t_{RW} \} = t_{DM} + t_{RW} \]

Write-back stage takes much less time than other stages. Suppose we combined it with the memory phase.
Write-back stage takes much less time than other stages. Suppose we combined it with the memory phase.

\[ t_C > \max \{ t_{IM}, t_{RF} + t_{ALU}, t_{DM} + t_{RW} \} = t_{DM} + t_{RW} \]

\( \Rightarrow \text{increase the critical path by 10\%} \)
# Maximum Speedup by Pipelining

<table>
<thead>
<tr>
<th>Assumptions</th>
<th>Unpipelined $t_C$</th>
<th>Pipelined $t_C$</th>
<th>Speedup</th>
</tr>
</thead>
</table>

Sanchez & Emer February 27, 2017
Maximum Speedup by Pipelining

Assumptions

1. $t_{IM} = t_{DM} = 10,$
   $t_{ALU} = 5,$
   $t_{RF} = t_{RW} = 1$
   4-stage pipeline

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<tbody>
<tr>
<td>1.</td>
<td></td>
<td></td>
<td></td>
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</table>
# Maximum Speedup by Pipelining

## Assumptions

1. $t_{IM} = t_{DM} = 10,$
   $t_{ALU} = 5,$
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4-stage pipeline

## Table

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<tbody>
<tr>
<td>4-stage</td>
<td></td>
<td></td>
<td>27</td>
</tr>
<tr>
<td>pipeline</td>
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## Maximum Speedup by Pipelining

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<td>27</td>
<td>10</td>
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</table>
# Maximum Speedup by Pipelining

## Assumptions

1. $t_{IM} = t_{DM} = 10,$
   
   $t_{ALU} = 5,$
   
   $t_{RF} = t_{RW} = 1$

## 4-stage pipeline

<table>
<thead>
<tr>
<th></th>
<th>Unpipelined $t_C$</th>
<th>Pipelined $t_C$</th>
<th>Speedup</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>27</td>
<td>10</td>
<td>2.7</td>
</tr>
</tbody>
</table>
Maximum Speedup by Pipelining

Assumptions

1. $t_{IM} = t_{DM} = 10,$
   $t_{ALU} = 5,$
   $t_{RF} = t_{RW} = 1$
   4-stage pipeline

2. $t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5$
   4-stage pipeline

<table>
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<tr>
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<td>10</td>
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</tbody>
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Maximum Speedup by Pipelining

Assumptions

1. $t_{IM} = t_{DM} = 10,$
   $t_{ALU} = 5,$
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   4-stage pipeline

2. $t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5$
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<tr>
<td>2.</td>
<td>25</td>
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<td>10</td>
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<tr>
<td>2. $t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5$ 4-stage pipeline</td>
<td>25</td>
<td>10</td>
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Maximum Speedup by Pipelining

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<tr>
<td>2. $t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5$</td>
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4-stage pipeline

5-stage pipeline
# Maximum Speedup by Pipelining

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4-stage pipeline

5-stage pipeline
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What seems to be the message here?
## Maximum Speedup by Pipelining

### Assumptions

1. \( t_{IM} = t_{DM} = 10, \)
   \( t_{ALU} = 5, \)
   \( t_{RF} = t_{RW} = 1 \)
   
   4-stage pipeline

2. \( t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5 \)
   
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3. \( t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5 \)
   
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What seems to be the message here?

*One can achieve higher speedup with more pipeline stages.*
5-Stage Pipelined Execution

*Instruction Flow Diagram*

- **I-Fetch (IF):**
  - PC
  - Addr
  - Inst. Memory
  - IR

- **Decode, Reg. Fetch (ID):**
  - Imm Ext

- **Execute (EX):**
  - ALU

- **Memory (MA):**
  - Addr
  - Data Memory
  - Wdata

- **Write Back (WB):**
  - We

Symbols:
- Rdata, Rd
- Rs1, Rs2
- Ws, Wd, Rd2
- PC
- IR
- ALU
- Memory

Example:
- 0x4
- Add
- Addr
- Inst. Memory
5-Stage Pipelined Execution

Instruction Flow Diagram

- **I-Fetch (IF)**
- **Decode, Reg. Fetch (ID)**
- **Execute (EX)**
- **Memory (MA)**
- **Write-Back (WB)**

- **time**
- **t0** t1 t2 t3 t4 t5 t6 t7 . . . .

- **PC**
- **Addr**
- **Inst. Memory**
- **IR**
- **Imm Ext**
- **Addr**
- **rdata**
- **we**
- **rs1**
- **rs2**
- **rd1**
- **ws**
- **wd**
- **rd2**
- **GPRs**
- **ALU**
- **Addr**
- **rdata**
- **Memory**
- **wdata**
- **Write-Back**
- **0x4**

Add
5-Stage Pipelined Execution

Instruction Flow Diagram

- I-Fetch (IF)
  - time
  - instruction1

- Decode, Reg. Fetch (ID)
  - t0
  - IF1
  - t1
  - ID1

- Execute (EX)
  - t2
  - EX1
  - t3
  - MA1
  - t4
  - WB1

- Memory (MA)
  - t5

- Write-Back (WB)
  - t6
  - t7
  - ...

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5-Stage Pipelined Execution

Instruction Flow Diagram

**I-Fetch (IF)**
- Time: $t_0$, $t_1$, $t_2$, $t_3$, $t_4$, $t_5$, $t_6$, $t_7$, ...
- Instruction: $I_F_1$, $I_F_2$

**Decode, Reg. Fetch (ID)**
- Time: $t_0$, $t_1$, $t_2$, $t_3$, $t_4$, $t_5$
- Registers: $r1$, $r2$, $rd_1$, $ws$, $wd$, $rd_2$

**Execute (EX)**
- ALU
- IMM
- Ext
- $addr$, $wdata$, $rdata$
- $Inst.$

**Memory (MA)**
- Memory
- $addr$, $rdata$
- $Data$, $Memory$, $wdata$

**Write-Back (WB)**
- Write-Back
- $we$, $rs_1$, $rs_2$, $rd_1$, $ws$, $wd$, $rd_2$
- GPRs

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5-Stage Pipelined Execution

Instruction Flow Diagram

$I$-Fetch (IF)

Decom, Reg. Fetch (ID)

Execute (EX)

Memory (MA)

Write-Back (WB)

<table>
<thead>
<tr>
<th>time</th>
<th>instruction1</th>
<th>instruction2</th>
<th>instruction3</th>
</tr>
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<tbody>
<tr>
<td>t0</td>
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<td>$ID_1$</td>
<td>$EX_1$</td>
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<td>$MA_1$</td>
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<td>$EX_2$</td>
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<td>. . .</td>
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<td>$EX_3$</td>
<td>$MA_3$</td>
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<tr>
<td></td>
<td>$EX_3$</td>
<td>$MA_3$</td>
<td>$WB_3$</td>
</tr>
</tbody>
</table>
5-Stage Pipelined Execution

Instruction Flow Diagram

- **I-Fetch (IF)**: PC → addr, rdata → Inst. Memory
- **Decode, Reg. Fetch (ID)**: IF → ID, EX, MA, WB
- **Execute (EX)**: ALU
- **Memory (MA)**: ALU → Memory
- **Write-Back (WB)**: Memory → ALU

Time:
- **t0**: IF1
- **t1**: ID1, EX1
- **t2**: MA1, WB1
- **t3**: IF2, ID2, EX2
- **t4**: MA2, WB2
- **t5**: IF3, ID3, EX3
- **t6**: MA3, WB3
- **t7**: IF4, ID4, EX4
- **WB4**
5-Stage Pipelined Execution

**Instruction Flow Diagram**

- **I-Fetch (IF)**
  - PC
  - Addr
  - Inst. Memory

- **Decode, Reg. Fetch (ID)**
  - IR
  - Imm
  - Ext

- **Execute (EX)**
  - ALU

- **Memory (MA)**
  - Data Memory

- **Write-Back (WB)**
  - Write-Back (WB)

**Table**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Time</th>
<th>IF</th>
<th>ID</th>
<th>EX</th>
<th>MA</th>
<th>WB</th>
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<td>t0</td>
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<td>8</td>
<td>t7</td>
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</tr>
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</table>

**Example Instruction**

- **Addr**: 0x4
- **Ext**: Add

**Data Memory**

- **addr**: wdata
- **rdata**: rdata

**GPRs**

- **rs1**: rs1
- **rs2**: rs2
- **rd1**: rd1
- **ws**: ws
- **rd2**: rd2

**IR**

- **PC**: IR

**ALU**

- **Imm Ext**: Imm Ext
- **we**: we
- **rs1**: rs1
- **rs2**: rs2
- **rd1**: rd1
- **ws**: ws
- **wd**: wd
- **rd2**: rd2
- **GPRs**: GPRs

**Memory (MA)**

- **addr**: addr
- **rdata**: rdata
- **Data Memory**: Data Memory
- **wdata**: wdata
5-Stage Pipelined Execution

Instruction Flow Diagram

I-Fetch (IF)

I-Fetch (IF) Diagram

Decode, Reg. Fetch (ID)

Execute (EX)

Memory (MA)

Write-Back (WB)

- PC
- Addr
- Rdata
- Inst. Memory
- 0x4

- Add

- Addr
- Rdata
- IR

- IP

- PC

- IF1

- IF2

- IF3

- IF4

- IF5

- EX1

- EX2

- EX3

- EX4

- EX5

- MA1

- MA2

- MA3

- MA4

- MA5

- WB1

- WB2

- WB3

- WB4

- WB5

- Addr

- Rdata

- Data Memory

- ALU

- Imm Ext

- IR

- PC

- L06-20
5-Stage Pipelined Execution

Resource Usage Diagram

Resources

I-Fetch (IF)
Decode, Reg. Fetch (ID)
Execute (EX)
Memory (MA)
Write-Back (WB)
5-Stage Pipelined Execution

Resource Usage Diagram

-I-Fetch (IF)

Decode, Reg. Fetch (ID)

Execute (EX)

Memory (MA)

Write - Back (WB)

Resources

time

t0 t1 t2 t3 t4 t5 t6 t7 ....

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5-Stage Pipelined Execution

Resource Usage Diagram

\[ \text{time} \]

\[ \text{IF} \]

\[ t_0 \quad t_1 \quad t_2 \quad t_3 \quad t_4 \quad t_5 \quad t_6 \quad t_7 \quad \ldots \]

\[ \text{Write-Back (WB)} \]

\[ \text{I-Fetch (IF)} \]

\[ \text{Decode, Reg. Fetch (ID)} \]

\[ \text{Execute (EX)} \]

\[ \text{Memory (MA)} \]

\[ \text{Resources} \]

\[ \text{IF} \]

\[ I_1 \quad I_2 \quad I_3 \quad I_4 \quad I_5 \]

\[ \text{Inst. Memory} \]

\[ \text{Add} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{PC} \]

\[ \text{Write-Back (WB)} \]

\[ \text{Addr} \]

\[ \text{I-Fetch (IF)} \]

\[ \text{Decode, Reg. Fetch (ID)} \]

\[ \text{Execute (EX)} \]

\[ \text{Memory (MA)} \]

\[ \text{Write-Back (WB)} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{ALU} \]

\[ \text{Imm Ext} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{Memory wdata} \]

\[ \text{Addr} \]

\[ \text{I-Fetch (IF)} \]

\[ \text{Decode, Reg. Fetch (ID)} \]

\[ \text{Execute (EX)} \]

\[ \text{Memory (MA)} \]

\[ \text{Write-Back (WB)} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{ALU} \]

\[ \text{Imm Ext} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{Memory wdata} \]

\[ \text{Addr} \]

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\[ \text{addr} \quad \text{rdata} \]

\[ \text{ALU} \]

\[ \text{Imm Ext} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{Memory wdata} \]

\[ \text{Addr} \]

\[ \text{I-Fetch (IF)} \]

\[ \text{Decode, Reg. Fetch (ID)} \]

\[ \text{Execute (EX)} \]

\[ \text{Memory (MA)} \]

\[ \text{Write-Back (WB)} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{ALU} \]

\[ \text{Imm Ext} \]

\[ \text{addr} \quad \text{rdata} \]

\[ \text{Memory wdata} \]

\[ \text{Addr} \]
5-Stage Pipelined Execution

Resource Usage Diagram

- **I-Fetch (IF):**
  - Resources: IF, ID
  - Time: t0, t1, t2, t3, t4, t5, t6, t7, ...

- **Decode, Reg. Fetch (ID):**
  - Resources: I1, I2, I3, I4, I5

- **Execute (EX):**
  - Resources: We, Rs1, Rs2, Rd1, Ws, Wd, Rd2

- **Memory (MA):**
  - Resources: We, Addr, Data, Memory, Wdata

- **Write-Back (WB):**
5-Stage Pipelined Execution

Resource Usage Diagram

- **I-Fetch (IF)**
- **Decode, Reg. Fetch (ID)**
- **Execute (EX)**
- **Memory (MA)**
- **Write-Back (WB)**

**Resources**
- **IF**
- **ID**
- **EX**

**Time**
- $t_0$, $t_1$, $t_2$, $t_3$, $t_4$, $t_5$, $t_6$, $t_7$, ...
5-Stage Pipelined Execution
Resource Usage Diagram

Resources

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L06-21
5-Stage Pipelined Execution

Resource Usage Diagram

```
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<th>Resources</th>
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<th>IF</th>
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</tr>
</tbody>
</table>
```

Add

Sanchez & Emer
5-Stage Pipelined Execution

Resource Usage Diagram

---

I-Fetch (IF)

Decode, Reg. Fetch (ID)

Execute (EX)

Memory (MA)

Write - Back (WB)

Resources: IF, ID, EX, MA, WB

Resources:
- IF
- ID
- EX
- MA
- WB

Time:
- t0
- t1
- t2
- t3
- t4
- t5
- t6
- t7

---

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Pipelined Execution: ALU Instructions
Pipelined Execution: ALU Instructions

Not quite correct!
Pipelined Execution: ALU Instructions

Not quite correct!

We need an Instruction Reg (IR) for each stage
Pipelined Execution: ALU Instructions

Not quite correct!

We need an Instruction Reg (IR) for each stage
Pipelined Execution: ALU Instructions

Not quite correct!

We need an Instruction Reg (IR) for each stage
Pipelined Execution:
ALU Instructions

Not quite correct!

We need an Instruction Reg (IR) for each stage
Pipelined MIPS Datapath

without jumps

What else is needed?
Pipelined MIPS Datapath

without jumps

What else is needed?

Control Points Need to Be Connected
Pipelined MIPS Datapath
without jumps

What else is needed?

Control Points Need to Be Connected
Pipelined MIPS Datapath
without jumps

What else is needed?

Control Points Need to Be Connected
Pipelined MIPS Datapath
without jumps

What else is needed?

Control Points Need to Be Connected
Pipelined MIPS Datapath
without jumps

What else is needed?

Control Points Need to Be Connected
Pipelined MIPS Datapath
without jumps

What else is needed?

Control Points Need to Be Connected
How instructions can interact with each other in a pipeline
How instructions can interact with each other in a pipeline

- An instruction in the pipeline may need a resource being used by another instruction in the pipeline → *structural hazard*
How instructions can interact with each other in a pipeline

• An instruction in the pipeline may need a resource being used by another instruction in the pipeline \(\rightarrow\) **structural hazard**

• An instruction may depend on something produced by an earlier instruction
  
  - Dependence may be for a data calculation \(\rightarrow\) **data hazard**
  
  - Dependence may be for calculating the next PC \(\rightarrow\) **control hazard (branches, interrupts)**
Data Hazards

... r1 ← r0 + 10 
... r4 ← r1 + 17 
...
Data Hazards

\[ r1 \leftarrow r0 + 10 \]
\[ r4 \leftarrow r1 + 17 \]

...
Data Hazards

... r4 ← r1 ...

r1 ← ...

... r1 ← r0 + 10
r4 ← r1 + 17
...

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Data Hazards

... r1 ← r0 + 10
r4 ← r1 + 17
...

r1 is stale. Oops!
Resolving Data Hazards

Strategy 1: *Wait for the result to be available by freezing earlier pipeline stages* → **stall**

Strategy 2: *Route data as soon as possible after it is calculated to the earlier pipeline stage* → **bypass**

Strategy 3: *Speculate on the dependence*

Two cases:
Resolving Data Hazards

Strategy 1: *Wait for the result to be available by freezing earlier pipeline stages → stall*

Strategy 2: *Route data as soon as possible after it is calculated to the earlier pipeline stage → bypass*

Strategy 3: *Speculate on the dependence*
   *Two cases:*
   - *Guessed correctly → do nothing*
Resolving Data Hazards

Strategy 1: *Wait for the result to be available by freezing earlier pipeline stages* → *stall*

Strategy 2: *Route data as soon as possible after it is calculated to the earlier pipeline stage* → *bypass*

Strategy 3: *Speculate on the dependence*

*Two cases:*

- *Guessed correctly* → *do nothing*
- *Guessed incorrectly* → *kill and restart*
Resolving Data Hazards (1)

Strategy 1:

*Wait for the result to be available by freezing earlier pipeline stages → stall*
Feedback to Resolve Hazards

- Later stages provide dependence information to earlier stages which can stall (or kill) instructions
Feedback to Resolve Hazards

- Later stages provide dependence information to earlier stages which can stall (or kill) instructions
Feedback to Resolve Hazards

- Later stages provide dependence information to earlier stages which can stall (or kill) instructions.
Feedback to Resolve Hazards

• Later stages provide dependence information to earlier stages which can *stall (or kill) instructions*
Feedback to Resolve Hazards

Later stages provide dependence information to earlier stages which can stall (or kill) instructions.
Feedback to Resolve Hazards

Later stages provide dependence information to earlier stages which can *stall (or kill) instructions*
Feedback to Resolve Hazards

Later stages provide dependence information to earlier stages which can stall (or kill) instructions.
Feedback to Resolve Hazards

- Later stages provide dependence information to earlier stages which can stall (or kill) instructions
Feedback to Resolve Hazards

- Later stages provide dependence information to earlier stages which can stall (or kill) instructions.

- Controlling a pipeline in this manner works provided the instruction at stage $i+1$ can complete without any interference from instructions in stages 1 to $i$ (otherwise deadlocks may occur).
Resolving Data Hazards by Stalling

... 
\( r1 \leftarrow r0 + 10 \)
\( r4 \leftarrow r1 + 17 \)
...
Resolving Data Hazards by Stalling

... r1 ← r0 + 10
r4 ← r1 + 17
...

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Resolving Data Hazards by Stalling

... r1 ← r0 + 10
r4 ← r1 + 17
...

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Resolving Data Hazards by Stalling

Stall Condition

... 
$r1 \leftarrow r0 + 10$
$r4 \leftarrow r1 + 17$
...
Stalled Stages and Pipeline Bubbles
Stalled Stages and Pipeline Bubbles

\begin{center}
time \\
t0 \ t1 \ t2 \ t3 \ t4 \ t5 \ t6 \ t7 \ \ldots
\end{center}
Stalled Stages and Pipeline Bubbles

\[ \text{time} \]
\[ t_0 \quad t_1 \quad t_2 \quad t_3 \quad t_4 \quad t_5 \quad t_6 \quad t_7 \quad \ldots \]

\[(I_1) \quad r_1 \leftarrow (r_0) + 10 \quad I_{F_1} \quad I_{D_1} \quad E_{X_1} \quad M_{A_1} \quad W_{B_1} \]
Stalled Stages and Pipeline Bubbles

\[ \begin{align*}
  \text{time} \\
  \text{t0} & \quad \text{t1} & \quad \text{t2} & \quad \text{t3} & \quad \text{t4} & \quad \text{t5} & \quad \text{t6} & \quad \text{t7} & \quad \ldots \\
  (I_1) \ r1 & \leftarrow (r0) + 10 & \text{IF}_1 & \text{ID}_1 & \text{EX}_1 & \text{MA}_1 & \text{WB}_1 \\
  (I_2) \ r4 & \leftarrow (r1) + 17 & \text{IF}_2 & \text{ID}_2 & \text{ID}_2 & \text{ID}_2 & \text{ID}_2 & \text{EX}_2 & \text{MA}_2 & \text{WB}_2
\end{align*} \]
Stalled Stages and Pipeline Bubbles

\[
\begin{align*}
\text{time} \\
\text{t0} & \quad \text{t1} & \quad \text{t2} & \quad \text{t3} & \quad \text{t4} & \quad \text{t5} & \quad \text{t6} & \quad \text{t7} & \quad \ldots \\
(I_1) & \quad r_1 \leftarrow (r_0) + 10 & \quad \text{IF}_1 & \quad \text{ID}_1 & \quad \text{EX}_1 & \quad \text{MA}_1 & \quad \text{WB}_1 \\
(I_2) & \quad r_4 \leftarrow (r_1) + 17 & \quad \text{IF}_1 & \quad \text{ID}_2 & \quad \text{ID}_2 & \quad \text{ID}_2 & \quad \text{EX}_2 & \quad \text{MA}_2 & \quad \text{WB}_2 \\
(I_3) & \quad & \quad \text{IF}_3 & \quad \text{IF}_3 & \quad \text{IF}_3 & \quad \text{ID}_3 & \quad \text{EX}_3 & \quad \text{MA}_3 & \quad \text{WB}_3
\end{align*}
\]
## Stalled Stages and Pipeline Bubbles

### Time

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<td>$r_4 \leftarrow (r_1) + 17$</td>
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<td>$ID_4$</td>
<td>$EX_4$</td>
<td>$MA_4$</td>
<td>$WB_4$</td>
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</tr>
</tbody>
</table>
Stalled Stages and Pipeline Bubbles

\[ \text{time} \]
\[ t_0 \quad t_1 \quad t_2 \quad t_3 \quad t_4 \quad t_5 \quad t_6 \quad t_7 \quad \ldots \quad \]

(I_1) \( r_1 \leftarrow (r_0) + 10 \)

IF_1 \quad ID_1 \quad EX_1 \quad MA_1 \quad WB_1

(I_2) \( r_4 \leftarrow (r_1) + 17 \)

IF_2 \quad ID_2 \quad ID_2 \quad ID_2 \quad ID_2 \quad EX_2 \quad MA_2 \quad WB_2

(I_3)

IF_3 \quad ID_3 \quad IF_3 \quad IF_3 \quad IF_3 \quad EX_3 \quad MA_3 \quad WB_3

(I_4)

IF_4 \quad ID_4 \quad EX_4 \quad MA_4 \quad WB_4

(I_5)

IF_5 \quad ID_5 \quad EX_5 \quad MA_5 \quad WB_5
Stalled Stages and Pipeline Bubbles

\[ \begin{align*}
(I_1) & \quad r_1 \leftarrow (r_0) + 10 \\
(I_2) & \quad r_4 \leftarrow (r_1) + 17 \\
(I_3) & \\
(I_4) & \\
(I_5) &
\end{align*} \]

\[ \begin{align*}
t & \quad t_0 \quad t_1 \quad t_2 \quad t_3 \quad t_4 \quad t_5 \quad t_6 \quad t_7 \quad \ldots
\end{align*} \]
Stalled Stages and Pipeline Bubbles

```
time  t0  t1  t2  t3  t4  t5  t6  t7  ....
(I_1) r1 ← (r0) + 10  IF_1
(I_2) r4 ← (r1) + 17  IF_2
(I_3)
(I_4)
(I_5)
```

```
ID_1  EX_1  MA_1  WB_1
IF_2  ID_2  ID_2  ID_2
IF_3  IF_3  IF_3  IF_3
```

Stalled stages
Stalled Stages and Pipeline Bubbles

Resource Usage

$t0$  $t1$  $t2$  $t3$  $t4$  $t5$  $t6$  $t7$  . . . .

(I_1) \ r_1 \leftarrow (r_0) + 10 \quad IF_1

(I_2) \ r_4 \leftarrow (r_1) + 17 \quad IF_2

(I_3)

(I_4)

(I_5)

stalled stages
Stalled Stages and Pipeline Bubbles

\[ (I_1) \ r_1 \leftarrow (r_0) + 10 \]
\[ (I_2) \ r_4 \leftarrow (r_1) + 17 \]

\[ (I_3) \]
\[ (I_4) \]
\[ (I_5) \]

Resource Usage
Stalled Stages and Pipeline Bubbles

\begin{equation*}
(I_1) \quad r_1 \leftarrow (r_0) + 10 \\
(I_2) \quad r_4 \leftarrow (r_1) + 17 \\
(I_3) \\
(I_4) \\
(I_5)
\end{equation*}

Resource Usage

\begin{equation*}
time \\
\begin{array}{cccccccc}
\text{time} & t_0 & t_1 & t_2 & t_3 & t_4 & t_5 & t_6 & t_7 & \ldots \\
\text{IF} & I_1 & I_2 & I_3 & I_3 & I_3 & I_3 & I_4 & I_5
\end{array}
\end{equation*}
Stalled Stages and Pipeline Bubbles

\[ \text{time} \]

\[
\begin{array}{cccccccc}
 t0 & t1 & t2 & t3 & t4 & t5 & t6 & t7 & \ldots \\
\end{array}
\]

\[
(I_1) \ r1 \leftarrow (r0) + 10
\]

\[
(I_2) \ r4 \leftarrow (r1) + 17
\]

\[
(I_3)
\]

\[
(I_4)
\]

\[
(I_5)
\]

\[
\text{stalled stages}
\]

Resource Usage

\[
\begin{array}{cccccccc}
\text{IF} & I_1 & I_2 & I_3 & I_3 & I_3 & I_3 & I_4 & I_5 \\
\text{ID} & I_1 & I_2 & I_2 & I_2 & I_2 & I_3 & I_4 & I_5 \\
\end{array}
\]
Stalled Stages and Pipeline Bubbles

\[
time \\
\begin{array}{cccccccc}
\text{t0} & \text{t1} & \text{t2} & \text{t3} & \text{t4} & \text{t5} & \text{t6} & \text{t7} \\
\text{IF}_1 & \text{ID}_1 & \text{EX}_1 & \text{MA}_1 & \text{WB}_1 & \text{ID}_2 & \text{ID}_2 & \text{ID}_2 \\
\text{IF}_2 & \text{ID}_2 & \text{ID}_2 & \text{ID}_2 & \text{ID}_2 & \text{EX}_2 & \text{MA}_2 & \text{WB}_2 \\
\text{IF}_3 & \text{IF}_3 & \text{IF}_3 & \text{IF}_3 & \text{IF}_3 & \text{IF}_3 & \text{IF}_3 & \text{IF}_3 \\
\text{IF}_4 & \text{ID}_4 & \text{EX}_4 & \text{MA}_4 & \text{WB}_4 & \text{IF}_5 & \text{ID}_5 & \text{EX}_5 & \text{MA}_5 & \text{WB}_5 \\
\end{array}
\]

\text{Stalled stages}

\text{(I_1)} r1 \leftarrow (r0) + 10 \quad \text{(I_2)} r4 \leftarrow (r1) + 17

Resource Usage

\[
\begin{array}{cccccccc}
\text{IF} & \text{ID} & \text{EX} \\
\text{I_1} & \text{I_2} & \text{nop} \\
\text{I_2} & \text{I_2} & \text{nop} \\
\text{I_3} & \text{I_2} & \text{nop} \\
\text{I_3} & \text{I_2} & \text{nop} \\
\text{I_3} & \text{I_2} & \text{nop} \\
\text{I_3} & \text{I_2} & \text{nop} \\
\text{I_3} & \text{I_2} & \text{nop} \\
\text{I_3} & \text{I_2} & \text{nop} \\
\end{array}
\]
Stalled Stages and Pipeline Bubbles

Resource Usage

| Time | t0 | t1 | t2 | t3 | t4 | t5 | t6 | t7 | ...
|------|----|----|----|----|----|----|----|----|------
| IF   | I1 | I2 | I3 | I3 | I3 | I3 | I4 | I5 |      |
| ID   | I1 | I2 | I2 | I2 | I2 | I3 | I4 | I5 |      |
| EX   | I1 |   |   | nop| nop| nop| I2 | I3 | I4 | I5 |
| MA   | I1 |   |   |   |   |   | I2 | I3 | I4 | I5 |

Stalled stages

(I_1) r1 ← (r0) + 10
(I_2) r4 ← (r1) + 17

IF
ID
EX
MA
## Stalled Stages and Pipeline Bubbles

### Time

<table>
<thead>
<tr>
<th>Time</th>
<th>Stage 1</th>
<th>Stage 2</th>
<th>Stage 3</th>
<th>Stage 4</th>
<th>Stage 5</th>
<th>Stage 6</th>
<th>Stage 7</th>
<th>...</th>
</tr>
</thead>
<tbody>
<tr>
<td>t0</td>
<td>IF1</td>
<td>ID1</td>
<td>EX1</td>
<td>MA1</td>
<td>WB1</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>t1</td>
<td>IF2</td>
<td>ID2</td>
<td>ID2</td>
<td>ID2</td>
<td>IF3</td>
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<td></td>
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<tr>
<td>t2</td>
<td>ID3</td>
<td>IF3</td>
<td>IF3</td>
<td>IF3</td>
<td>ID4</td>
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</tr>
<tr>
<td>t3</td>
<td>ID5</td>
<td>EX3</td>
<td>MA3</td>
<td>WB3</td>
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<td></td>
</tr>
<tr>
<td>t4</td>
<td>IF4</td>
<td>ID4</td>
<td>EX4</td>
<td>MA4</td>
<td>WB4</td>
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<tr>
<td>t5</td>
<td>IF5</td>
<td>ID5</td>
<td>EX5</td>
<td>MA5</td>
<td>WB5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Stalled Stages

- (I₁) \( r1 \leftarrow (r0) + 10 \)
- (I₂) \( r4 \leftarrow (r1) + 17 \)

### Resource Usage

- **IF**
  - t0: \( I₁ \)
  - t1: \( I₂ \)
  - t2: \( I₃ \)
  - t3: \( I₃ \)
  - t4: \( I₃ \)
  - t5: \( I₄ \)
  - t6: \( I₅ \)
  - t7: \( I₅ \)

- **ID**
  - t0: \( I₁ \)
  - t1: \( I₂ \)
  - t2: \( I₂ \)
  - t3: \( I₂ \)
  - t4: \( I₂ \)
  - t5: \( I₃ \)
  - t6: \( I₄ \)
  - t7: \( I₅ \)

- **EX**
  - t0: \( I₁ \)
  - t1: \( I₁ \)
  - t2: \( nop \)
  - t3: \( nop \)
  - t4: \( nop \)
  - t5: \( nop \)
  - t6: \( nop \)
  - t7: \( nop \)

- **MA**
  - t0: \( I₁ \)
  - t1: \( I₁ \)
  - t2: \( nop \)
  - t3: \( nop \)
  - t4: \( nop \)
  - t5: \( nop \)
  - t6: \( nop \)
  - t7: \( nop \)

- **WB**
  - t0: \( I₁ \)
  - t1: \( I₁ \)
  - t2: \( nop \)
  - t3: \( nop \)
  - t4: \( nop \)
  - t5: \( nop \)
  - t6: \( nop \)
  - t7: \( nop \)
Stalled Stages and Pipeline Bubbles

\[
\begin{align*}
\text{time} & \quad t0 \quad t1 \quad t2 \quad t3 \quad t4 \quad t5 \quad t6 \quad t7 \quad \ldots \ldots \\
(\text{I}_1) & \quad r1 \leftarrow (r0) + 10 \quad \text{IF}_1 \quad \text{ID}_1 \quad \text{EX}_1 \quad \text{MA}_1 \quad \text{WB}_1 \\
(\text{I}_2) & \quad r4 \leftarrow (r1) + 17 \quad \text{IF}_2 \quad \text{ID}_2 \quad \text{EX}_2 \quad \text{MA}_2 \quad \text{WB}_2 \\
(\text{I}_3) & \quad \text{ID}_2 \quad \text{ID}_2 \quad \text{ID}_2 \quad \text{ID}_2 \\
(\text{I}_4) & \quad \text{IF}_3 \quad \text{IF}_3 \quad \text{IF}_3 \quad \text{IF}_3 \\
(\text{I}_5) & \quad \text{EX}_3 \quad \text{MA}_3 \quad \text{WB}_3 \\
(\text{I}_6) & \quad \text{EX}_4 \quad \text{MA}_4 \quad \text{WB}_4 \\
(\text{I}_7) & \quad \text{EX}_5 \quad \text{MA}_5 \quad \text{WB}_5
\end{align*}
\]

Resource Usage

- IF
- ID
- EX
- MA
- WB

Stalled stages

February 27, 2017  Sanchez & Emer
Stalled Stages and Pipeline Bubbles

(time)

\( t_0 \quad t_1 \quad t_2 \quad t_3 \quad t_4 \quad t_5 \quad t_6 \quad t_7 \quad \ldots \)

(I_1) \ r_1 \leftarrow (r_0) + 10

(I_2) \ r_4 \leftarrow (r_1) + 17

(I_3)

(I_4)

(I_5)

\hline

\textbf{Stalled Stages}

\hline

Resource Usage

<table>
<thead>
<tr>
<th>IF</th>
<th>ID</th>
<th>EX</th>
<th>MA</th>
<th>WB</th>
</tr>
</thead>
<tbody>
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<td>I_1</td>
<td>I_1</td>
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<td>I_4</td>
<td>I_4</td>
<td>I_4</td>
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</tbody>
</table>

\textbf{nop} \Rightarrow \text{pipeline bubble}
Stall Control Logic

Compare the source registers of the instruction in the decode stage with the destination register of the uncommitted instructions.
Stall Control Logic

Compare the source registers of the instruction in the decode stage with the destination register of the uncommitted instructions.
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Compare the source registers of the instruction in the decode stage with the destination register of the uncommitted instructions.