Cache Coherence

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http://www.csg.csail.mit.edu/6.823
The Shift to Multicore

[Produced with CPUBDB, cpudb.stanford.edu]
The Shift to Multicore

- Since 2005, improvements in system performance mainly due to increasing cores per chip

[Produced with CPUDB, cpudb.stanford.edu]
The Shift to Multicore

- Since 2005, improvements in system performance mainly due to increasing cores per chip
- Why?

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- Why? Limited instruction-level parallelism
The Shift to Multicore

- Since 2005, improvements in system performance mainly due to increasing cores per chip
- Why? Limited instruction-level parallelism
  Technology scaling

[Produced with CPUDB, cpudb.stanford.edu]
Multicore Performance

Cost/perf curve of possible core designs

High-perf, expensive core

Cost (area, energy...)

Performance
Multicore Performance

Cost/perf curve of possible core designs

Performance

Cost (area, energy...)

High-perf, expensive core

Moderate perf, efficient core
Multicore Performance

Cost/perf curve of possible core designs

- High-perf, expensive core
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2 cores
Multicore Performance

Cost/perf curve of possible core designs

High-perf, expensive core

Moderate perf, efficient core

Performance

Cost (area, energy...)

2 cores

4 cores

L14-3
Multicore Performance

Cost (area, energy...) vs. Performance

- High-perf, expensive core
- Moderate perf, efficient core

Cost/perf curve of possible core designs

2 cores

4 cores

What factors may limit multicore performance?
Multicore Performance

Cost/perf curve of possible core designs

High-perf, expensive core

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Cost (area, energy...)

Performance

What factors may limit multicore performance?

Limited application parallelism

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Sanchez & Emer
Multicore Performance

Cost/perf curve of possible core designs

High-perf, expensive core

Moderate perf, efficient core

What factors may limit multicore performance?

- Limited application parallelism
- Memory accesses and inter-core communication
Multicore Performance

What factors may limit multicore performance?

- Limited application parallelism
- Memory accesses and inter-core communication
- Programming complexity

Cost/perf curve of possible core designs

- High-perf, expensive core
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2 cores
4 cores
Amdahl’s Law

- Speedup = \( \frac{\text{time without enhancement}}{\text{time with enhancement}} \)
- Suppose an enhancement speeds up a fraction \( f \) of a task by a factor of \( S \)
  \[
  \text{time}_{\text{new}} = \text{time}_{\text{old}} \cdot \left( (1-f) + \frac{f}{S} \right)
  \]
  \[
  S_{\text{overall}} = \frac{1}{(1-f) + \frac{f}{S}}
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Amdahl’s Law

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**Corollary:** Make the common case fast
Amdahl’s Law and Parallelism

- Say you write a program that can do 90% of the work in parallel, but the other 10% is sequential.
- What is the maximum speedup you can get by running on a multicore machine?
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\[ f = 0.9, S = \infty \rightarrow S_{\text{overall}} = 10 \]
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- \( f = 0.9, \ S=\infty \rightarrow S_{\text{overall}} = 10 \)

What \( f \) do you need to use a 1000-core machine well?
Communication Models

• Shared memory:
  – Single address space
  – Implicit communication by reading/writing memory
    • Data
    • Control (semaphores, locks, barriers, ...)
  – Low-level programming model: threads
Communication Models

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• Message passing:
  – Separate address spaces
  – Explicit communication by send/rcv messages
    • Data & control (blocking msgs, barriers, ...)
  – Low-level programming model: processes + inter-process communication (e.g., MPI)
Communication Models

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• Pros/cons of each model?
Coherence & Consistency

• Shared memory systems:
  - Have multiple private caches for performance reasons
  - Need to provide the illusion of a single shared memory
Coherence & Consistency

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• Intuition: A read should return the most recently written value
  - What is “most recent”?
Coherence & Consistency

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- Formally:
  - Coherence: What values can a read return?
    - Concerns reads/writes to a single memory location
  - Consistency: When do writes become visible to reads?
    - Concerns reads/writes to multiple memory locations
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Cache Coherence Avoids Stale Data
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1. LD 0xA → 2
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
Cache Coherence Avoids Stale Data

1. LD 0xA \rightarrow 2
2. ST 3 \rightarrow 0xA
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
Cache Coherence Avoids Stale Data

1. LD 0xA → 2
2. ST 3 → 0xA
3. LD 0xA → 2 (stale!)
Cache Coherence Avoids Stale Data

- A cache coherence protocol controls cache contents to avoid stale cache lines

1. LD 0xA → 2
2. ST 3 → 0xA
3. LD 0xA → 2 (stale!)
Implementing Cache Coherence

Coherence protocols must enforce two rules:
- Write propagation: Writes eventually become visible to all processors
- Write serialization: Writes to the same location are serialized (all processors see them in the same order)
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How to ensure write propagation?
- Write-invalidate protocols: Invalidate all other cached copies before performing the write
- Write-update protocols: Update all other cached copies after performing the write
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• How to track sharing state of cached data and serialize requests to the same address?
  – Snooping-based protocols: All caches observe each other’s actions through a shared bus
  – Directory-based protocols: A coherence directory tracks contents of private caches and serializes requests
Snooping-Based Coherence [Goodman 1983]

Caches watch (snoop on) bus to keep all processors’ view of memory coherent
Snooping-Based Coherence

- Bus provides serialization point
  - Broadcast, totally ordered
  - Each cache controller “snoops” all bus transactions
  - Controller updates state of cache in response to processor and snoop events and generates bus transactions
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- Snoopy protocol (FSM)
  - State-transition diagram
  - Actions

![Diagram of Processor, Cache, and Snoop (observed bus transaction)](http://www.csg.csail.mit.edu/6.823)
Snooping-Based Coherence

- **Bus provides serialization point**
  - Broadcast, totally *ordered*
  - Each cache controller “snoops” all bus transactions
  - Controller updates state of cache in response to processor and snoop events and generates bus transactions

- **Snoopy protocol (FSM)**
  - State-transition diagram
  - Actions

- **Handling writes:**
  - Write-invalidate
  - Write-update

---

![Diagram](http://www.csg.csail.mit.edu/6.823)
A Simple Protocol: Valid/Invalid (VI)

- Assume write-through caches

**Actions**

- Processor Read (PrRd)
- Processor Write (PrWr)
- Bus Read (BusRd)
- Bus Write (BusWr)
Valid/Invalid Example

![Diagram showing main memory, cache, and two cores](http://www.csg.csail.mit.edu/6.823)

- Main Memory
- Cache
- Core 0
- Core 1
- Table: Tag, State, Data

Valid/Invalid Example

1. LD 0xA
Valid/Invalid Example

Main Memory

BusRd 0xA

Cache

<table>
<thead>
<tr>
<th>Tag</th>
<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Core 0

Core 1

1 LD 0xA

Valid/Invalid Example

Main Memory

BusRd 0xA

Cache

<table>
<thead>
<tr>
<th>Tag</th>
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<th>Data</th>
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</thead>
<tbody>
<tr>
<td>0xA</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

Core 0

Core 1

1 LD 0xA
Valid/Invalid Example

LD 0xA
Valid/Invalid Example

1. LD 0xA

Core 0

Cache

<table>
<thead>
<tr>
<th>Tag</th>
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</thead>
<tbody>
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</table>

Core 1

Cache

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<tr>
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<th>State</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
Valid/Invalid Example

1. LD 0xA

2. LD 0xA
Valid/Invalid Example

Additional loads satisfied locally, without BusRd
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
Valid/Invalid Example

BusWr 0xA, 3

Core 0

1. LD 0xA
2. ST 0xA

Core 1

2. LD 0xA
Valid/Invalid Example

BusWr 0xA, 3

Core 0
1. LD 0xA
2. ST 0xA

Core 1
2. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>0xA</td>
<td>V</td>
<td>3</td>
</tr>
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</table>

<table>
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<tr>
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</tr>
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<td>0xA</td>
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<td>2</td>
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</table>
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA
Valid/Invalid Example

1. LD 0xA
2. LD 0xA
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Valid/Invalid Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. LD 0xA

VI Problems?
Valid/Invalid Example

Every write updates main memory
Every write requires broadcast & snoop
Modified/Shared/Invalid (MSI) Protocol

- Allows writeback caches + satisfying writes locally

Actions

<table>
<thead>
<tr>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Read (PrRd)</td>
</tr>
<tr>
<td>Processor Write (PrWr)</td>
</tr>
<tr>
<td>Bus Read (BusRd)</td>
</tr>
<tr>
<td>Bus Read Exclusive (BusRdX)</td>
</tr>
<tr>
<td>Bus Writeback (BusWB)</td>
</tr>
</tbody>
</table>
MSI Example
MSI Example

1. LD 0xA
MSI Example

Main Memory

BusRd 0xA

Cache

<table>
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<tr>
<th>Tag</th>
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</table>

Core 0

Core 1

1 LD 0xA
MSI Example

BusRd 0xA

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Core 0

Core 1

1. LD 0xA
MSI Example

1. LD 0xA
MSI Example

1. LD 0xA

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2. LD 0xA
MSI Example

1. LD 0xA
2. LD 0xA

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</table>
MSI Example

1. LD 0xA

2. LD 0xA
MSI Example

Additional loads satisfied locally, without BusRd (like in VI)
MSI Example

1. LD 0xA

2. LD 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
**MSI Example**

Main Memory

**BusRdX 0xA**

<table>
<thead>
<tr>
<th>Cache</th>
<th>Cache</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tag</strong></td>
<td><strong>State</strong></td>
</tr>
<tr>
<td>0xA</td>
<td>M</td>
</tr>
<tr>
<td>0xA</td>
<td>I</td>
</tr>
</tbody>
</table>

**Core 0**

1. LD 0xA
2. ST 0xA
3. LD 0xA
MSI Example

Additional loads *and stores* from core 0 satisfied locally, without bus transactions (unlike in VI)
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA

<table>
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<tr>
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<tbody>
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<td>M</td>
<td>3</td>
</tr>
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<td>I</td>
<td>2</td>
</tr>
</tbody>
</table>
### MSI Example

1. **LD 0xA**
2. **ST 0xA**

#### Cache Details:

**Core 0**
- **Tag:** 0xA
- **State:** M
- **Data:** 3

**Core 1**
- **Tag:** 0xA
- **State:** I
- **Data:** 2

#### Main Memory

**BusRdX 0xA**
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
Cache interventions

- MSI allows caches to serve writes without updating memory, so main memory can have stale data
  - Core 0’s cache needs to supply data
  - But main memory may also respond!

- Cache must override response from main memory
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
MSI Example

1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA

Core 0

Cache

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Core 1

Cache

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<th>State</th>
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</tr>
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<tr>
<td>0xA</td>
<td>M</td>
<td>10</td>
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MSI Example

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2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA
MSI Example

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MSI Example

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1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA
MSI Optimizations: Exclusive State

• Observation: Doing read-modify-write sequences on private data is common
  – What’s the problem with MSI?
MSI Optimizations: Exclusive State

• Observation: Doing read-modify-write sequences on private data is common
  – What’s the problem with MSI?

• Solution: E state (exclusive, clean)
  – If no other sharers, a read acquires line in E instead of S
  – Writes silently cause E→M (exclusive, dirty)
MESI: An Enhanced MSI protocol
increased performance for private read-write data

Each cache line has a tag

- **M**: Modified Exclusive
- **E**: Exclusive, unmodified
- **S**: Shared
- **I**: Invalid

<table>
<thead>
<tr>
<th>Address tag</th>
<th>state bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>PrWr / --</td>
<td>PrRd / --</td>
</tr>
<tr>
<td>BusRd / BusWB</td>
<td>PrWr / BusRdX</td>
</tr>
<tr>
<td>PrRd / BusRdX</td>
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if no other sharers
if other sharers
MSI Optimizations: Owner State

- Observation: On M→S transitions, must write back line!
  - What happens with frequent read-write sharing?
  - Can we defer the write after S?
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• Solution: O state (Owner)
  - O = S + responsibility to write back
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• MSI, MESI, MOSI, MOESI...
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- MSI, MESI, MOSI, MOESI...
  - Typically E if private read-write >> shared read-only (common)
  - Typically O only if writebacks are expensive (main mem vs L3)
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

- **Req**
- **Delay**
- **Response**

*Simple, but low throughput!*
Split-Transaction and Pipelined Buses

Atomic Transaction Bus

- Supports multiple simultaneous transactions
  - Higher throughput
  - Responses may arrive out of order

- Often implemented as multiple buses (req+resp)

Split-Transaction Bus

- Simple, but low throughput!
Non-Atomicity $\rightarrow$ Transient States

- Protocol must handle lack of atomicity
- Two types of states
  - Stable (e.g. MSI)
  - Transient
- Split + race transitions
- Higher complexity

### Actions

<table>
<thead>
<tr>
<th>Actions</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Request</td>
<td>(BusReq)</td>
</tr>
<tr>
<td>Bus Grant</td>
<td>(BusGnt)</td>
</tr>
</tbody>
</table>

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Sanchez & Emer
Scaling Cache Coherence

- Can implement ordered interconnects that scale better than buses...

Starfire E10000 (drawn with only eight processors for clarity). A coherence request is unicast up to the root, where it is serialized, before being broadcast down to all processors.
Scaling Cache Coherence

- Can implement ordered interconnects that scale better than buses...

Starfire E10000 (drawn with only eight processors for clarity). A coherence request is unicast up to the root, where it is serialized, before being broadcast down to all processors.

- ...but broadcast is fundamentally unscalable
  - Bandwidth, energy of transactions with 100s of cache snoops?
Directory-Based Coherence

- Route all coherence transactions through a directory
  - Tracks contents of private caches → No broadcasts
  - Serves as ordering point for conflicting requests → Unordered networks

(more on next lecture)
A cache block contains more than one word and cache coherence is done at the block-level and not word-level

Suppose $P_1$ writes $\text{word}_i$ and $P_2$ writes $\text{word}_k$ and both words have the same block address.

What can happen?
A cache block contains more than one word and cache coherence is done at the block-level and not word-level.

Suppose $P_1$ writes $\text{word}_i$ and $P_2$ writes $\text{word}_k$ and both words have the same block address.

**What can happen?** The block may be invalidated (ping-pong) many times unnecessarily because addresses are in the same block.
Cache coherence protocols will cause mutex to ping-pong between P1’s and P2’s caches.

Ping-ponging can be reduced by first reading the mutex location (non-atomically) and executing a swap only if it is found to be zero (test&test&set).
In general, an atomic *read-modify-write* instruction requires two memory (bus) operations without intervening memory operations by other processors.
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⇒ expensive for simple buses

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In a multiprocessor setting, bus needs to be locked for the entire duration of the atomic read and write operation:
- \(\Rightarrow\) expensive for simple buses
- \(\Rightarrow\) *very expensive* for split-transaction buses

Modern processors use

- *load-reserve*
- *store-conditional*
Load-reserve & Store-conditional

Special register(s) to hold reservation flag and address, and the outcome of store-conditional

Load-reserve R, (a):
<flag, adr> ← <1, a>;
R ← M[a];

Store-conditional (a), R:
if <flag, adr> == <1, a>
then cancel other procs’ reservation on a;
M[a] ← <R>;
status ← succeed;
else status ← fail;

If the snooper sees a store transaction to the address in the reserve register, the reserve bit is set to 0

- Several processors may reserve ‘a’ simultaneously
- These instructions are like ordinary loads and stores with respect to the bus traffic
Performance: Load-reserve & Store-conditional

The total number of memory (bus) transactions is not necessarily reduced, but splitting an atomic instruction into load-reserve & store-conditional:

- *increases bus utilization* (and reduces processor stall time), especially in split-transaction buses

- *reduces cache ping-pong effect* because processors trying to acquire a mutex do not have to perform stores each time