

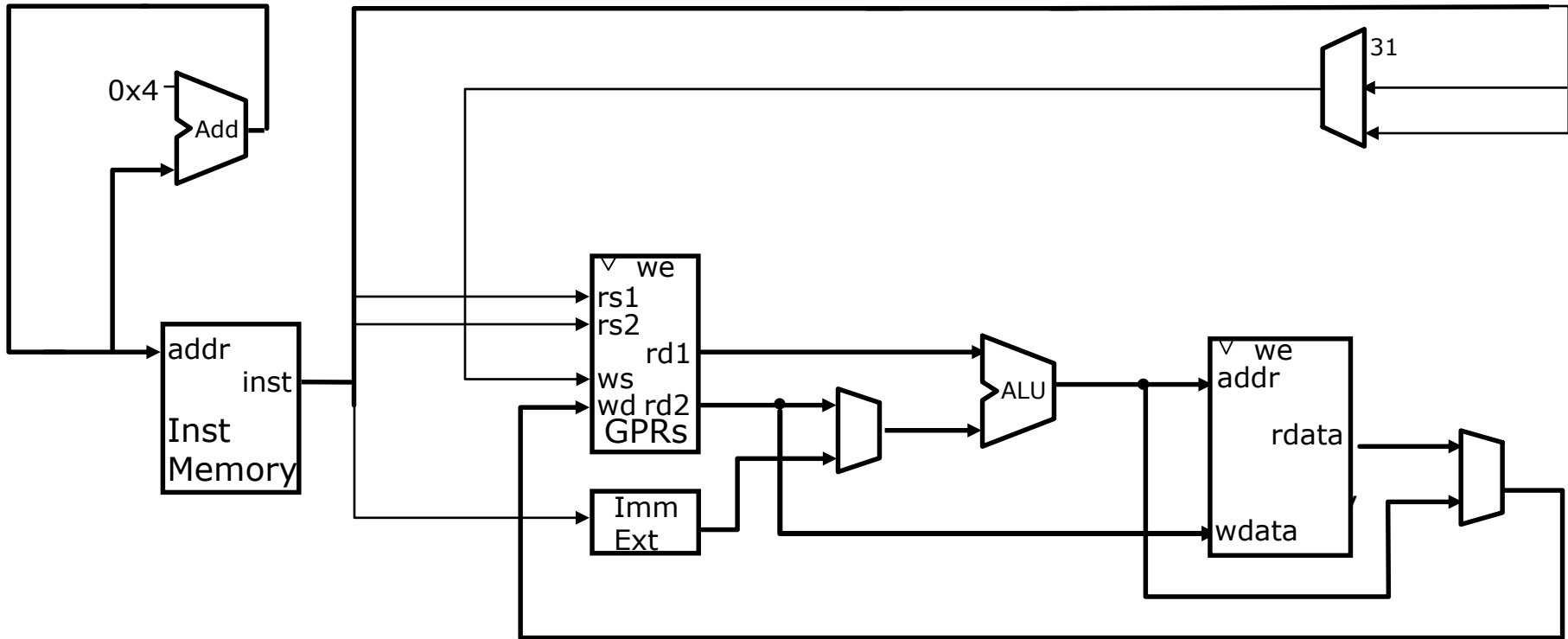
Instruction Pipelining: Hazard Resolution, Timing Constraints

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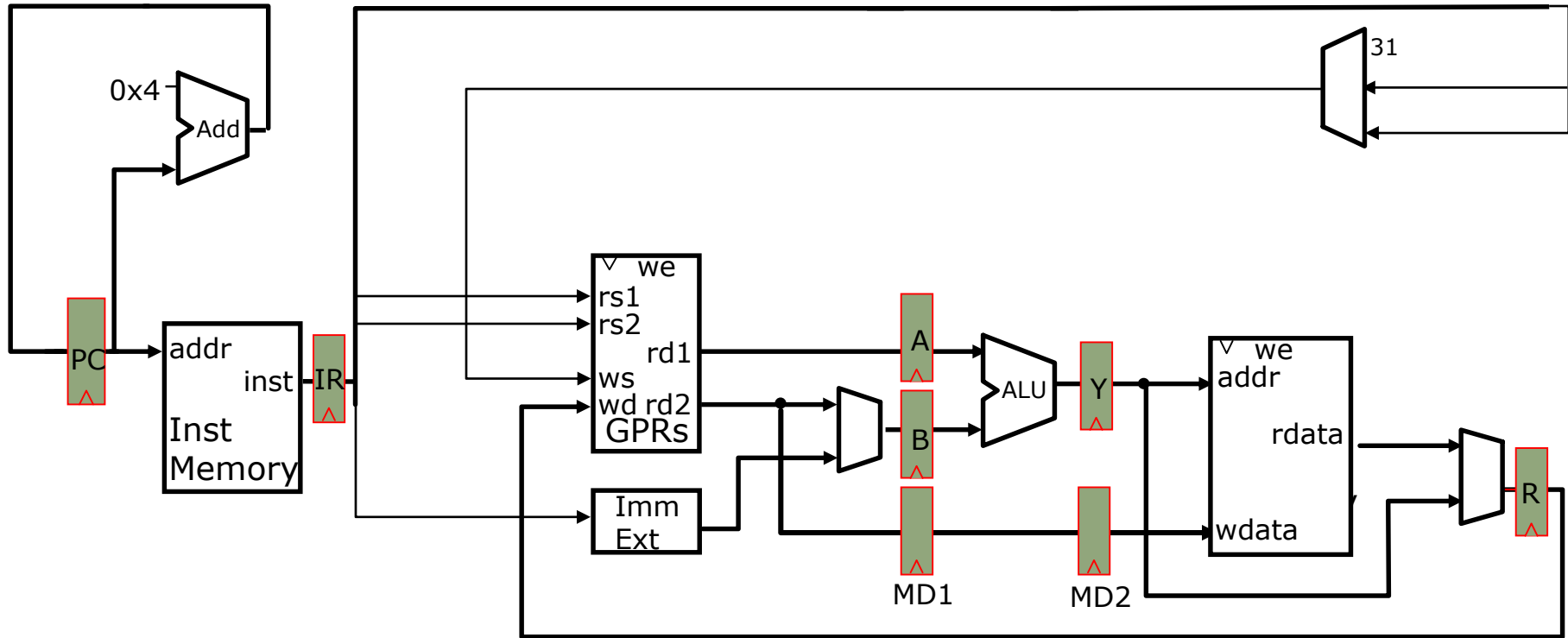
Reminder: Pipelined MIPS Datapath

without jumps

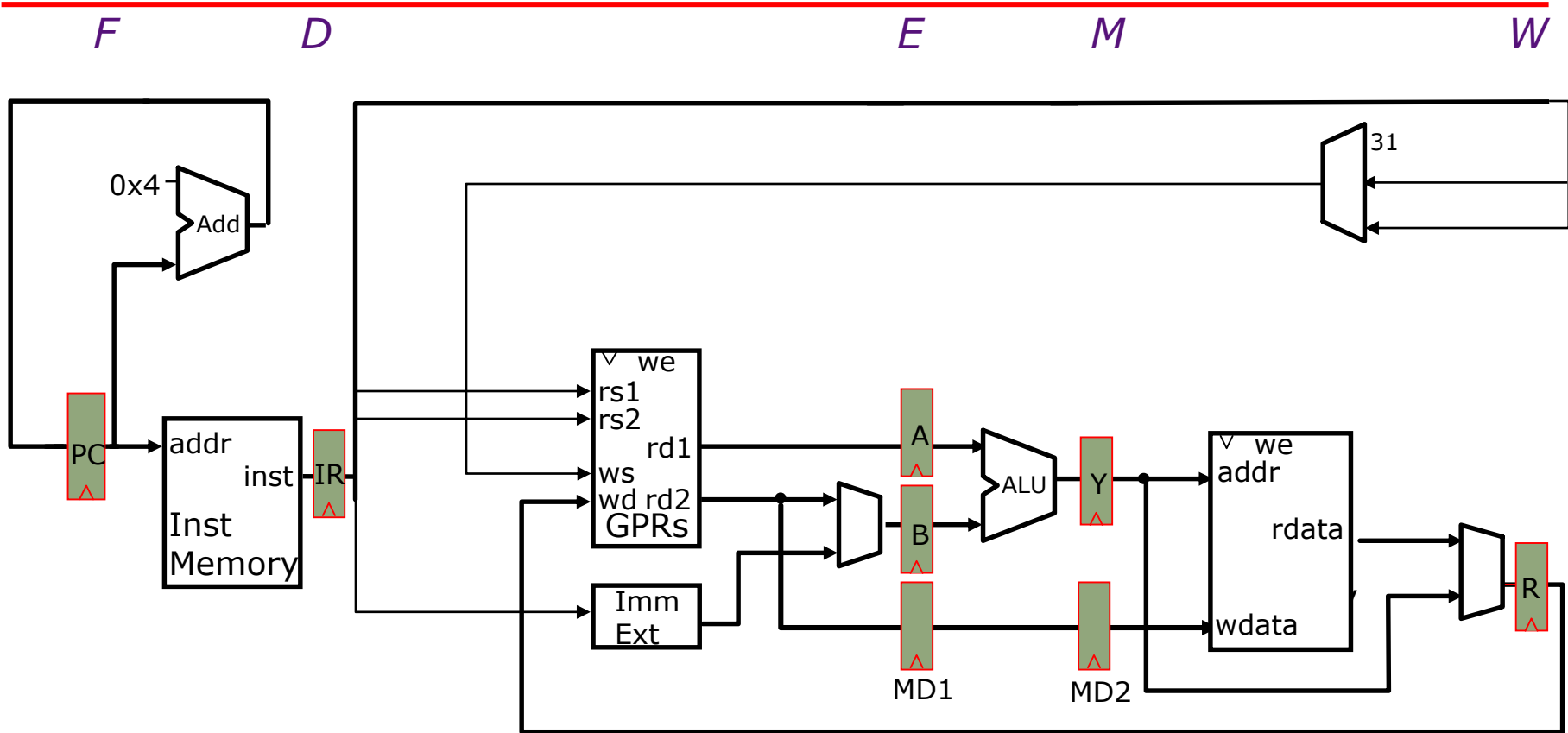


Reminder: Pipelined MIPS Datapath

without jumps

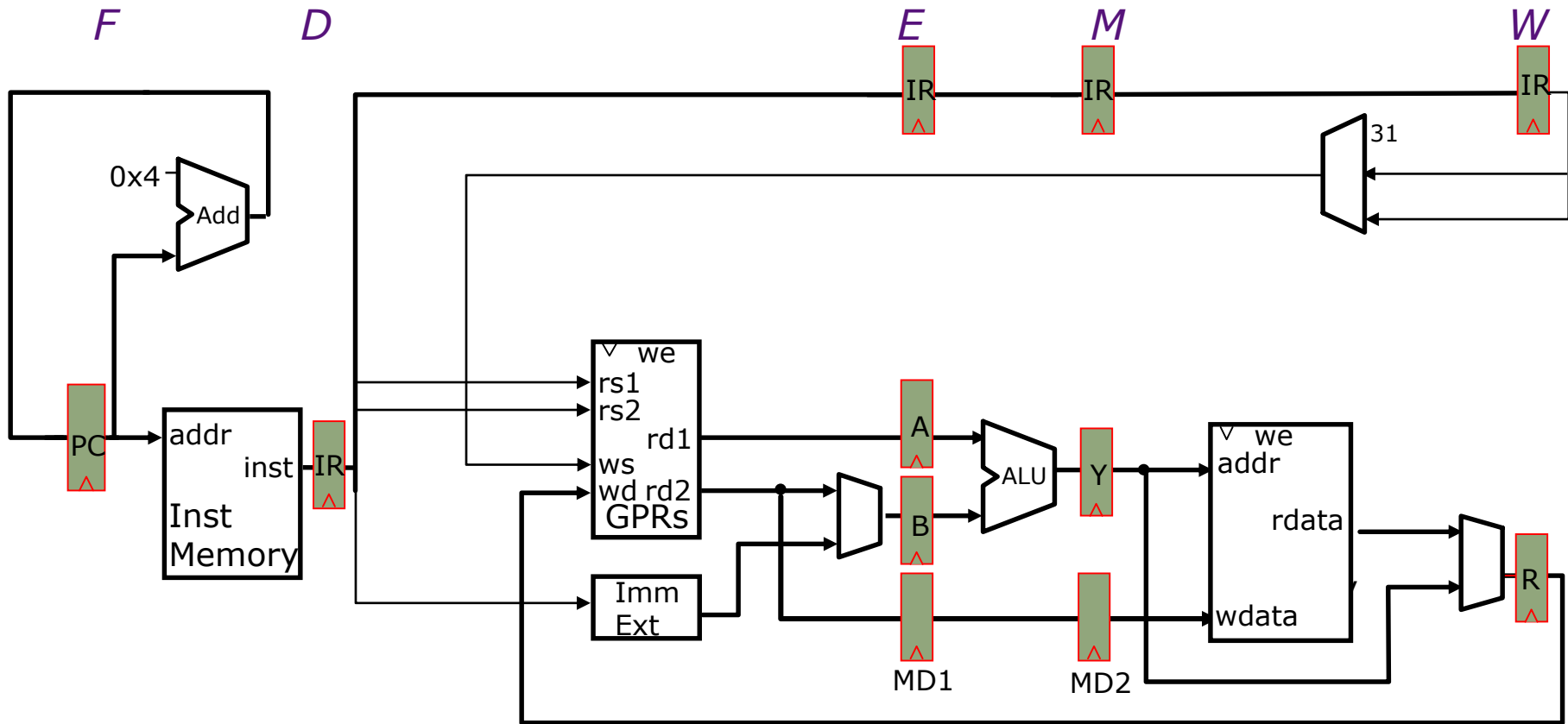


Reminder: Pipelined MIPS Datapath *without jumps*



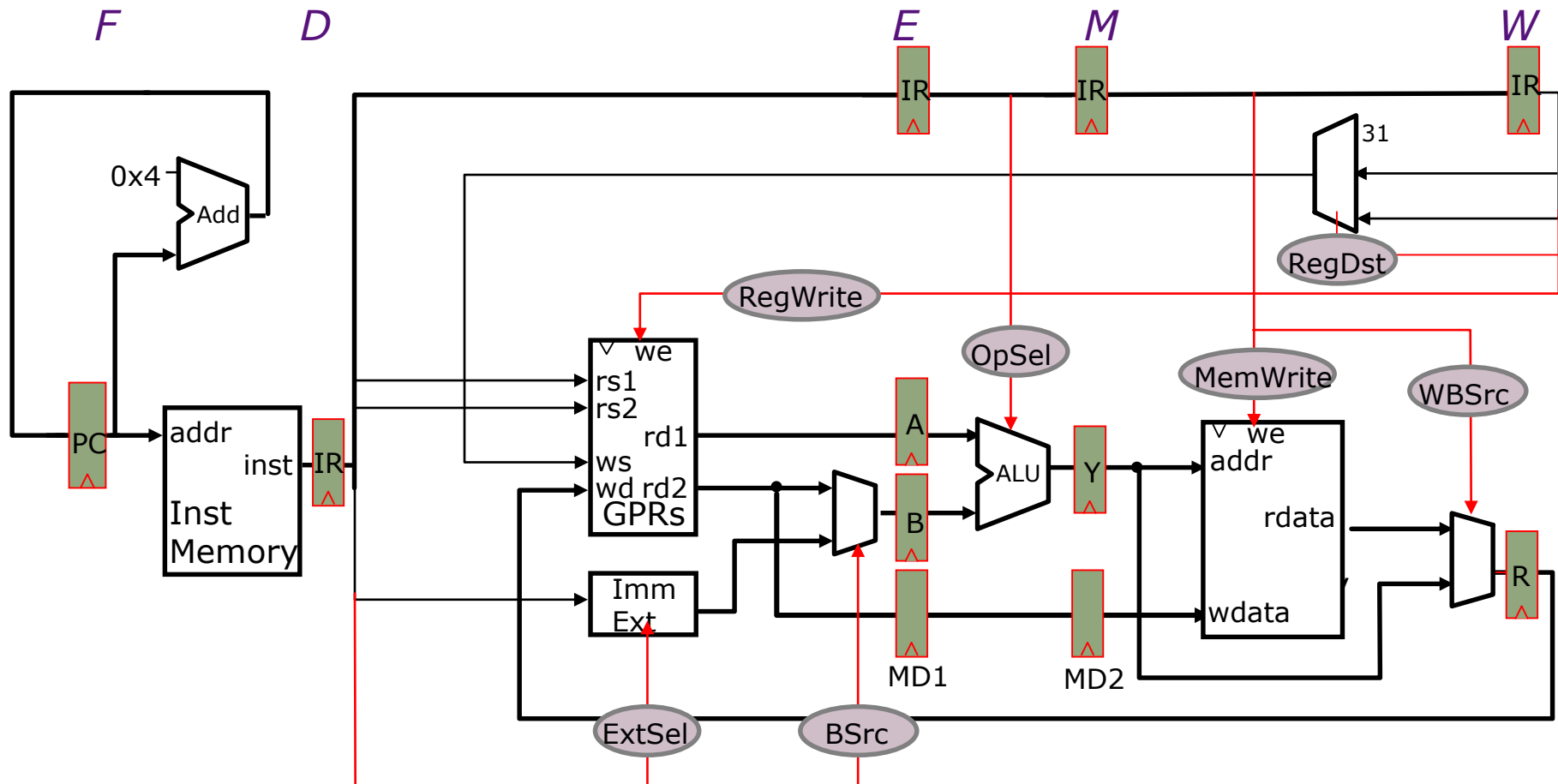
Reminder: Pipelined MIPS Datapath

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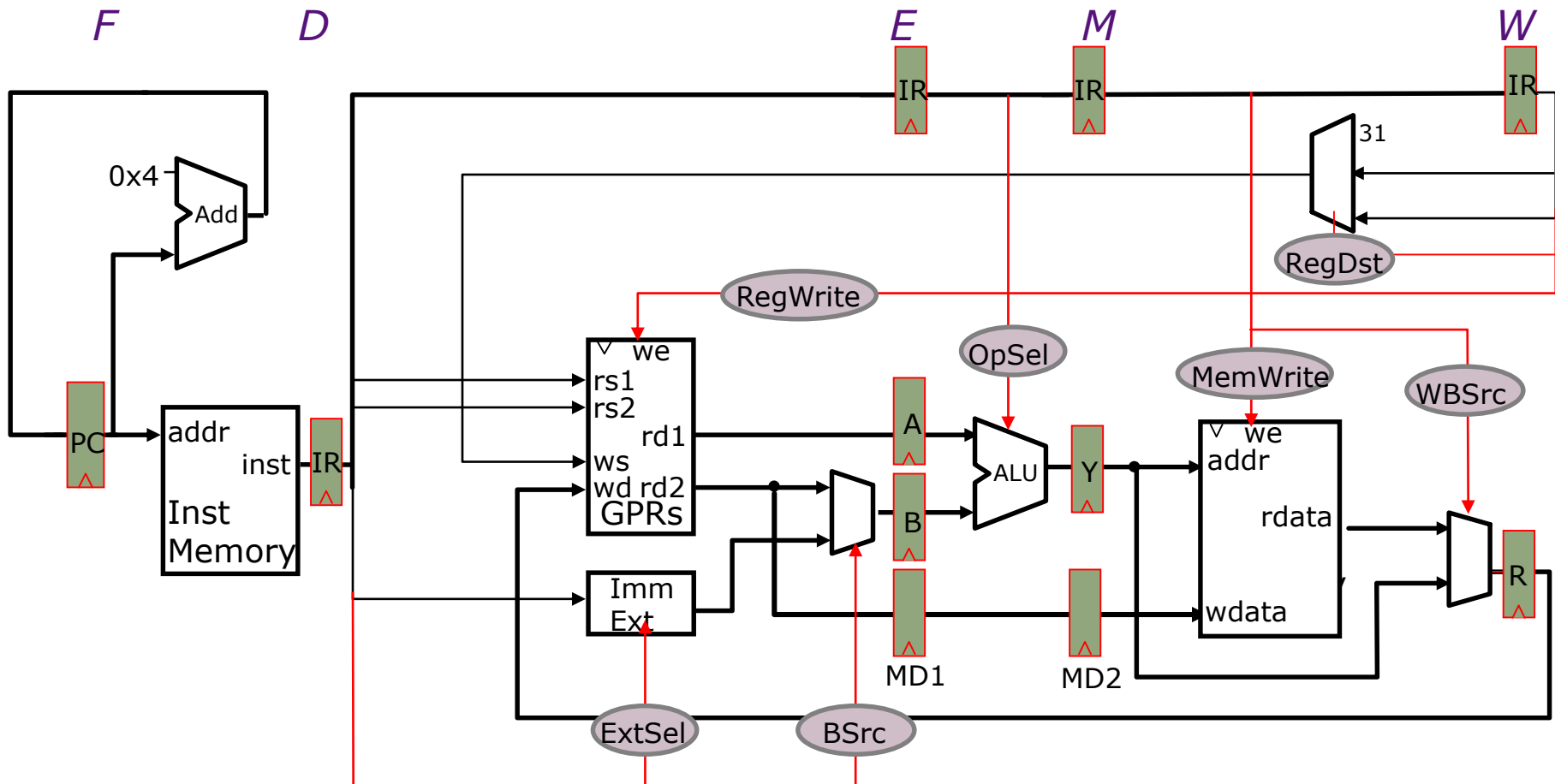


Reminder: Pipelined MIPS Datapath

without jumps



Reminder: Pipelined MIPS Datapath *without jumps*



Pipelining increases clock frequency,
but instruction dependences may increase CPI

How instructions can interact with each other in a pipeline

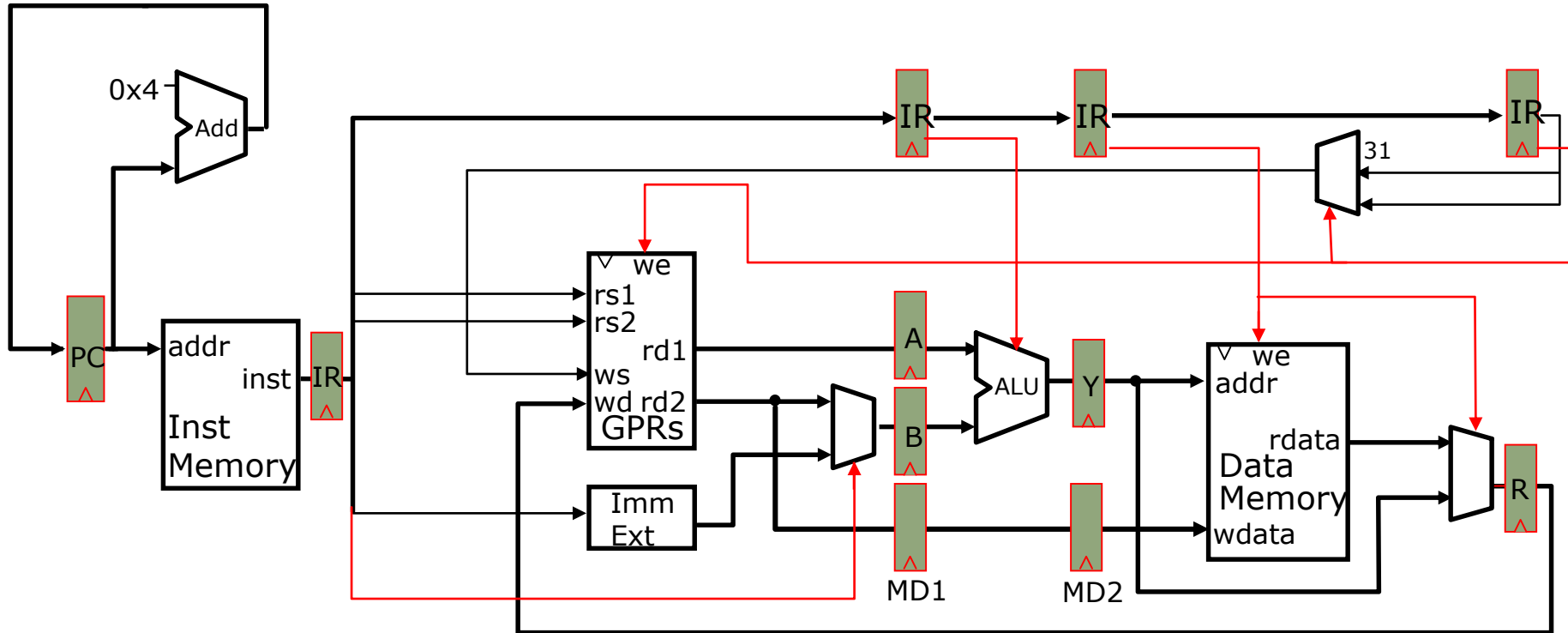
How instructions can interact with each other in a pipeline

- An instruction in the pipeline may need a resource being used by another instruction in the pipeline
→ *structural hazard*

How instructions can interact with each other in a pipeline

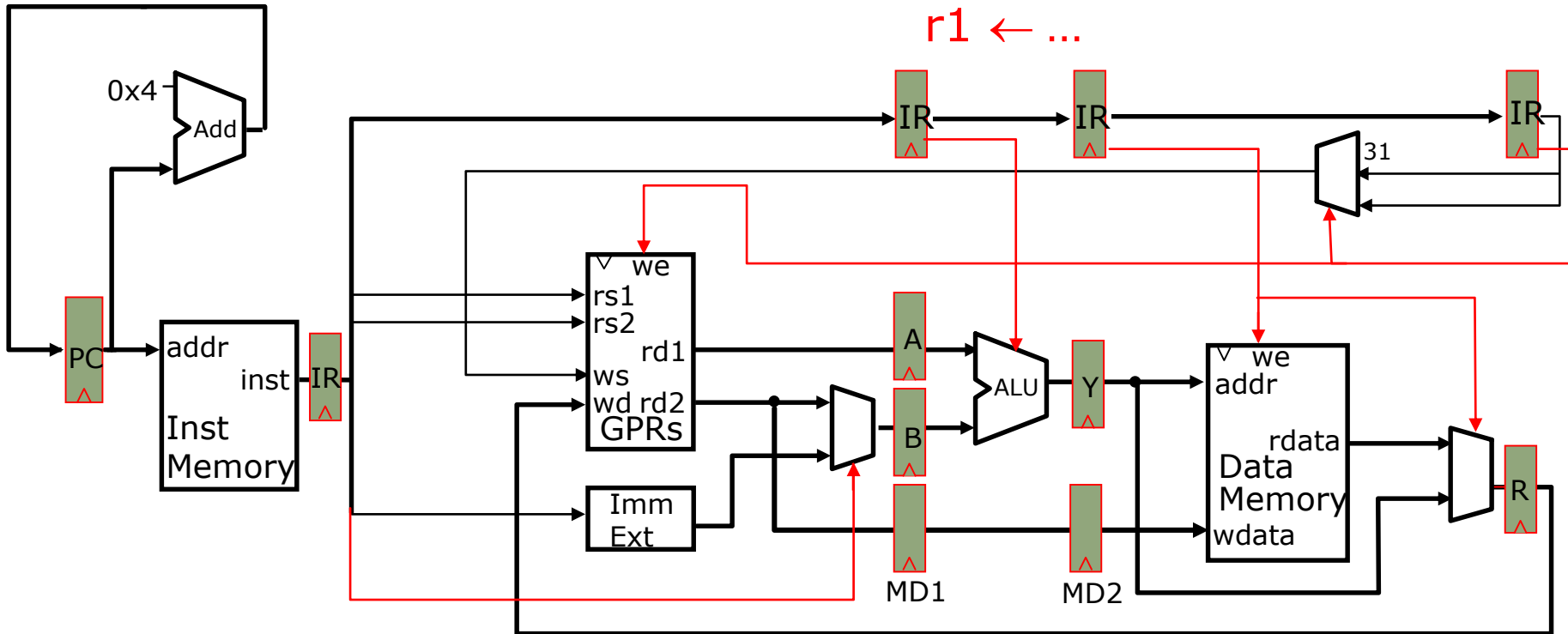
- An instruction in the pipeline may need a resource being used by another instruction in the pipeline
→ *structural hazard*
- An instruction may depend on a value produced by an earlier instruction
 - Dependence may be for a data calculation
→ *data hazard*
 - Dependence may be for calculating the next PC
→ *control hazard (branches, interrupts)*

Data Hazards



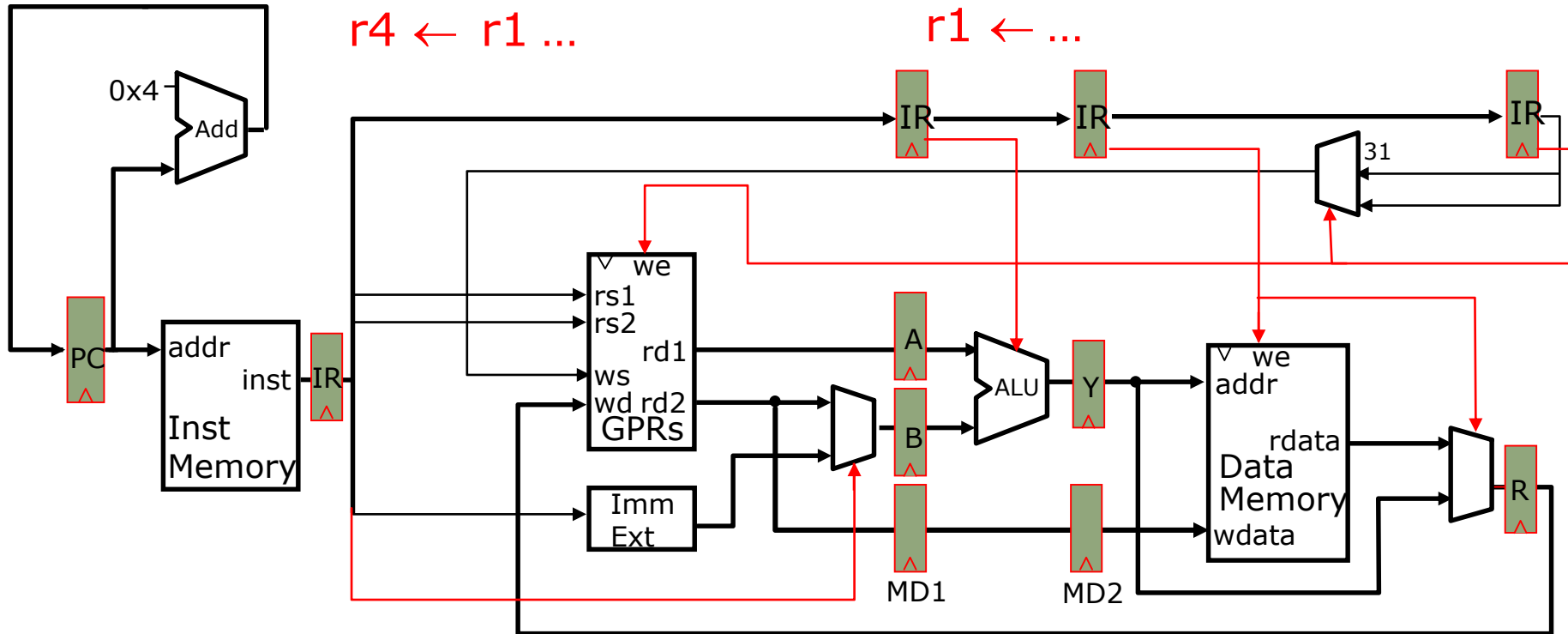
...
 $r1 \leftarrow r0 + 10$
 $r4 \leftarrow r1 + 17$
...

Data Hazards



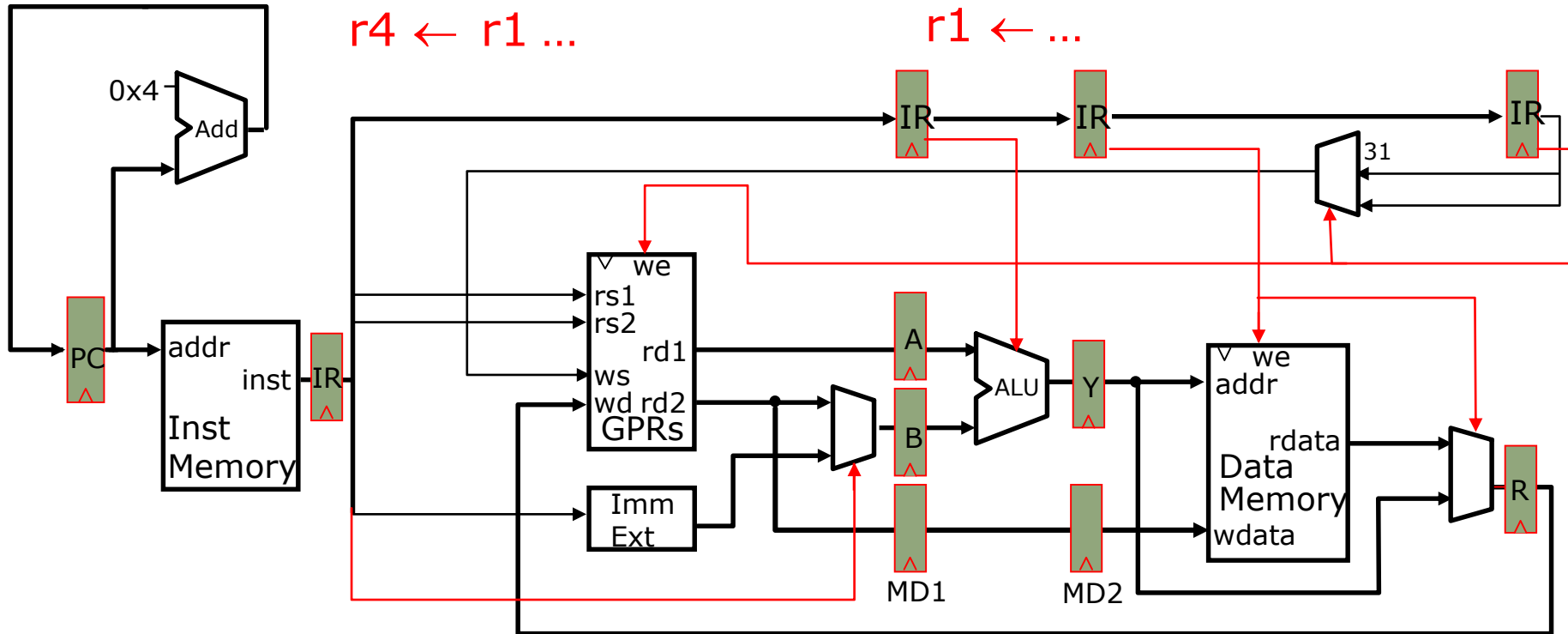
...
 $r1 \leftarrow r0 + 10$
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 ...

Data Hazards



...
 $r1 \leftarrow r0 + 10$
 $r4 \leftarrow r1 + 17$
 ...

Data Hazards



$r4 \leftarrow r1 \dots$

$r1 \leftarrow \dots$

...
 $r1 \leftarrow r0 + 10$
 $r4 \leftarrow r1 + 17$
...

r1 is stale. Oops!

Resolving Data Hazards

Strategy 1: *Wait for the result to be available by freezing earlier pipeline stages* → *stall*

Strategy 2: *Route data as soon as possible after it is calculated to the earlier pipeline stage* → *bypass*

Strategy 3: *Speculate on the dependence*
Two cases:

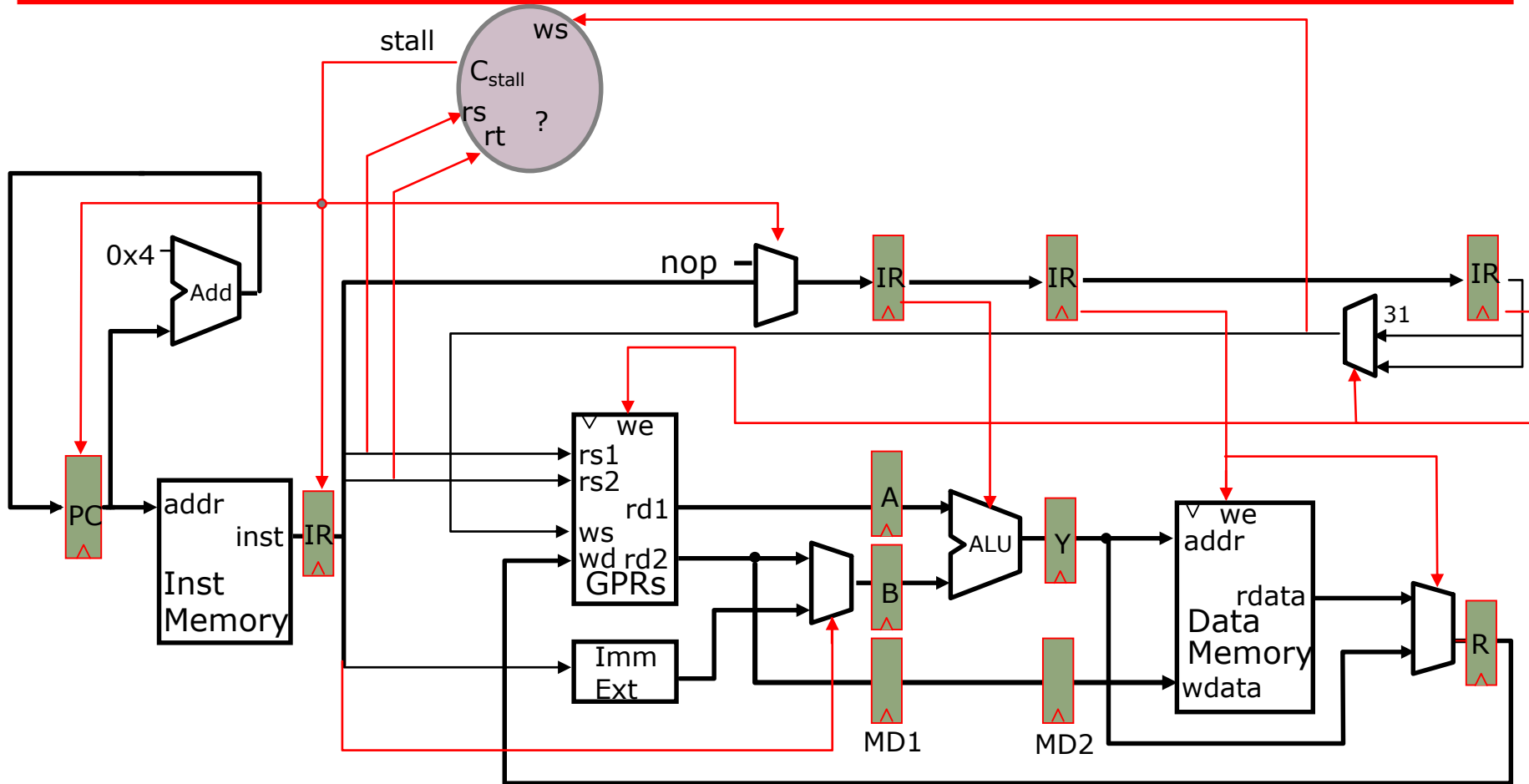
Guessed correctly → no special action required
Guessed incorrectly → kill and restart

Resolving Data Hazards

Strategy 1: *Wait for the result to be available by freezing earlier pipeline stages → stall*

Reminder: Stall Control Logic

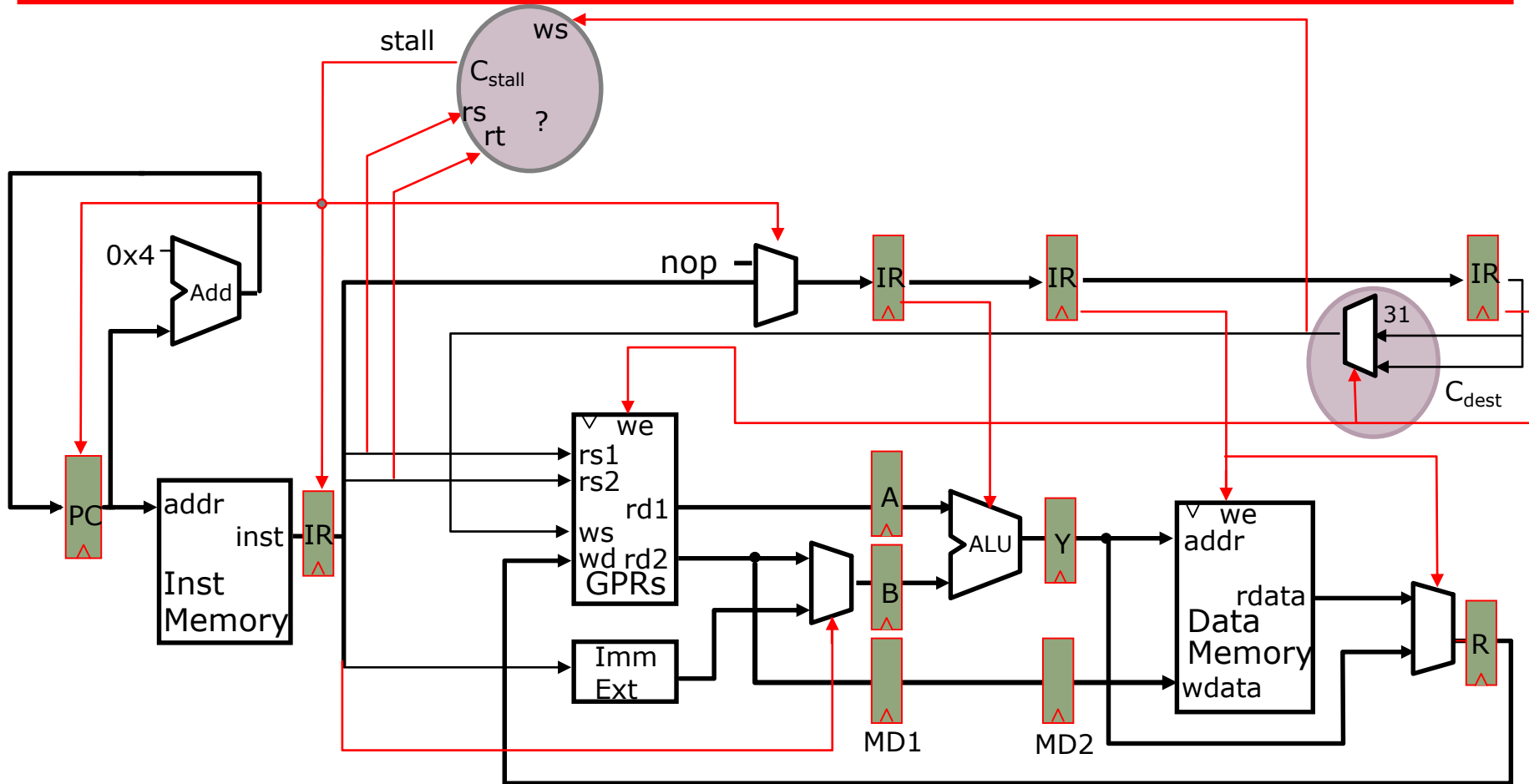
ignoring jumps & branches



Stall DEC & IF when instruction in DEC reads a register that is written by any earlier in-flight instruction (in EXE, MEM, or WB)

Reminder: Stall Control Logic

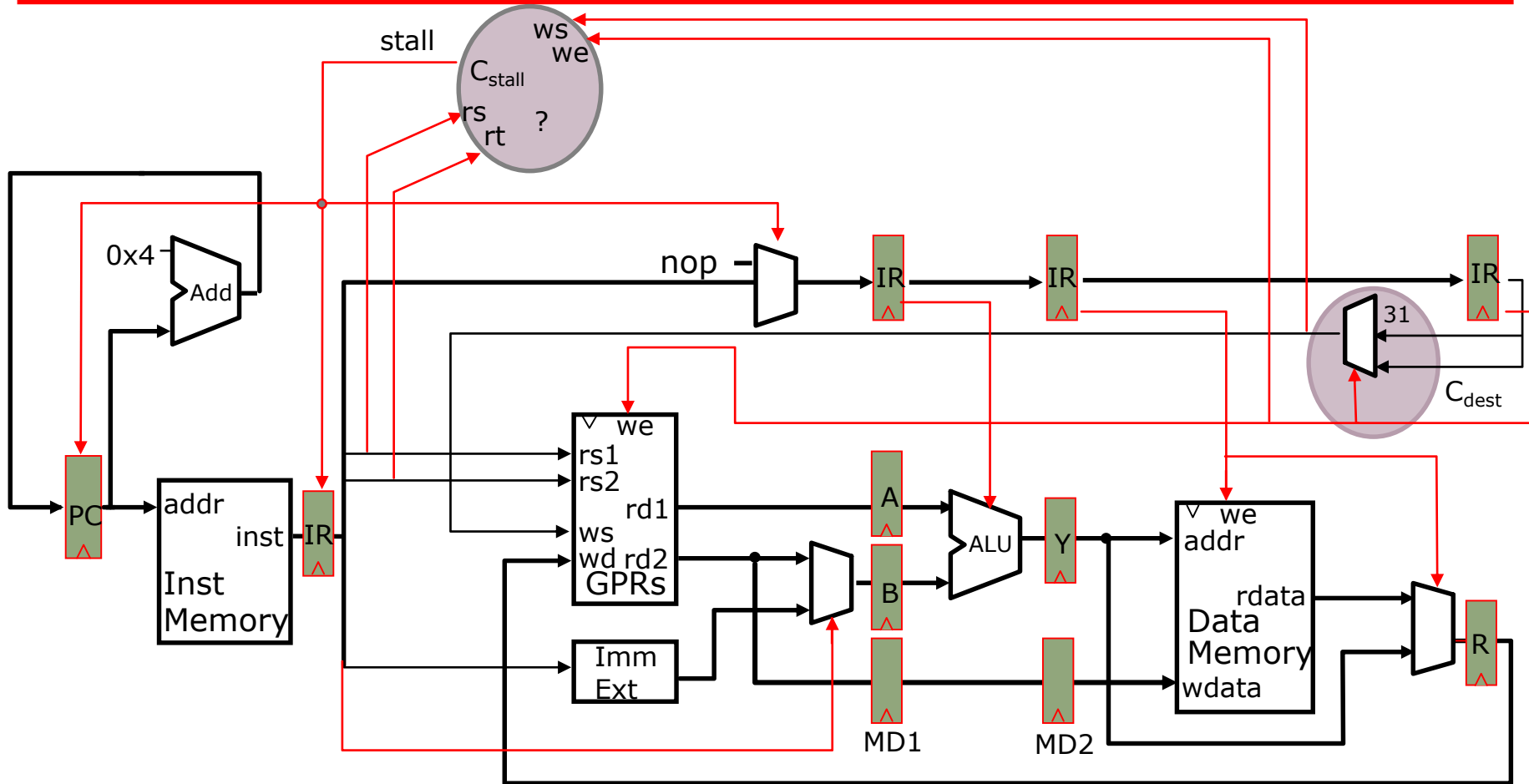
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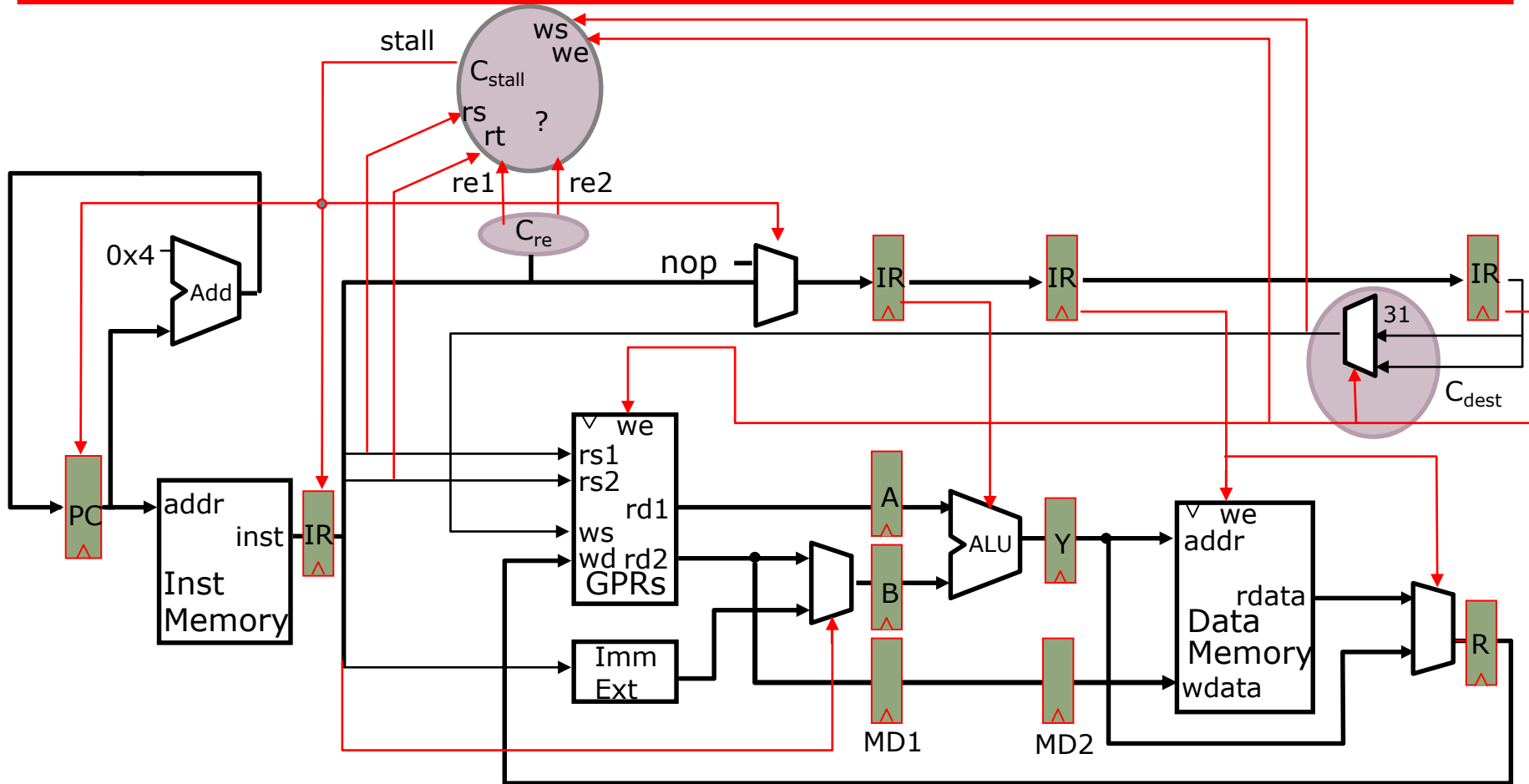
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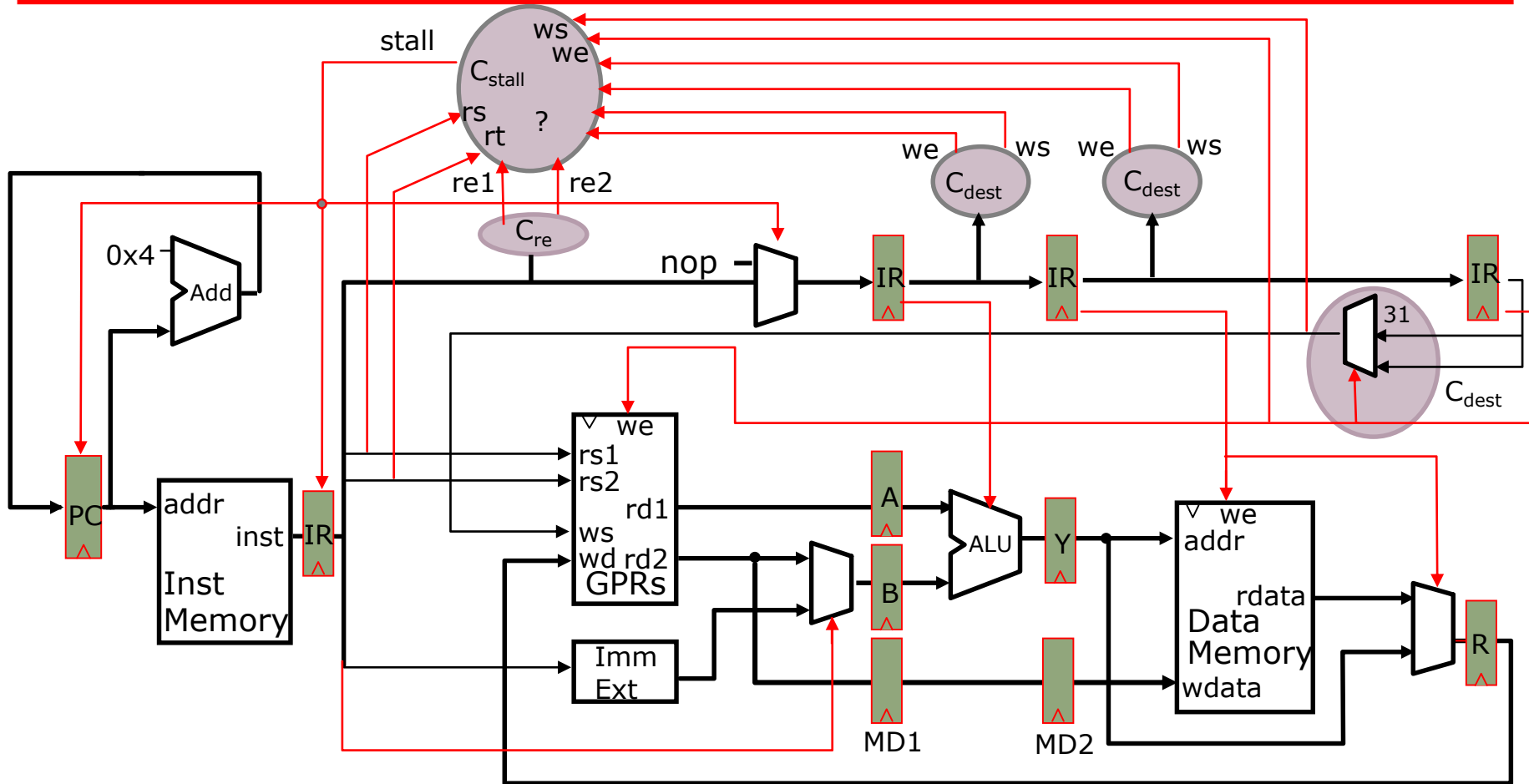
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Reminder: Stall Control Logic

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Stall DEC & IF when instruction in DEC reads a register that is written by any earlier in-flight instruction (in EXE, MEM, or WB)

Source & Destination Registers



source(s) destination

ALU	$rd \leftarrow (rs) \text{ func } (rt)$	rs, rt	rd
ALUi	$rt \leftarrow (rs) \text{ op } \text{imm}$	rs	rt
LW	$rt \leftarrow M [(rs) + \text{imm}]$	rs	rt
SW	$M [(rs) + \text{imm}] \leftarrow (rt)$	rs, rt	
BZ	<i>cond</i> (rs)		
	<i>true:</i> $PC \leftarrow (PC) + \text{imm}$	rs	
	<i>false:</i> $PC \leftarrow (PC) + 4$	rs	
J	$PC \leftarrow (PC) + \text{imm}$		
JAL	$r31 \leftarrow (PC), PC \leftarrow (PC) + \text{imm}$		31
JR	$PC \leftarrow (rs)$	rs	
JALR	$r31 \leftarrow (PC), PC \leftarrow (rs)$	rs	31

Deriving the Stall Signal

Deriving the Stall Signal

C_{dest}

$ws = \text{Case opcode}$

ALU $\Rightarrow rd$

ALUi, LW $\Rightarrow rt$

JAL, JALR $\Rightarrow R31$

$we = \text{Case opcode}$

ALU, ALUi, LW $\Rightarrow (ws \neq 0)$

JAL, JALR $\Rightarrow on$

... $\Rightarrow off$

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... $\Rightarrow \text{off}$

C_{re}

$re1 = \text{Case opcode}$

ALU, ALUi,

$\Rightarrow \text{on}$

$\Rightarrow \text{off}$

$re2 = \text{Case opcode}$

$\Rightarrow \text{on}$

$\Rightarrow \text{off}$

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LW, SW, BZ,
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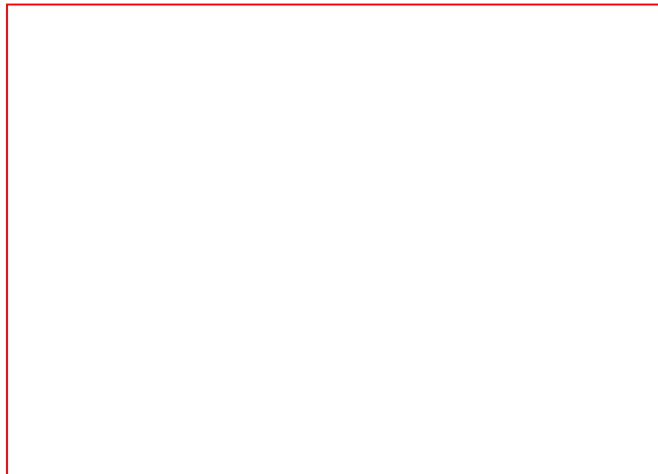
C_{re}

$re1 = \text{Case opcode}$

ALU, ALUi,
LW, SW, BZ,
JR, JALR $\Rightarrow \text{on}$
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ALU, SW $\Rightarrow \text{on}$
... $\Rightarrow \text{off}$

C_{stall}

Deriving the Stall Signal

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ALUi, LW $\Rightarrow rt$
JAL, JALR $\Rightarrow R31$

$we = \text{Case opcode}$

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JAL, JALR $\Rightarrow \text{on}$
... $\Rightarrow \text{off}$

C_{re}

$re1 = \text{Case opcode}$

ALU, ALUi,
LW, SW, BZ,
JR, JALR $\Rightarrow \text{on}$
J, JAL $\Rightarrow \text{off}$

$re2 = \text{Case opcode}$

ALU, SW $\Rightarrow \text{on}$
... $\Rightarrow \text{off}$

C_{stall}

$$\text{stall} = ((rs_D == ws_E) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D +$$

Deriving the Stall Signal

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C_{re}

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ALU, ALUi,
LW, SW, BZ,
JR, JALR $\Rightarrow on$
J, JAL $\Rightarrow off$

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ALU, SW $\Rightarrow on$
... $\Rightarrow off$

C_{stall}

$$\begin{aligned} \text{stall} = & ((rs_D == ws_E) \cdot we_E + \\ & (rs_D == ws_M) \cdot we_M + \\ & (rs_D == ws_W) \cdot we_W) \cdot re1_D + \\ & ((rt_D == ws_E) \cdot we_E + \\ & (rt_D == ws_M) \cdot we_M + \\ & (rt_D == ws_W) \cdot we_W) \cdot re2_D \end{aligned}$$

Deriving the Stall Signal

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 ALUi, LW $\Rightarrow rt$
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$re2 = \text{Case opcode}$

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 ... $\Rightarrow off$

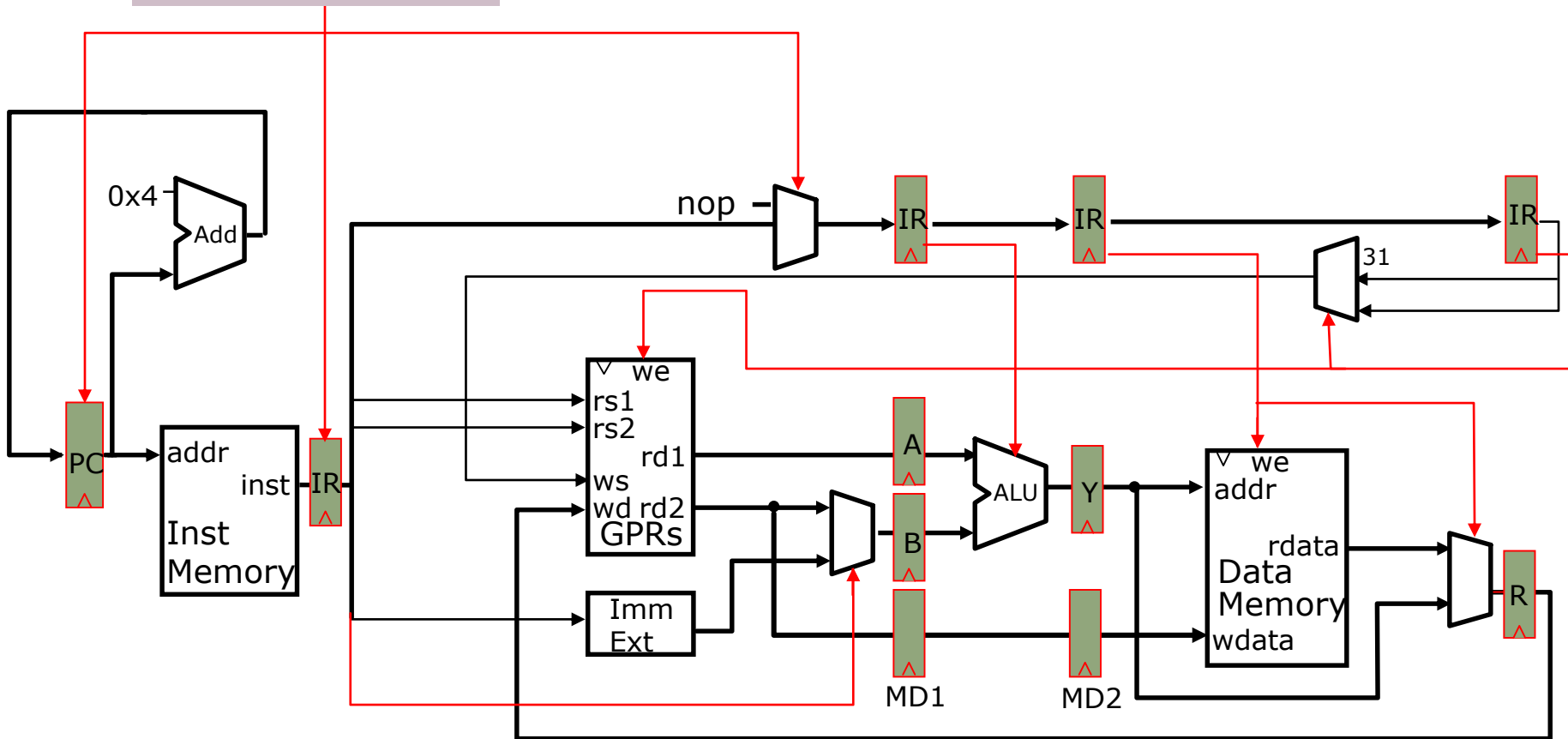
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$$\begin{aligned} \text{stall} = & ((rs_D == ws_E) \cdot we_E + \\ & (rs_D == ws_M) \cdot we_M + \\ & (rs_D == ws_W) \cdot we_W) \cdot re1_D + \\ & ((rt_D == ws_E) \cdot we_E + \\ & (rt_D == ws_M) \cdot we_M + \\ & (rt_D == ws_W) \cdot we_W) \cdot re2_D \end{aligned}$$

*This is not
the full story!*

Hazards due to Loads & Stores

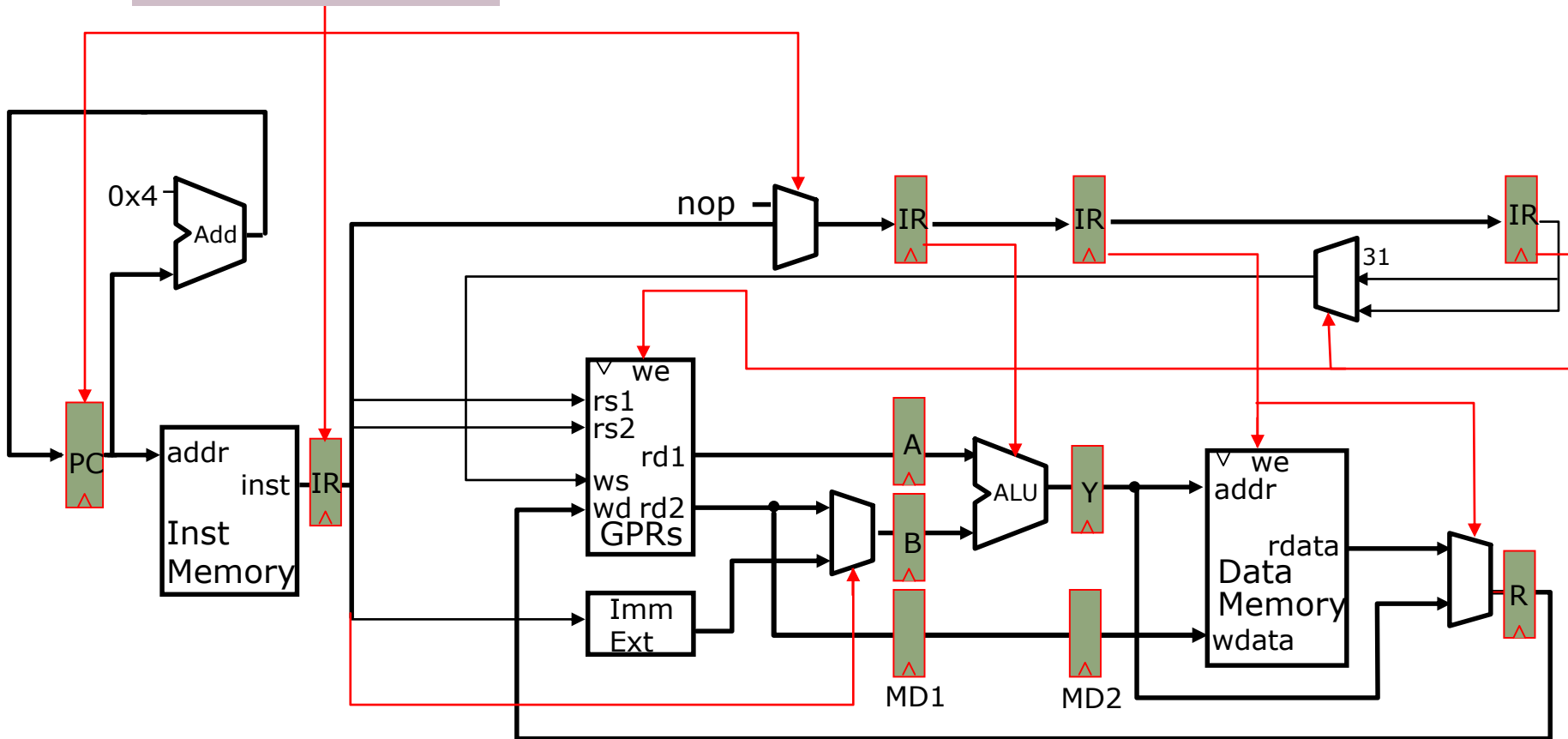
Stall Condition



...
 $M[(r1)+7] \leftarrow (r2)$
 $r4 \leftarrow M[(r3)+5]$

Hazards due to Loads & Stores

Stall Condition



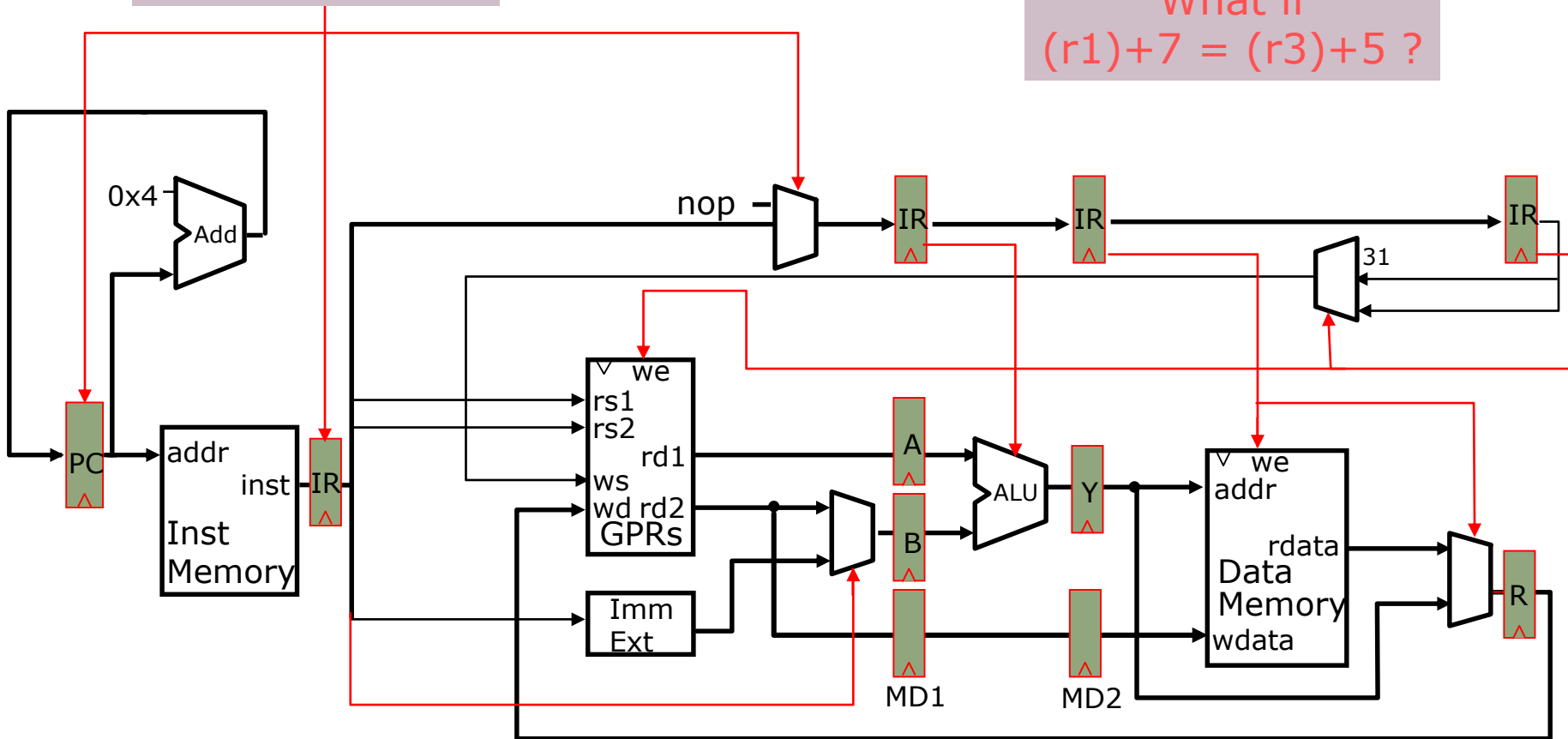
...
 $M[(r1)+7] \leftarrow (r2)$
 $r4 \leftarrow M[(r3)+5]$

Is there any possible data hazard in this instruction sequence?

Hazards due to Loads & Stores

Stall Condition

What if
 $(r1)+7 = (r3)+5$?



...
 $M[(r1)+7] \leftarrow (r2)$
 $r4 \leftarrow M[(r3)+5]$

*Is there any possible data hazard
in this instruction sequence?*

Load & Store Hazards

```
...  
M[(r1)+7] ← (r2)  
r4 ← M[(r3)+5]  
...
```

$(r1)+7 = (r3)+5 \Rightarrow$ *data hazard*

Load & Store Hazards

```
...  
M[(r1)+7] ← (r2)  
r4 ← M[(r3)+5]  
...
```

$(r1)+7 = (r3)+5 \Rightarrow$ *data hazard*

However, the hazard is avoided because *our memory system completes writes in one cycle!*

Load & Store Hazards

```
...  
M[(r1)+7] ← (r2)  
r4 ← M[(r3)+5]  
...
```

$(r1)+7 = (r3)+5 \Rightarrow \textit{data hazard}$

However, the hazard is avoided because *our memory system completes writes in one cycle!*

Load/Store hazards are sometimes resolved in the pipeline and sometimes in the memory system itself.

Load & Store Hazards

```
...  
M[(r1)+7] ← (r2)  
r4 ← M[(r3)+5]  
...
```

$(r1)+7 = (r3)+5 \Rightarrow$ *data hazard*

However, the hazard is avoided because *our memory system completes writes in one cycle!*

Load/Store hazards are sometimes resolved in the pipeline and sometimes in the memory system itself.

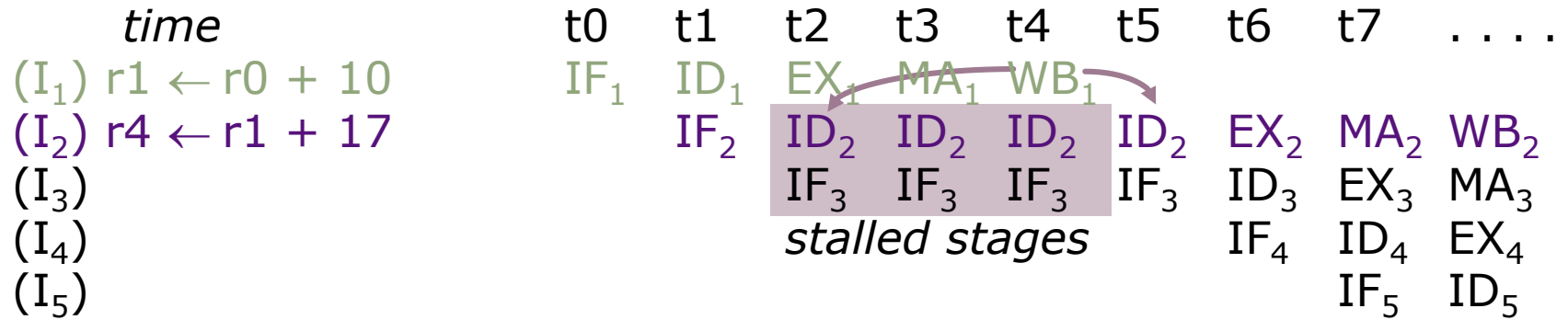
More on this later in the course.

Resolving Data Hazards (2)

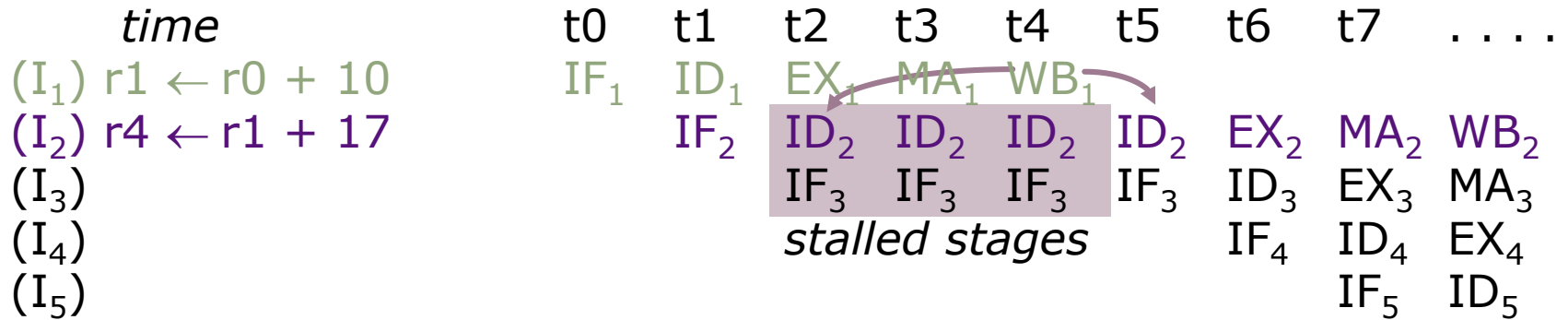
Strategy 2:

Route data as soon as possible after it is calculated to the earlier pipeline stage → *bypass*

Bypassing

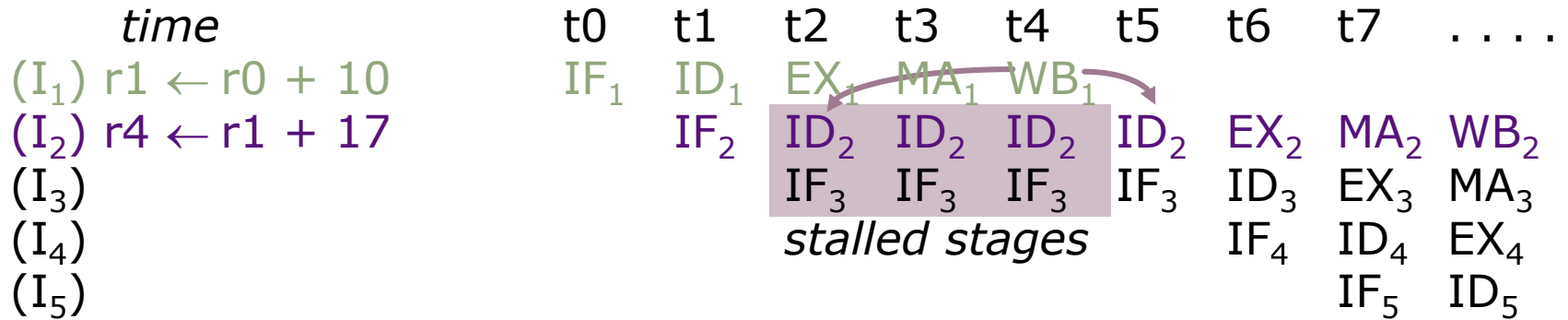


Bypassing



Each *stall or kill* introduces a bubble $\Rightarrow CPI > 1$

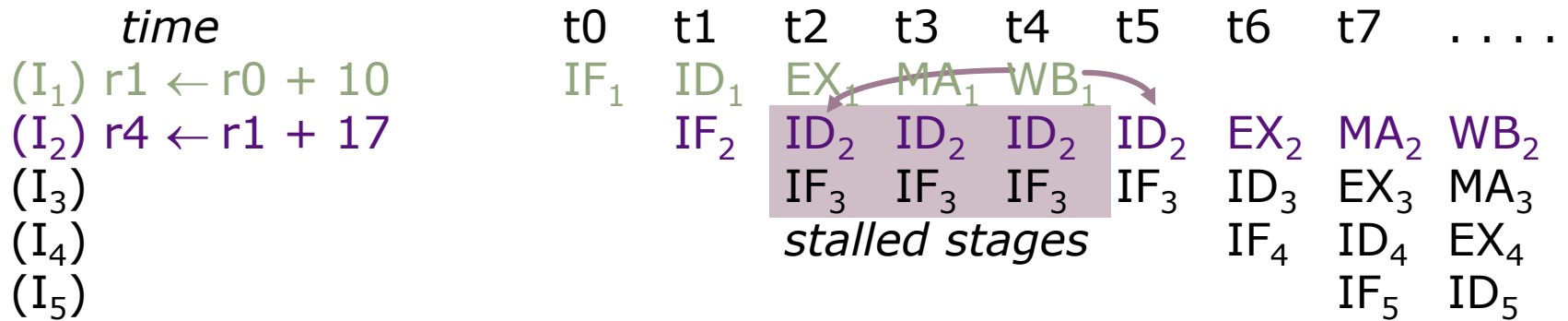
Bypassing



Each *stall or kill* introduces a bubble $\Rightarrow CPI > 1$

When is data actually available?

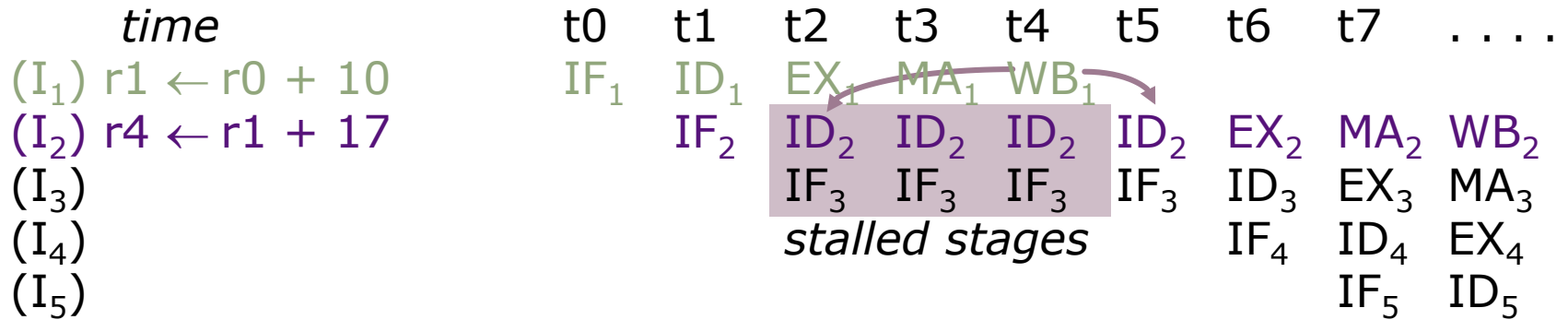
Bypassing



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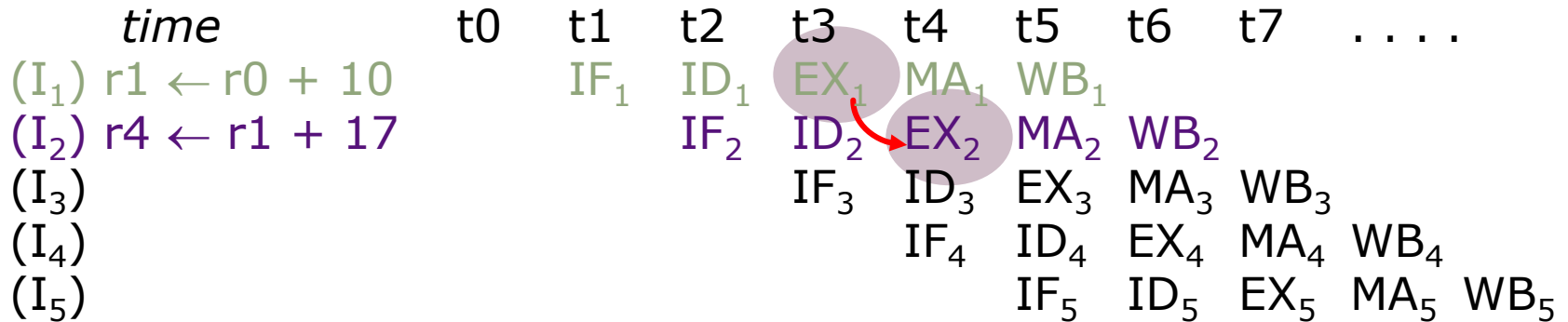
When is data actually available? **At Execute**

Bypassing

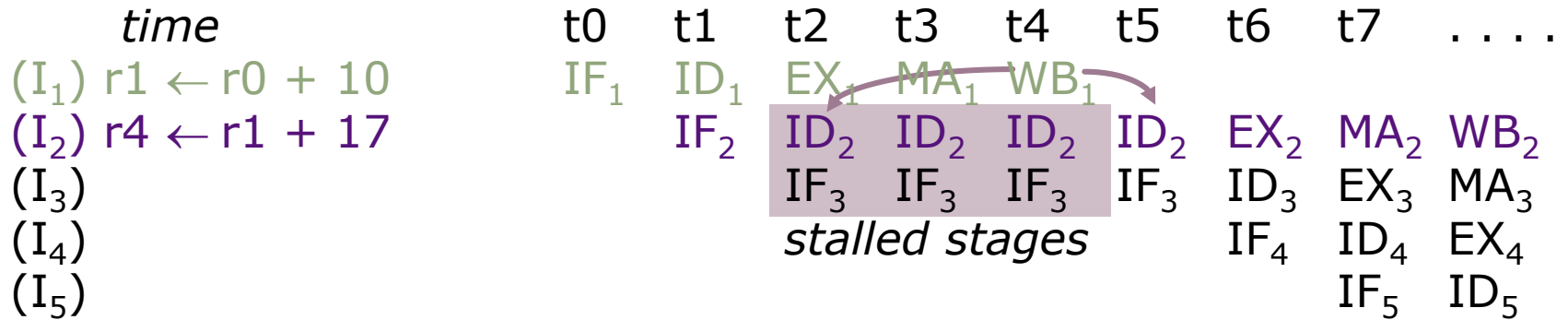


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When is data actually available? **At Execute**

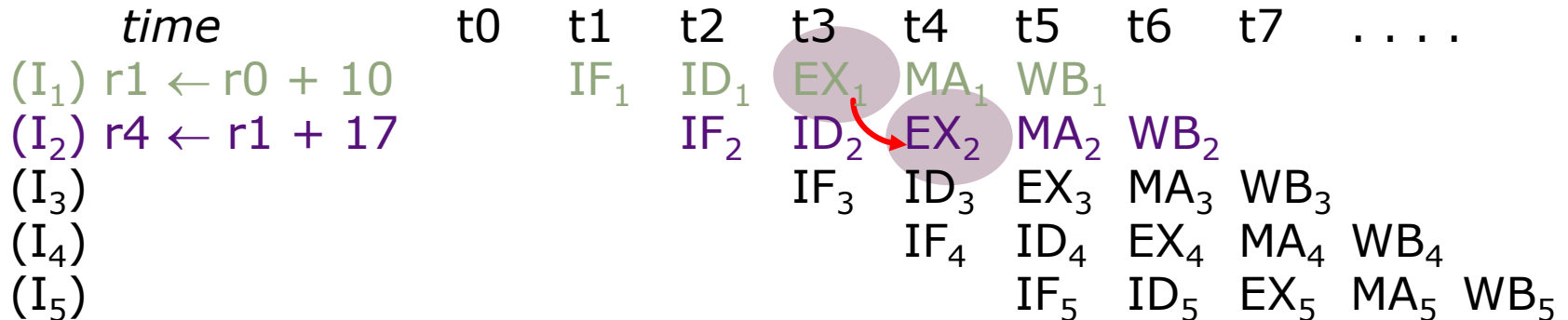


Bypassing



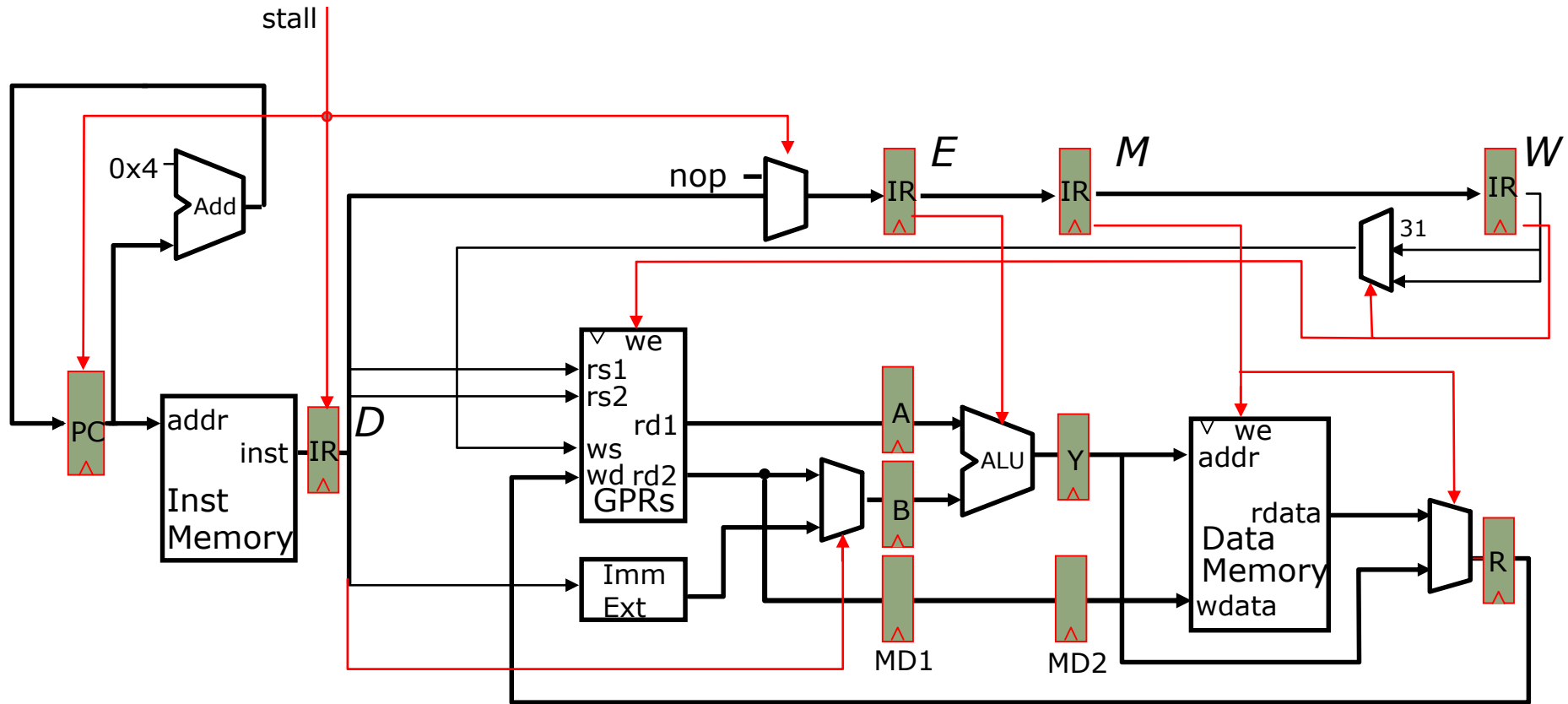
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When is data actually available? **At Execute**

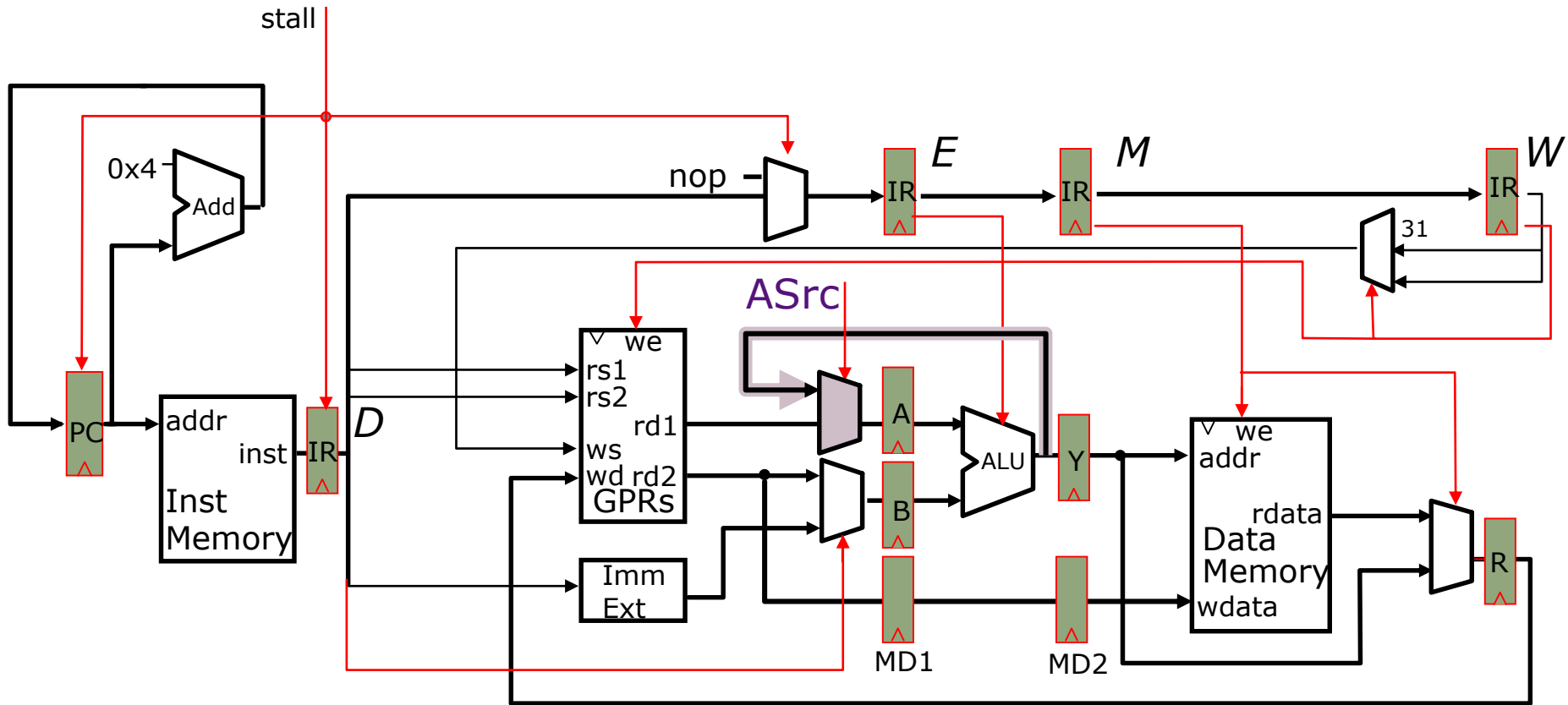


A new datapath, i.e., a *bypass*, can get the data from the output of the ALU to its input

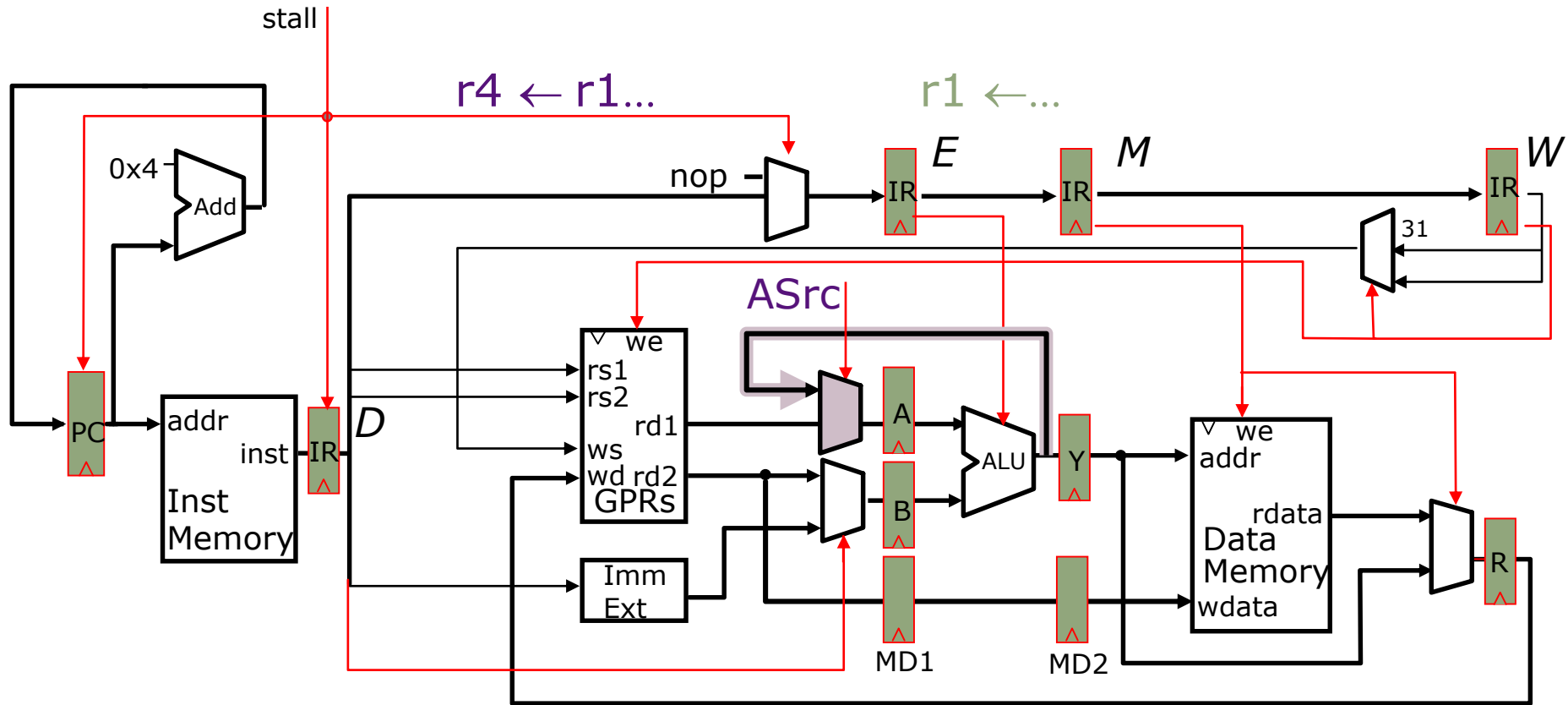
Adding a Bypass



Adding a Bypass



Adding a Bypass

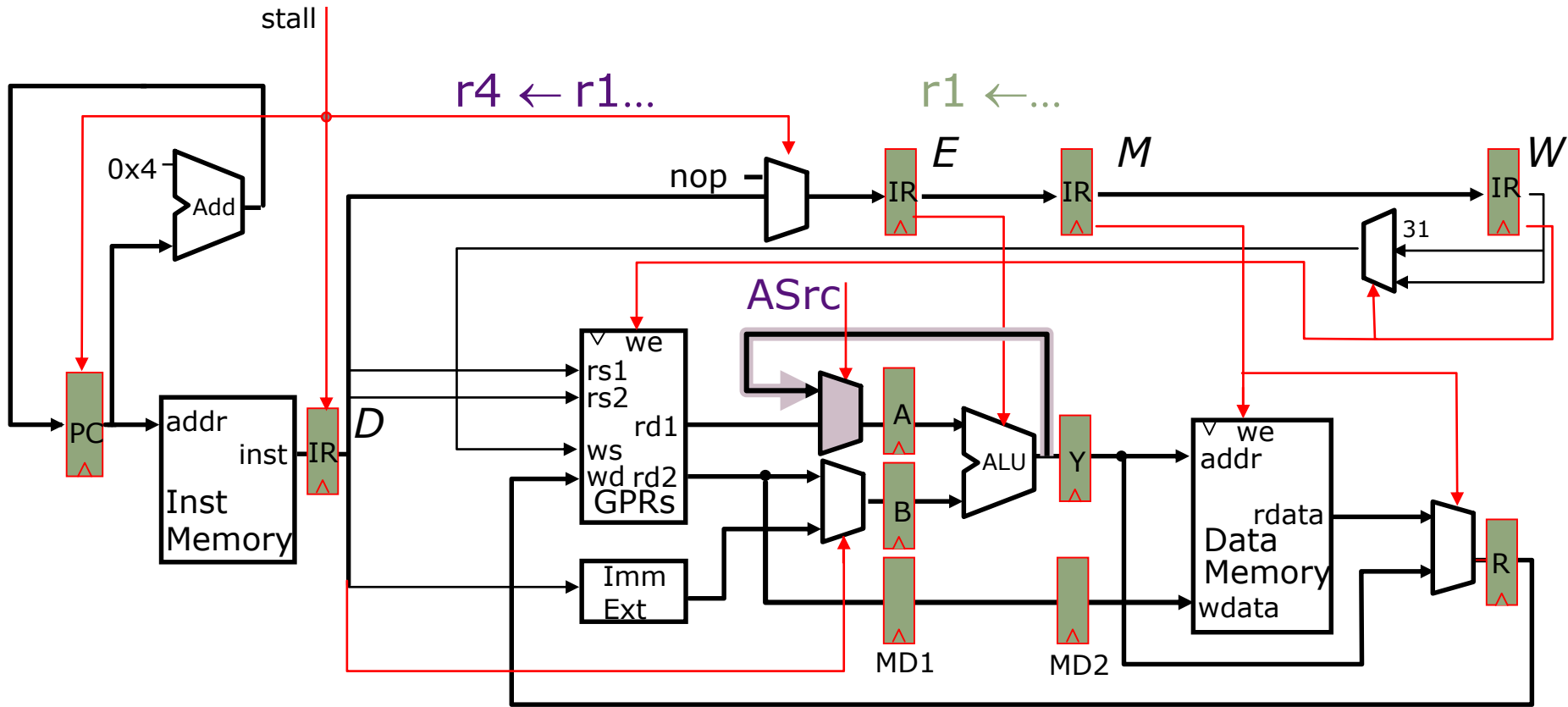


$r4 \leftarrow r1 \dots$

$r1 \leftarrow \dots$

- ...
- (I₁) $r1 \leftarrow r0 + 10$
 - (I₂) $r4 \leftarrow r1 + 17$

Adding a Bypass



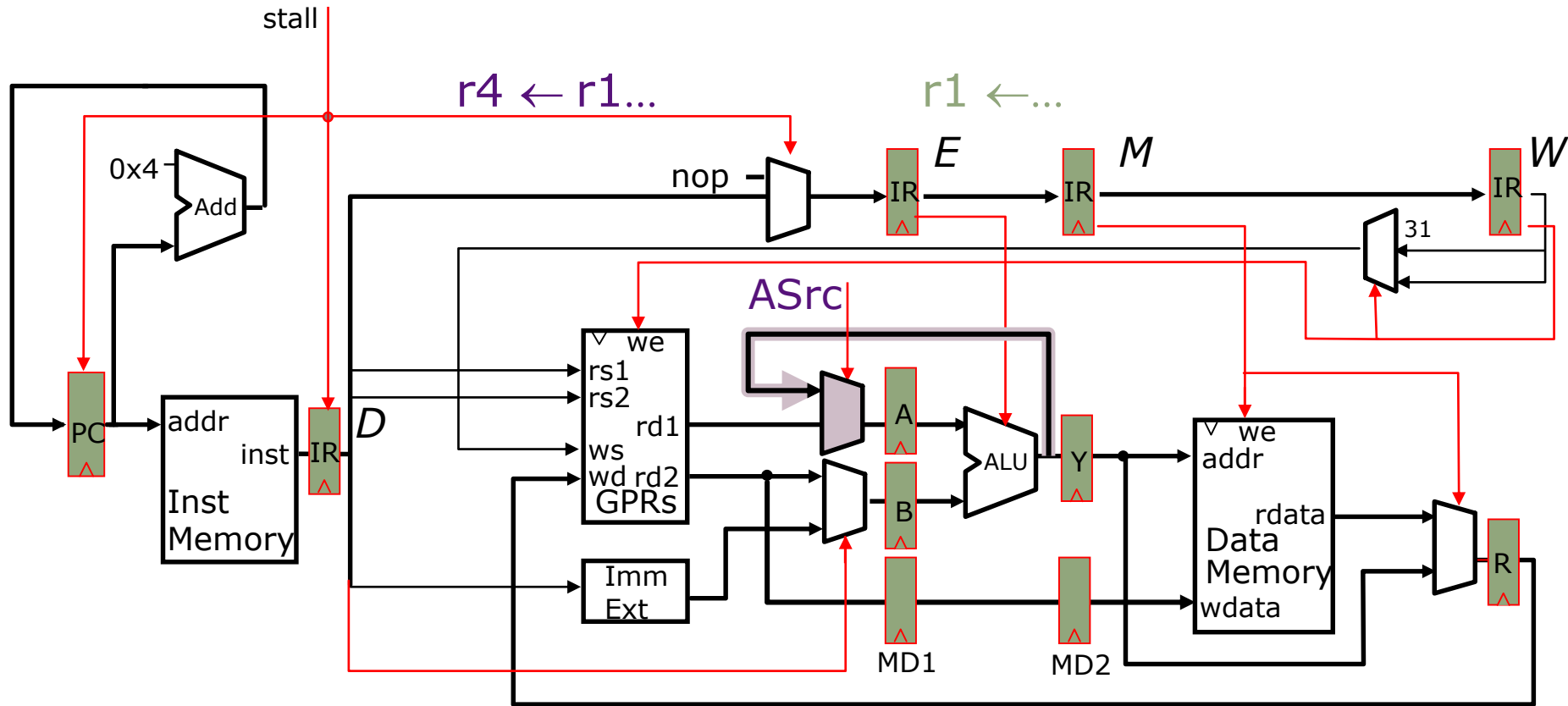
When does this bypass help?

...

(I₁) $r1 \leftarrow r0 + 10$

(I₂) $r4 \leftarrow r1 + 17$

Adding a Bypass



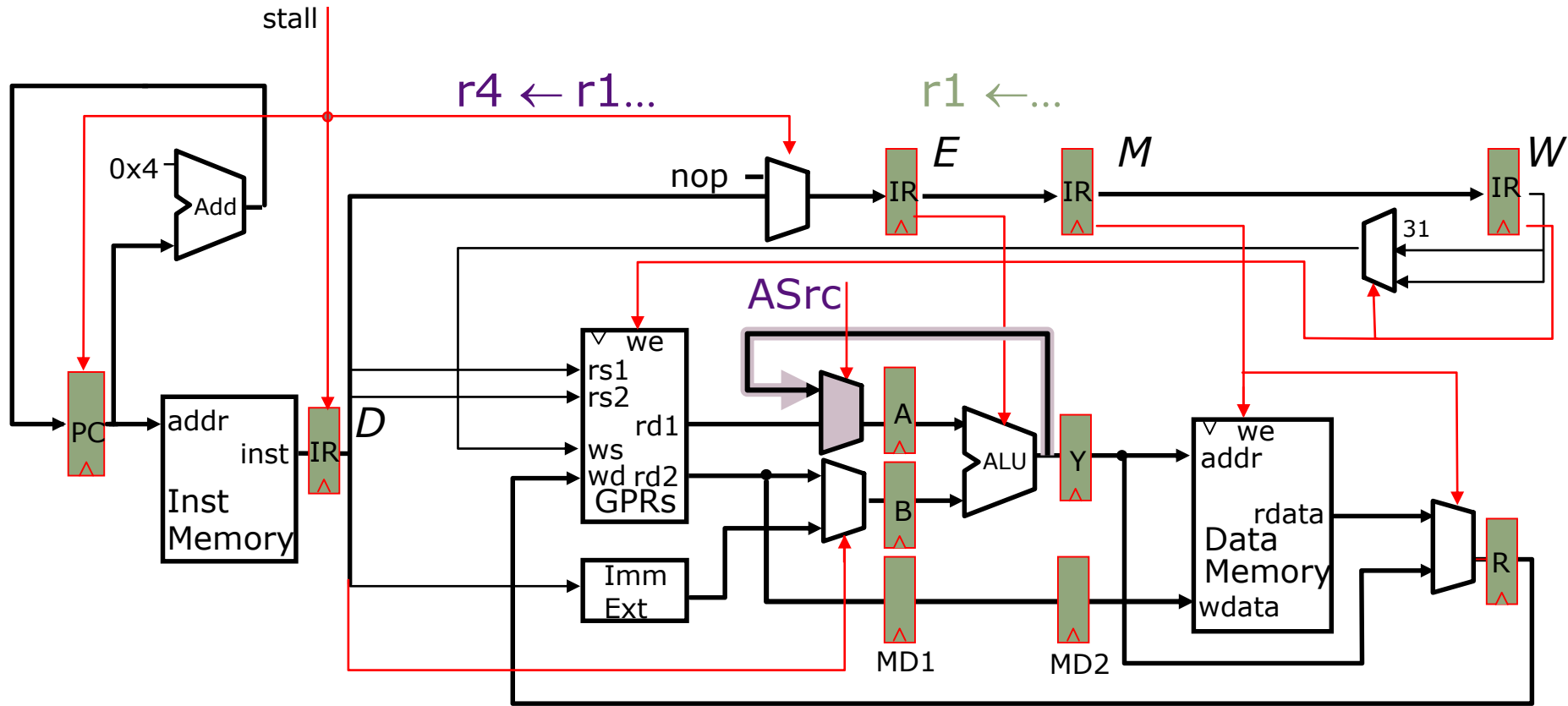
When does this bypass help?

...

(I₁) $r1 \leftarrow r0 + 10$

(I₂) $r4 \leftarrow r1 + 17$
yes

Adding a Bypass

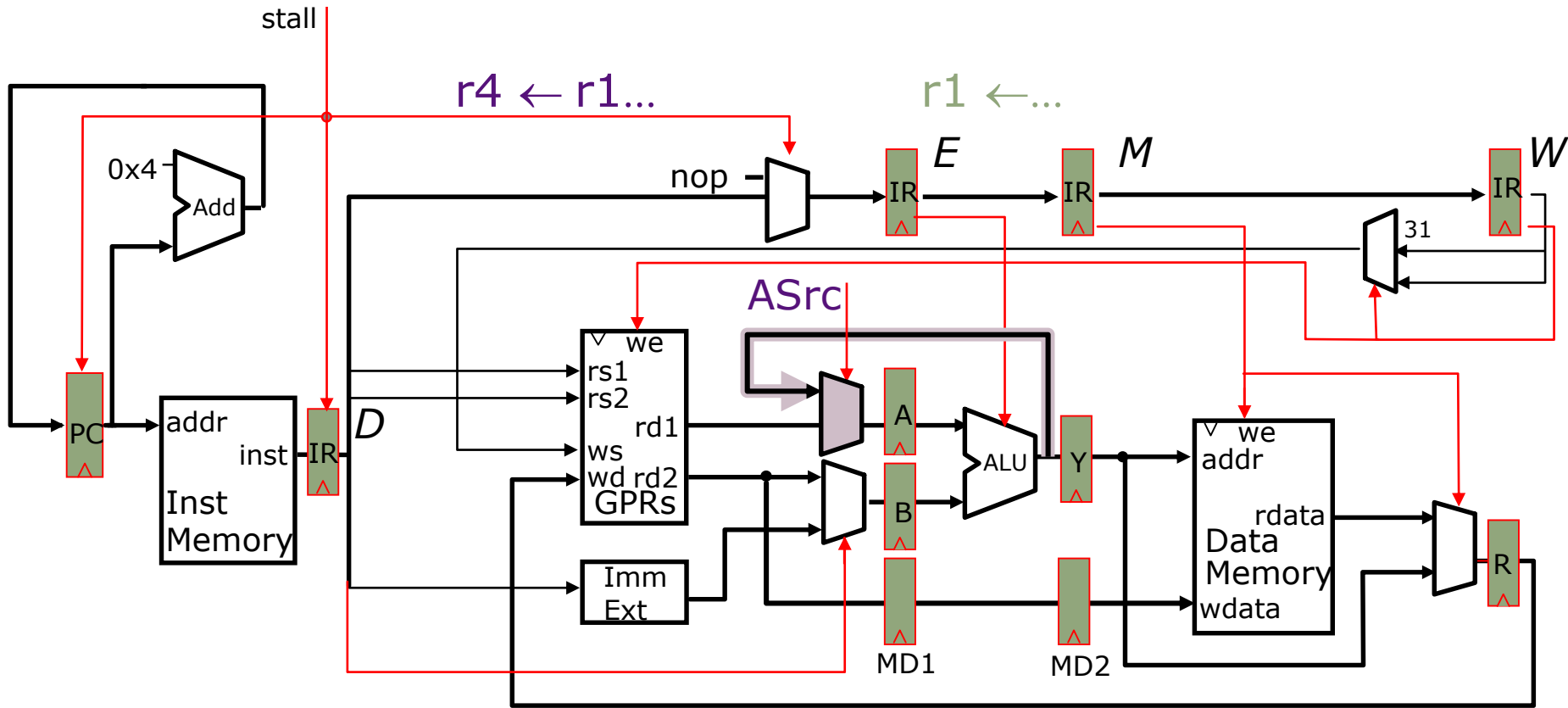


When does this bypass help?

...
 (I₁) r1 ← r0 + 10
 (I₂) r4 ← r1 + 17
 yes

r1 ← M[r0 + 10]
 r4 ← r1 + 17

Adding a Bypass

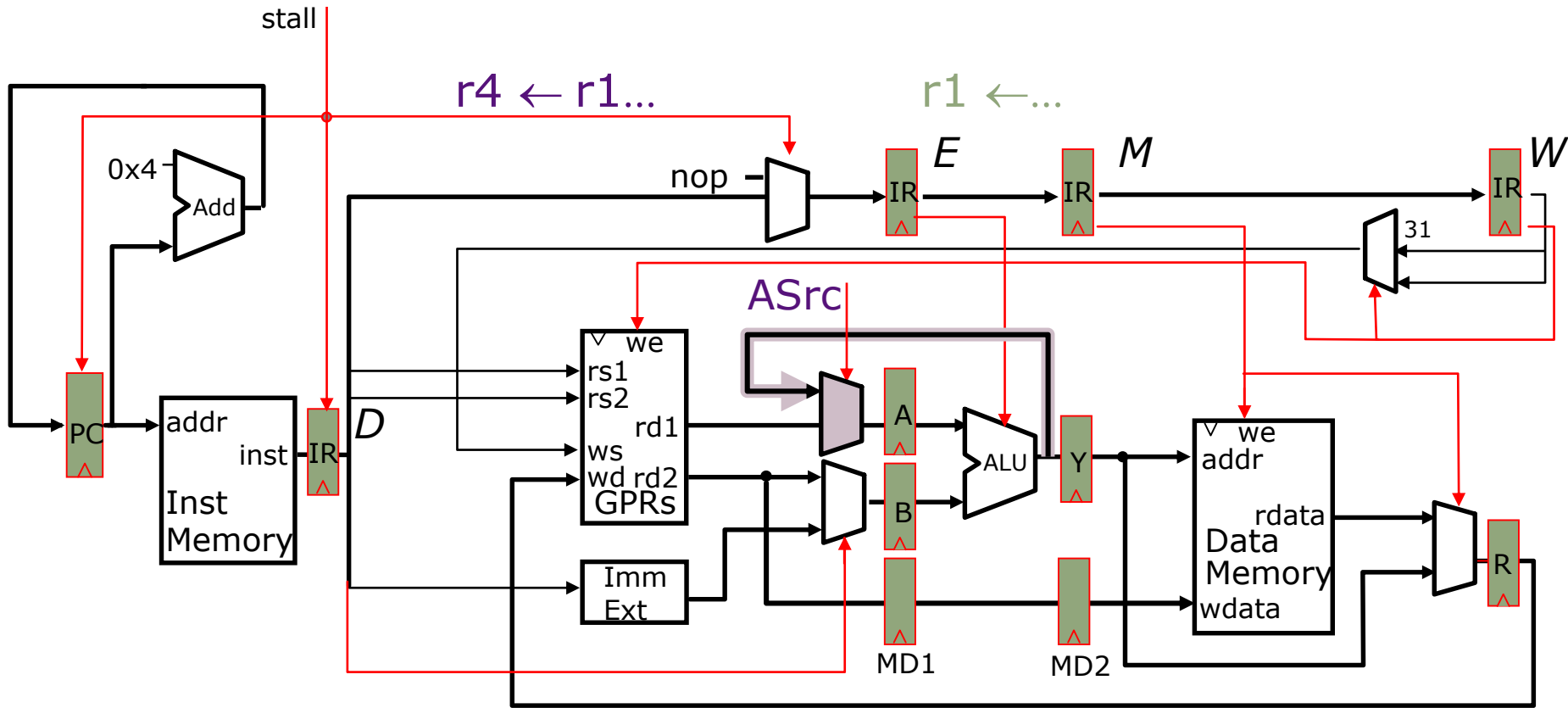


When does this bypass help?

...
 $(I_1) \quad r1 \leftarrow r0 + 10$
 $(I_2) \quad r4 \leftarrow r1 + 17$
yes

$r1 \leftarrow M[r0 + 10]$
 $r4 \leftarrow r1 + 17$
no

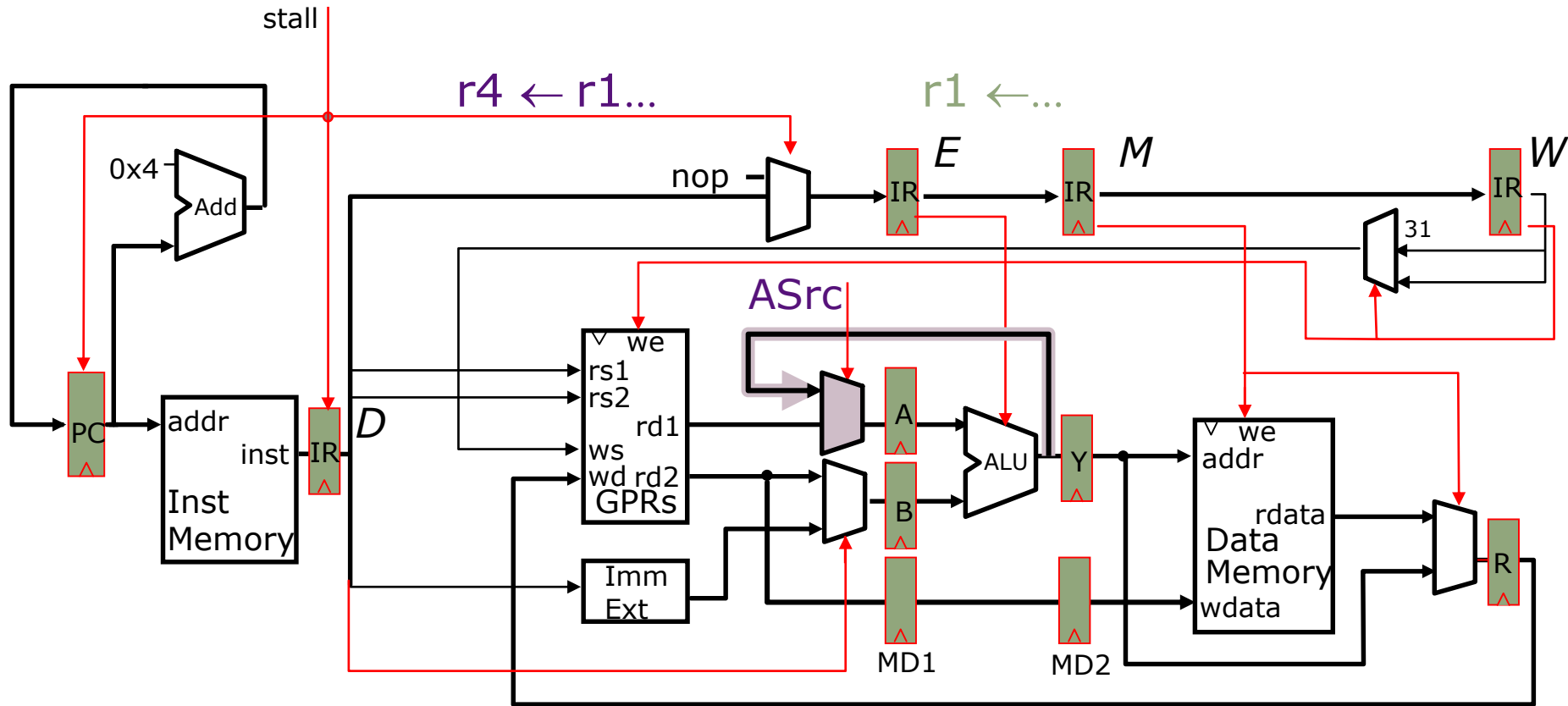
Adding a Bypass



When does this bypass help?

...			
(I ₁)	$r1 \leftarrow r0 + 10$	$r1 \leftarrow M[r0 + 10]$	JAL 500
(I ₂)	$r4 \leftarrow r1 + 17$ <i>yes</i>	$r4 \leftarrow r1 + 17$ <i>no</i>	$r4 \leftarrow r31 + 17$

Adding a Bypass



When does this bypass help?

...			
(I ₁)	$r1 \leftarrow r0 + 10$	$r1 \leftarrow M[r0 + 10]$	JAL 500
(I ₂)	$r4 \leftarrow r1 + 17$ <i>yes</i>	$r4 \leftarrow r1 + 17$ <i>no</i>	$r4 \leftarrow r31 + 17$ <i>no</i>

The Bypass Signal

Deriving it from the Stall Signal

$$\text{stall} = ((rs_D == ws_E) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D \\ + ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D$$

ws = Case opcode

ALU \Rightarrow rd
ALUi, LW \Rightarrow rt
JAL, JALR \Rightarrow R31

we = Case opcode

ALU, ALUi, LW \Rightarrow (ws \neq 0)
JAL, JALR \Rightarrow on
... \Rightarrow off

The Bypass Signal

Deriving it from the Stall Signal

$$\text{stall} = \left(\cancel{(rs_D == ws_E)} \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W \right) \cdot re1_D \\ + \left((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W \right) \cdot re2_D$$

ws = Case opcode

ALU ⇒ rd
ALUi, LW ⇒ rt
JAL, JALR ⇒ R31

we = Case opcode

ALU, ALUi, LW ⇒ (ws ≠ 0)
JAL, JALR ⇒ on
... ⇒ off

The Bypass Signal

Deriving it from the Stall Signal

$$\text{stall} = ((\cancel{rs_D == ws_E}) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D \\ + ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D$$

ws = Case opcode

ALU ⇒ rd
ALUi, LW ⇒ rt
JAL, JALR ⇒ R31

we = Case opcode

ALU, ALUi, LW ⇒ (ws ≠ 0)
JAL, JALR ⇒ on
... ⇒ off

$$\text{ASrc} = (rs_D == ws_E) \cdot we_E \cdot re1_D$$

The Bypass Signal

Deriving it from the Stall Signal

$$\text{stall} = ((\cancel{rs_D == ws_E}) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D \\ + ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D$$

ws = Case opcode

ALU \Rightarrow rd

ALUi, LW \Rightarrow rt

JAL, JALR \Rightarrow R31

we = Case opcode

ALU, ALUi, LW \Rightarrow (ws \neq 0)

JAL, JALR \Rightarrow on

... \Rightarrow off

$$\text{ASrc} = (rs_D == ws_E) \cdot we_E \cdot re1_D$$

Is this correct?

The Bypass Signal

Deriving it from the Stall Signal

$$\text{stall} = \left(\cancel{(rs_D == ws_E) \cdot we_E} + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W \right) \cdot re1_D \\ + \left((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W \right) \cdot re2_D$$

ws = Case opcode

ALU \Rightarrow rd

ALUi, LW \Rightarrow rt

JAL, JALR \Rightarrow R31

we = Case opcode

ALU, ALUi, LW \Rightarrow (ws \neq 0)

JAL, JALR \Rightarrow on

... \Rightarrow off

$$\text{ASrc} = (rs_D == ws_E) \cdot we_E \cdot re1_D$$

Is this correct?

No, because only ALU and ALUi instructions can benefit from this bypass

The Bypass Signal

Deriving it from the Stall Signal

$$\text{stall} = ((\cancel{rs_D == ws_E}) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D \\ + ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D$$

ws = Case opcode

ALU \Rightarrow rd

ALUi, LW \Rightarrow rt

JAL, JALR \Rightarrow R31

we = Case opcode

ALU, ALUi, LW \Rightarrow (ws \neq 0)

JAL, JALR \Rightarrow on

... \Rightarrow off

$$\text{ASrc} = (rs_D == ws_E) \cdot we_E \cdot re1_D$$

Is this correct?

No, because only ALU and ALUi instructions can benefit from this bypass

How might we address this?

The Bypass Signal

Deriving it from the Stall Signal

$$\text{stall} = ((\cancel{rs_D == ws_E}) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D \\ + ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D$$

ws = Case opcode

ALU \Rightarrow rd

ALUi, LW \Rightarrow rt

JAL, JALR \Rightarrow R31

we = Case opcode

ALU, ALUi, LW \Rightarrow (ws \neq 0)

JAL, JALR \Rightarrow on

... \Rightarrow off

$$\text{ASrc} = (rs_D == ws_E) \cdot we_E \cdot re1_D$$

Is this correct?

No, because only ALU and ALUi instructions can benefit from this bypass

How might we address this?

Split we_E into two components: we-bypass, we-stall

Bypass and Stall Signals

Split we_E into two components: we-bypass, we-stall

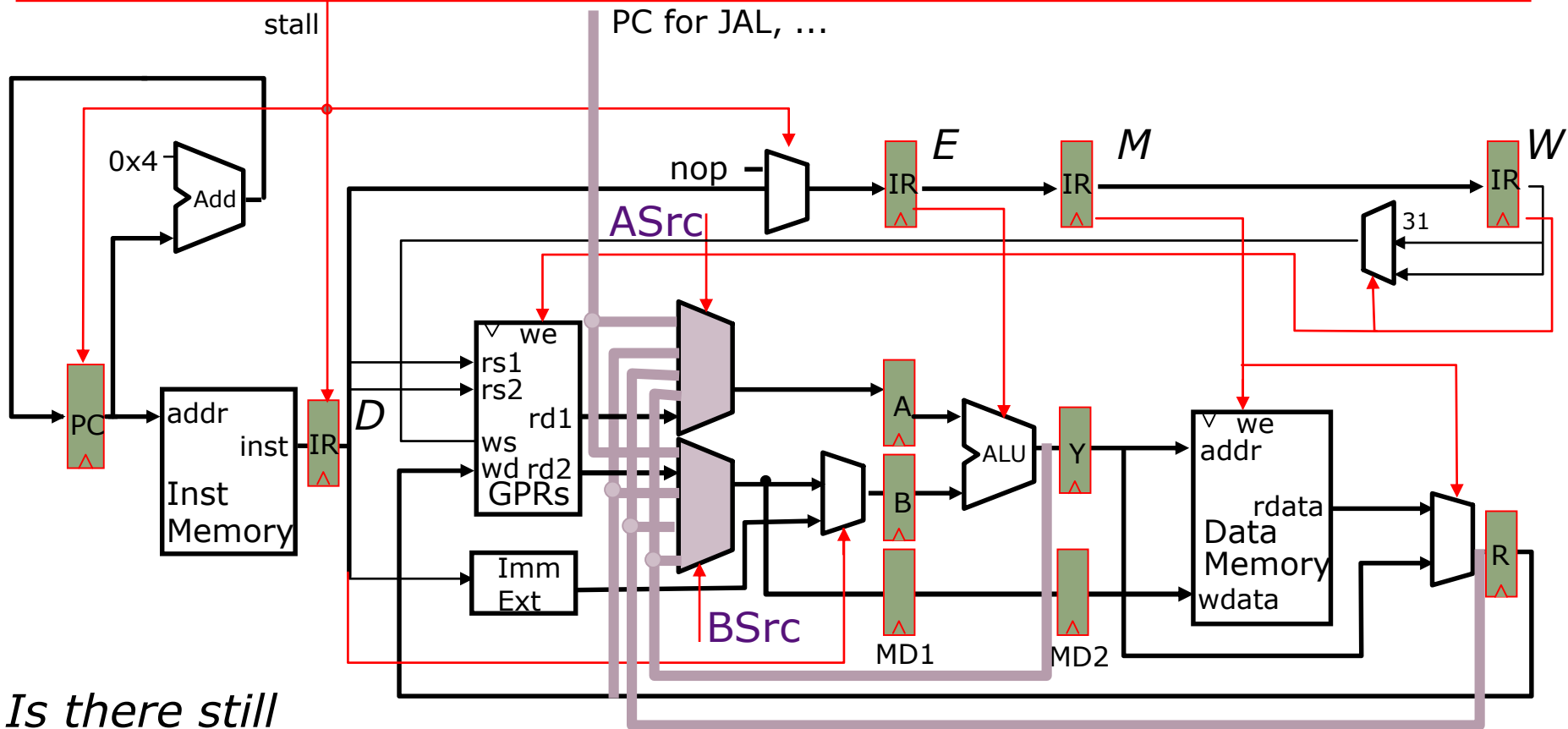
$we_bypass_E = \text{Case opcode}_E$
ALU, ALUi $\Rightarrow (ws \neq 0)$
... $\Rightarrow \text{off}$

$we_stall_E = \text{Case opcode}_E$
LW $\Rightarrow (ws \neq 0)$
JAL, JALR $\Rightarrow \text{on}$
... $\Rightarrow \text{off}$

$ASrc = (rs_D == ws_E) \cdot we_bypass_E \cdot re1_D$

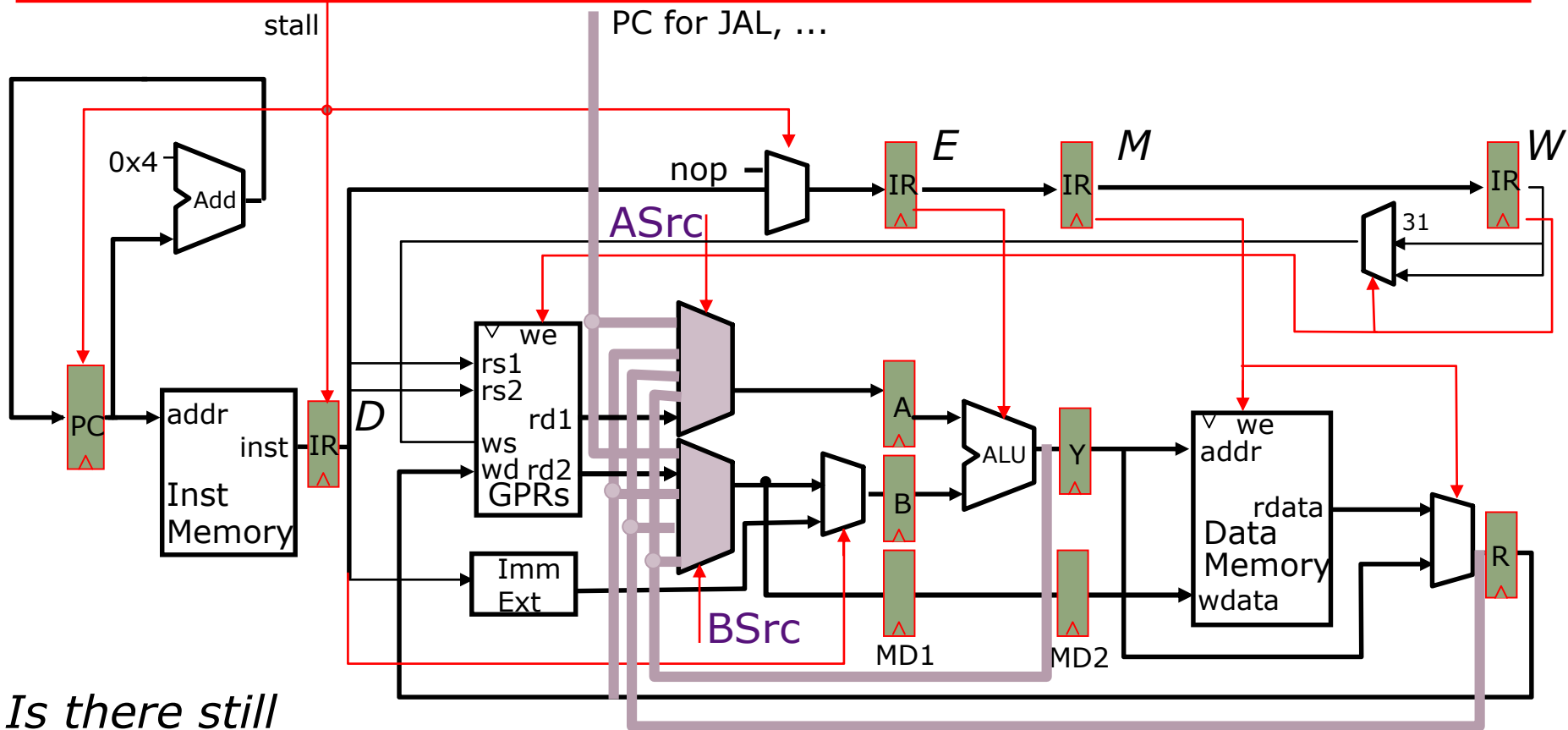
$stall = ((rs_D == ws_E) \cdot we_stall_E +$
 $(rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D$
 $+ ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D$

Fully Bypassed Datapath



Is there still a need for the stall signal?

Fully Bypassed Datapath



*Is there still
a need for the
stall signal?*

$$\text{stall} = (rs_D == ws_E) \cdot (\text{opcode}_E == LW_E) \cdot (ws_E \neq 0) \cdot re1_D \\ + (rt_D == ws_E) \cdot (\text{opcode}_E == LW_E) \cdot (ws_E \neq 0) \cdot re2_D$$

Resolving Data Hazards (3)

Strategy 3:

Speculate on the dependence. Two cases:

Resolving Data Hazards (3)

Strategy 3:

Speculate on the dependence. Two cases:

Guessed correctly \diamond no special action required

Resolving Data Hazards (3)

Strategy 3:

Speculate on the dependence. Two cases:

Guessed correctly \diamond no special action required

Guessed incorrectly \rightarrow kill and restart

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)
 - For all others

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)
 - For all others
 - Opcode and PC

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)
 - For all others
 - Opcode and PC
- In what stage do we know these?

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)
 - For all others
 - Opcode and PC
- In what stage do we know these?
 - PC → Fetch

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)
 - For all others
 - Opcode and PC
- In what stage do we know these?
 - PC → Fetch
 - Opcode, offset → Decode (or Fetch?)

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)
 - For all others
 - Opcode and PC
- In what stage do we know these?
 - PC → Fetch
 - Opcode, offset → Decode (or Fetch?)
 - Register value → Decode

Instruction to Instruction Dependence

- What do we need to calculate next PC?
 - For Jumps
 - Opcode, offset, and PC
 - For Jump Register
 - Opcode and register value
 - For Conditional Branches
 - Opcode, offset, PC, and register (for condition)
 - For all others
 - Opcode and PC
- In what stage do we know these?
 - PC → Fetch
 - Opcode, offset → Decode (or Fetch?)
 - Register value → Decode
 - Branch condition $((rs) == 0)$ → Execute (or Decode?)

NextPC Calculation Bubbles

NextPC Calculation Bubbles

time

t0 t1 t2 t3 t4 t5 t6 t7

NextPC Calculation Bubbles

	<i>time</i>								
	t0	t1	t2	t3	t4	t5	t6	t7	...
(I ₁) $r1 \leftarrow (r0) + 10$	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁				

NextPC Calculation Bubbles

	<i>time</i>								
	t0	t1	t2	t3	t4	t5	t6	t7	...
(I ₁) r1 ← (r0) + 10	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁				
(I ₂) r3 ← (r2) + 17		IF ₂	IF ₂	ID ₂	EX ₂	MA ₂	WB ₂		

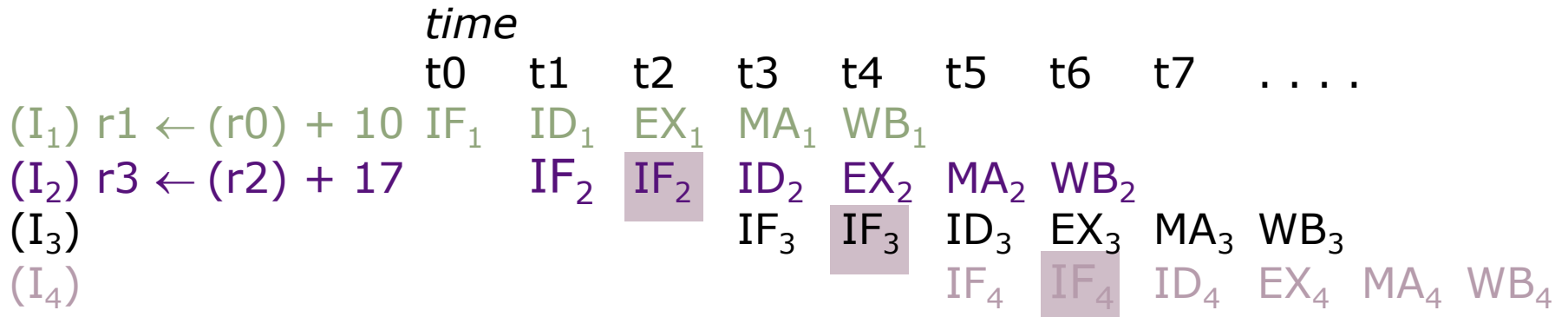
NextPC Calculation Bubbles

	<i>time</i>								
	t0	t1	t2	t3	t4	t5	t6	t7	...
(I ₁) $r1 \leftarrow (r0) + 10$	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁				
(I ₂) $r3 \leftarrow (r2) + 17$		IF ₂	IF ₂	ID ₂	EX ₂	MA ₂	WB ₂		
(I ₃)				IF ₃	IF ₃	ID ₃	EX ₃	MA ₃	WB ₃

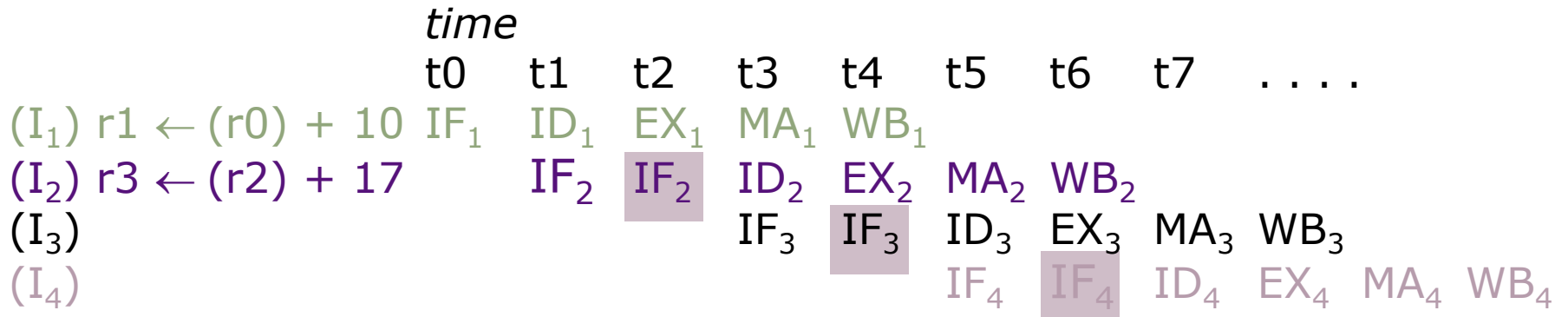
NextPC Calculation Bubbles

	<i>time</i>										
	t0	t1	t2	t3	t4	t5	t6	t7	...		
(I ₁) $r1 \leftarrow (r0) + 10$	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁						
(I ₂) $r3 \leftarrow (r2) + 17$		IF ₂	IF ₂	ID ₂	EX ₂	MA ₂	WB ₂				
(I ₃)				IF ₃	IF ₃	ID ₃	EX ₃	MA ₃	WB ₃		
(I ₄)						IF ₄	IF ₄	ID ₄	EX ₄	MA ₄	WB ₄

NextPC Calculation Bubbles

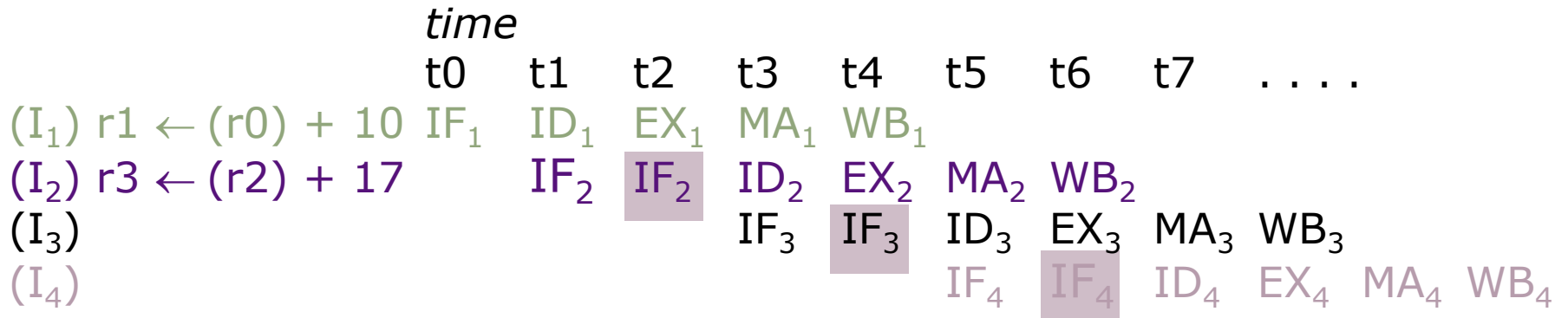


NextPC Calculation Bubbles



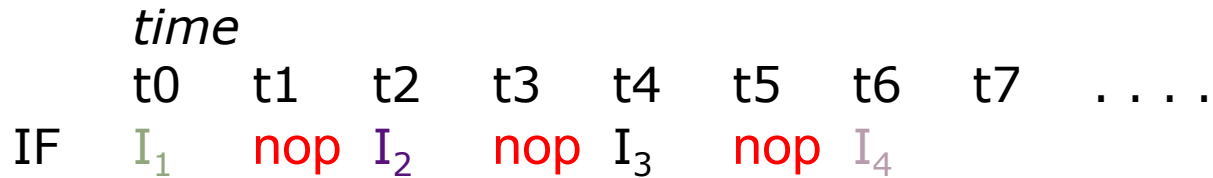
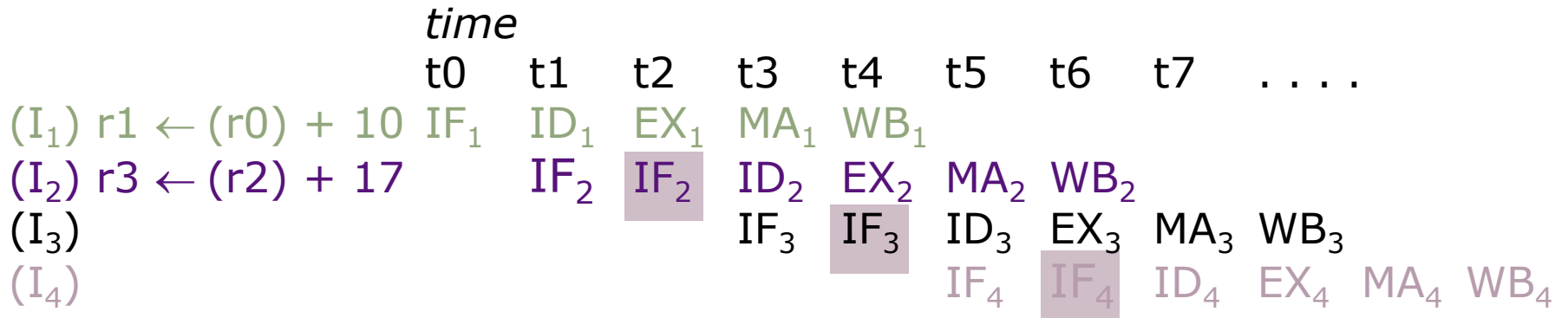
*Resource
Usage*

NextPC Calculation Bubbles



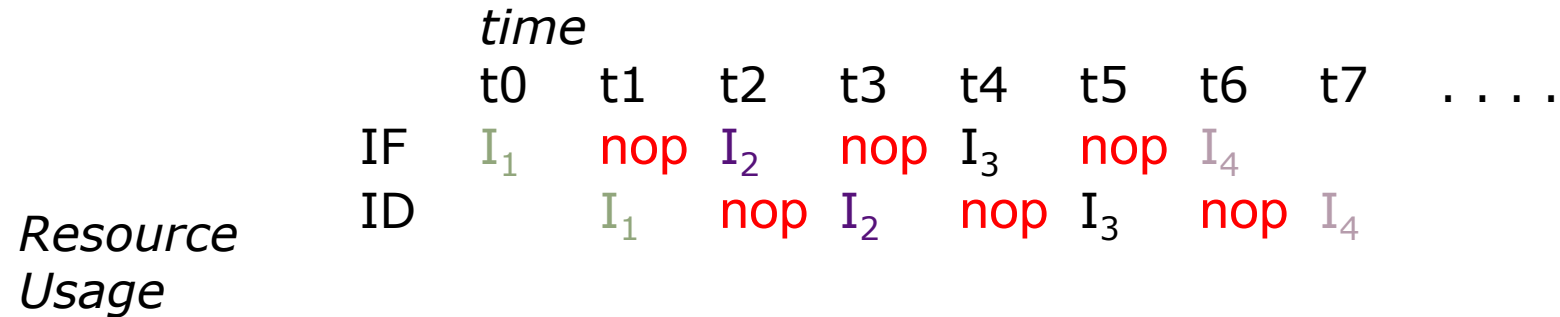
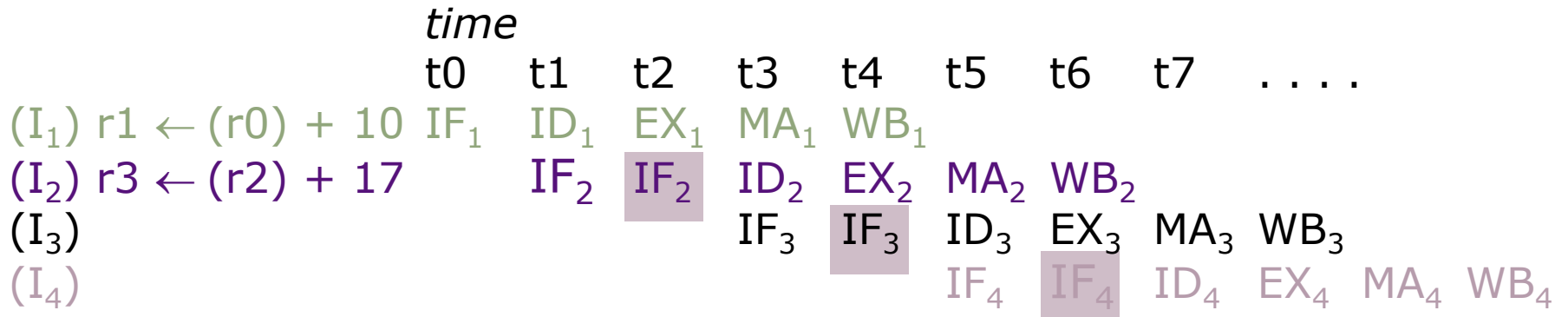
*Resource
Usage*

NextPC Calculation Bubbles

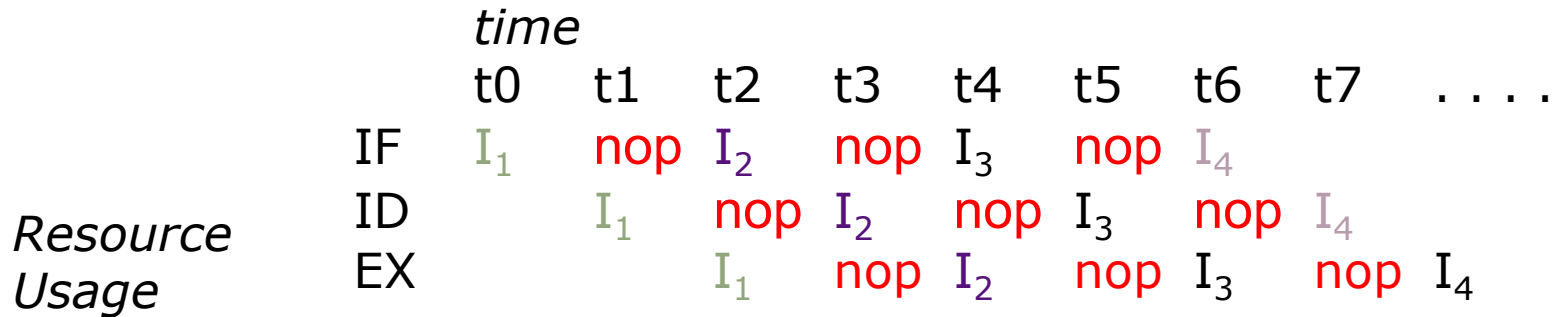
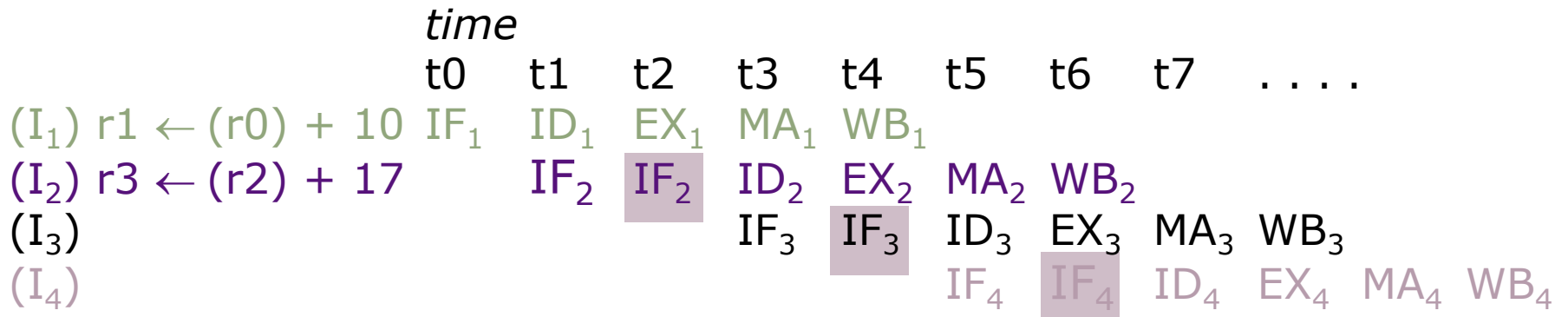


Resource Usage

NextPC Calculation Bubbles



NextPC Calculation Bubbles

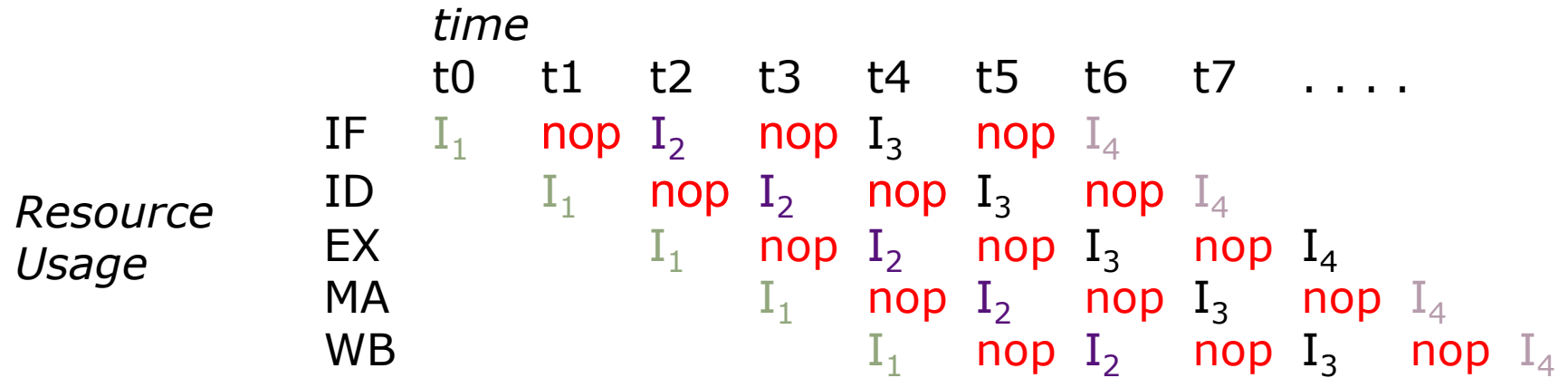
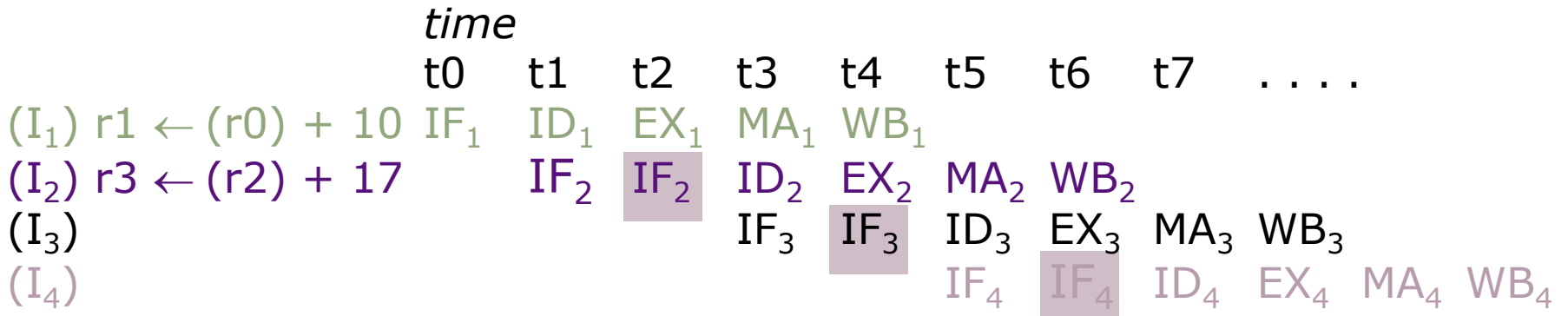


NextPC Calculation Bubbles

	<i>time</i>									
	t0	t1	t2	t3	t4	t5	t6	t7
(I ₁) r1 ← (r0) + 10	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁					
(I ₂) r3 ← (r2) + 17		IF ₂	IF ₂	ID ₂	EX ₂	MA ₂	WB ₂			
(I ₃)				IF ₃	IF ₃	ID ₃	EX ₃	MA ₃	WB ₃	
(I ₄)						IF ₄	IF ₄	ID ₄	EX ₄	MA ₄ WB ₄

	<i>time</i>									
	t0	t1	t2	t3	t4	t5	t6	t7
IF	I ₁	nop	I ₂	nop	I ₃	nop	I ₄			
ID		I ₁	nop	I ₂	nop	I ₃	nop	I ₄		
EX			I ₁	nop	I ₂	nop	I ₃	nop	I ₄	
MA				I ₁	nop	I ₂	nop	I ₃	nop	I ₄

NextPC Calculation Bubbles



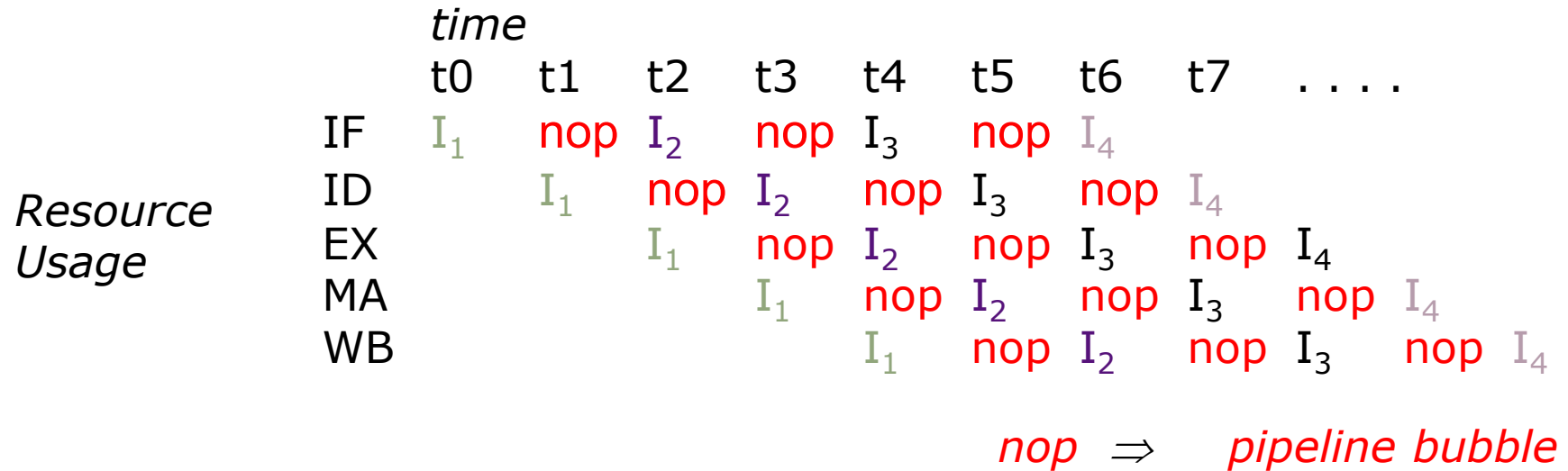
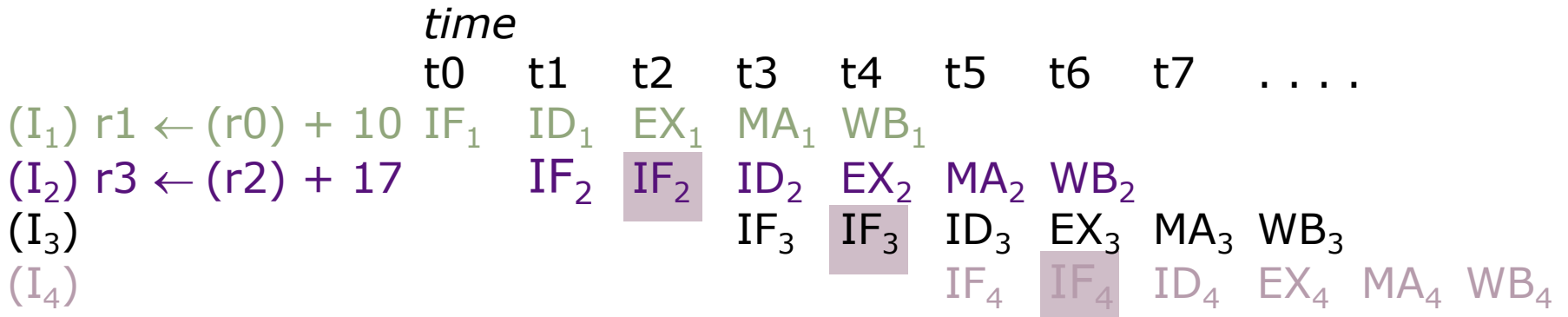
NextPC Calculation Bubbles

	<i>time</i>									
	t0	t1	t2	t3	t4	t5	t6	t7
(I ₁) r1 ← (r0) + 10	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁					
(I ₂) r3 ← (r2) + 17		IF ₂	IF ₂	ID ₂	EX ₂	MA ₂	WB ₂			
(I ₃)				IF ₃	IF ₃	ID ₃	EX ₃	MA ₃	WB ₃	
(I ₄)						IF ₄	IF ₄	ID ₄	EX ₄	MA ₄ WB ₄

	<i>time</i>										
	t0	t1	t2	t3	t4	t5	t6	t7	
IF	I ₁	nop	I ₂	nop	I ₃	nop	I ₄				
ID		I ₁	nop	I ₂	nop	I ₃	nop	I ₄			
EX			I ₁	nop	I ₂	nop	I ₃	nop	I ₄		
MA				I ₁	nop	I ₂	nop	I ₃	nop	I ₄	
WB					I ₁	nop	I ₂	nop	I ₃	nop	I ₄

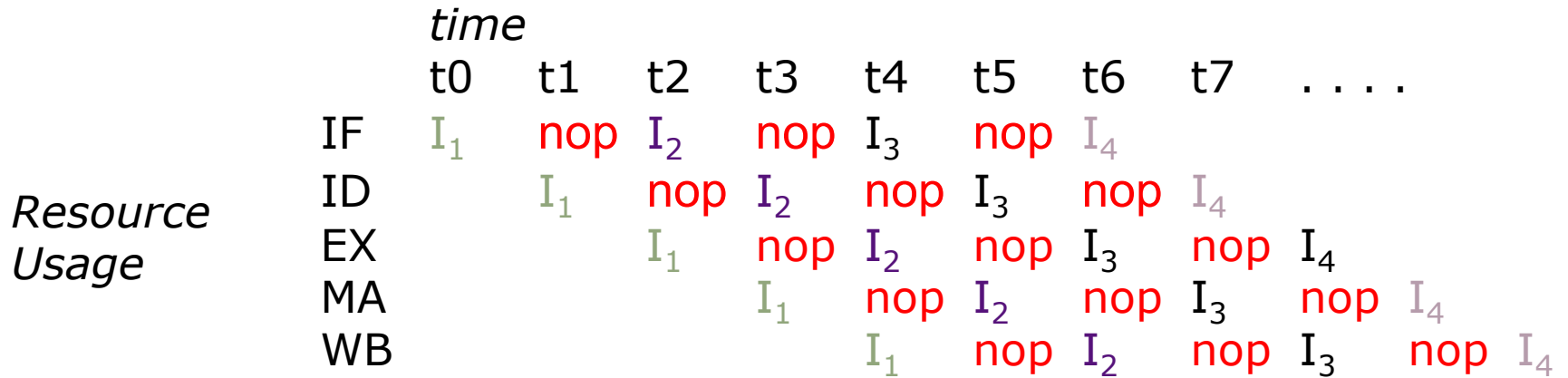
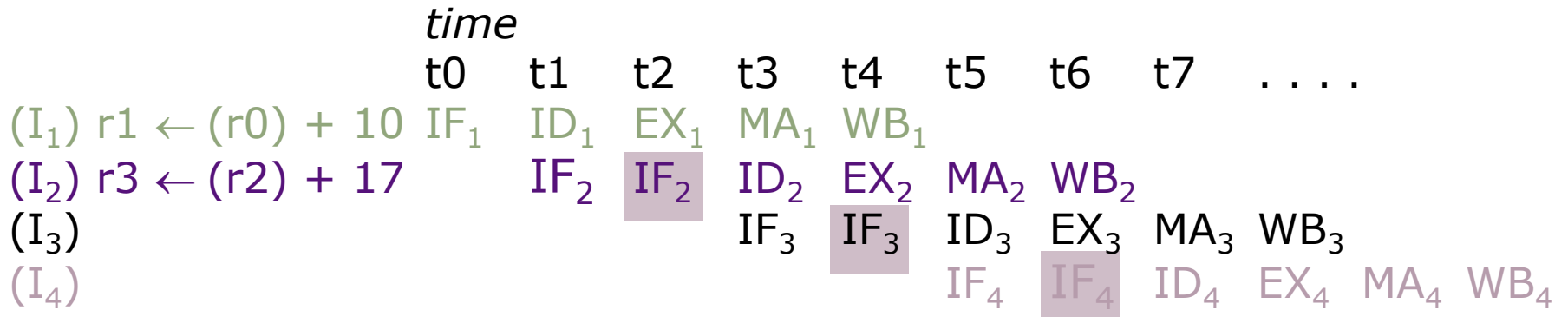
nop ⇒ *pipeline bubble*

NextPC Calculation Bubbles



What's a good guess for next PC?

NextPC Calculation Bubbles

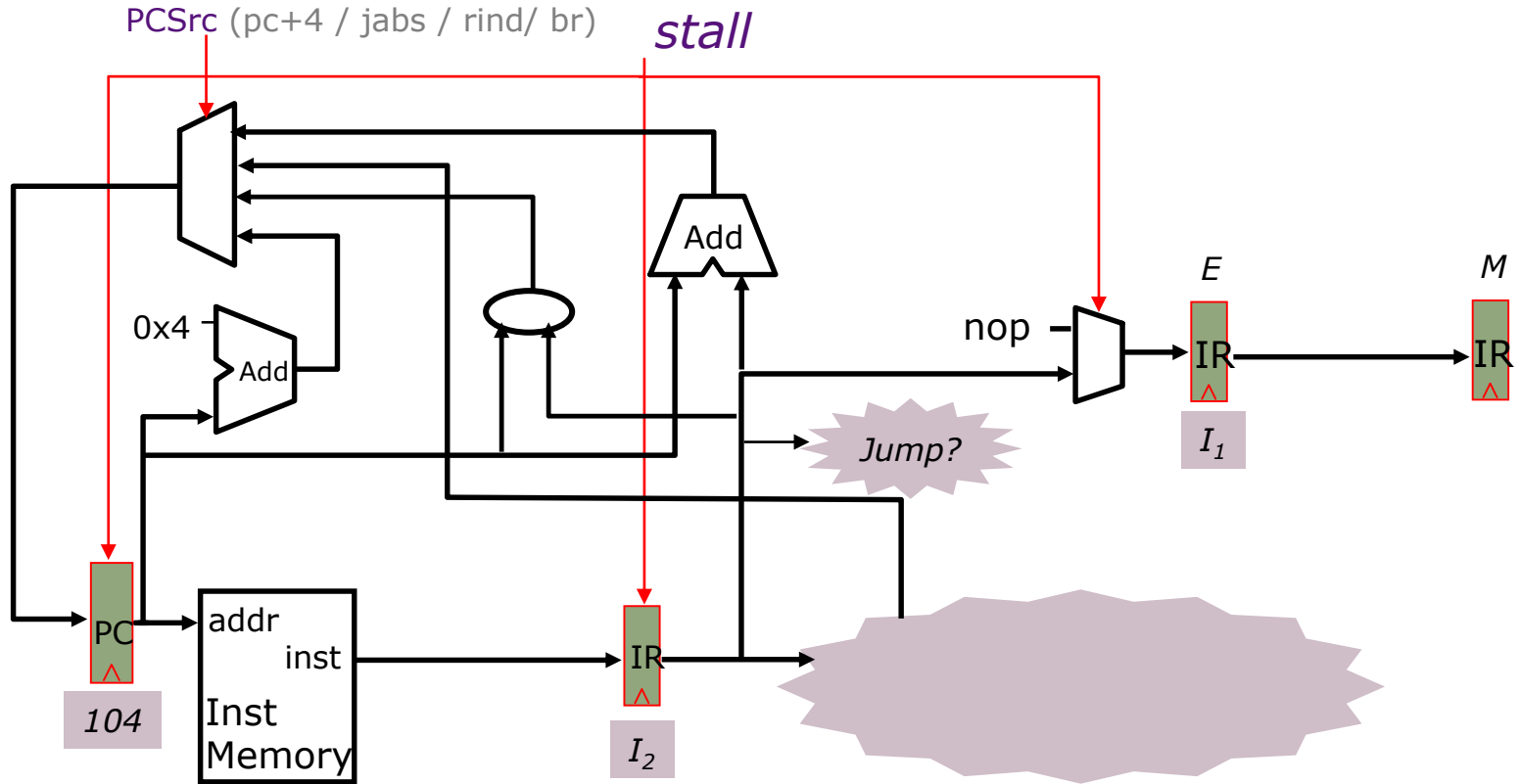


nop ⇒ *pipeline bubble*

What's a good guess for next PC?

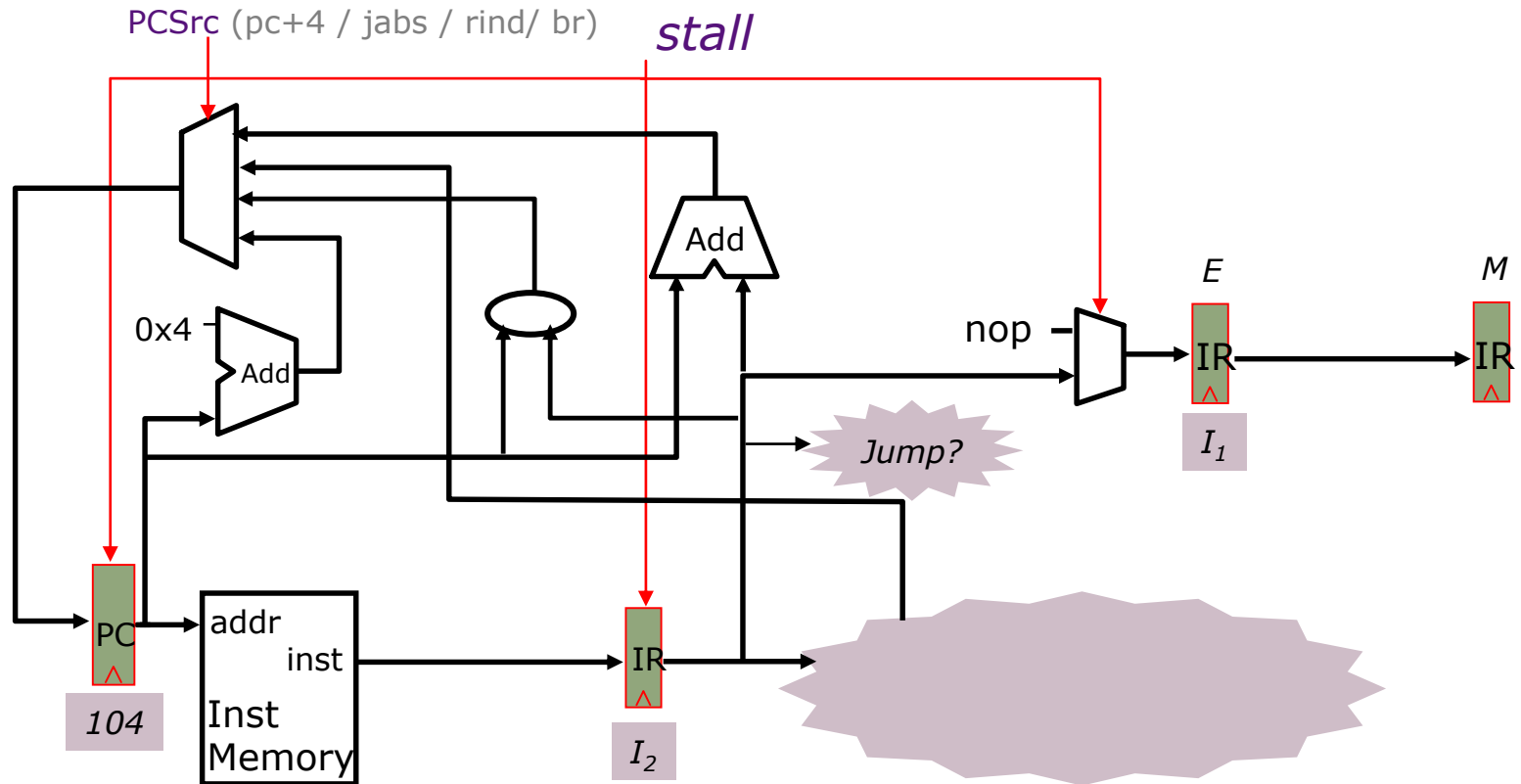
PC+4

Speculate NextPC is PC+4



I_1	096	ADD	
I_2	100	J	200
I_3	104	ADD	
I_4	304	ADD	

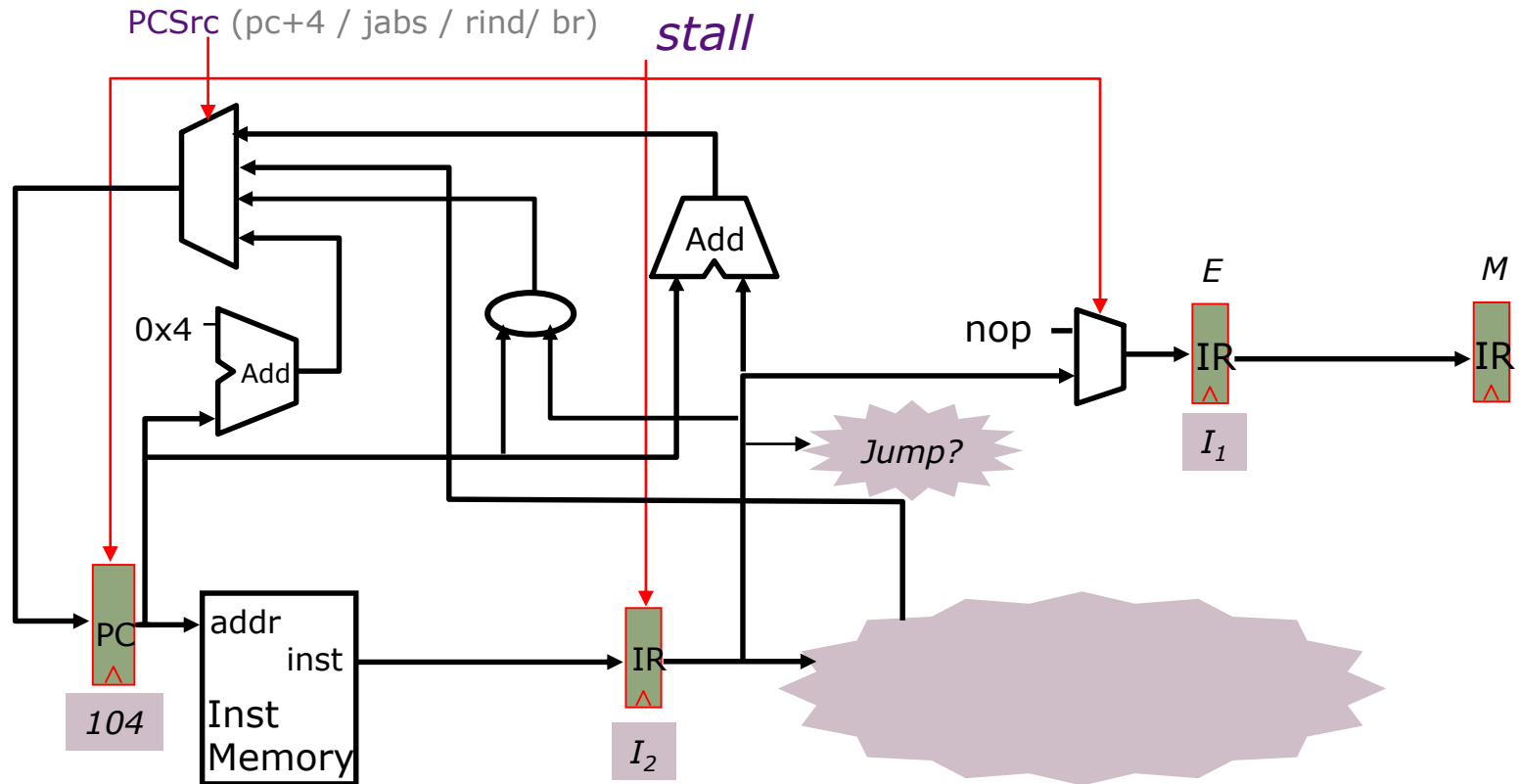
Speculate NextPC is PC+4



I_1	096	ADD	
I_2	100	J	200
I_3	104	ADD	
I_4	304	ADD	

What happens on mis-speculation, i.e., when next instruction is not PC+4?

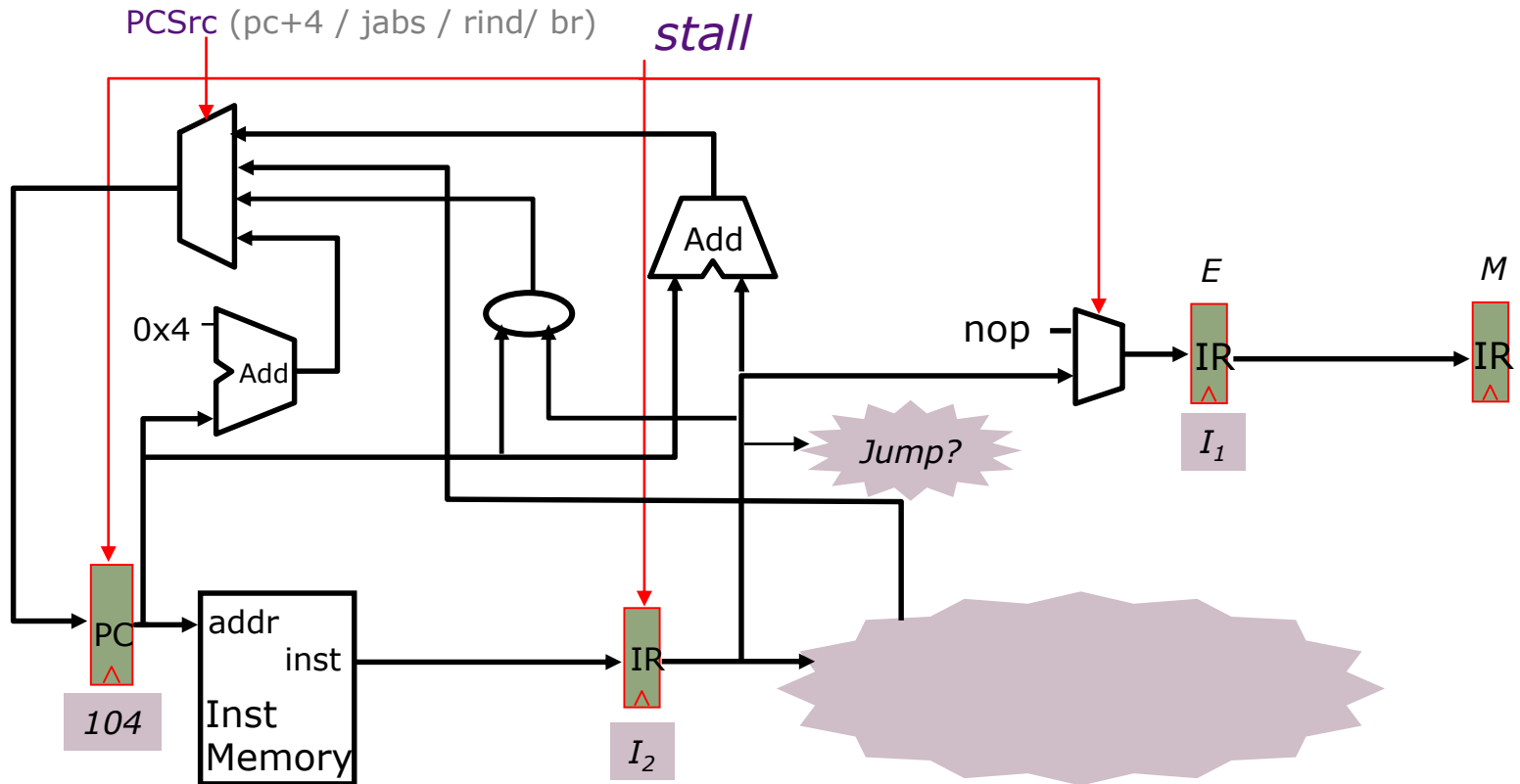
Speculate NextPC is PC+4



I_1	096	ADD	
I_2	100	J	200
I_3	104	ADD	<i>kill</i>
I_4	304	ADD	

What happens on mis-speculation, i.e., when next instruction is not PC+4?

Speculate NextPC is PC+4

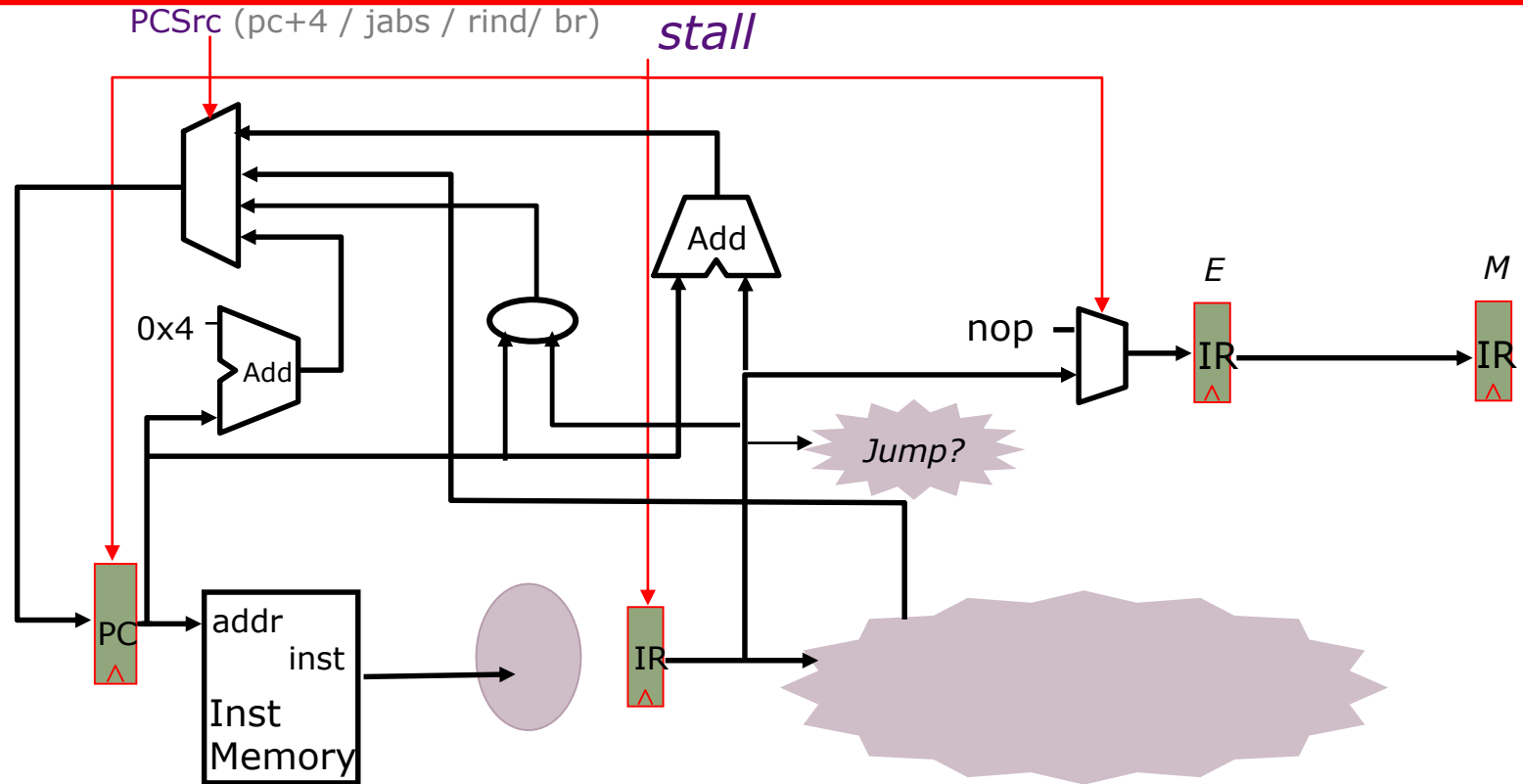


I_1	096	ADD	
I_2	100	J	200
I_3	104	ADD	<i>kill</i>
I_4	304	ADD	

What happens on mis-speculation, i.e., when next instruction is not PC+4?

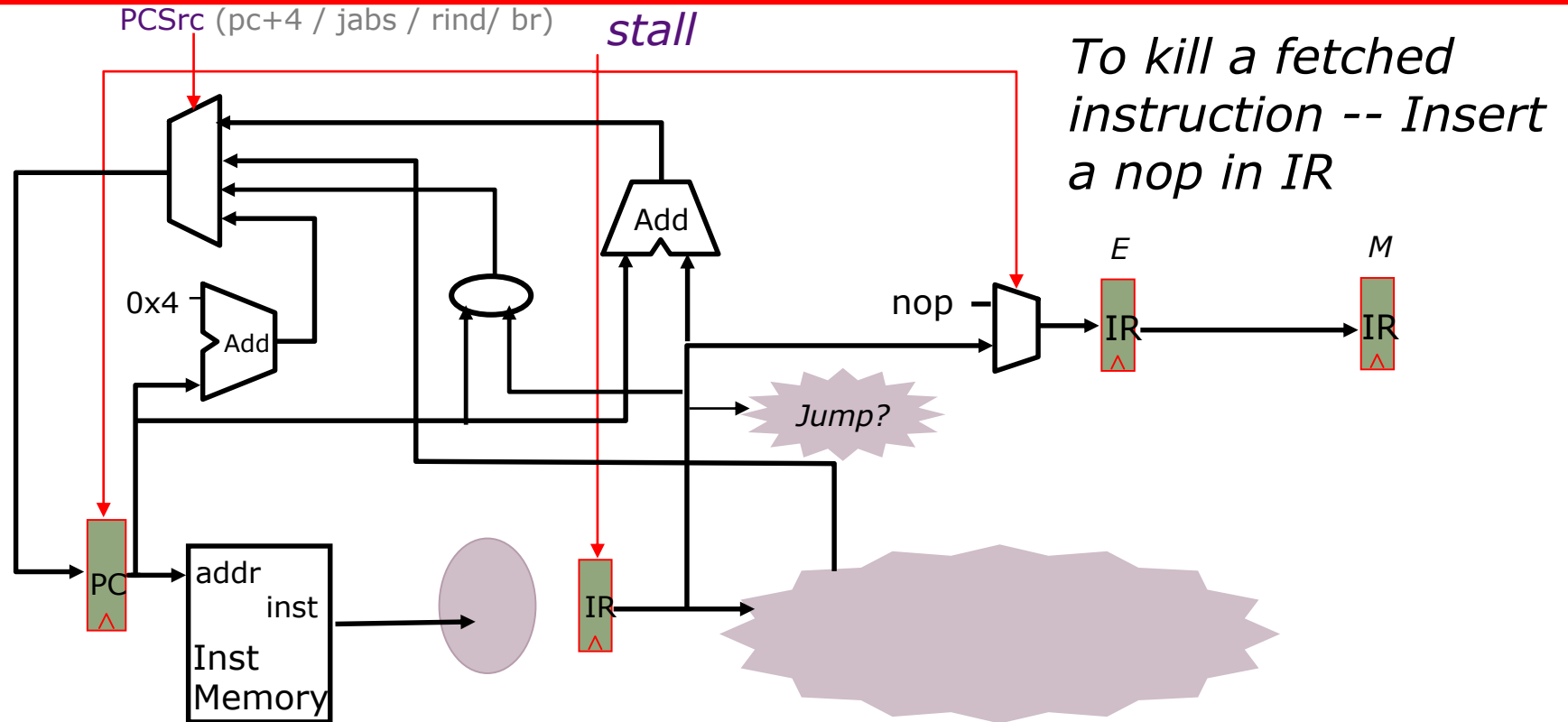
How?

Pipelining Jumps



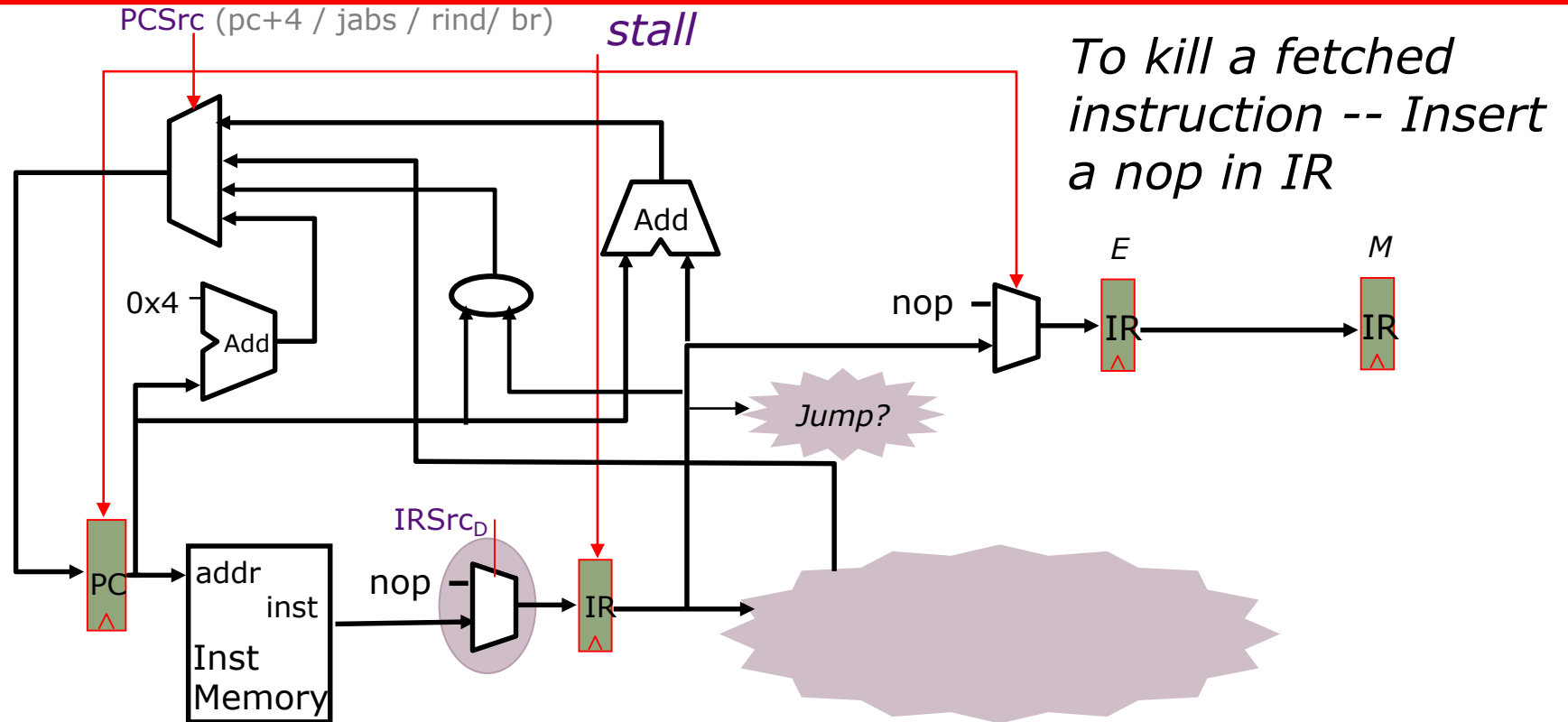
I ₁	096	ADD	
I ₂	100	J	200
I ₃	104	ADD	<i>kill</i>
I ₄	304	ADD	

Pipelining Jumps



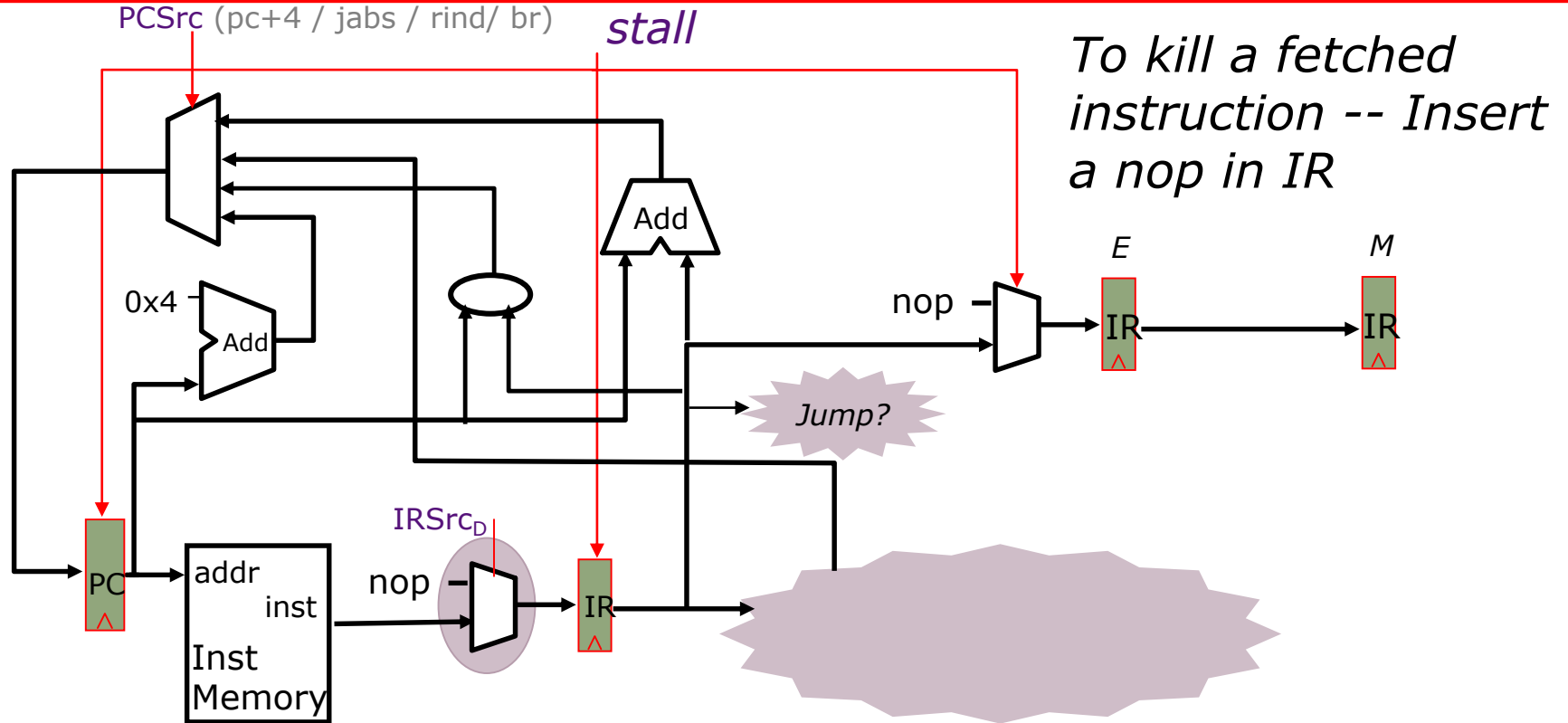
I ₁	096	ADD	
I ₂	100	J	200
I ₃	104	ADD	<i>kill</i>
I ₄	304	ADD	

Pipelining Jumps



I ₁	096	ADD	
I ₂	100	J	200
I ₃	104	ADD	<i>kill</i>
I ₄	304	ADD	

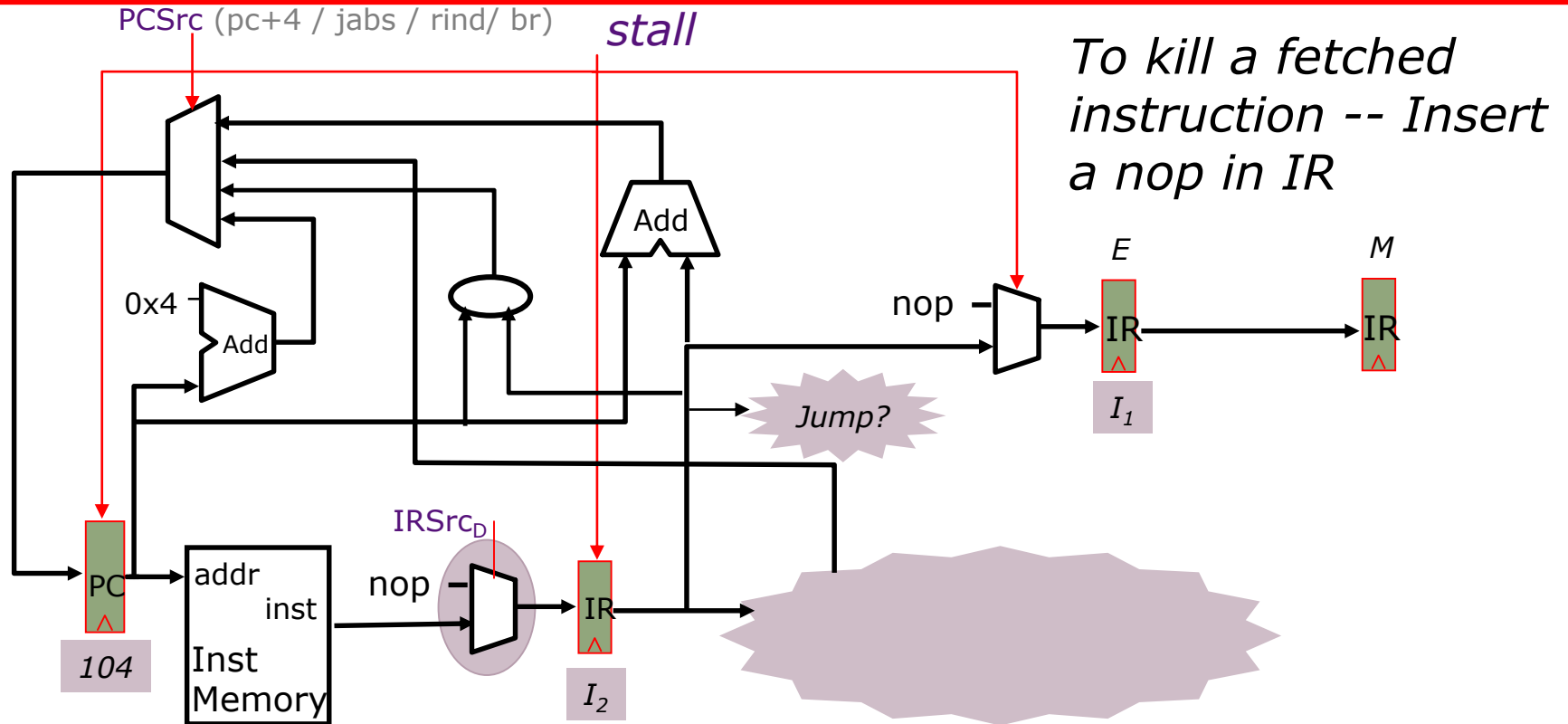
Pipelining Jumps



I ₁	096	ADD	
I ₂	100	J	200
I ₃	104	ADD	<i>kill</i>
I ₄	304	ADD	

IRSrc_D = Case opcode_D
 J, JAL ⇒ nop
 ... ⇒ IM

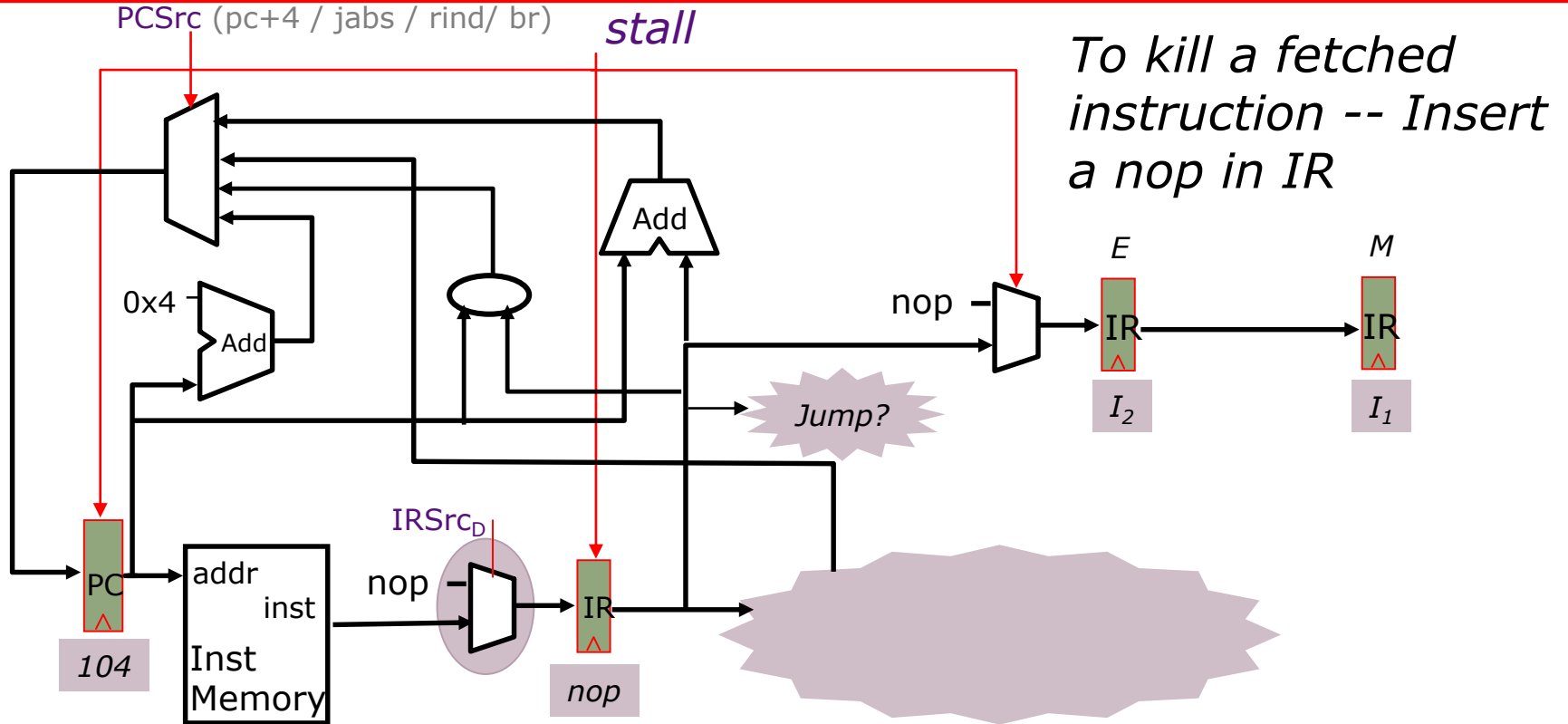
Pipelining Jumps



I ₁	096	ADD	
I ₂	100	J	200
I ₃	104	ADD	<i>kill</i>
I ₄	304	ADD	

IRSrc_D = Case opcode_D
 J, JAL ⇒ nop
 ... ⇒ IM

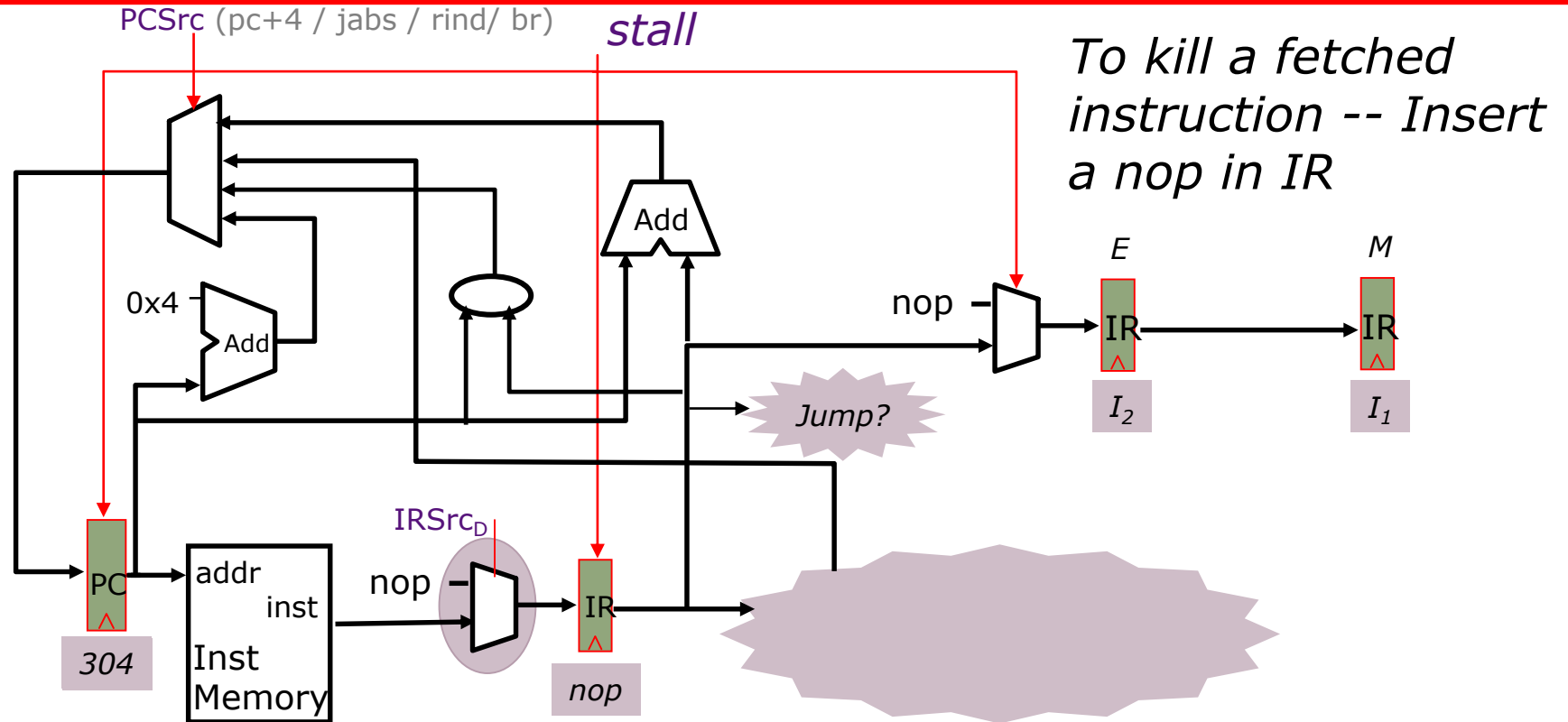
Pipelining Jumps



I_1	096	ADD	
I_2	100	J	200
I_3	104	ADD	kill
I_4	304	ADD	

$IRSrc_D = \text{Case opcode}_D$
 J, JAL \Rightarrow nop
 ... \Rightarrow IM

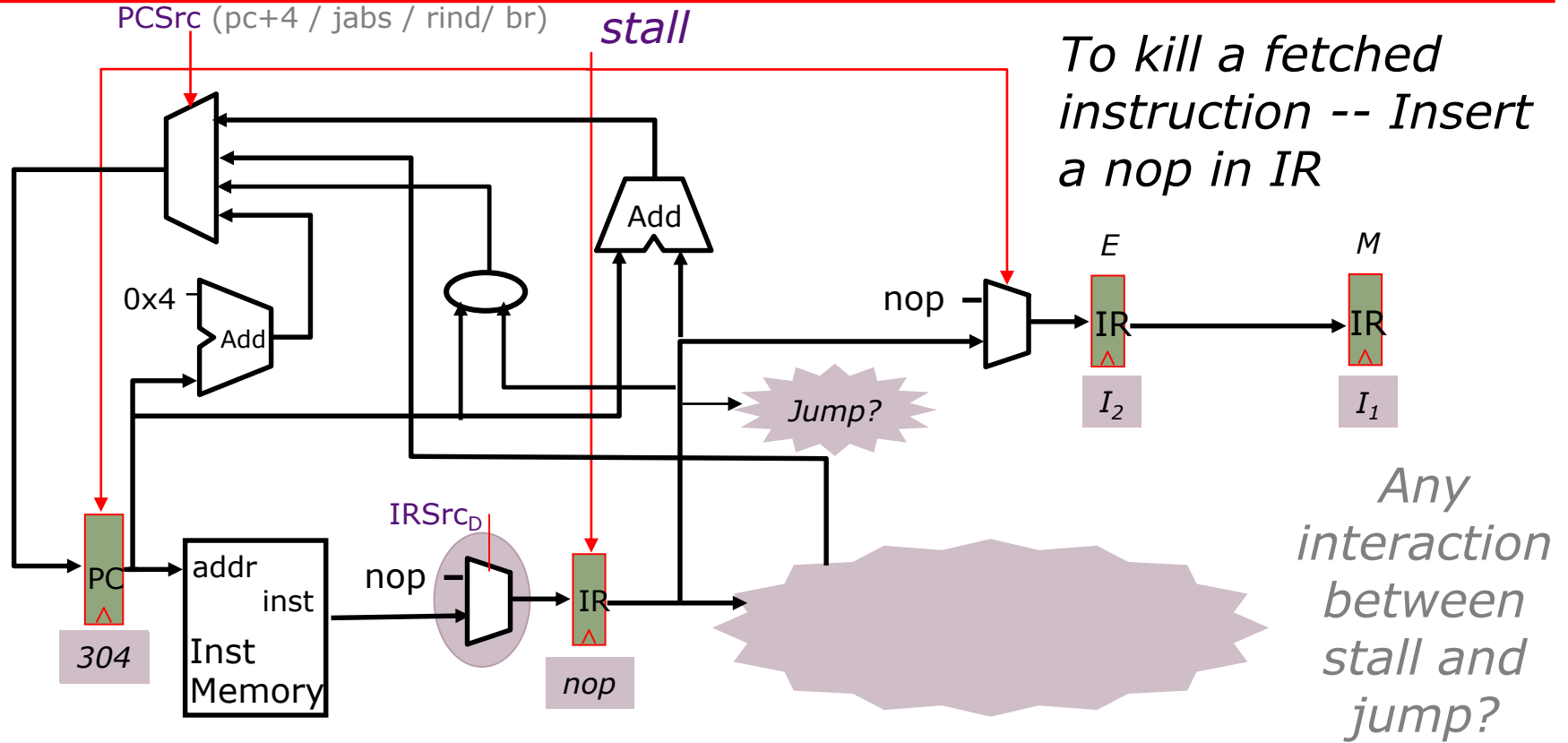
Pipelining Jumps



I_1	096	ADD	
I_2	100	J	200
I_3	104	ADD	<i>kill</i>
I_4	304	ADD	

$IRSrc_D = \text{Case opcode}_D$
 J, JAL \Rightarrow nop
 ... \Rightarrow IM

Pipelining Jumps



I_1	096	ADD	
I_2	100	J	200
I_3	104	ADD	<i>kill</i>
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$IRSrc_D = \text{Case opcode}_D$
 J, JAL \Rightarrow nop
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Jump Pipeline Diagrams

Jump Pipeline Diagrams

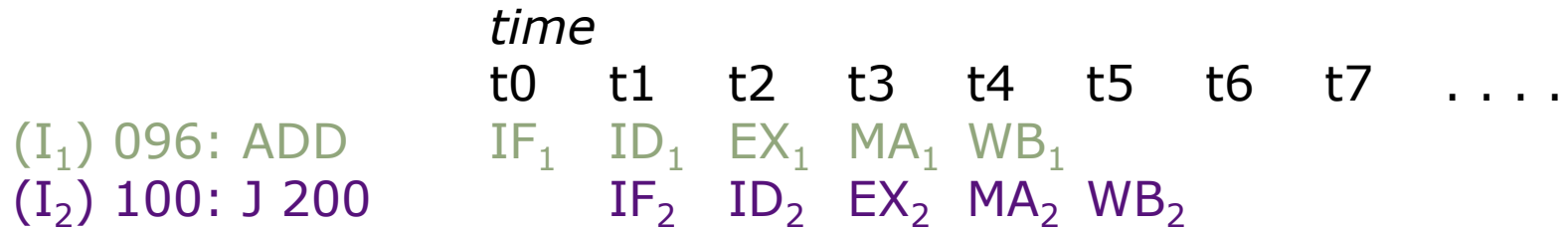
time

t0 t1 t2 t3 t4 t5 t6 t7

Jump Pipeline Diagrams

	<i>time</i>									
	t0	t1	t2	t3	t4	t5	t6	t7
(I ₁) 096: ADD	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁					

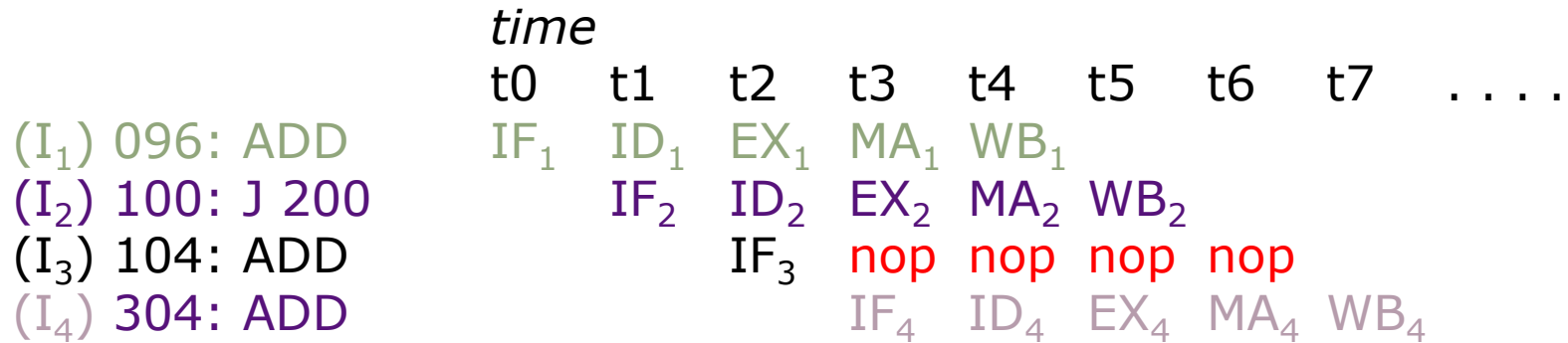
Jump Pipeline Diagrams



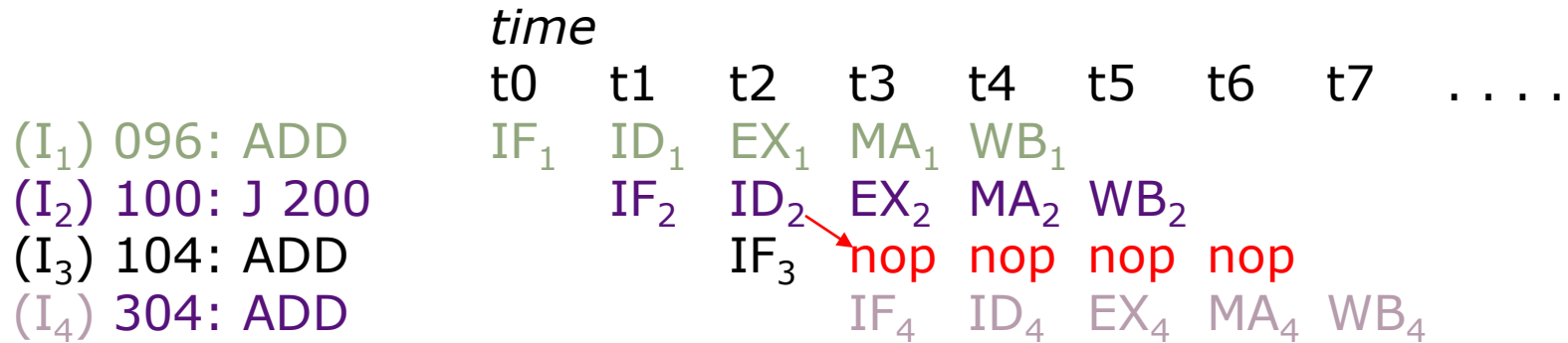
Jump Pipeline Diagrams

	<i>time</i>								
	t0	t1	t2	t3	t4	t5	t6	t7	...
(I ₁) 096: ADD	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁				
(I ₂) 100: J 200		IF ₂	ID ₂	EX ₂	MA ₂	WB ₂			
(I ₃) 104: ADD			IF ₃	nop	nop	nop	nop		

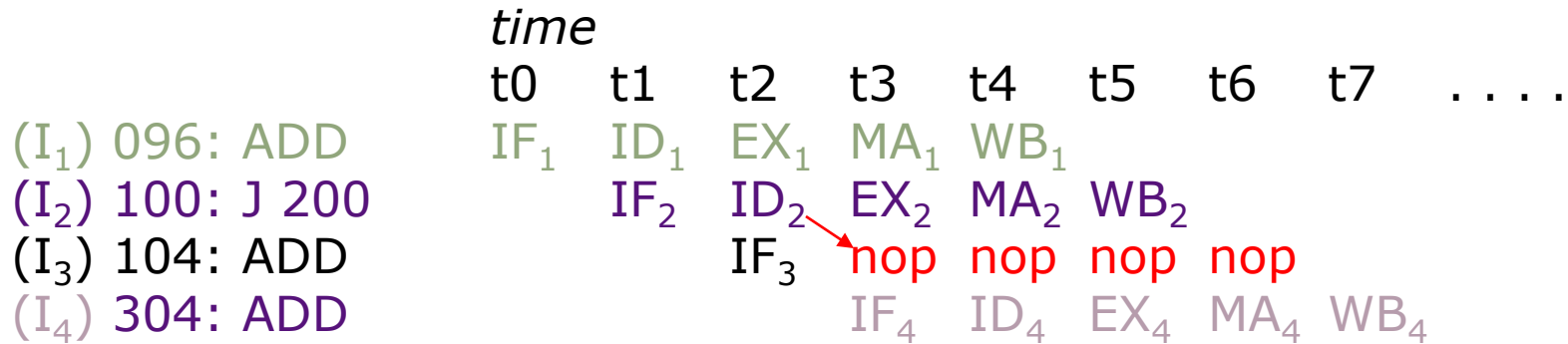
Jump Pipeline Diagrams



Jump Pipeline Diagrams

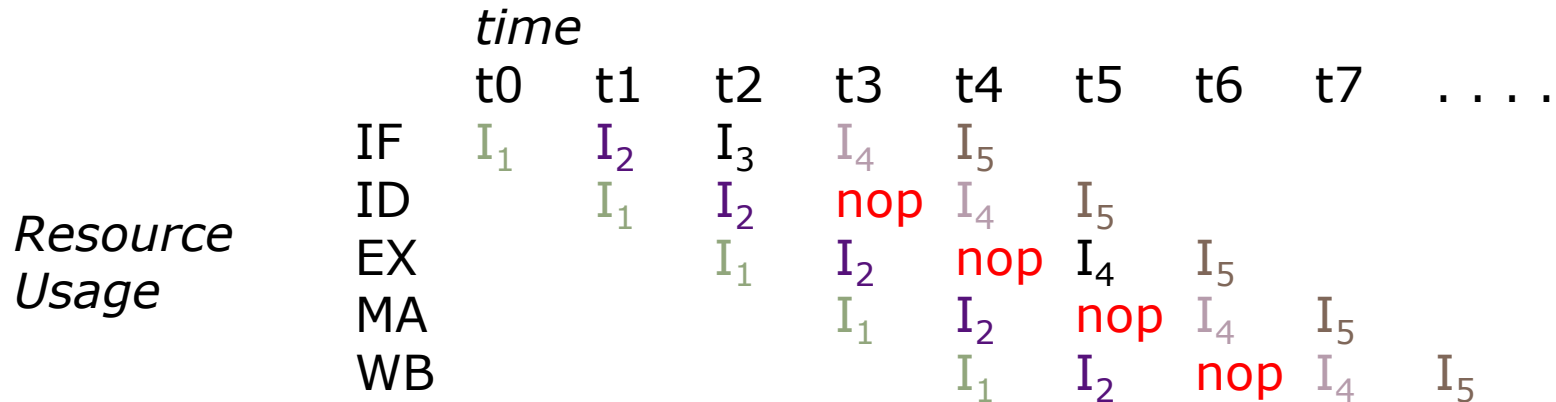
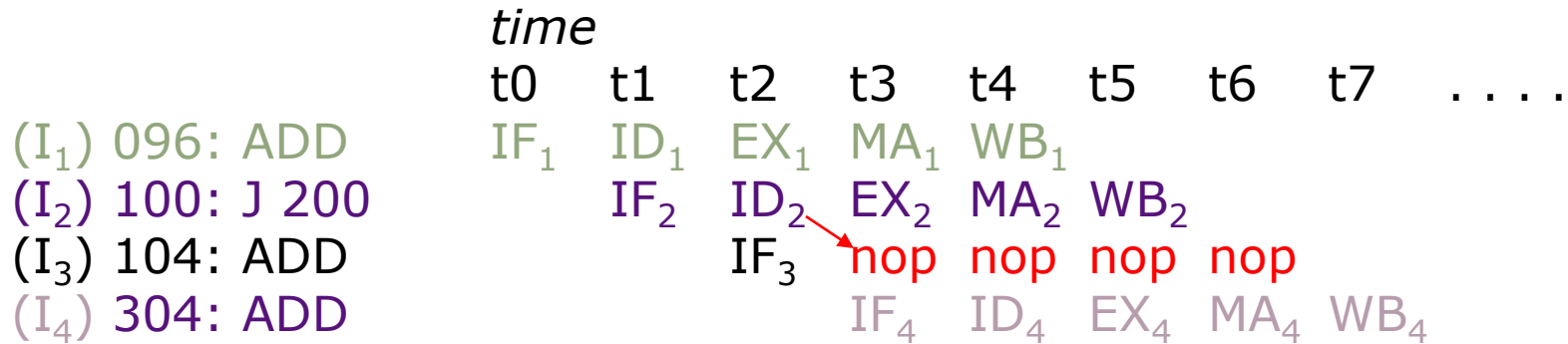


Jump Pipeline Diagrams

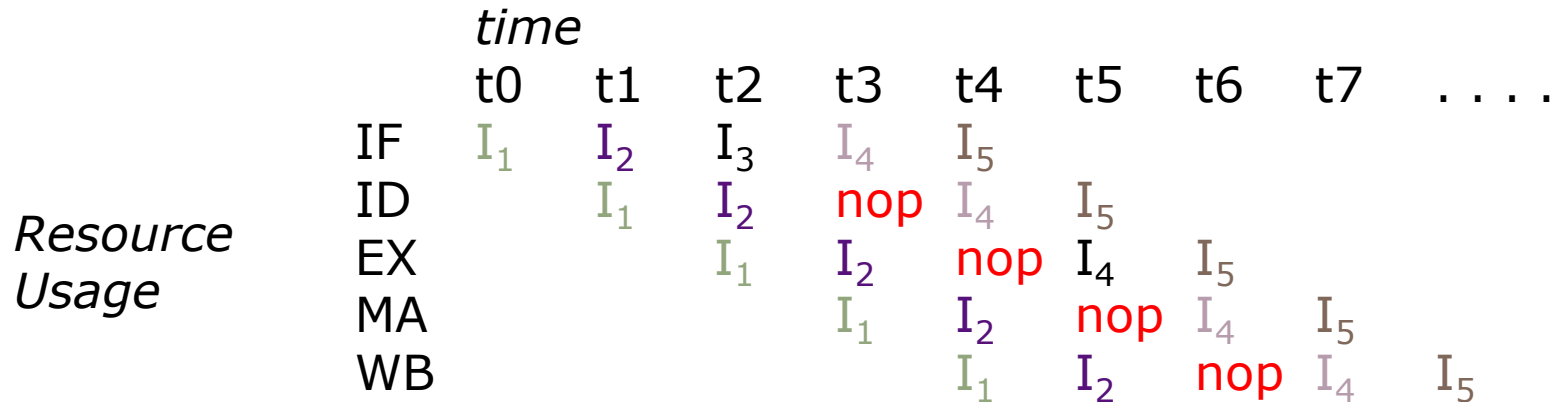
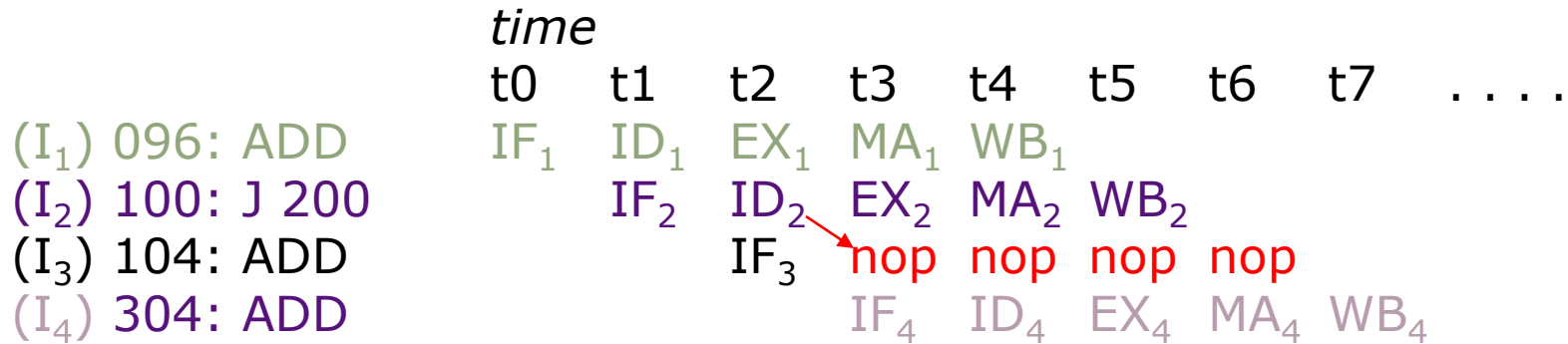


*Resource
Usage*

Jump Pipeline Diagrams

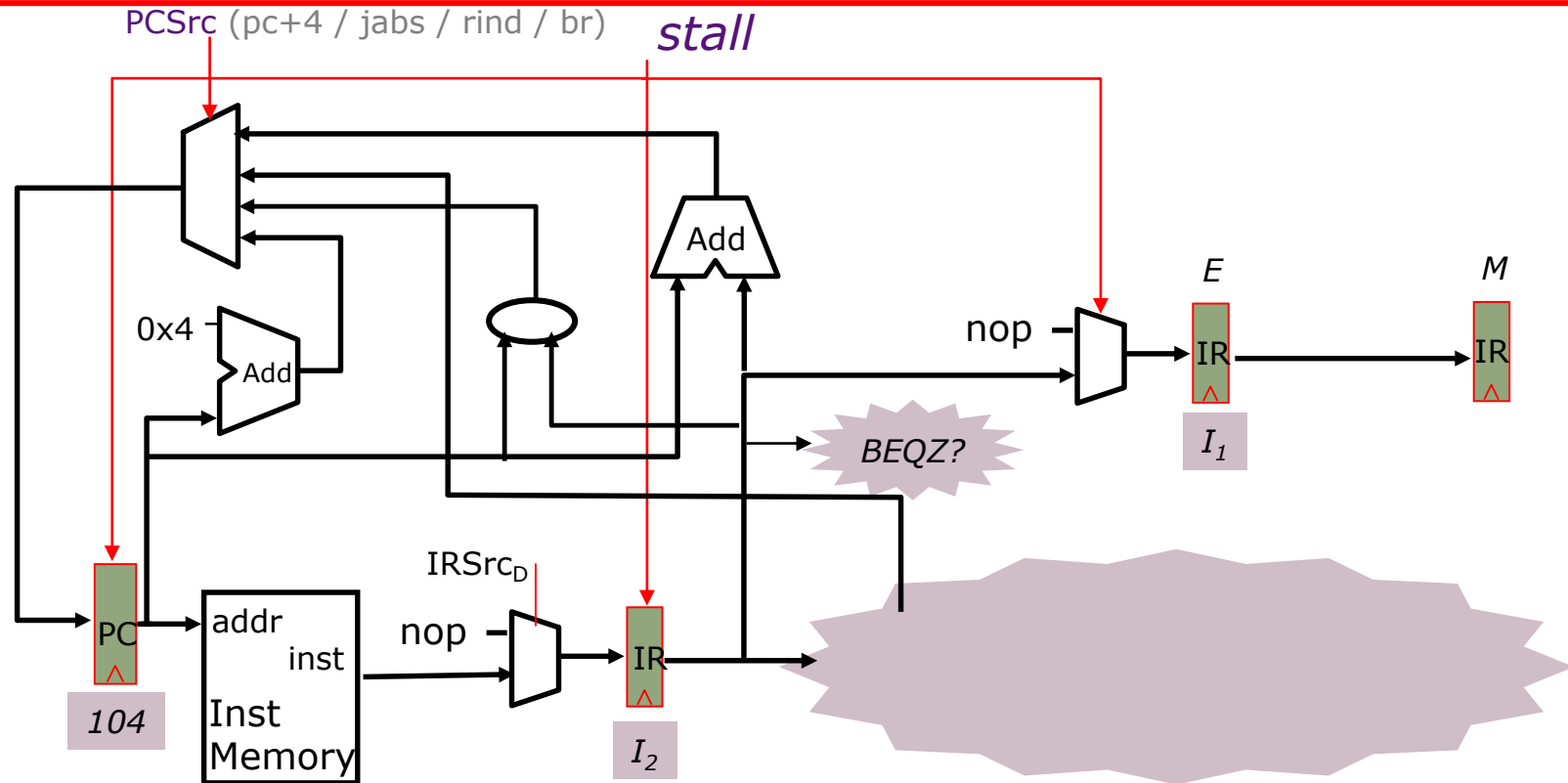


Jump Pipeline Diagrams



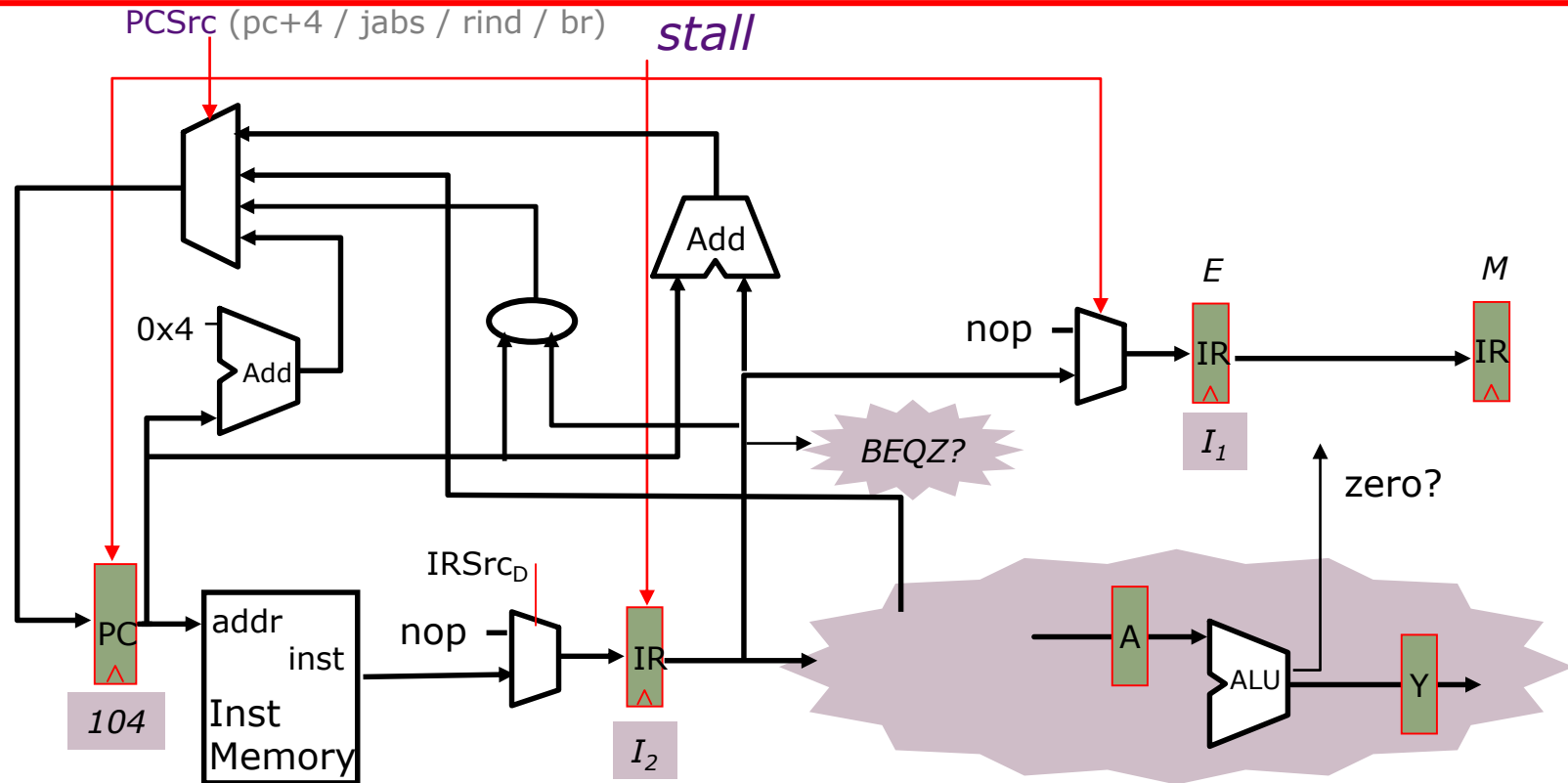
nop ⇒ *pipeline bubble*

Pipelining Conditional Branches



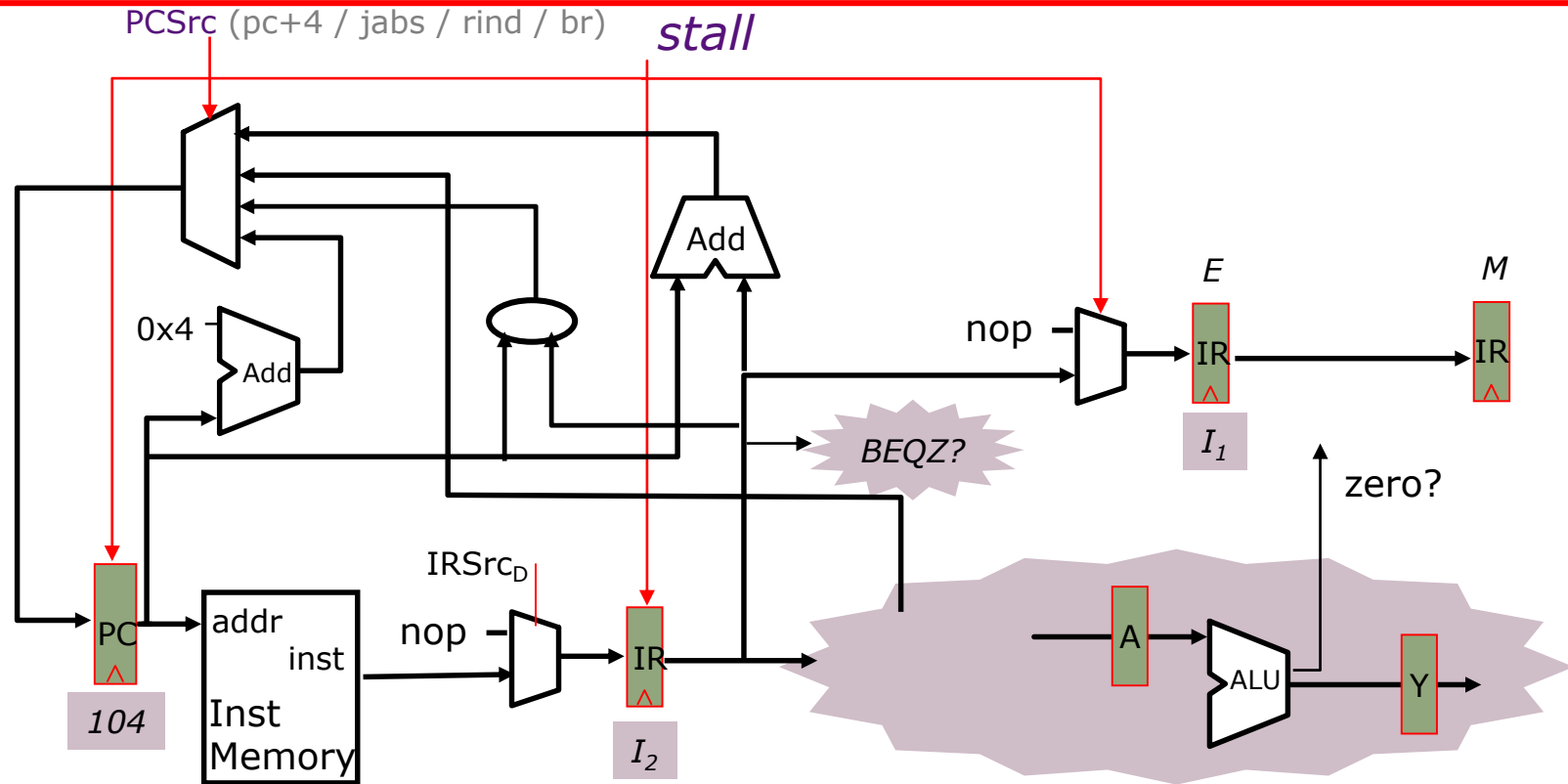
I ₁	096	ADD
I ₂	100	BEQZ r1 200
I ₃	104	ADD
I ₄	304	ADD

Pipelining Conditional Branches



I_1	096	ADD
I_2	100	BEQZ r1 200
I_3	104	ADD
I_4	304	ADD

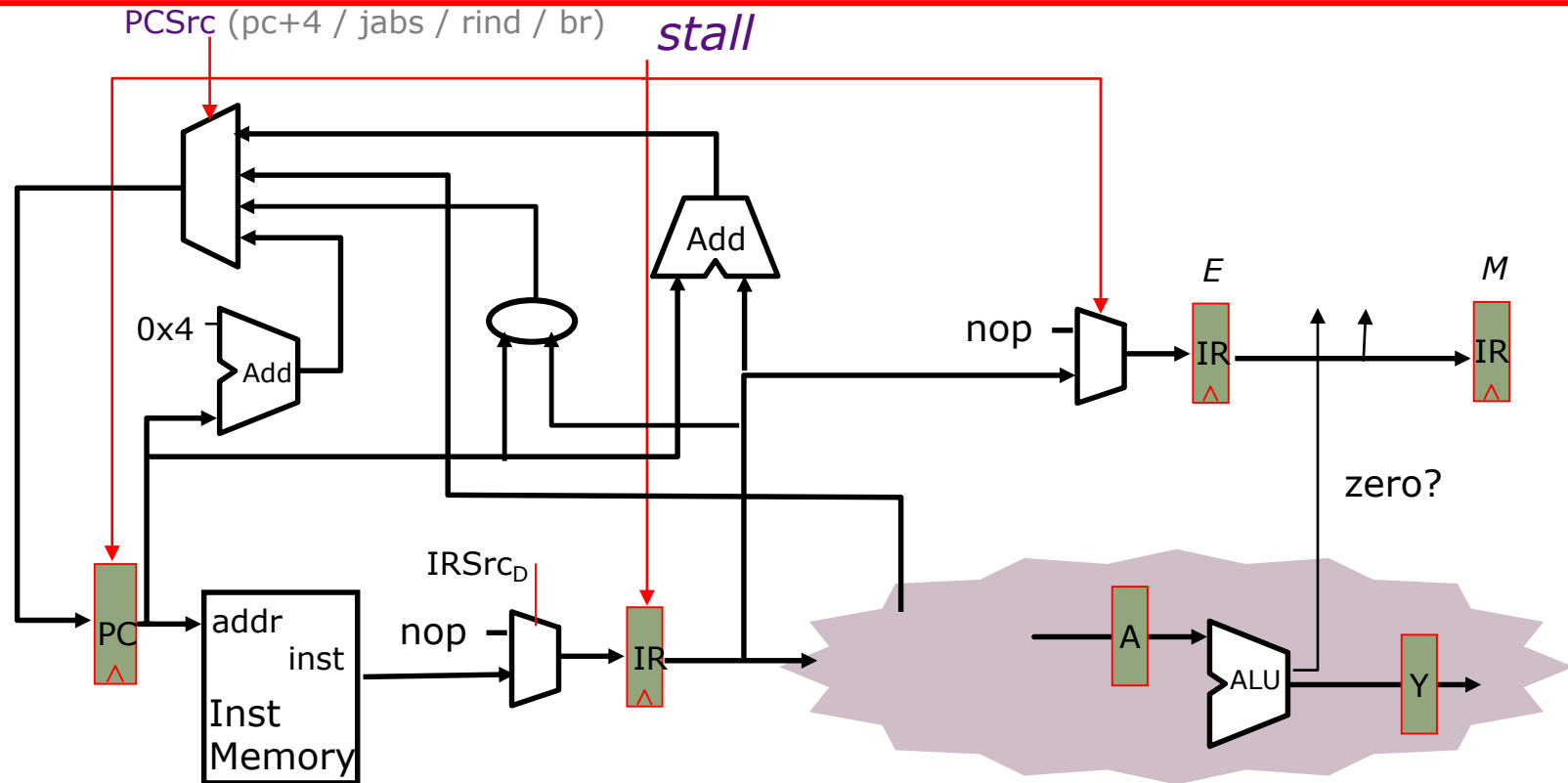
Pipelining Conditional Branches



I ₁	096	ADD
I ₂	100	BEQZ r1 200
I ₃	104	ADD
I ₄	304	ADD

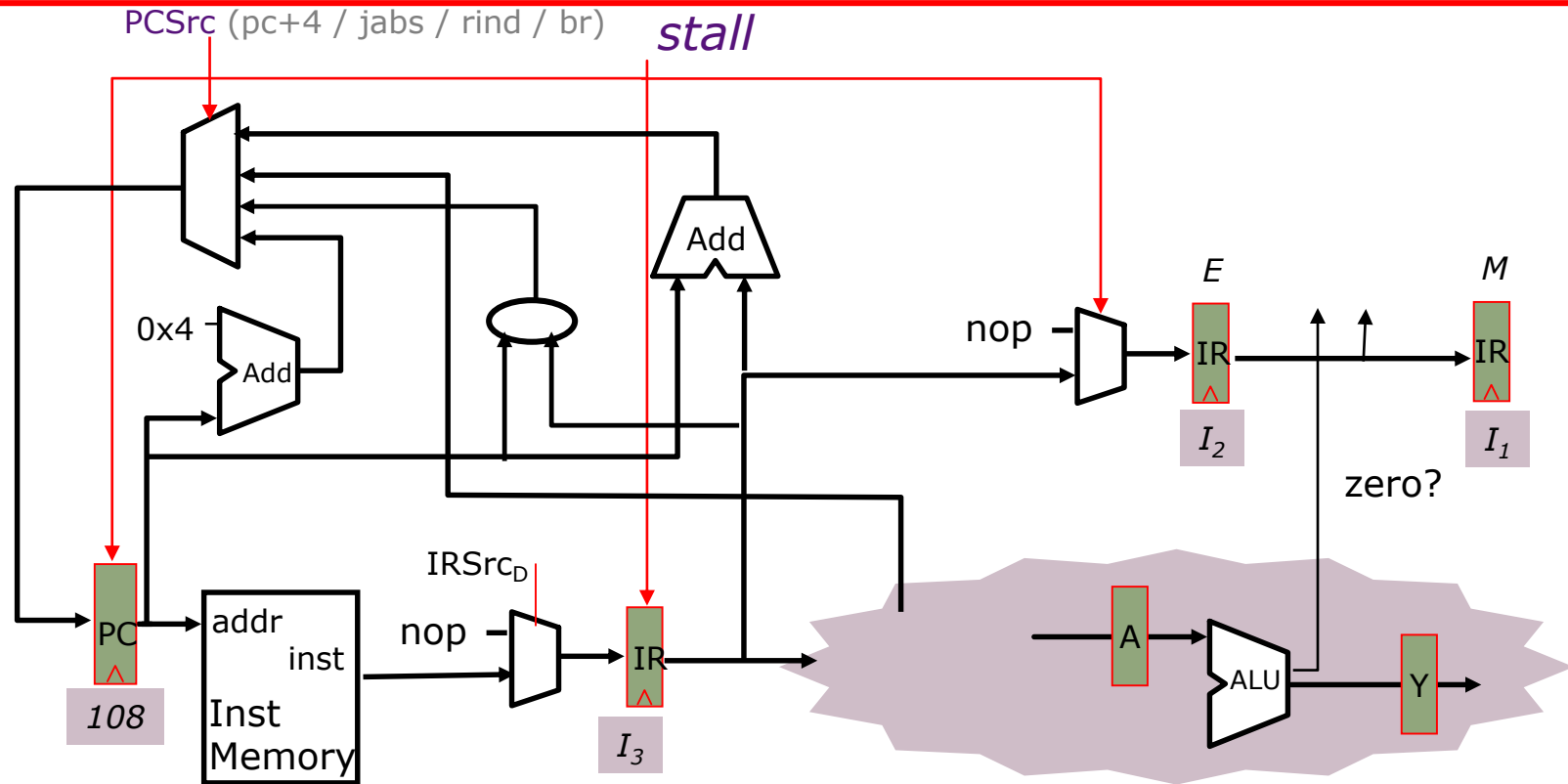
Branch condition is not known until the execute stage
what action should be taken in the decode stage?

Pipelining Conditional Branches



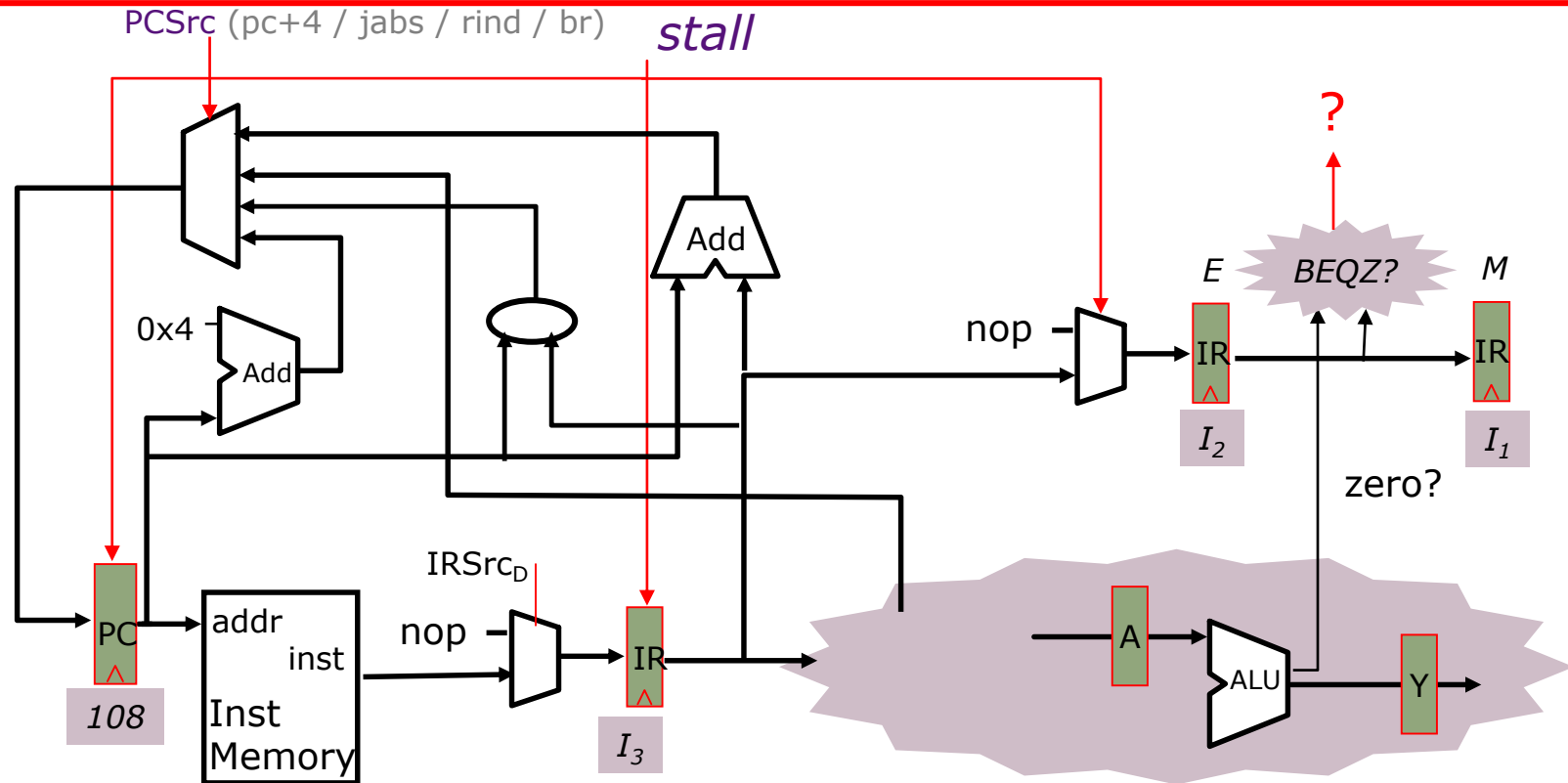
I ₁	096	ADD
I ₂	100	BEQZ r1 200
I ₃	104	ADD
I ₄	304	ADD

Pipelining Conditional Branches



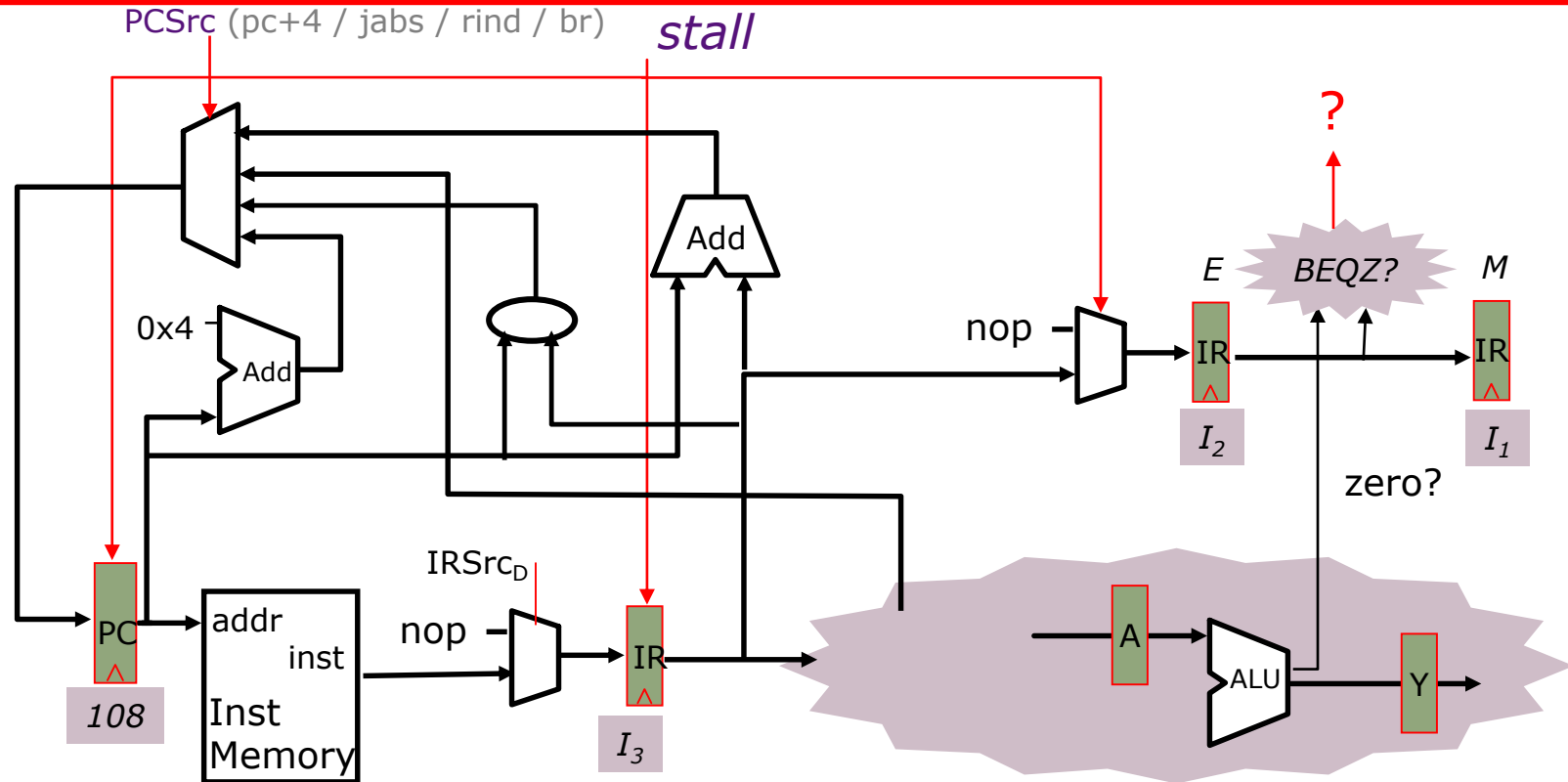
I_1	096	ADD
I_2	100	BEQZ r1 200
I_3	104	ADD
I_4	304	ADD

Pipelining Conditional Branches



I_1	096	ADD
I_2	100	BEQZ r1 200
I_3	104	ADD
I_4	304	ADD

Pipelining Conditional Branches

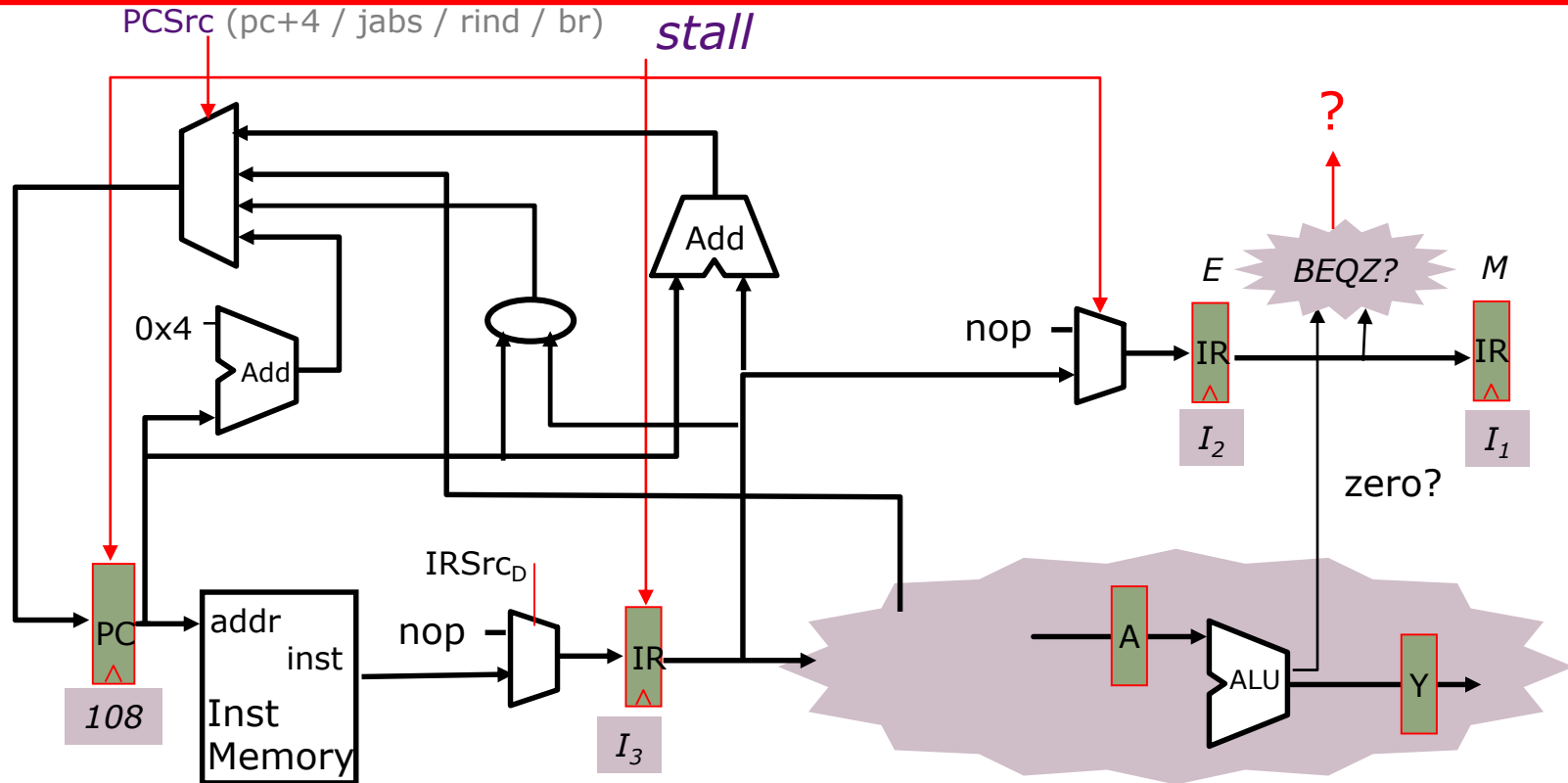


If the branch is taken

- kill the two following instructions
- the instruction at the decode stage is not valid

I_1	096	ADD
I_2	100	BEQZ r1 200
I_3	104	ADD
I_4	304	ADD

Pipelining Conditional Branches



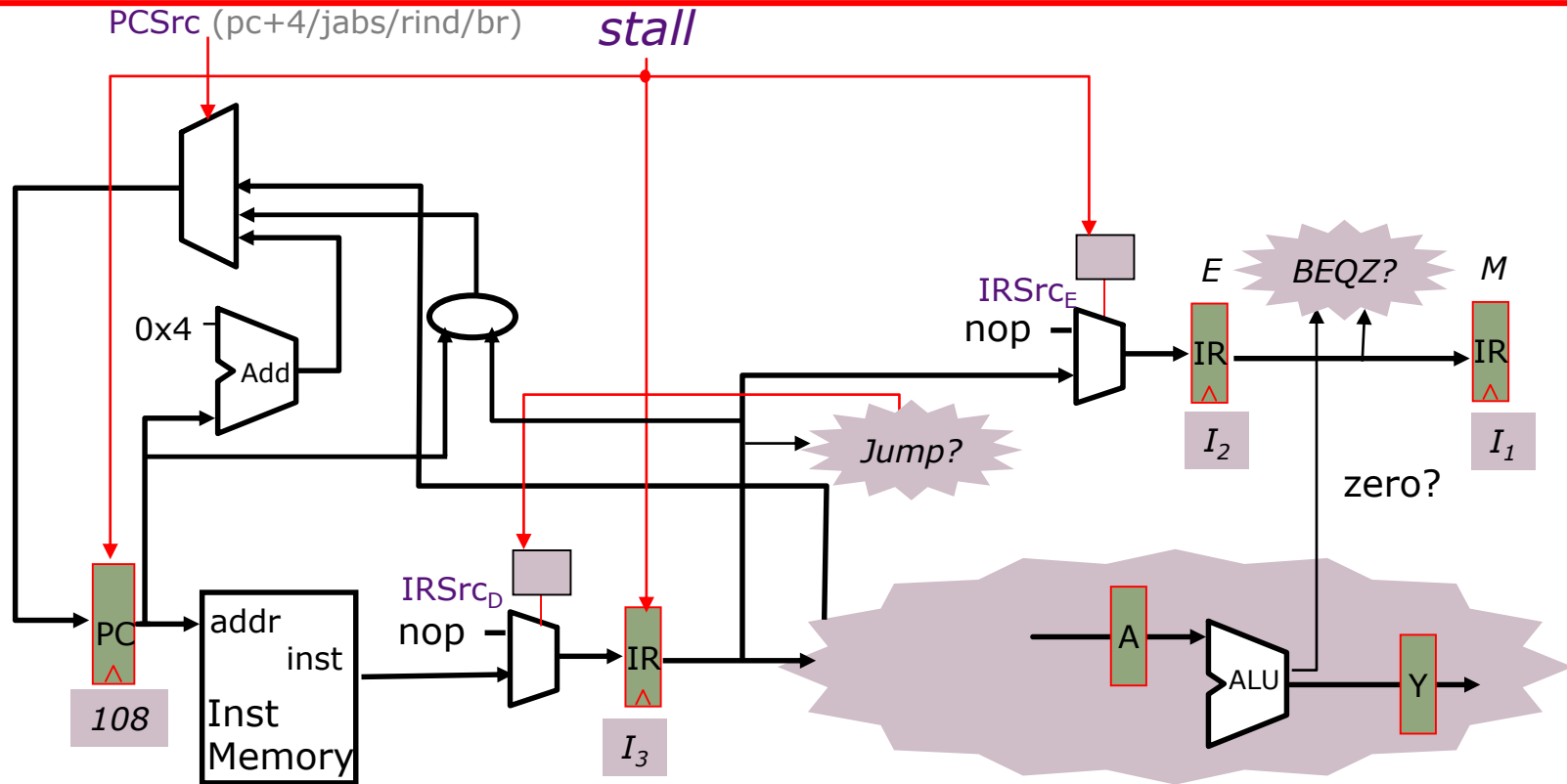
If the branch is taken

- kill the two following instructions
- the instruction at the decode stage is not valid

⇒ *stall signal is not valid*

I ₁	096	ADD
I ₂	100	BEQZ r1 200
I ₃	104	ADD
I ₄	304	ADD

Pipelining Conditional Branches



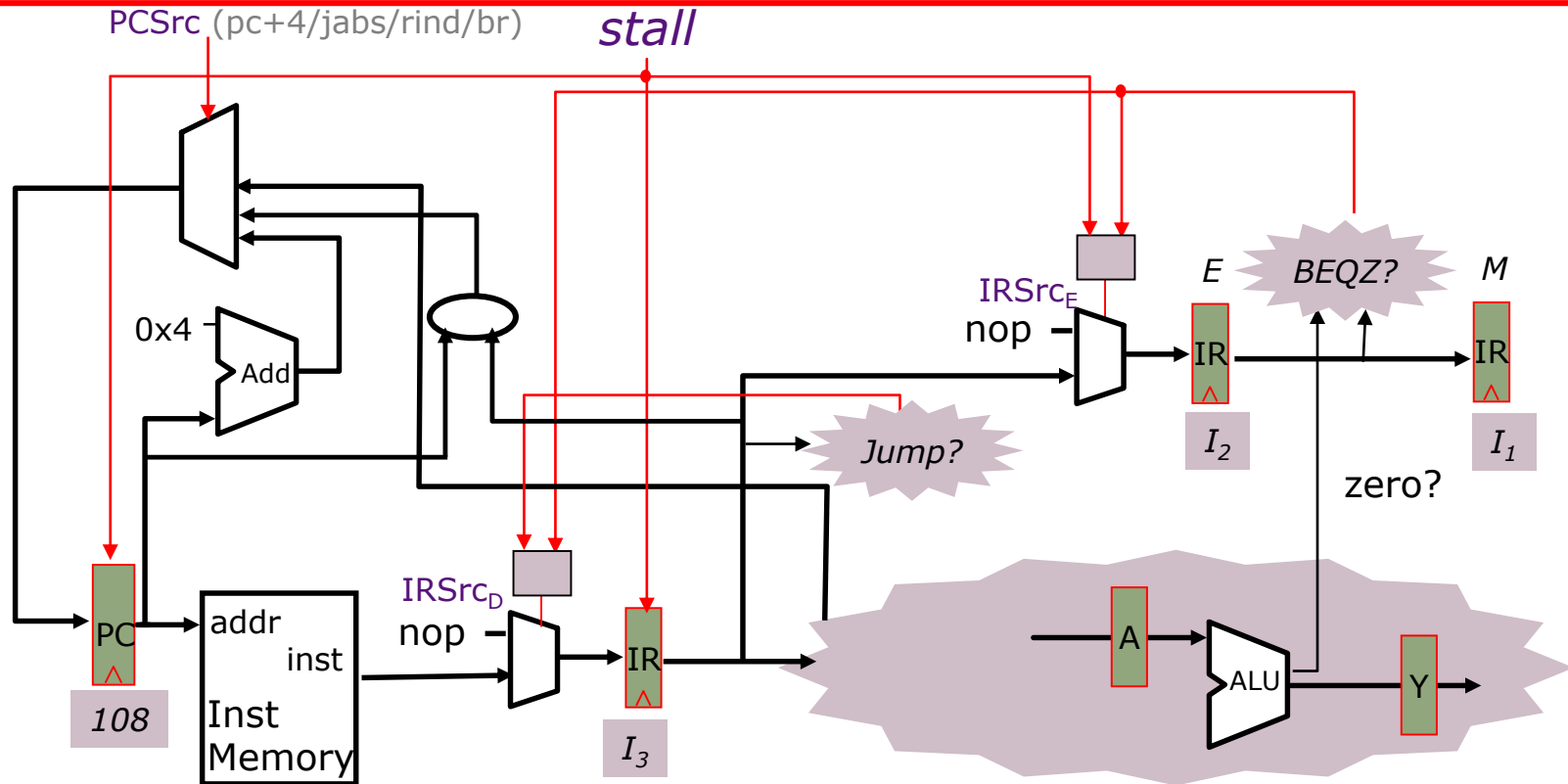
If the branch is taken

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I_1	096	ADD
I_2	100	BEQZ r1 200
I_3	104	ADD
I_4	304	ADD

Pipelining Conditional Branches



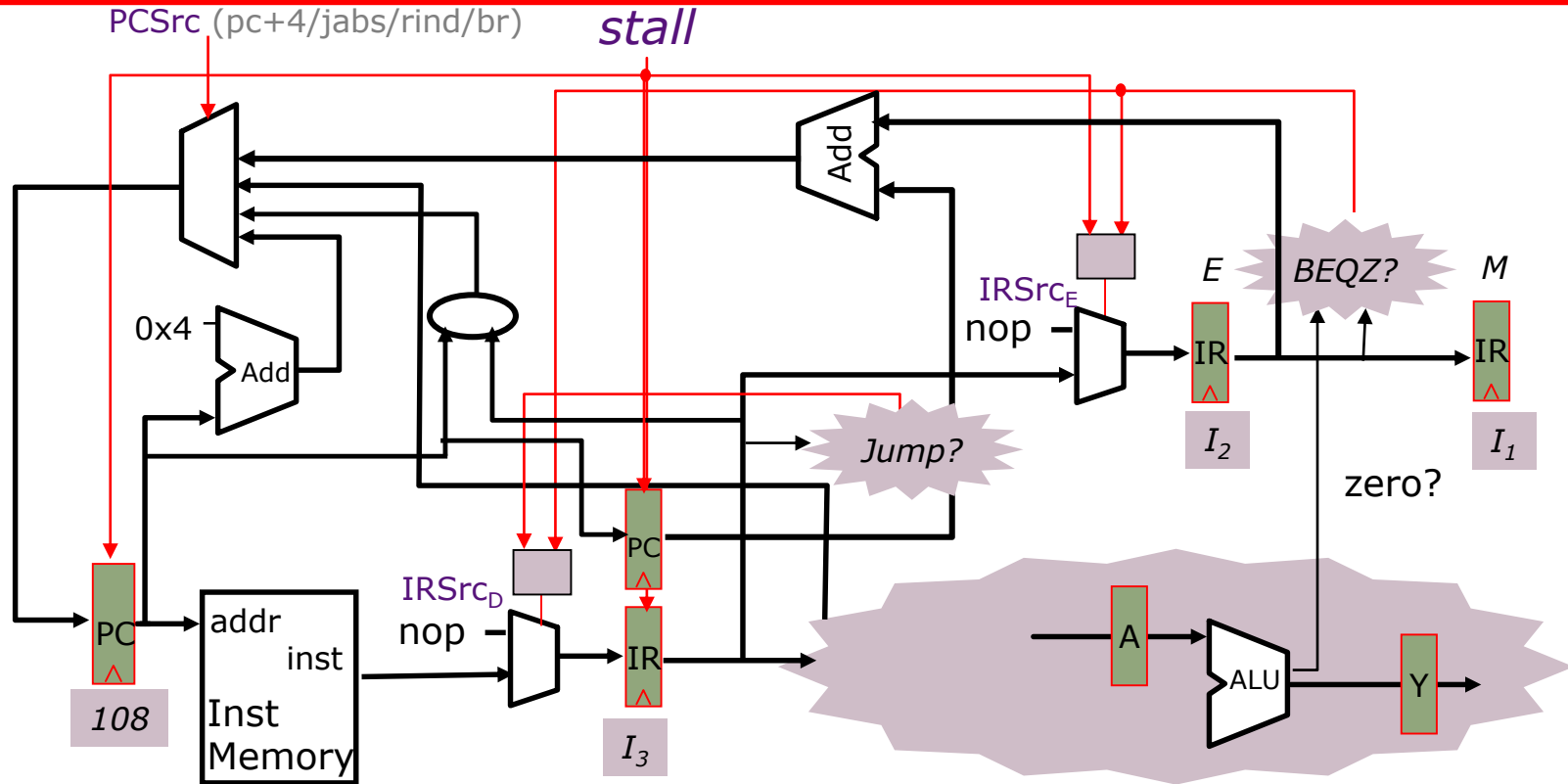
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I ₃	104	ADD
I ₄	304	ADD

Pipelining Conditional Branches



If the branch is taken

- kill the two following instructions
- the instruction at the decode stage is not valid

⇒ *stall signal is not valid*

I ₁	096	ADD
I ₂	100	BEQZ r1 200
I ₃	104	ADD
I ₄	304	ADD

New Stall Signal

$$\text{stall} = (((rs_D == ws_E) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D \\ + ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D \\) \cdot !((opcode_E == BEQZ) \cdot z + (opcode_E == BNEZ) \cdot !z)$$

Don't stall if the branch is taken. Why?

New Stall Signal

$$\text{stall} = (((rs_D == ws_E) \cdot we_E + (rs_D == ws_M) \cdot we_M + (rs_D == ws_W) \cdot we_W) \cdot re1_D \\ + ((rt_D == ws_E) \cdot we_E + (rt_D == ws_M) \cdot we_M + (rt_D == ws_W) \cdot we_W) \cdot re2_D \\) \cdot !((opcode_E == BEQZ) \cdot z + (opcode_E == BNEZ) \cdot !z)$$

Don't stall if the branch is taken. Why?

Instruction at the decode stage is invalid

Control Equations for PC and IR Muxes

$IRSrc_D = \text{Case opcode}_E$
BEQZ·z, BNEZ·!z \Rightarrow nop
... \Rightarrow
Case opcode_D
J, JAL, JR, JALR \Rightarrow nop
... \Rightarrow IM

$IRSrc_E = \text{Case opcode}_E$
BEQZ·z, BNEZ·!z \Rightarrow nop
... \Rightarrow stall·nop + !stall·IR_D

$PCSrc = \text{Case opcode}_E$
BEQZ·z, BNEZ·!z \Rightarrow br
... \Rightarrow
Case opcode_D
J, JAL \Rightarrow jabs
JR, JALR \Rightarrow rind
... \Rightarrow pc+4

nop \Rightarrow Kill
br/jabs/rind \Rightarrow Restart
pc+4 \Rightarrow Speculate

Control Equations for PC and IR Muxes

$IRSrc_D = \text{Case opcode}_E$
 $\text{BEQZ}\cdot z, \text{BNEZ}\cdot !z \Rightarrow \text{nop}$
 $\dots \Rightarrow$
 Case opcode_D
 $\text{J, JAL, JR, JALR} \Rightarrow \text{nop}$
 $\dots \Rightarrow \text{IM}$

Give priority to the older instruction, i.e., execute stage instruction over decode stage instruction

$IRSrc_E = \text{Case opcode}_E$
 $\text{BEQZ}\cdot z, \text{BNEZ}\cdot !z \Rightarrow \text{nop}$
 $\dots \Rightarrow \text{stall}\cdot \text{nop} + !\text{stall}\cdot IR_D$

$PCSrc = \text{Case opcode}_E$
 $\text{BEQZ}\cdot z, \text{BNEZ}\cdot !z \Rightarrow \text{br}$
 $\dots \Rightarrow$
 Case opcode_D
 $\text{J, JAL} \Rightarrow \text{jabs}$
 $\text{JR, JALR} \Rightarrow \text{rind}$
 $\dots \Rightarrow \text{pc}+4$

$\text{nop} \Rightarrow \text{Kill}$
 $\text{br/jabs/rind} \Rightarrow \text{Restart}$
 $\text{pc}+4 \Rightarrow \text{Speculate}$

Control Equations for PC and IR Muxes

$IRSrc_D = \text{Case opcode}_E$
 $\text{BEQZ}\cdot z, \text{BNEZ}\cdot !z \Rightarrow \text{nop}$
 $\dots \Rightarrow$
 Case opcode_D
 $\text{J, JAL, JR, JALR} \Rightarrow \text{nop}$
 $\dots \Rightarrow \text{IM}$

Give priority to the older instruction, i.e., execute stage instruction over decode stage instruction

$IRSrc_E = \text{Case opcode}_E$
 $\text{BEQZ}\cdot z, \text{BNEZ}\cdot !z \Rightarrow \text{nop}$
 $\dots \Rightarrow \text{stall}\cdot \text{nop} + !\text{stall}\cdot IR_D$

$PCSrc = \text{Case opcode}_E$
 $\text{BEQZ}\cdot z, \text{BNEZ}\cdot !z \Rightarrow \text{br}$
 $\dots \Rightarrow$
 Case opcode_D
 $\text{J, JAL} \Rightarrow \text{jabs}$
 $\text{JR, JALR} \Rightarrow \text{rind}$
 $\dots \Rightarrow \text{pc}+4$

pc+4 is a speculative guess

$\text{nop} \Rightarrow \text{Kill}$
 $\text{br/jabs/rind} \Rightarrow \text{Restart}$
 $\text{pc}+4 \Rightarrow \text{Speculate}$

Branch Pipeline Diagrams

(resolved in execute stage)

Branch Pipeline Diagrams

(resolved in execute stage)

time
t0 t1 t2 t3 t4 t5 t6 t7

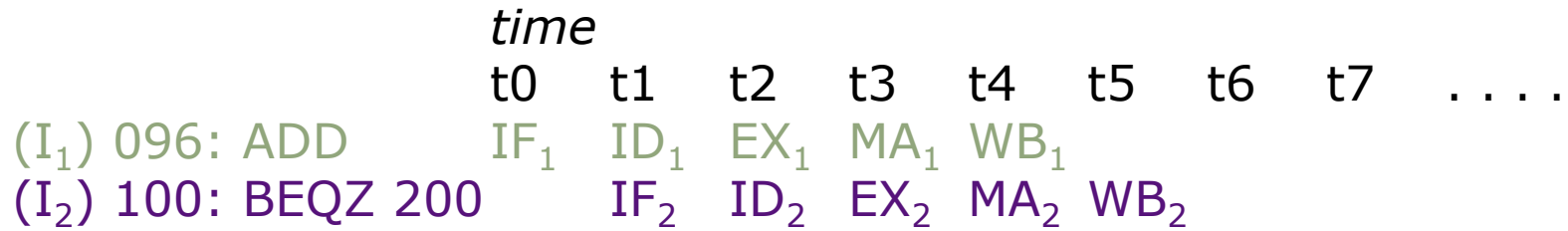
Branch Pipeline Diagrams

(resolved in execute stage)

	<i>time</i>									
	t0	t1	t2	t3	t4	t5	t6	t7
(I ₁) 096: ADD	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁					

Branch Pipeline Diagrams

(resolved in execute stage)



Branch Pipeline Diagrams

(resolved in execute stage)

	<i>time</i>								
	t0	t1	t2	t3	t4	t5	t6	t7
(I ₁) 096: ADD	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁				
(I ₂) 100: BEQZ 200		IF ₂	ID ₂	EX ₂	MA ₂	WB ₂			
(I ₃) 104: ADD			IF ₃	ID ₃	nop	nop	nop		

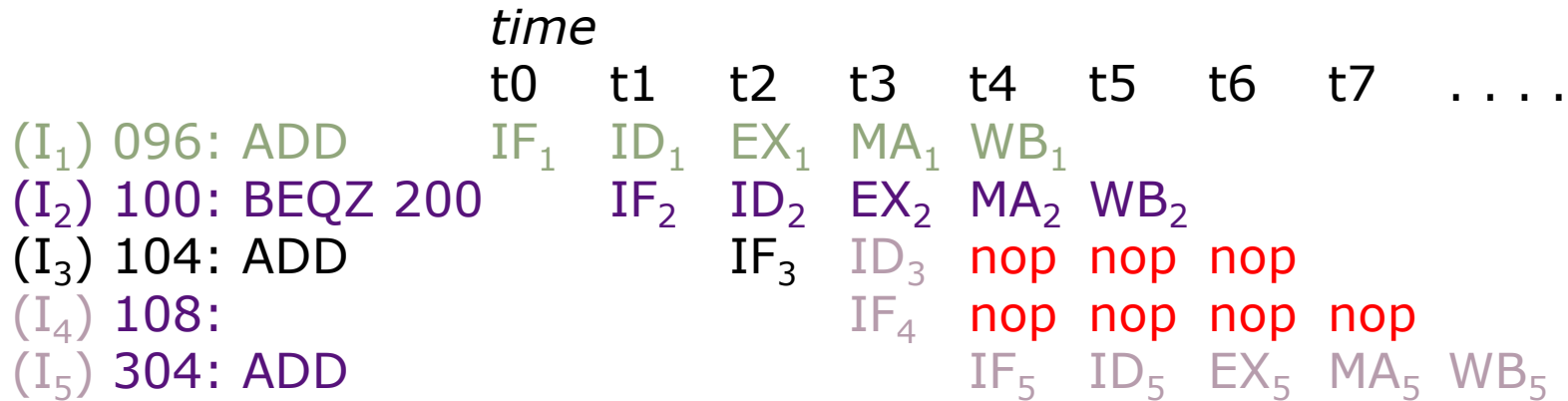
Branch Pipeline Diagrams

(resolved in execute stage)

	<i>time</i>								
	t0	t1	t2	t3	t4	t5	t6	t7	...
(I ₁) 096: ADD	IF ₁	ID ₁	EX ₁	MA ₁	WB ₁				
(I ₂) 100: BEQZ 200		IF ₂	ID ₂	EX ₂	MA ₂	WB ₂			
(I ₃) 104: ADD			IF ₃	ID ₃	nop	nop	nop		
(I ₄) 108:				IF ₄	nop	nop	nop	nop	

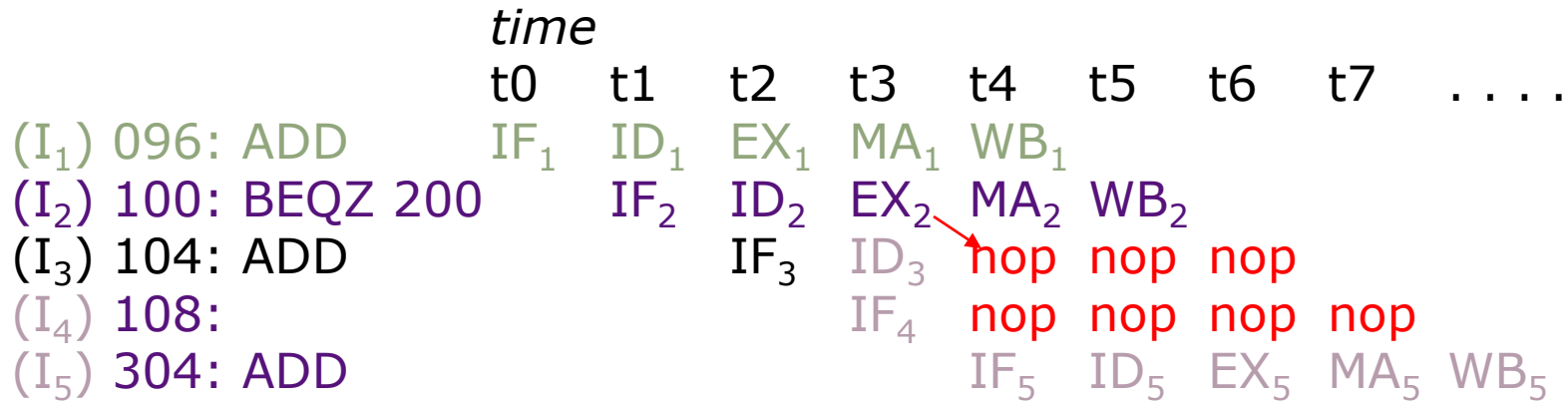
Branch Pipeline Diagrams

(resolved in execute stage)



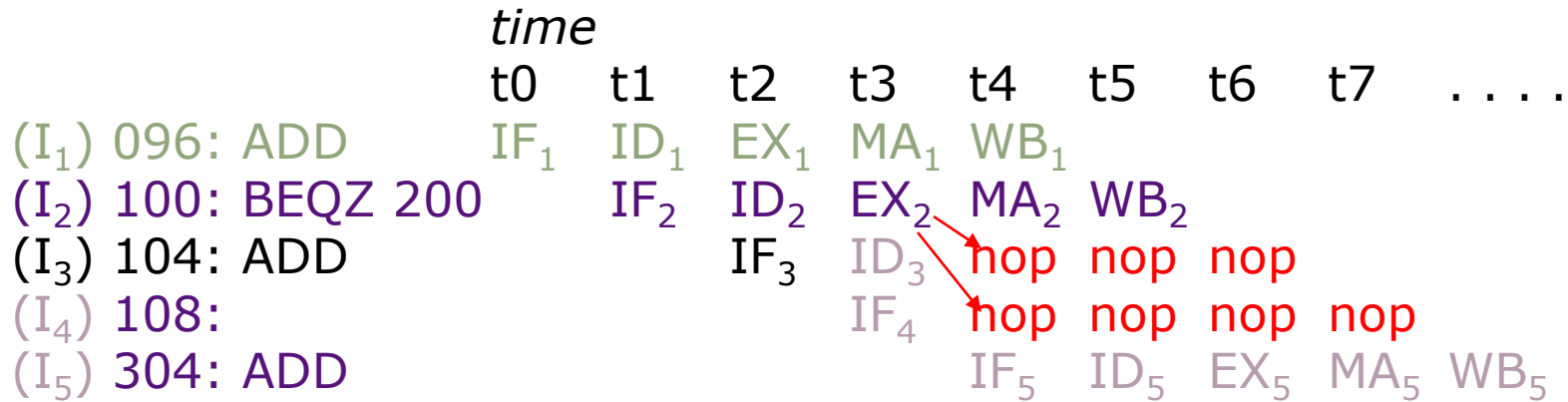
Branch Pipeline Diagrams

(resolved in execute stage)



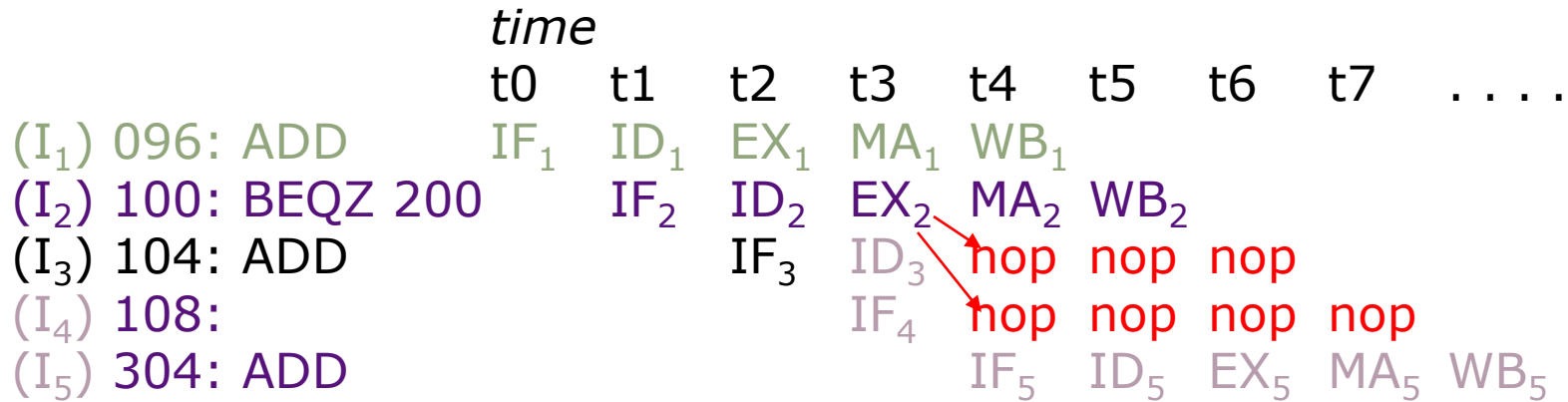
Branch Pipeline Diagrams

(resolved in execute stage)



Branch Pipeline Diagrams

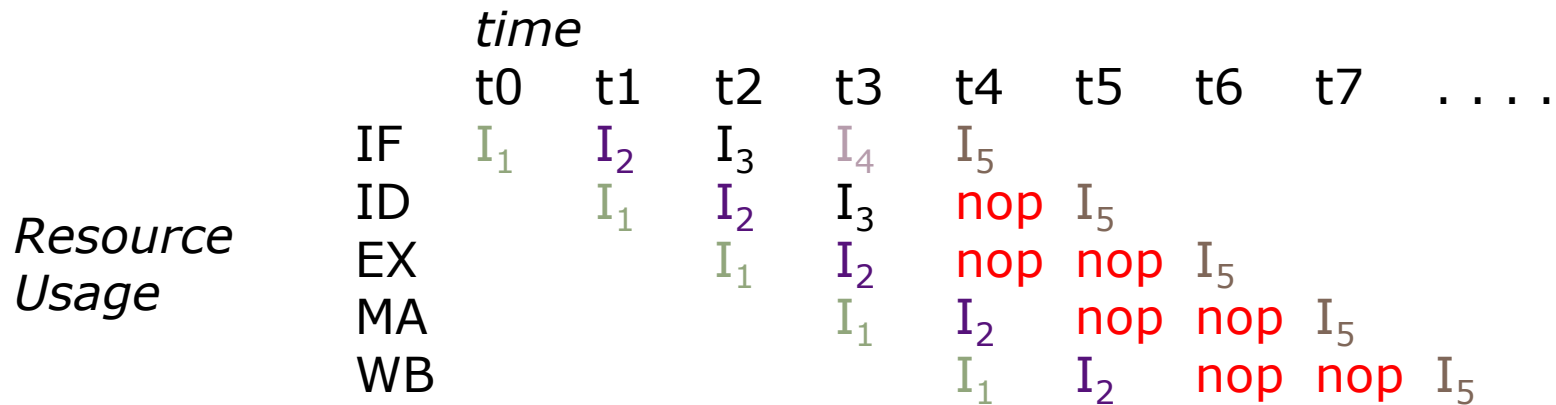
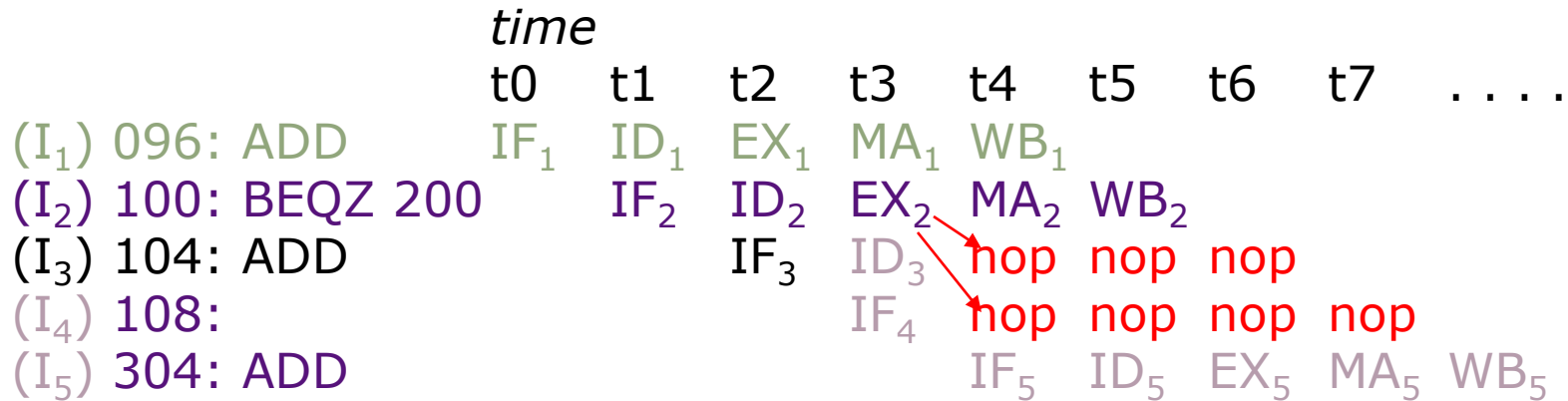
(resolved in execute stage)



*Resource
Usage*

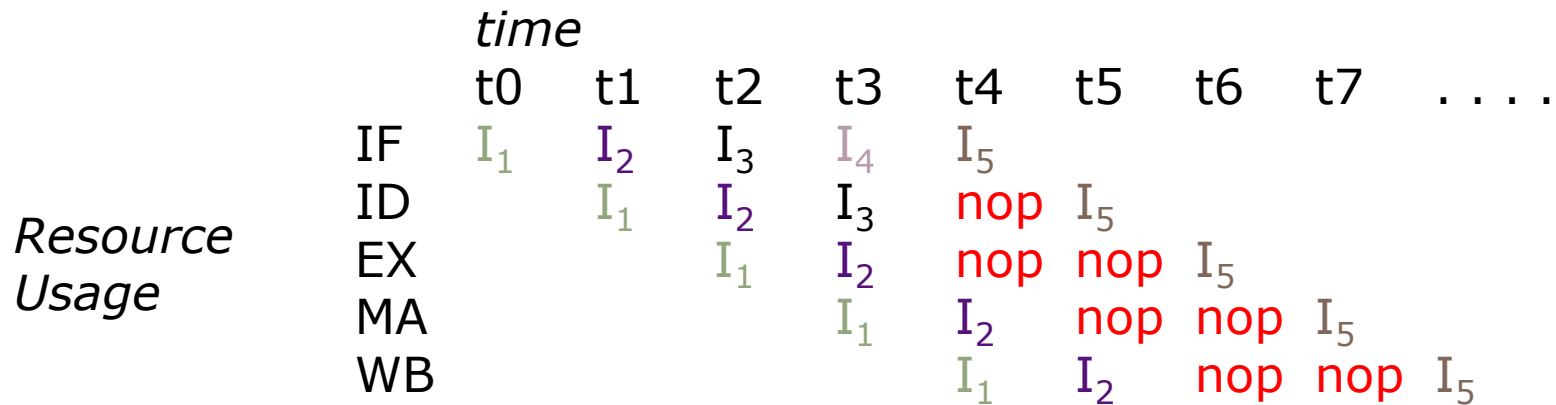
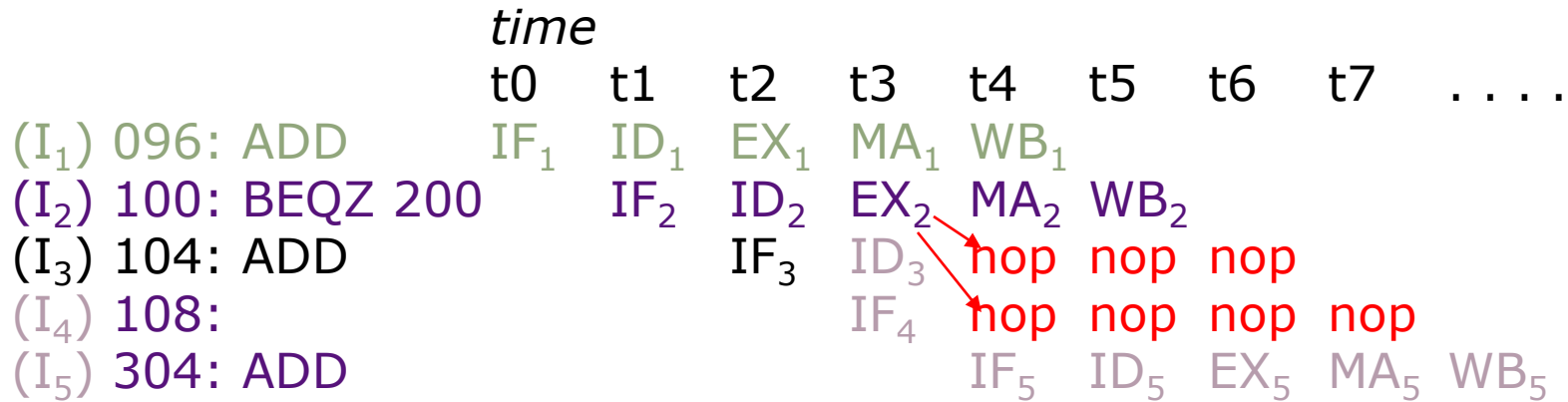
Branch Pipeline Diagrams

(resolved in execute stage)



Branch Pipeline Diagrams

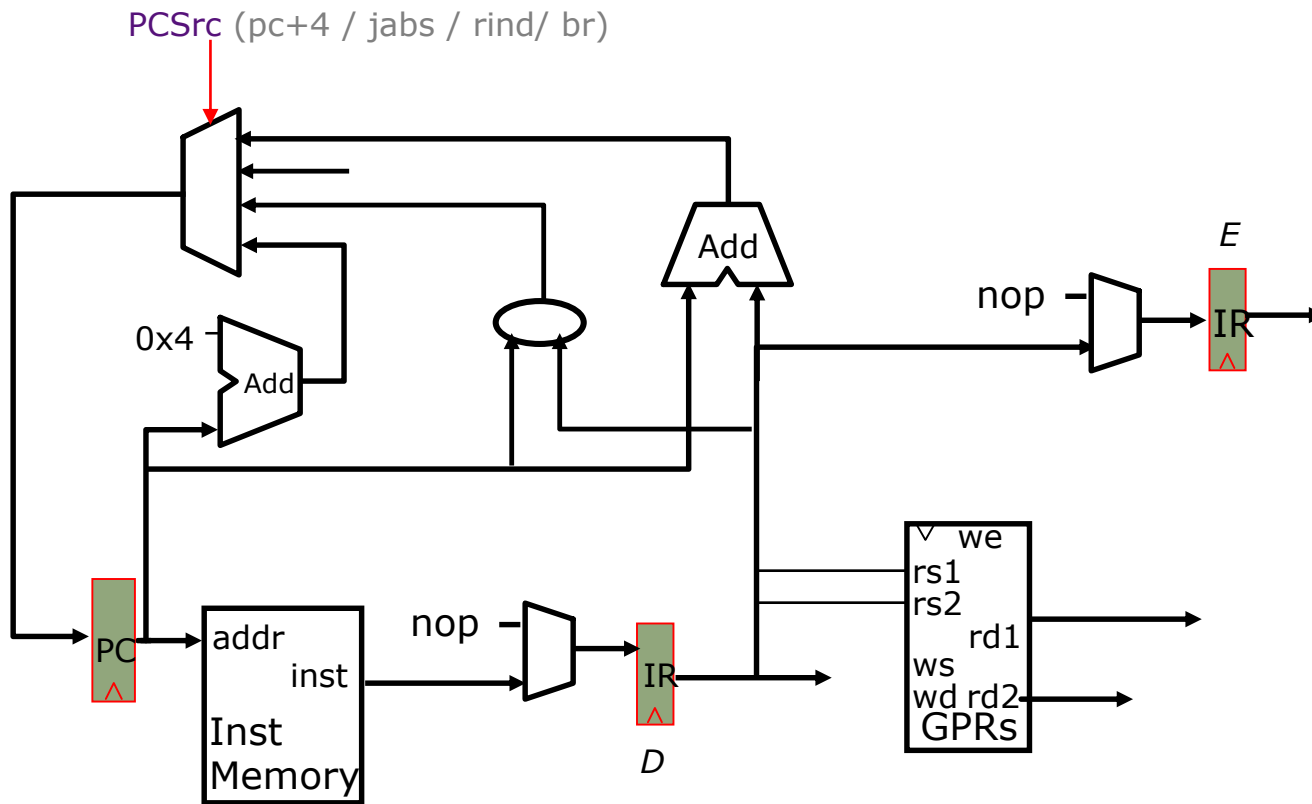
(resolved in execute stage)



nop ⇒ *pipeline bubble*

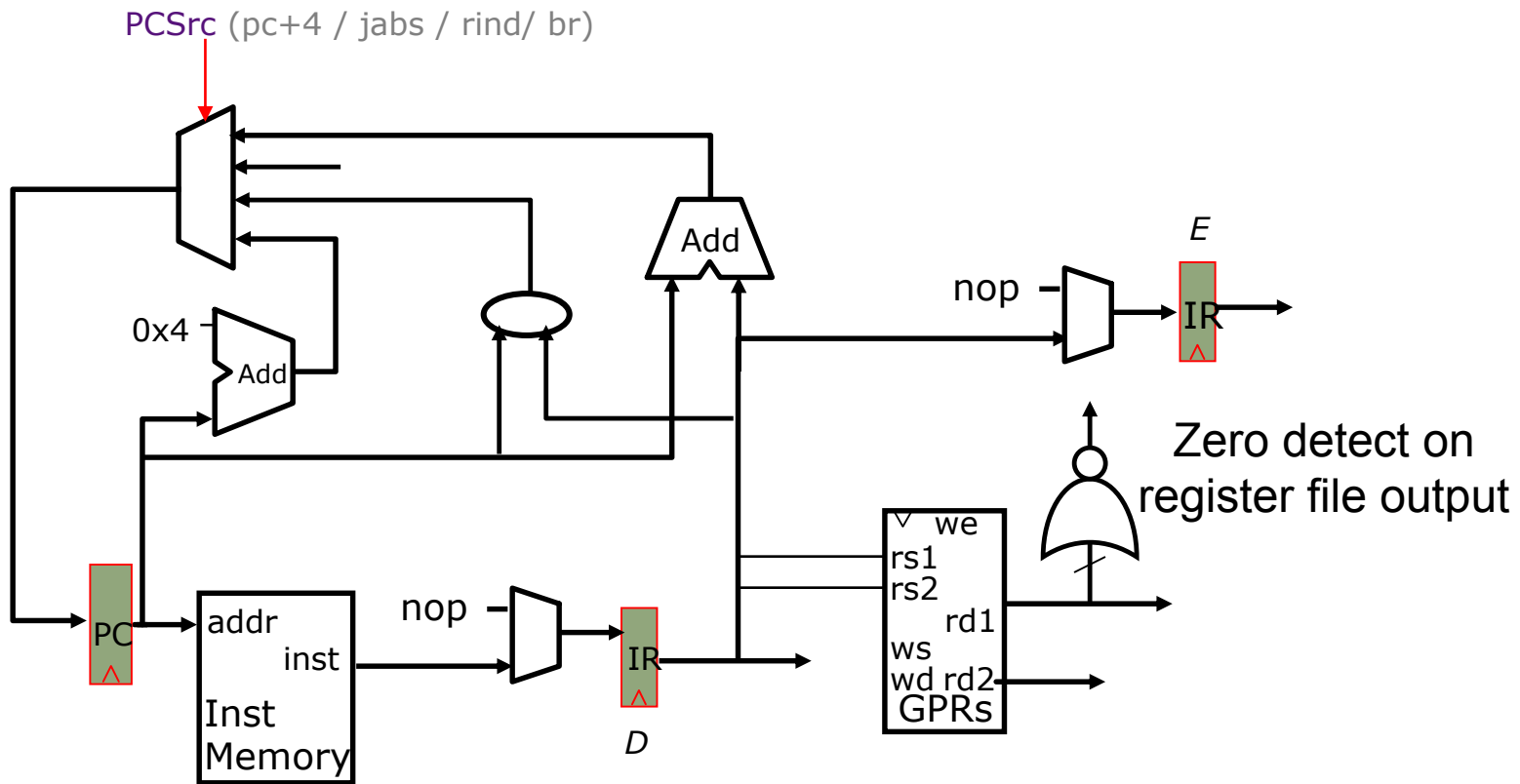
Reducing Branch Penalty (resolve in decode stage)

- One pipeline bubble can be removed if an extra comparator is used in the Decode stage



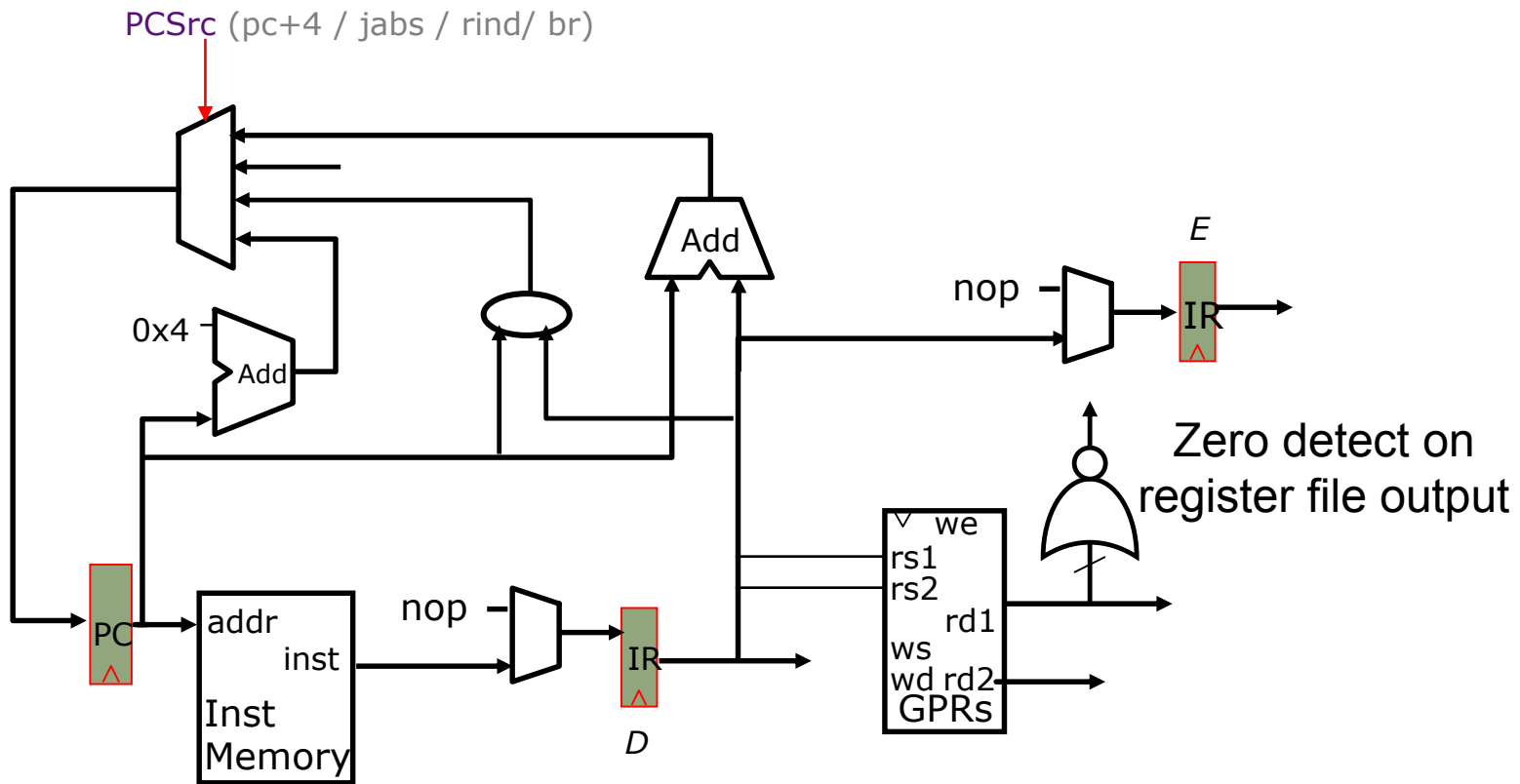
Reducing Branch Penalty (resolve in decode stage)

- One pipeline bubble can be removed if an extra comparator is used in the Decode stage



Reducing Branch Penalty (resolve in decode stage)

- One pipeline bubble can be removed if an extra comparator is used in the Decode stage



Pipeline diagram now same as for jumps

Branch Delay Slots

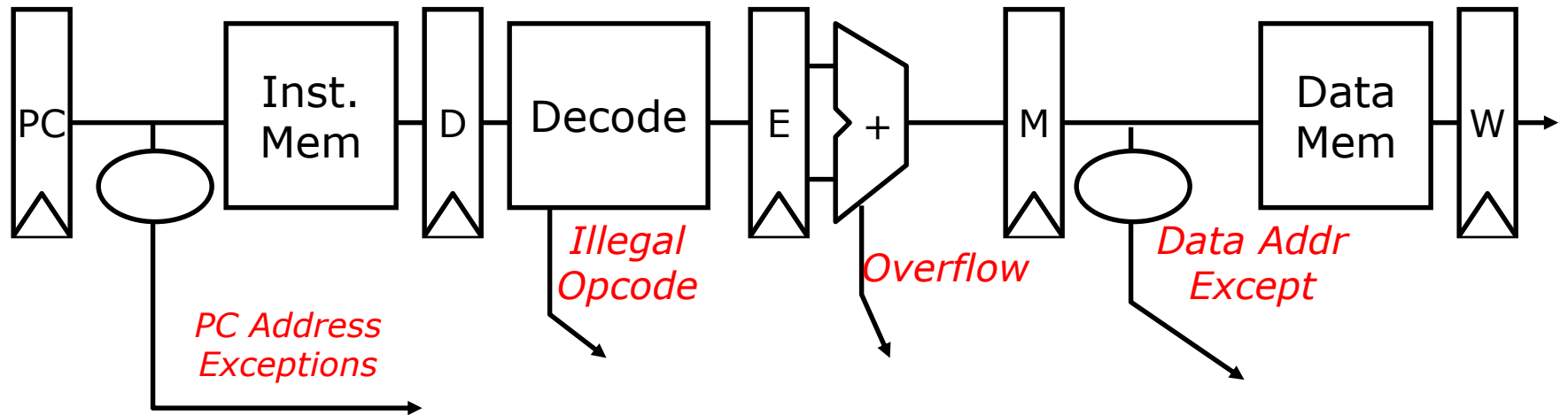
(expose control hazard to software)

- Change the ISA semantics so that the instruction that follows a jump or branch is always executed
 - gives compiler the flexibility to put in a useful instruction where normally a pipeline bubble would have resulted.

I ₁	096	ADD	
I ₂	100	BEQZ r1 200	<i>Delay slot instruction</i>
I ₃	104	ADD	← <i>executed regardless of</i>
I ₄	304	ADD	<i>branch outcome</i>

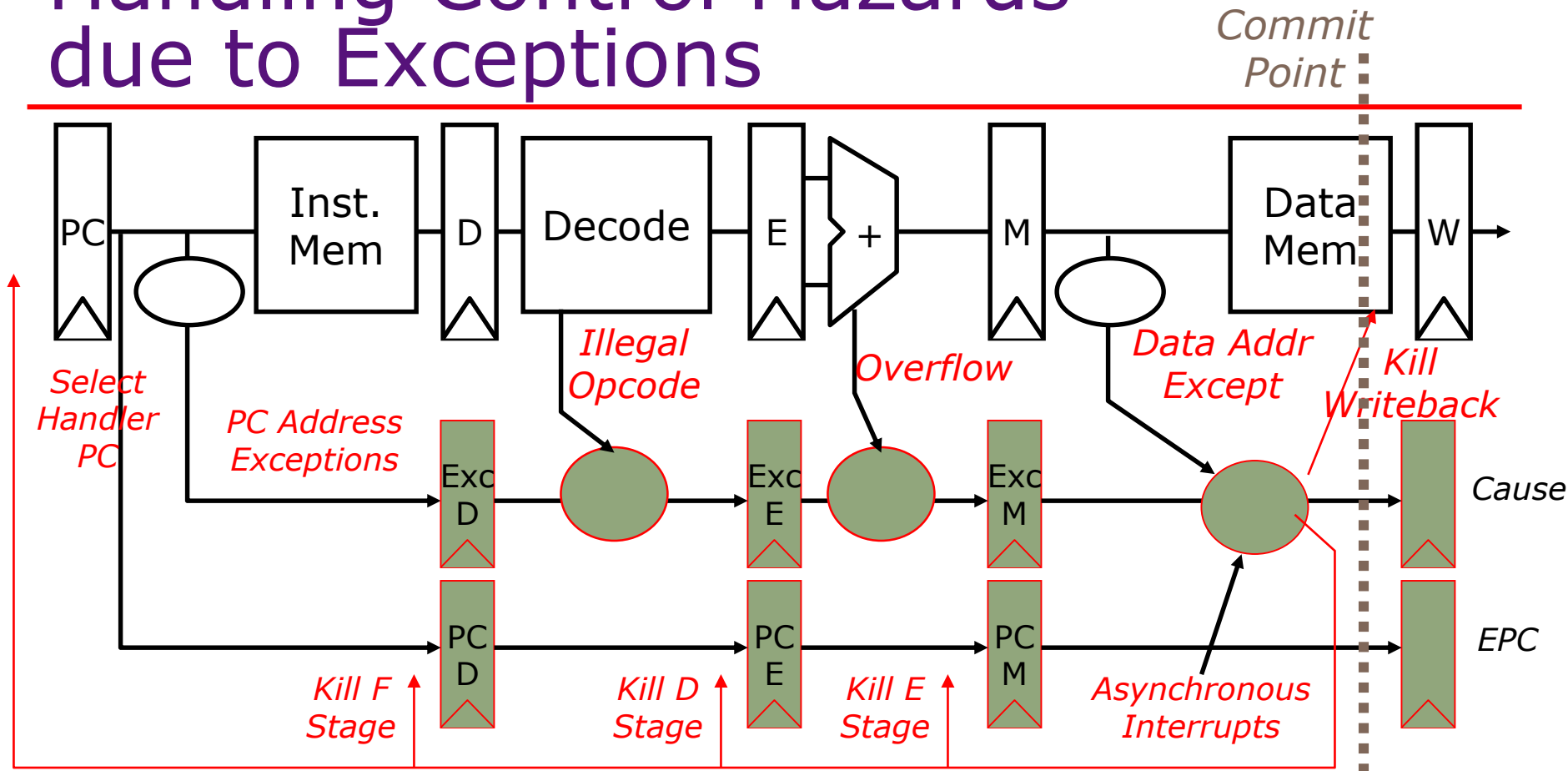
- Other techniques include branch prediction, which can dramatically reduce the branch penalty... *to come later*

Handling Control Hazards due to Exceptions



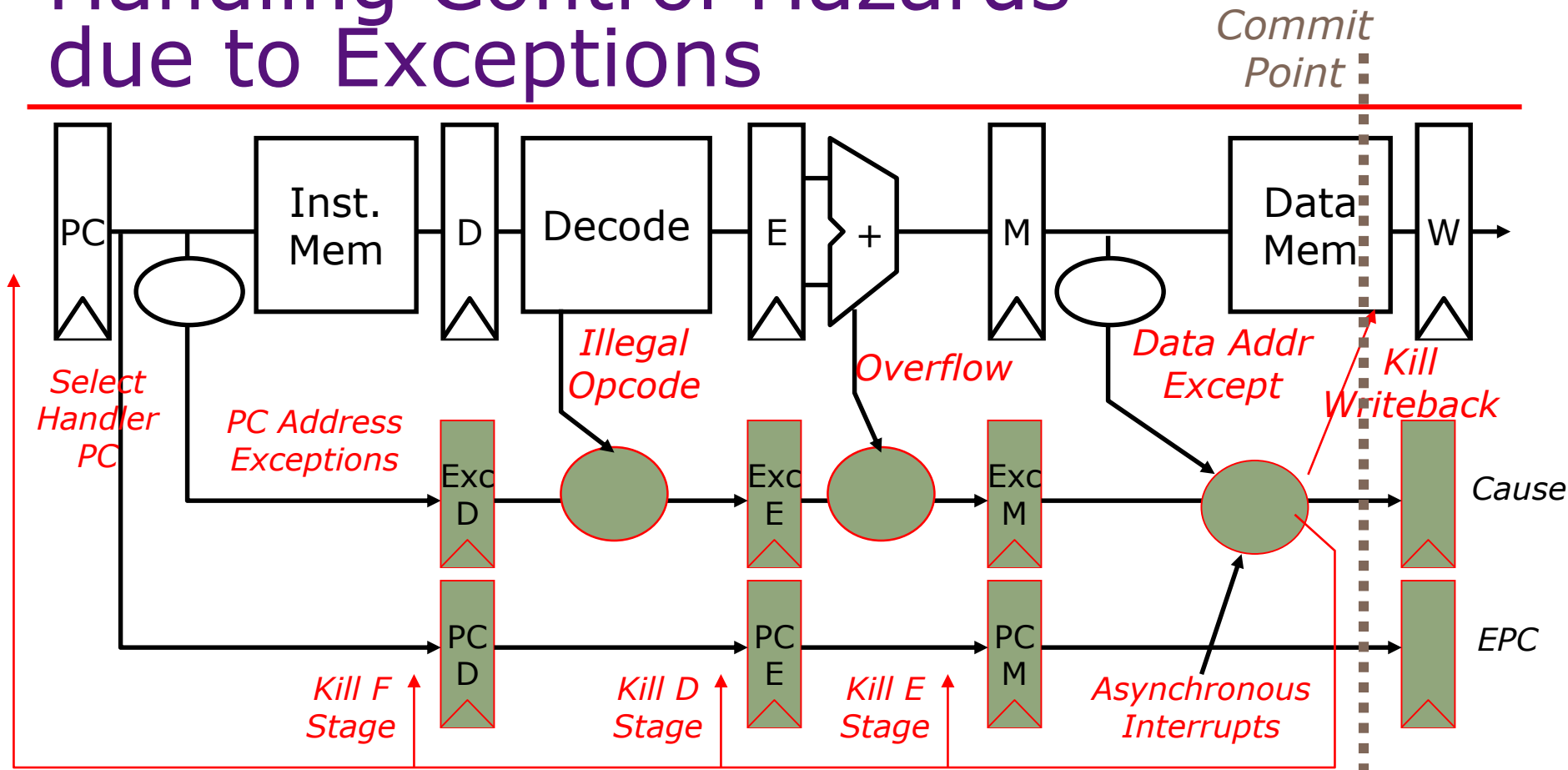
- Instructions may suffer exceptions in different pipeline stages
- Must prioritize exceptions from earlier instructions

Handling Control Hazards due to Exceptions



- Typical strategy: Record exceptions, process the first one to reach commit point (i.e., the point where architectural state is modified)

Handling Control Hazards due to Exceptions



- Typical strategy: Record exceptions, process the first one to reach commit point (i.e., the point where architectural state is modified)
 - *Pros/cons vs handling exceptions eagerly, like branches?*

Why an instruction may not be dispatched every cycle (CPI>1)

- Full bypassing may be too expensive to implement
 - Typically all frequently used paths are provided
 - Some infrequently used bypass paths may increase cycle time and counteract the benefit of reducing CPI
- Loads have two-cycle latency
 - Instruction after load cannot use load result
 - MIPS-I ISA defined *load delay slots*, a software-visible pipeline hazard (compiler schedules independent instruction or inserts NOP to avoid hazard). Removed in MIPS-II.
- Conditional branches, jumps, and exceptions may cause bubbles
 - Kill instruction(s) following branch if no delay slots

Machines with software-visible delay slots may execute significant number of NOP instructions inserted by the compiler.

Next lecture:
Superscalar & Scoreboarded
Pipelines