

Security

*Joel Emer**

Computer Science & Artificial Intelligence Lab
M.I.T.

*With some slide credits to: Chris Fletcher and Mengia Yan

Security and Information Leakage

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 - Specify *what* should happen, not *when*

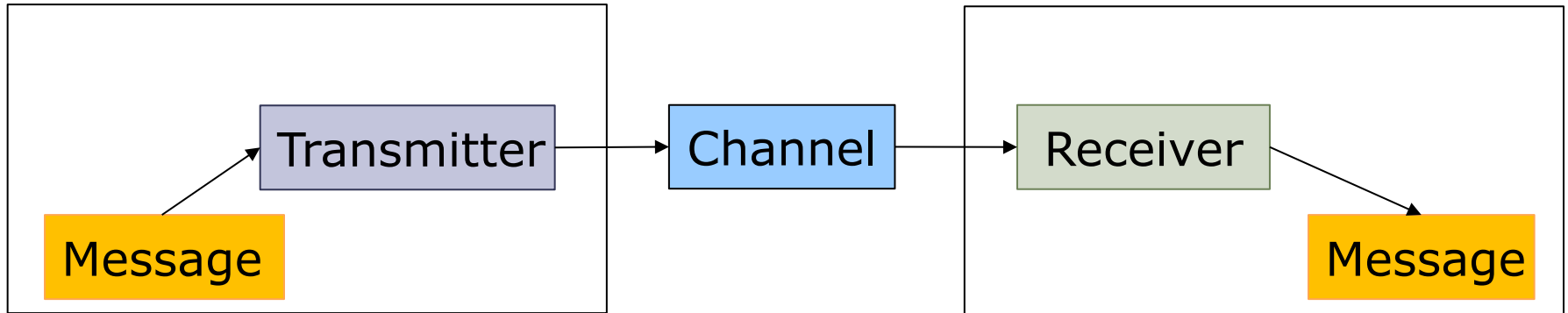
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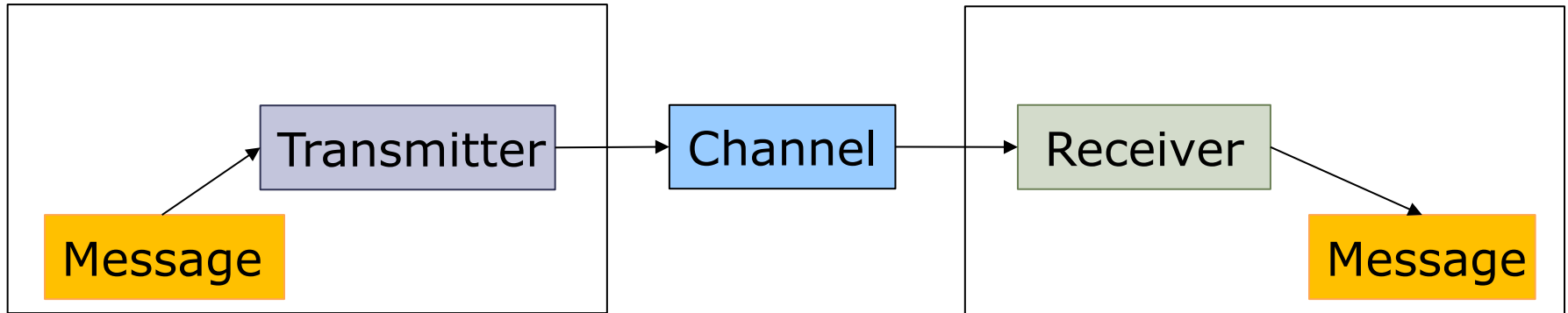
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- ISA and ABS only specify **architectural** updates
 - *Micro-architectural changes are left unspecified*
- ...so implementation details and timing behaviors (e.g., microarchitectural state, power, etc.) may be used as **channels** to leak information!

Simple Communication Model

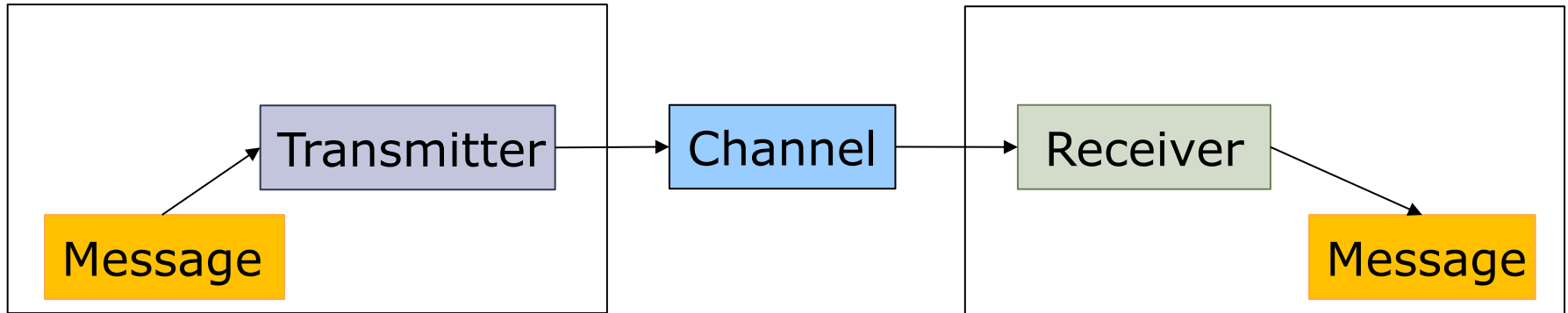


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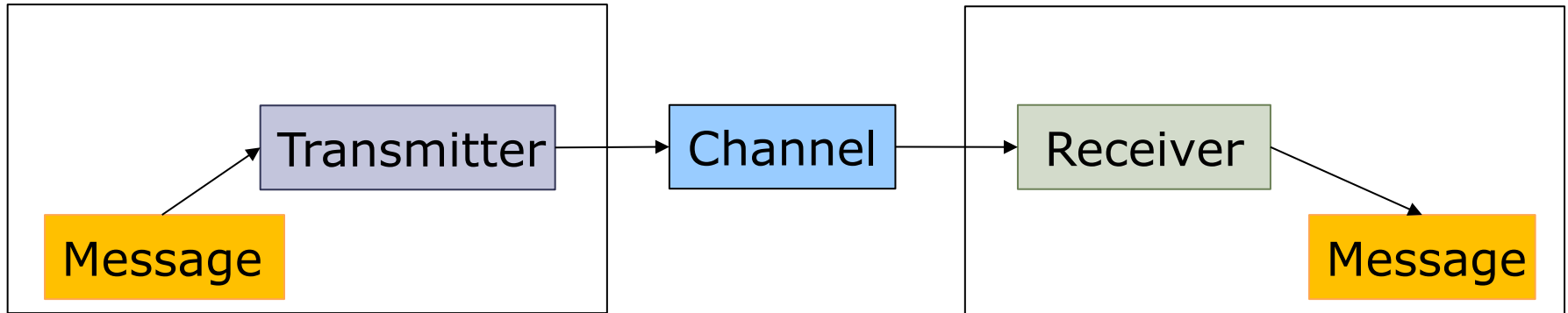
- Transmitter accepts message

Simple Communication Model



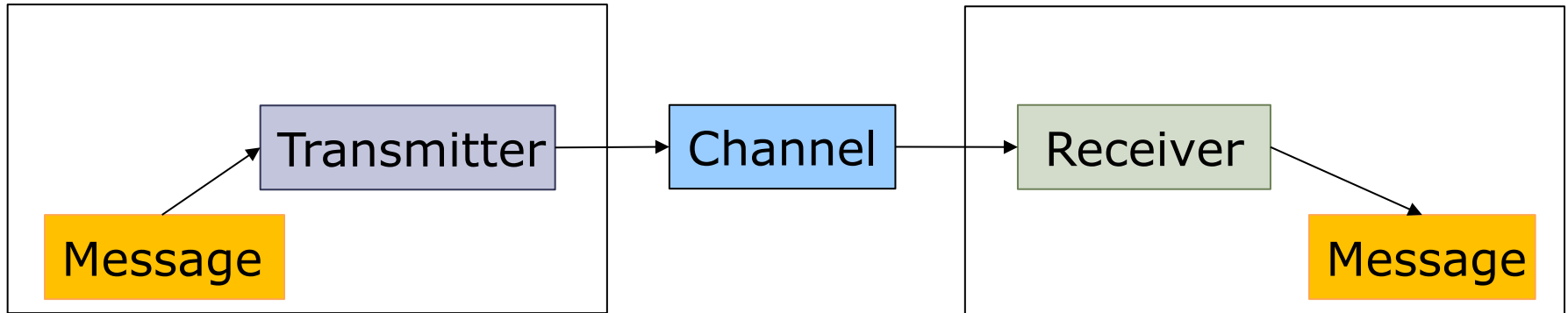
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Simple Communication Model



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- Receiver detects modulation on channel

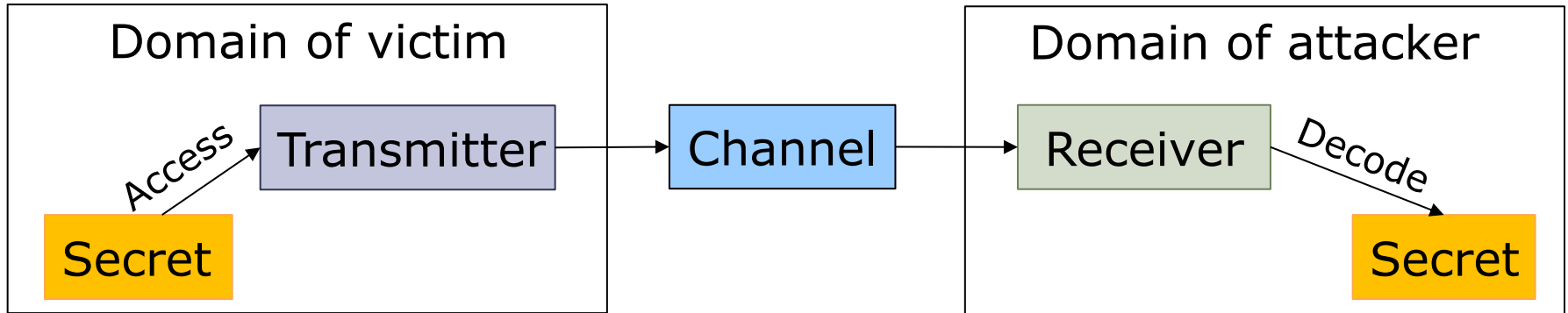
Simple Communication Model



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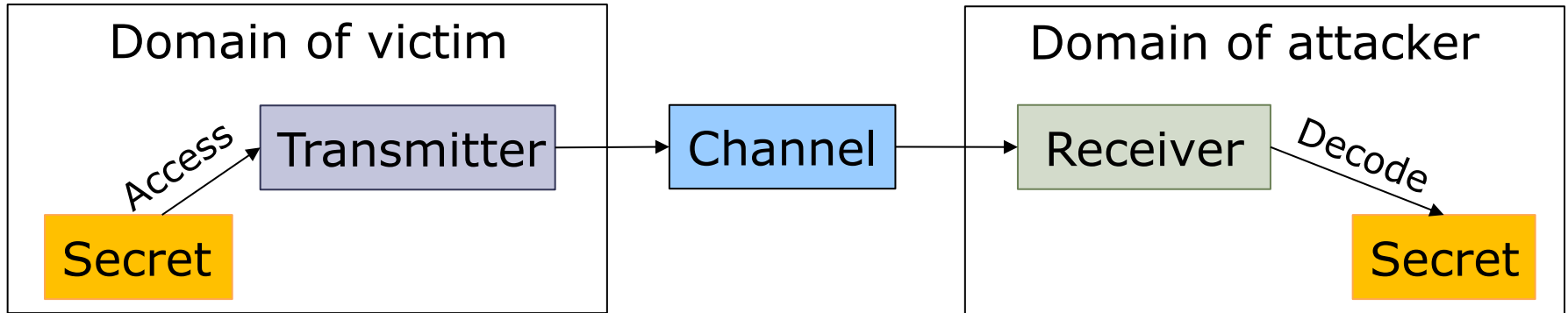
Communication Model of Attacks

[Belay, Devadas, Emer]



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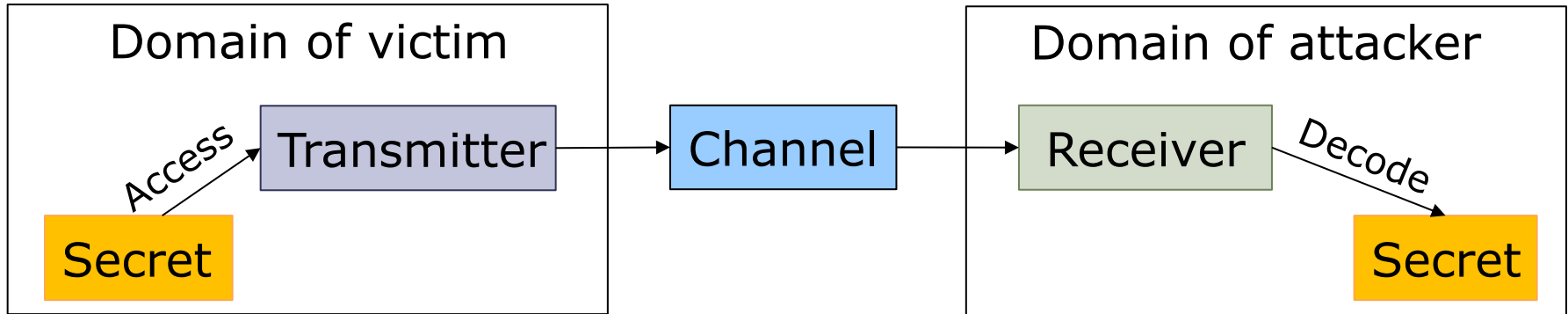
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- Domains – Distinct architectural domains in which architectural state is not shared.

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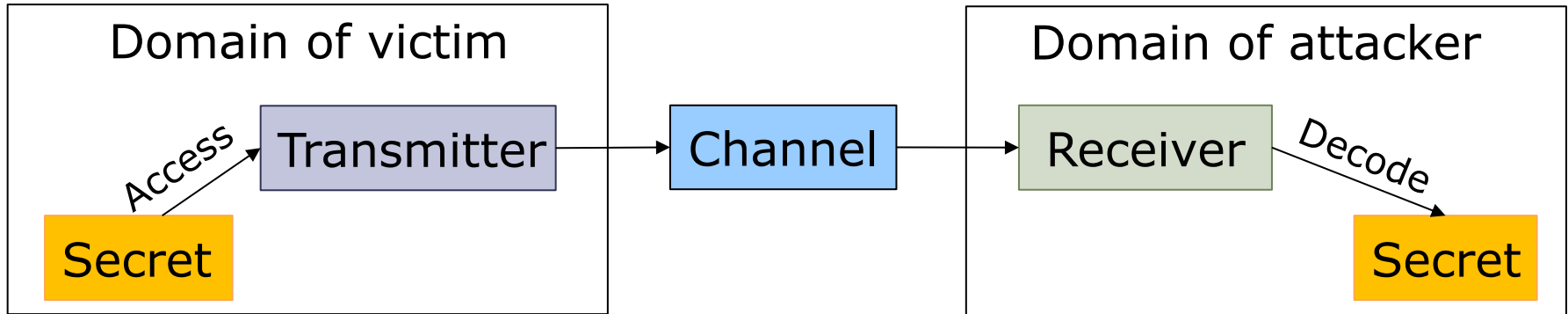
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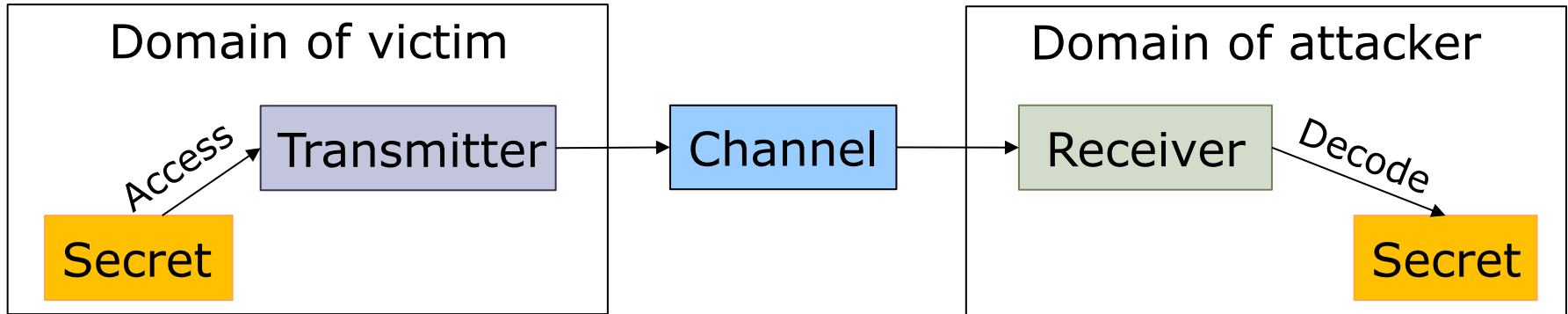
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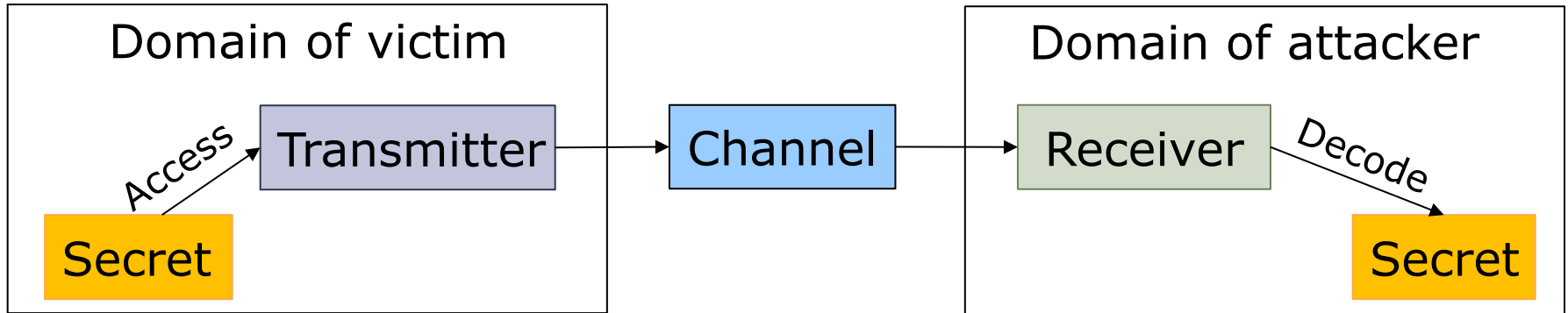


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Because channel is not a “direct” communication channel it is often referred to as a “side channel”

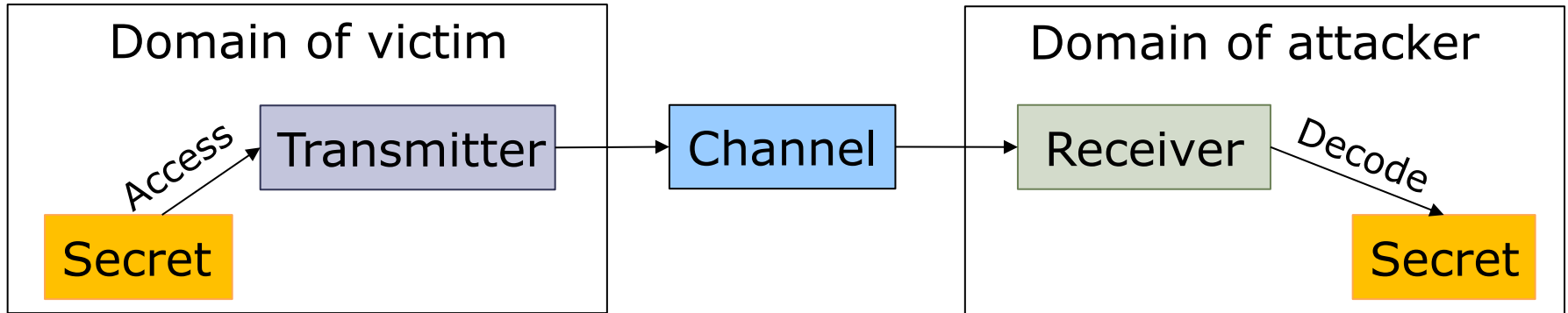
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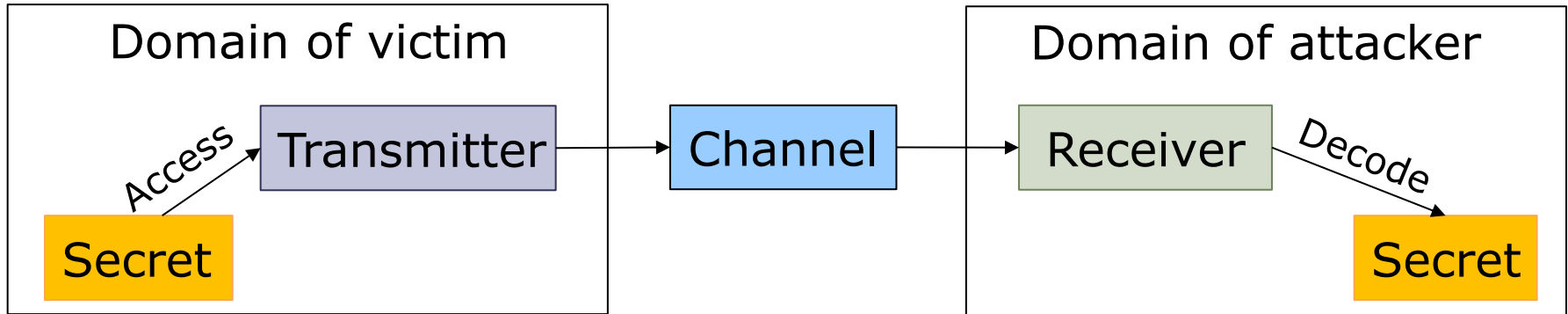
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1. Transmitter "accesses" secret

Communication Model of Attacks

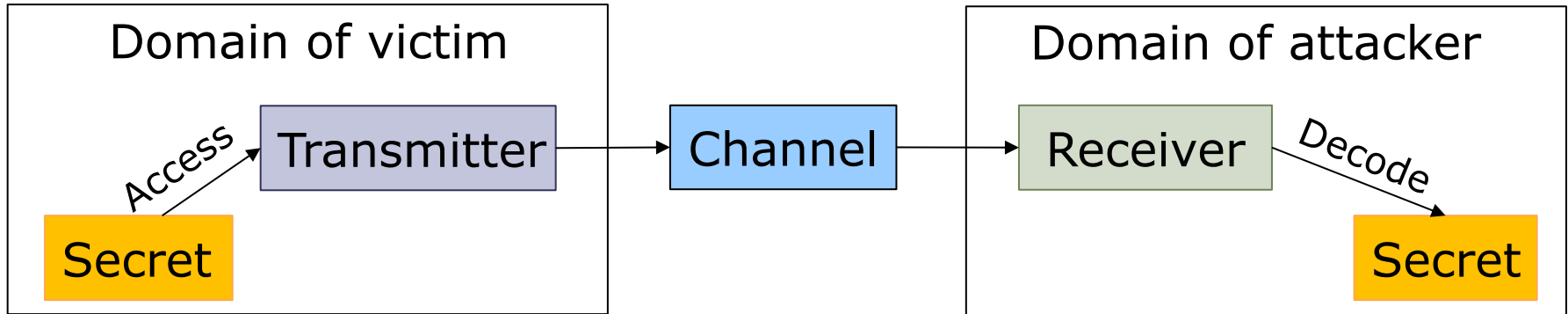
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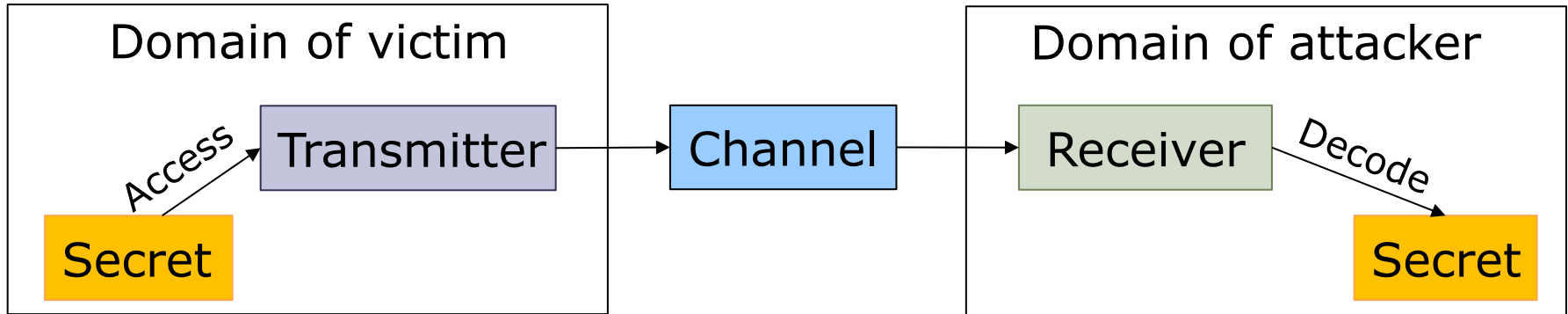
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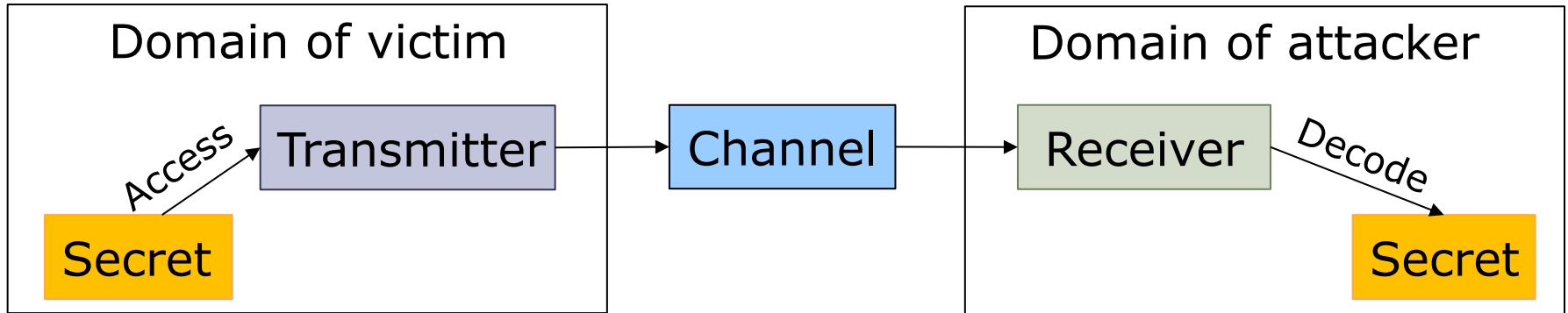
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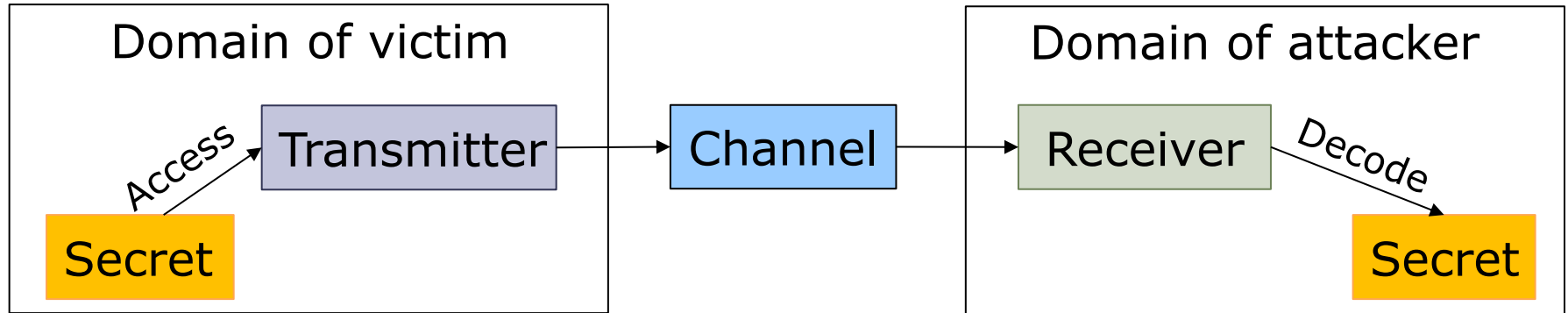


1. Transmitter "accesses" secret
2. Transmitter modulates channel with a message based on secret
3. Receiver detects modulation on channel
4. Receiver decodes modulation as a message containing the secret

ATM Acoustic Channels

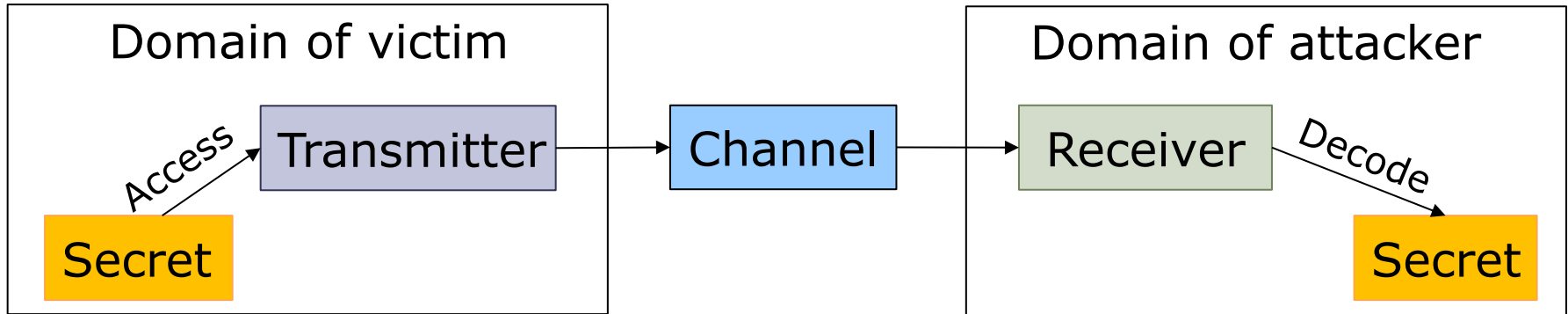


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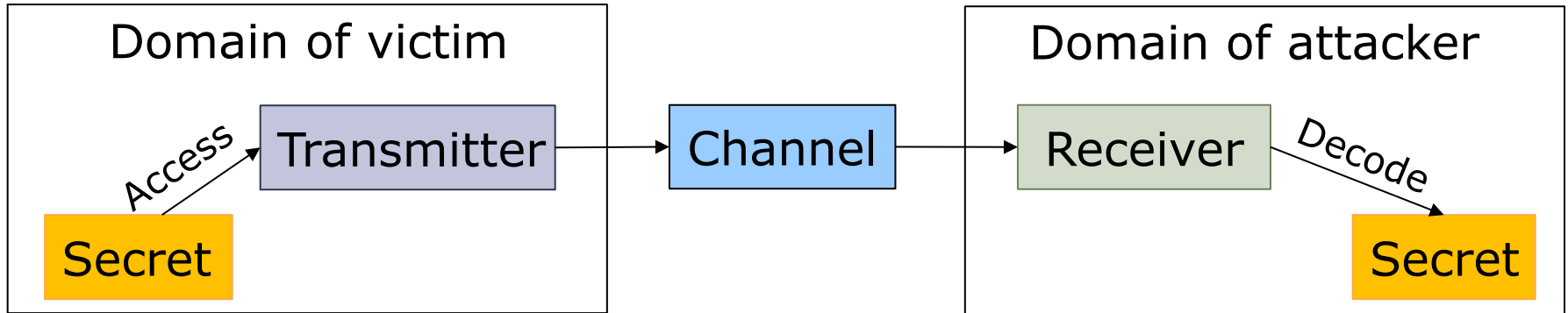
- Secret: Pin

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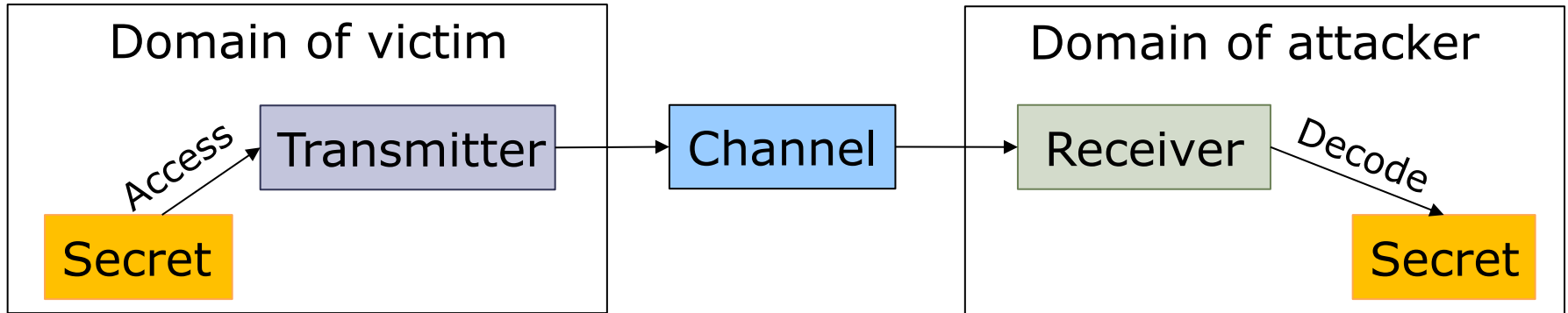
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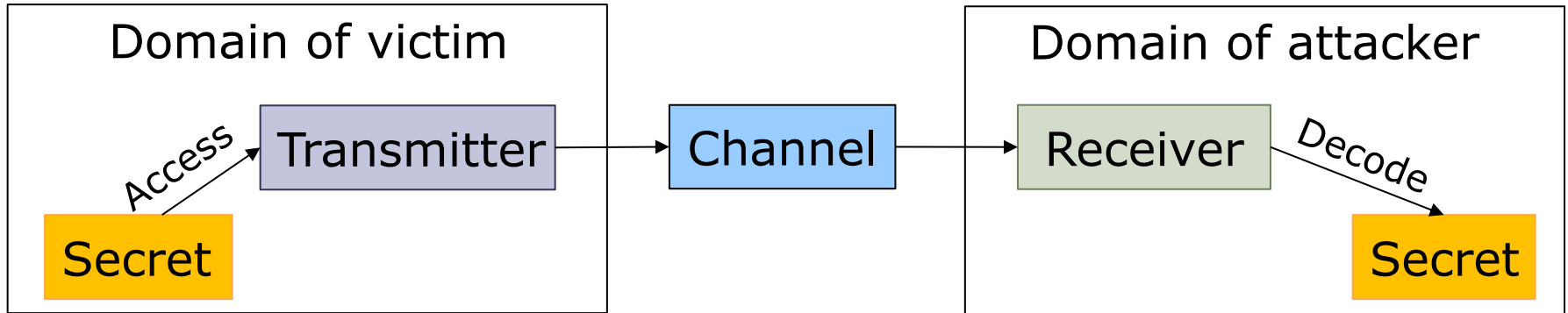
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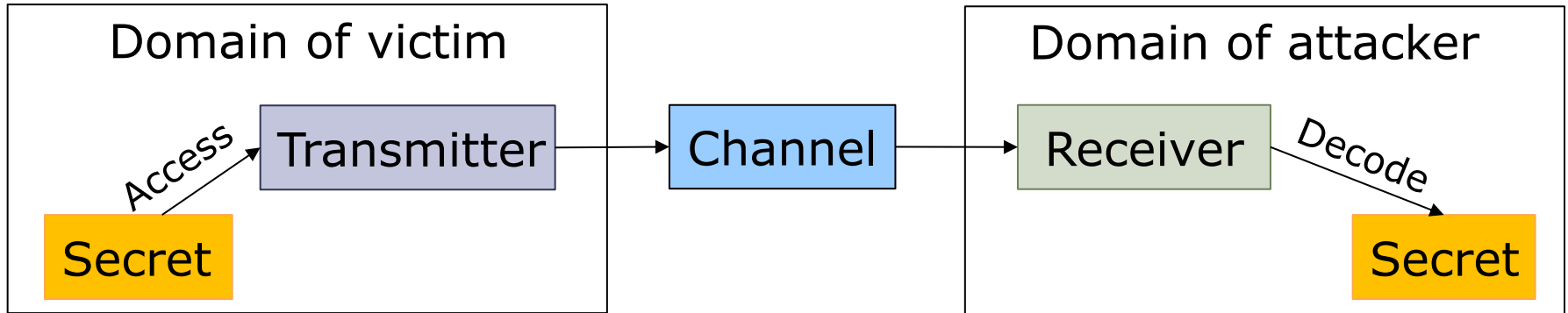
- Secret: Pin
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- Channel: Air
- Modulation: Acoustic waves

ATM Acoustic Channels



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ATM Acoustic Channels



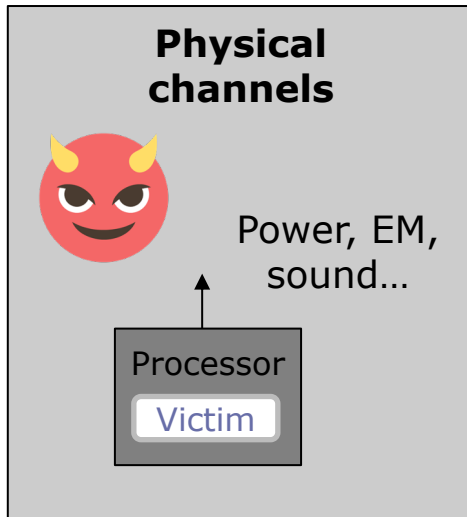
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- Modulation: Acoustic waves
- Receiver: Cheap Microphone
- Decoders: ML Model

Physical vs Timing vs uArch Channel

- What can the adversary observe?

Physical vs Timing vs uArch Channel

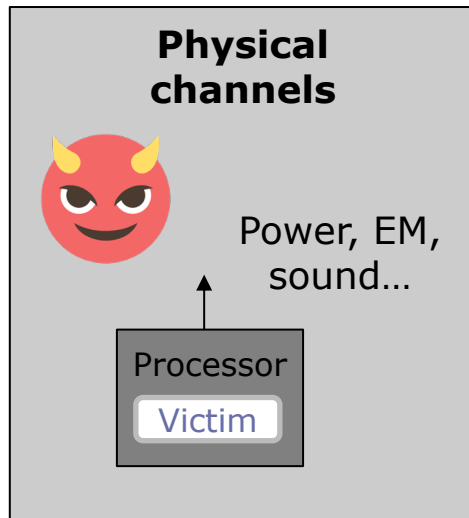
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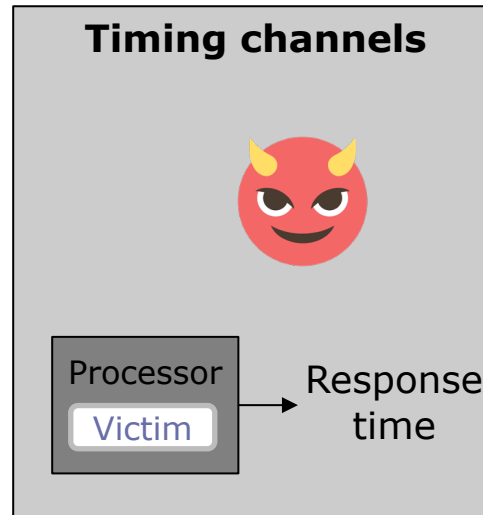
Attacker requires
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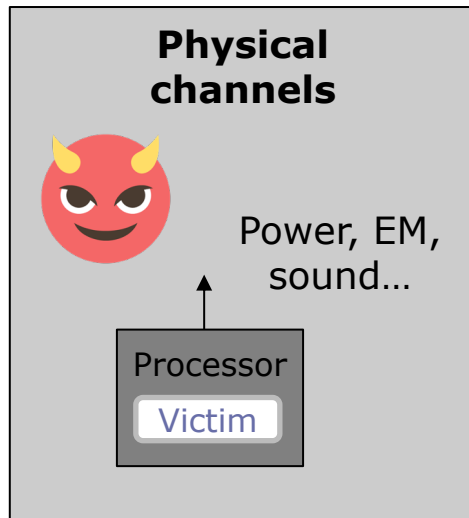
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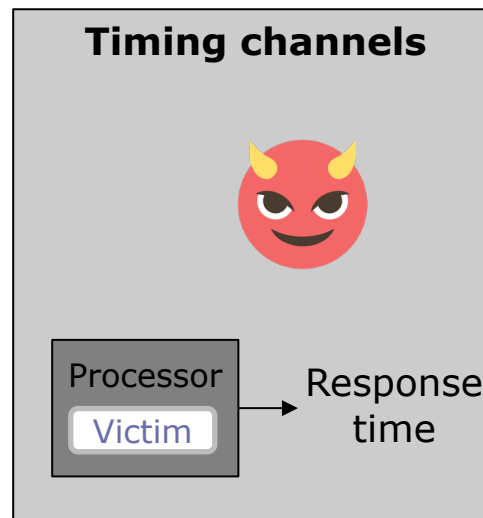
Attacker may be remote (e.g., over an internet connection)

Physical vs Timing vs uArch Channel

- What can the adversary observe?



Attacker requires measurement equipment → physical access



Attacker may be remote (e.g., over an internet connection)



Attacker may be remote, or be co-located

What can you do with these channels?

- Violate privilege boundaries
 - Inter-process communication
 - Infer an application's secret
- (Semi-Invasive) application profiling

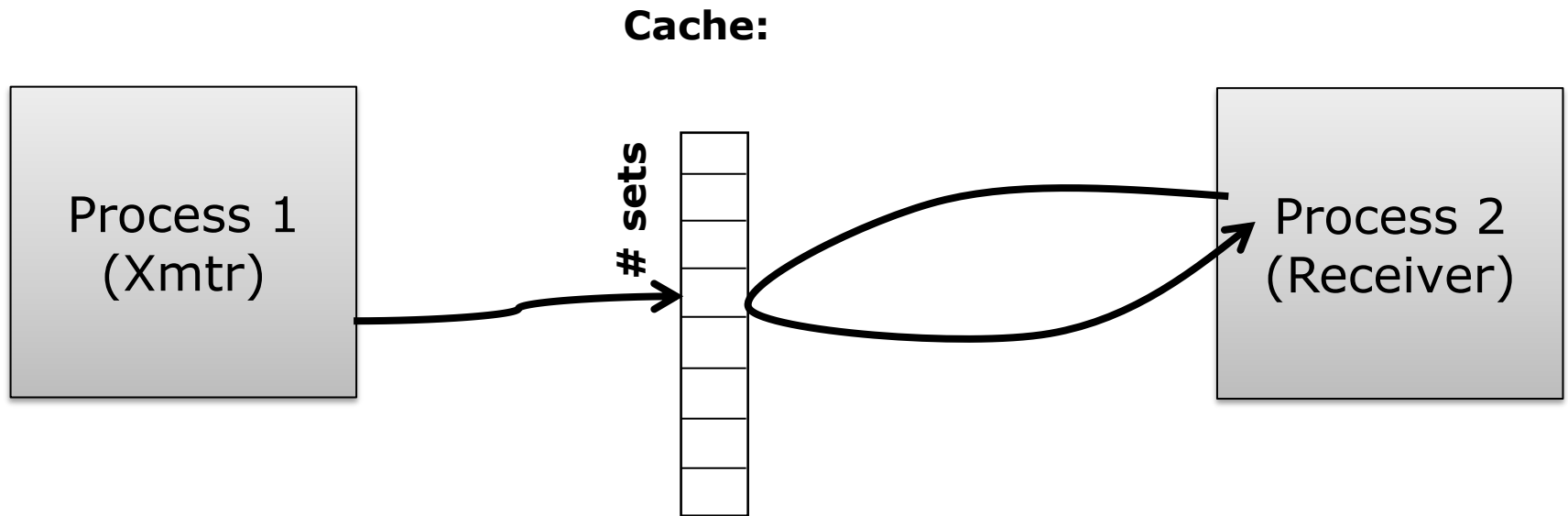
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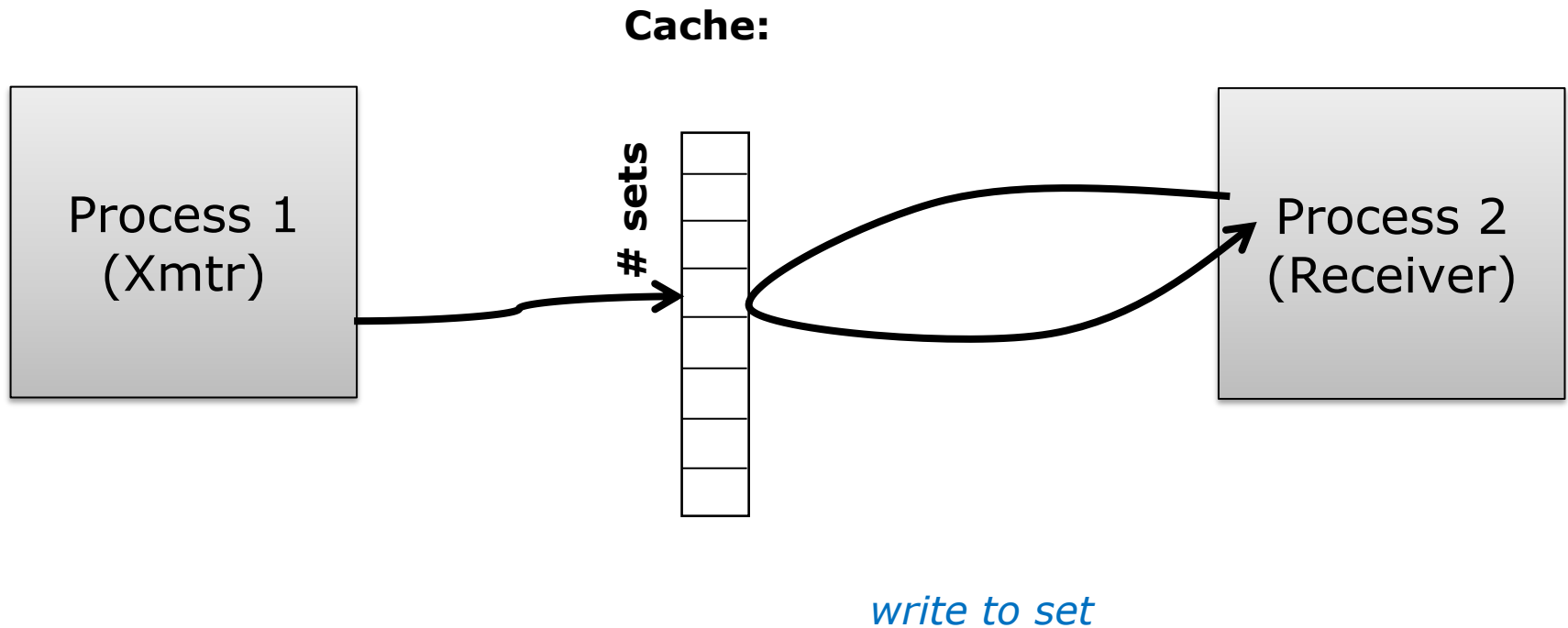
Different from traditional software or physical attacks:

- Stealthy. Sophisticated mechanisms needed to detect channel
- Usually, no permanent indication one has been exploited

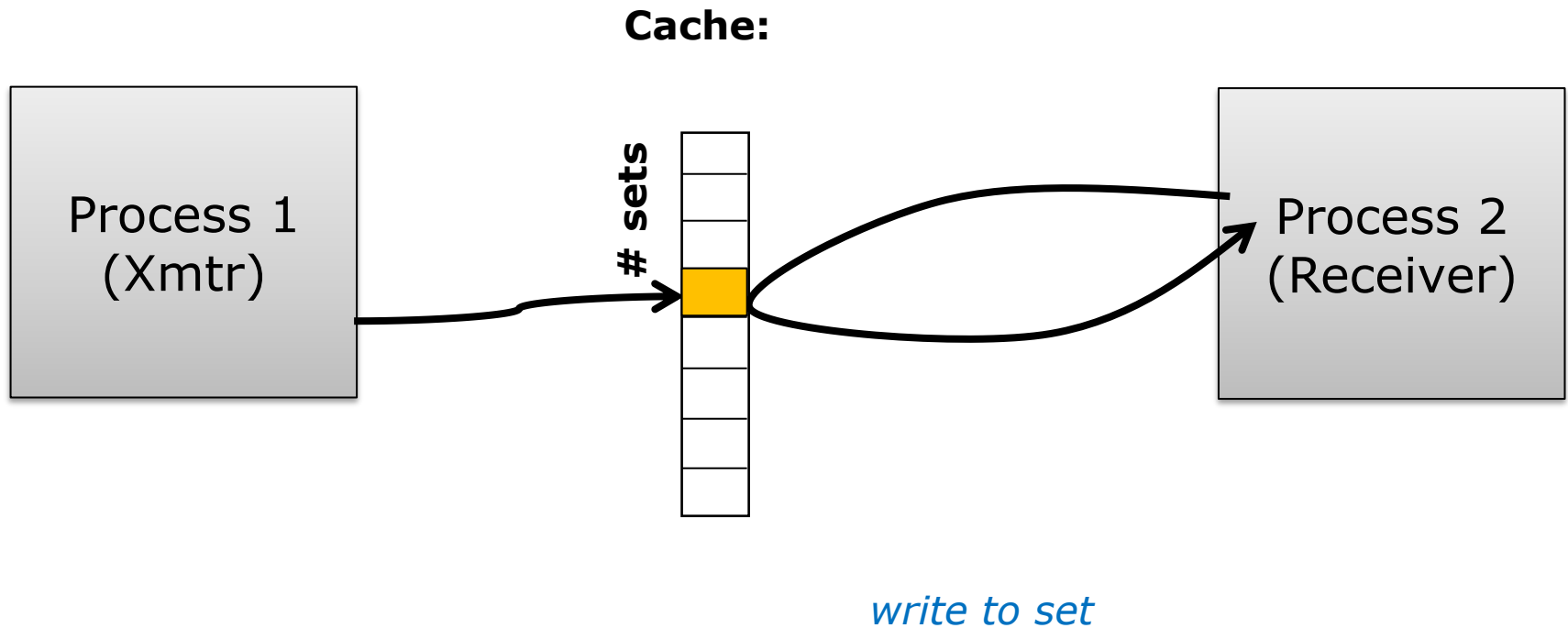
A Cache-based Channel



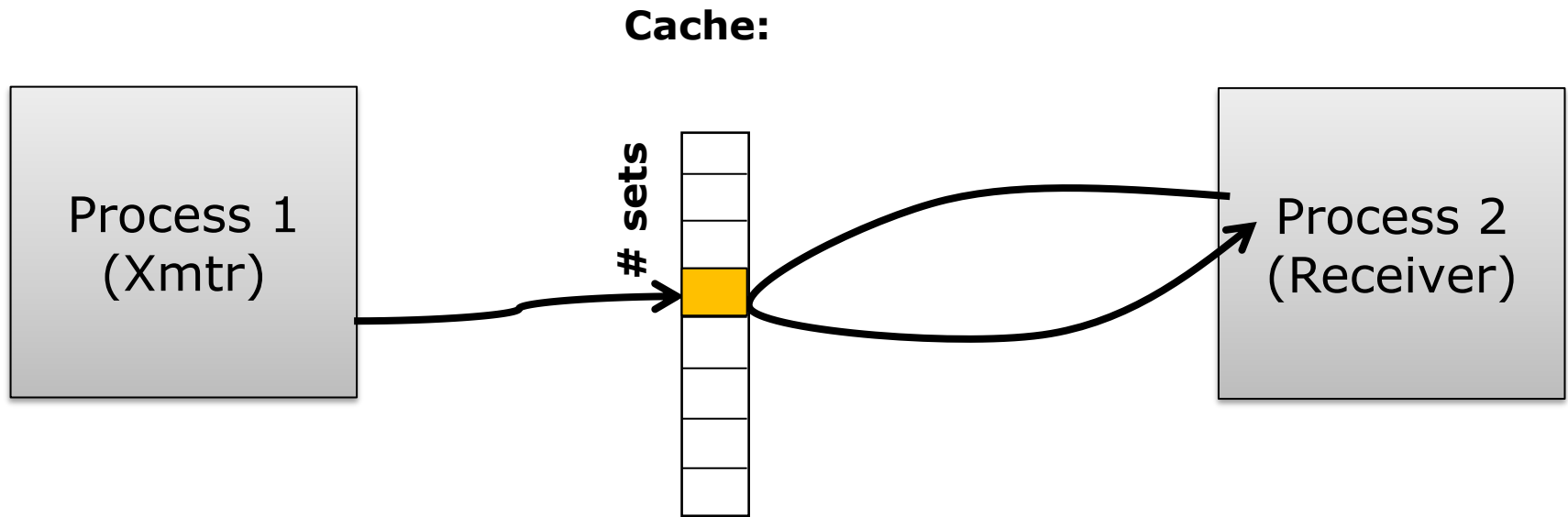
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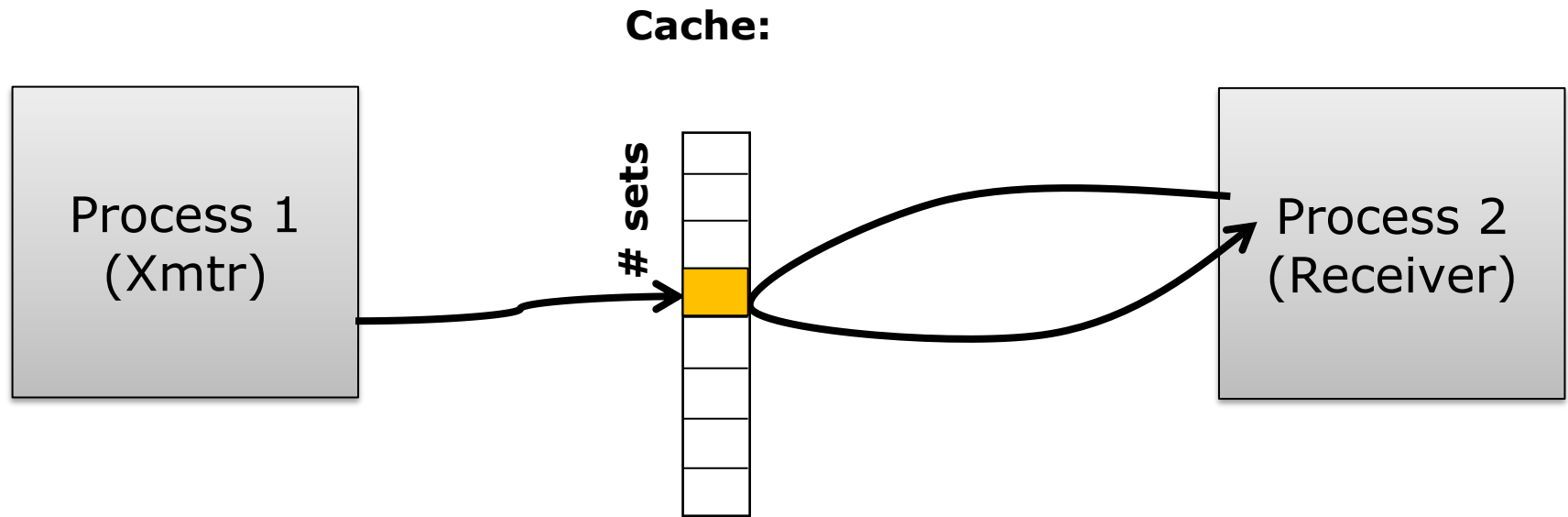
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  idle  
else  
  write to a set
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write to set

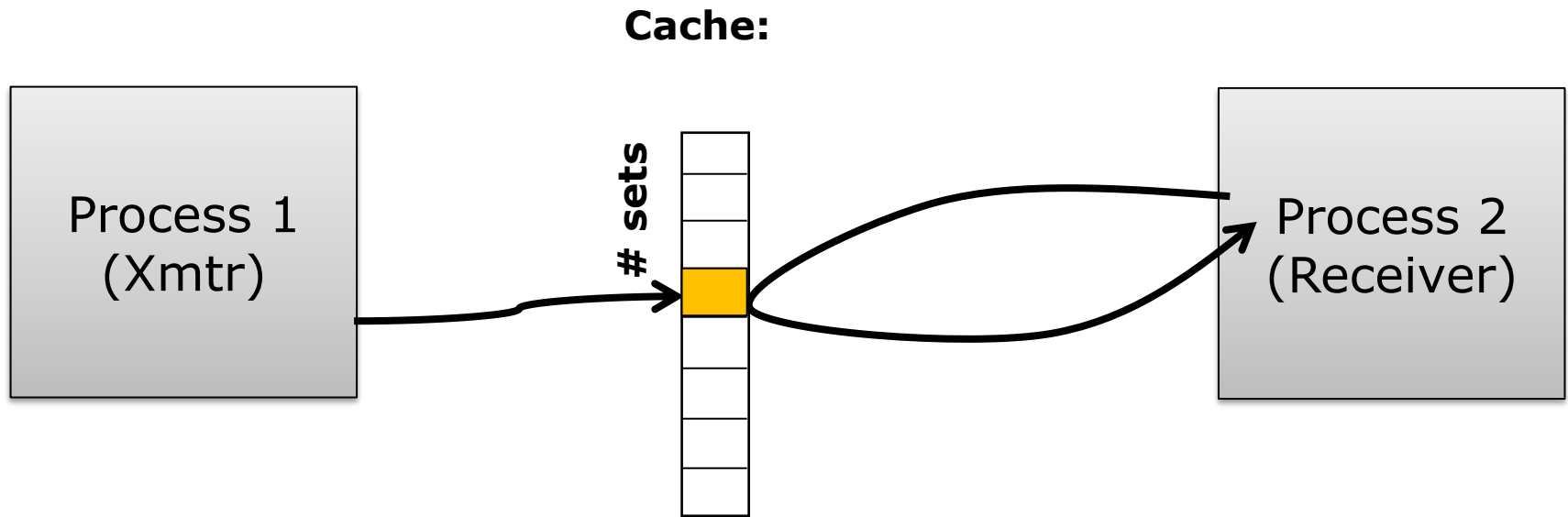
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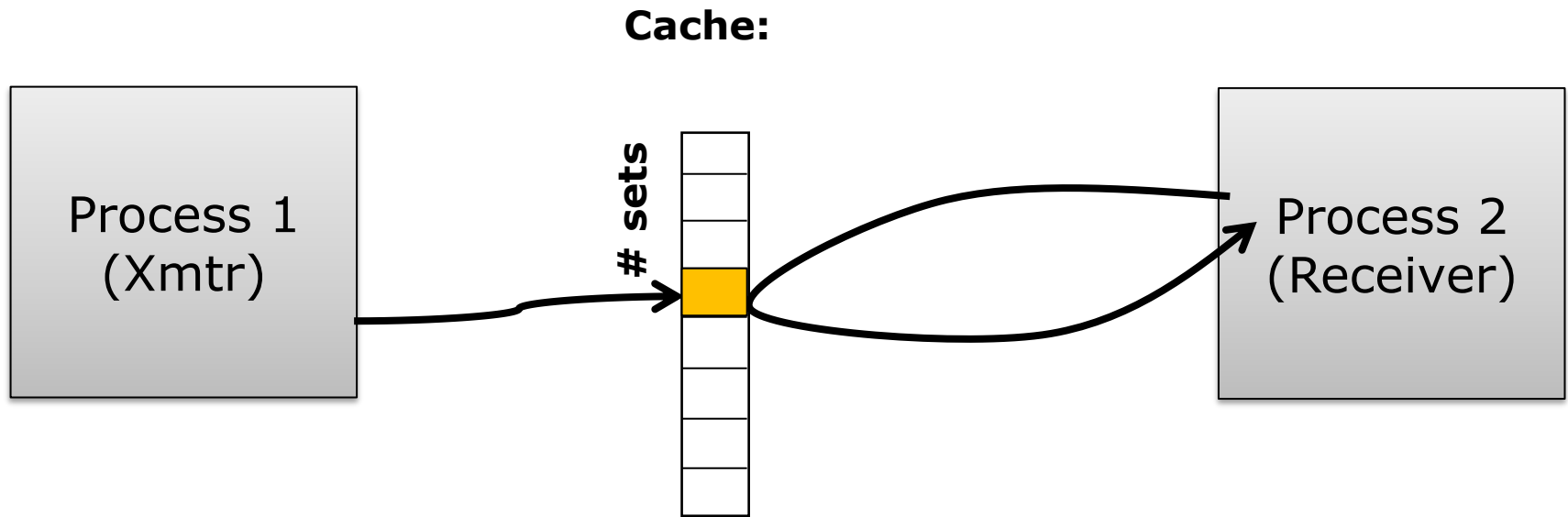
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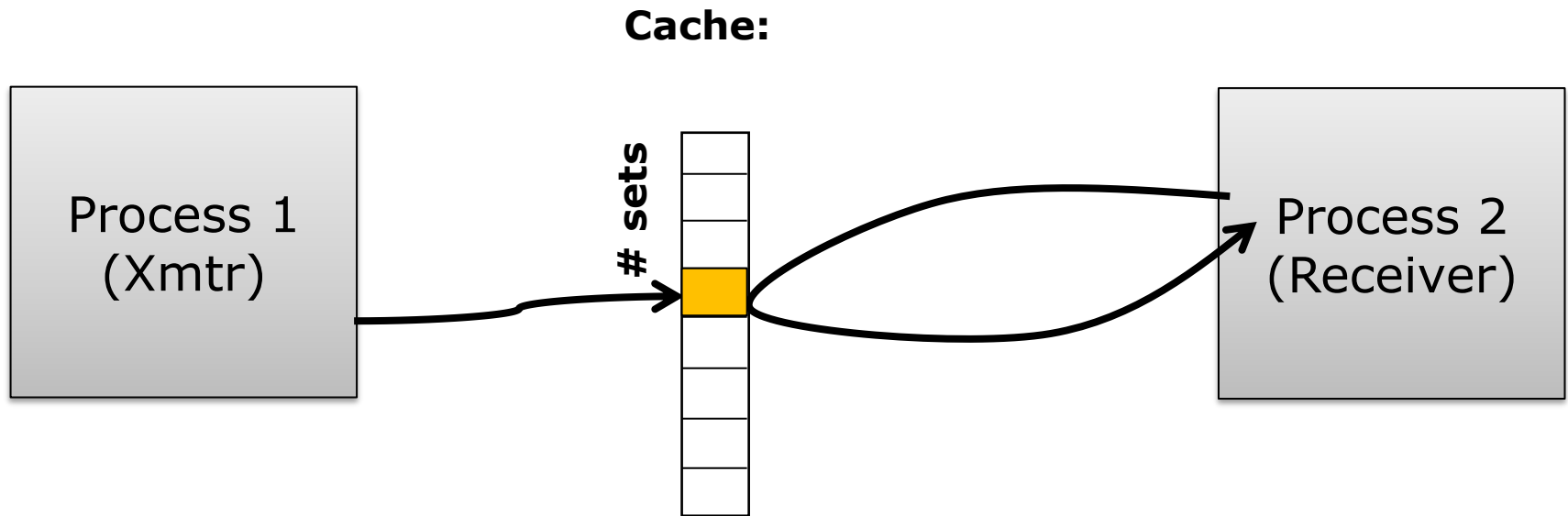


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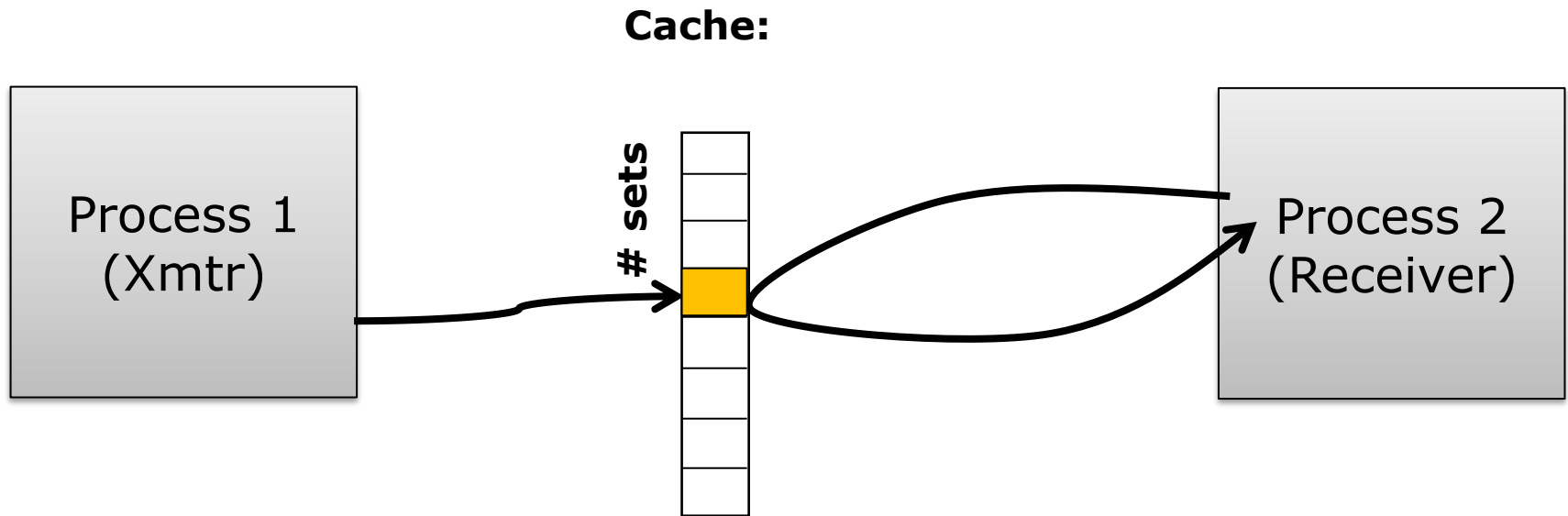
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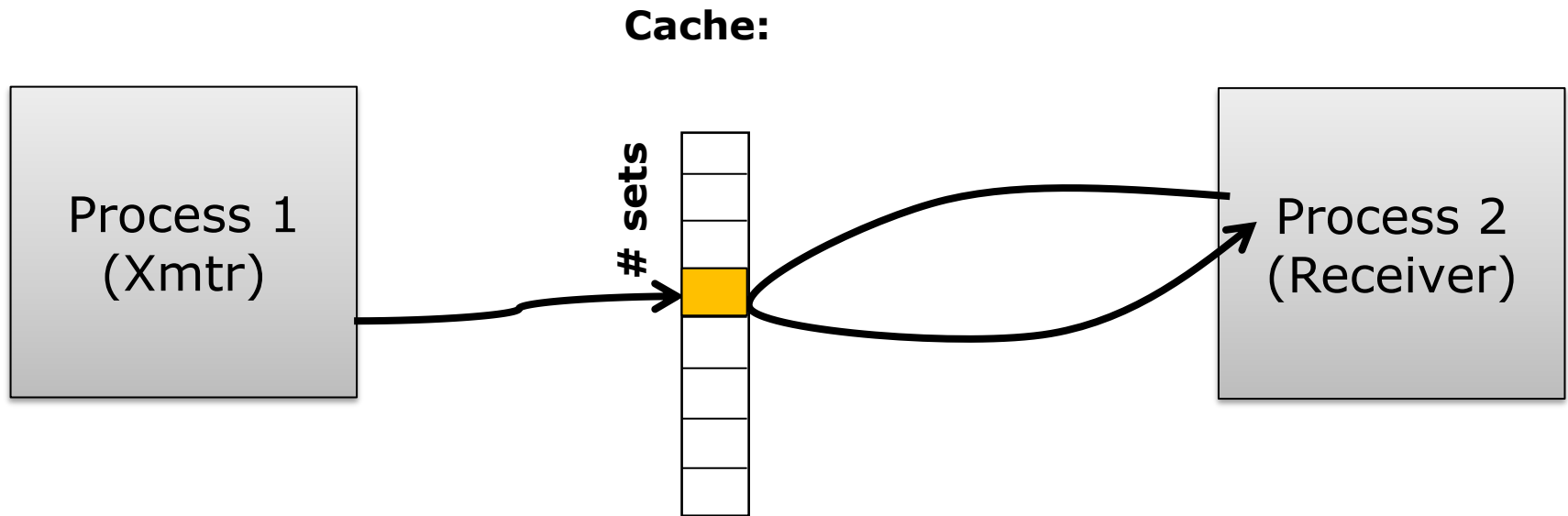
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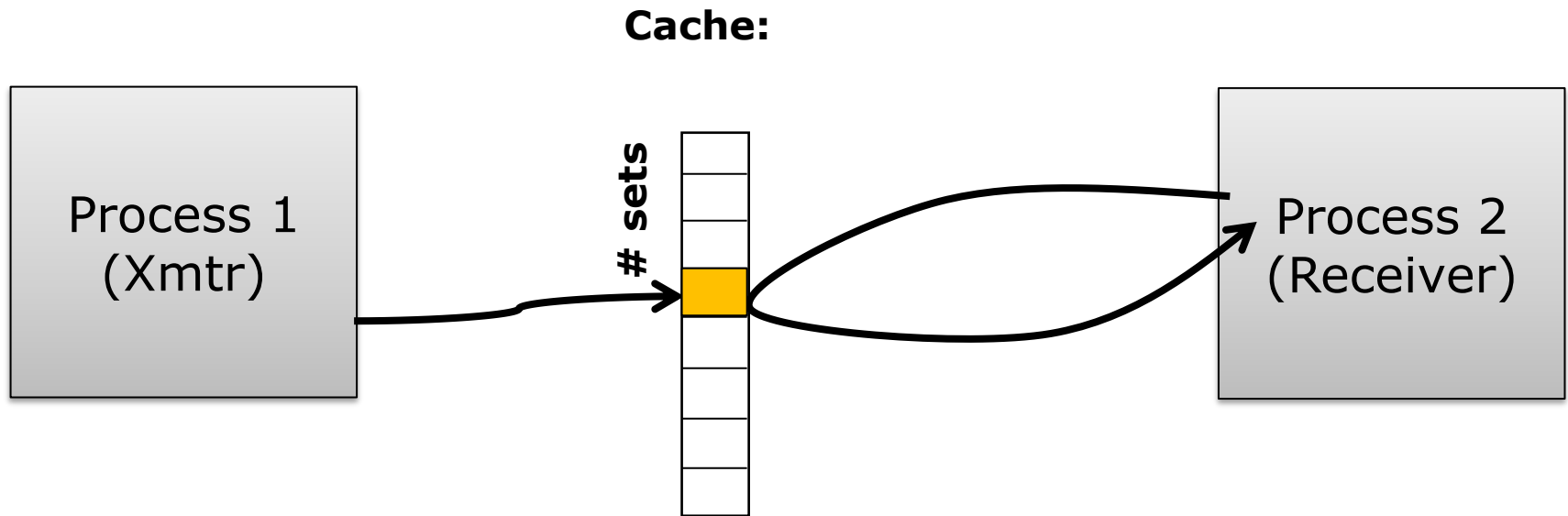
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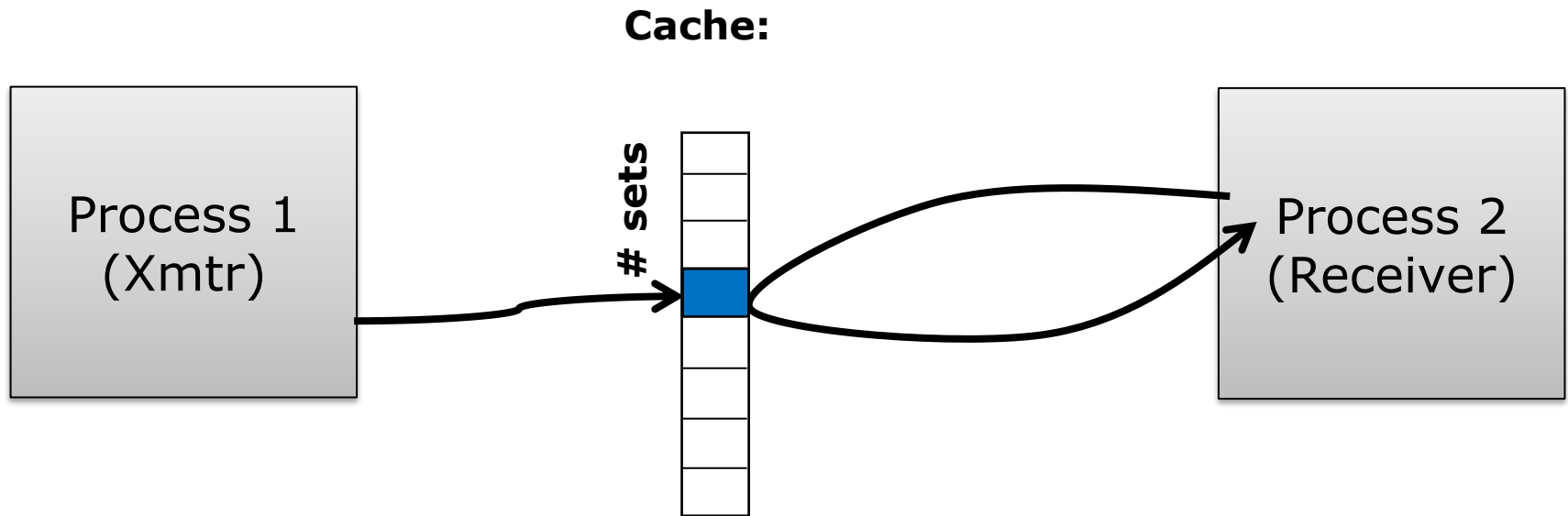
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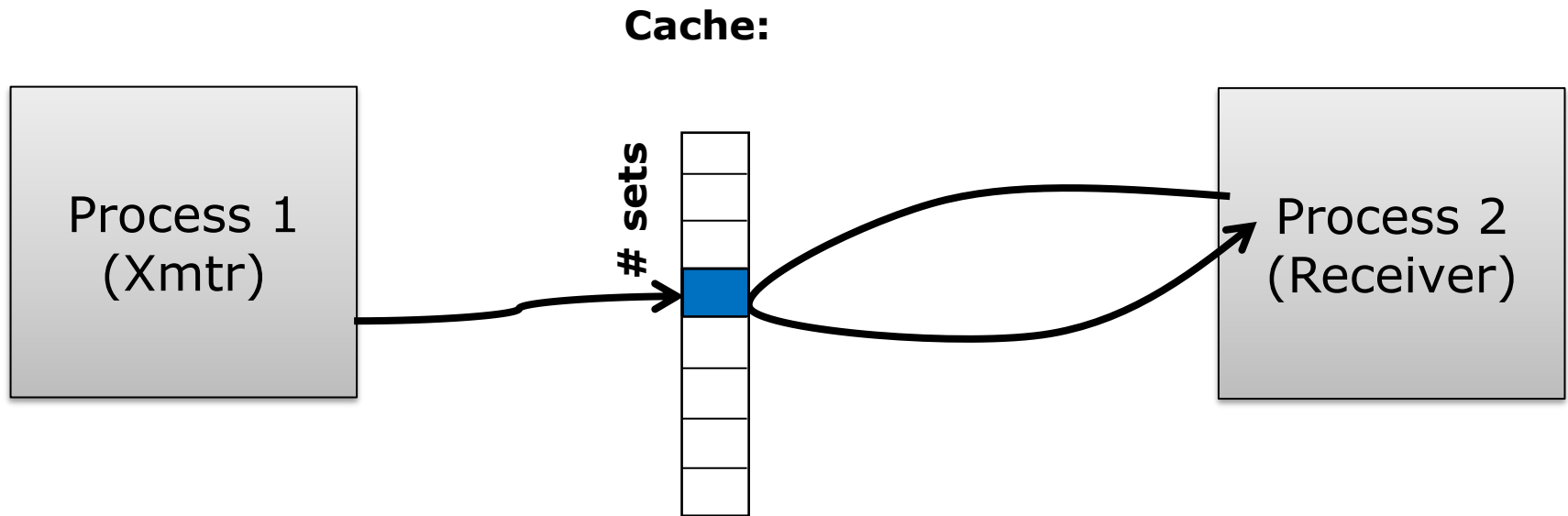
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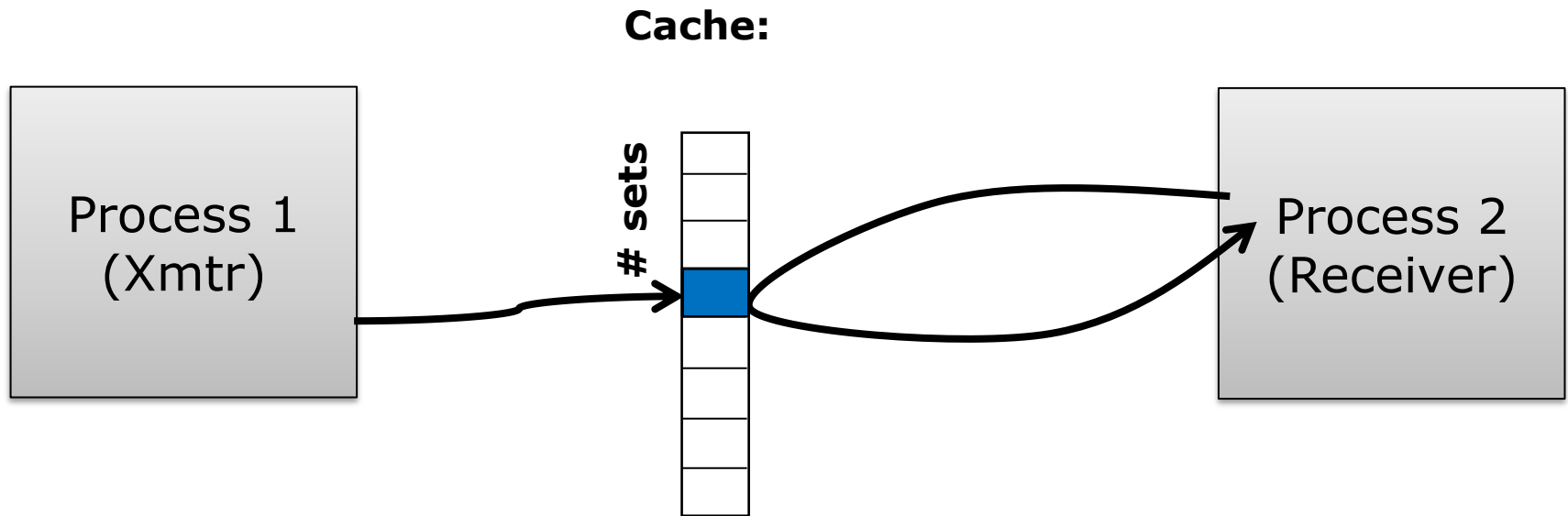
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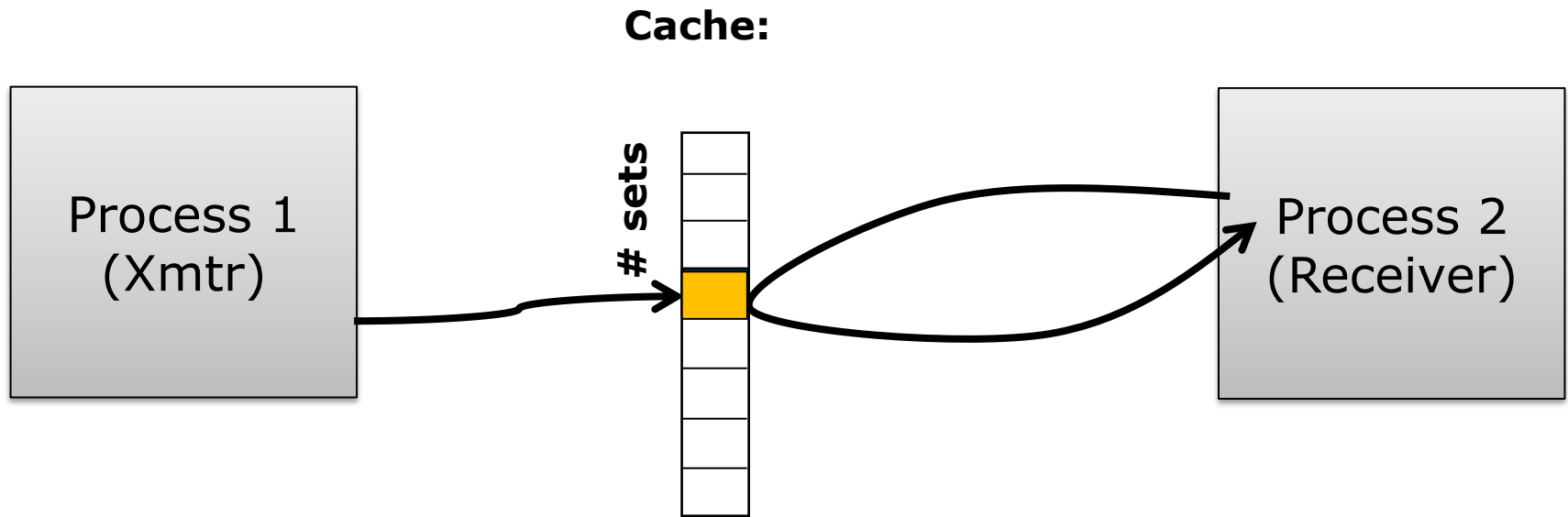
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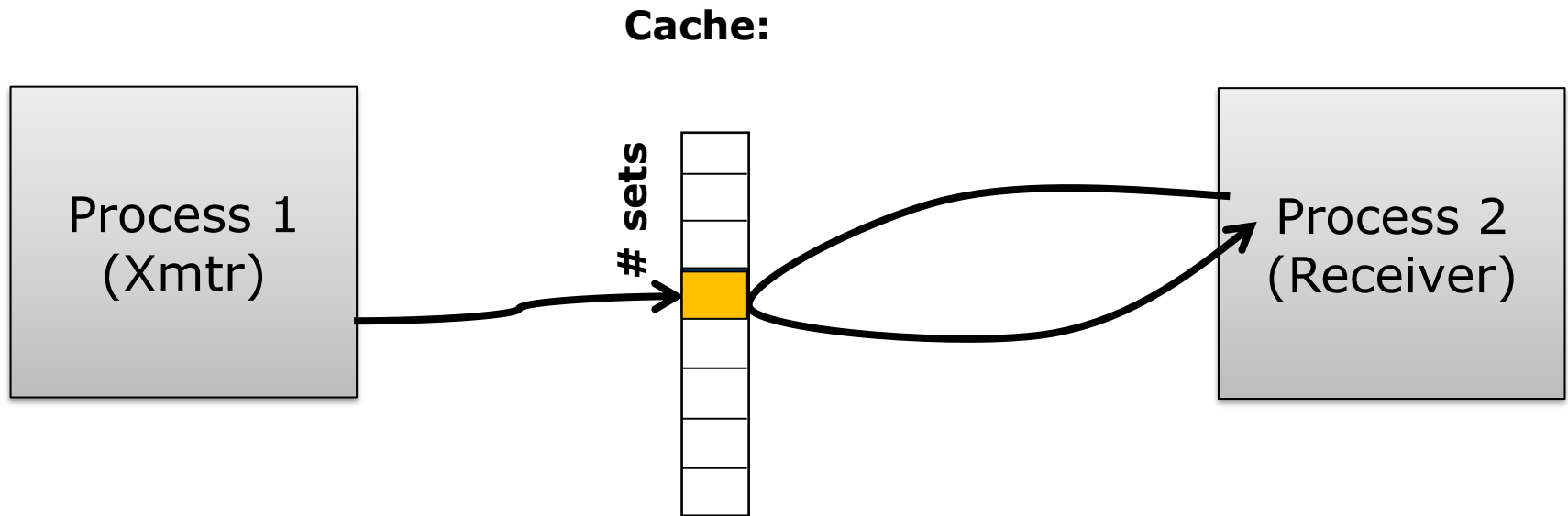
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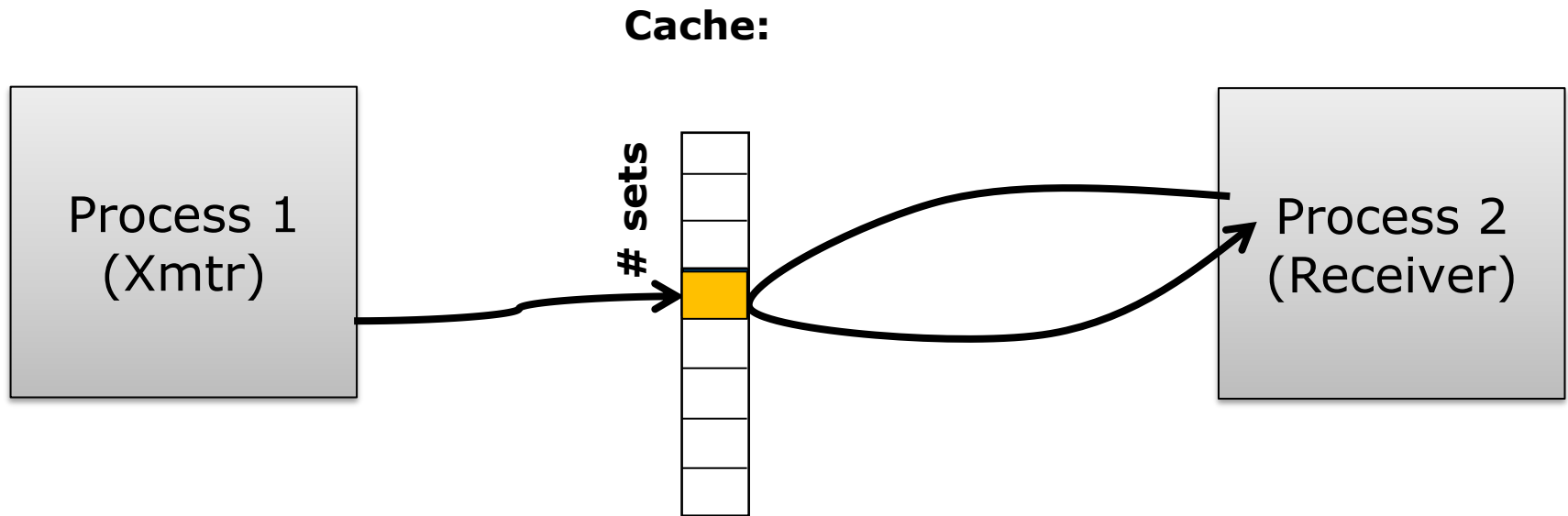
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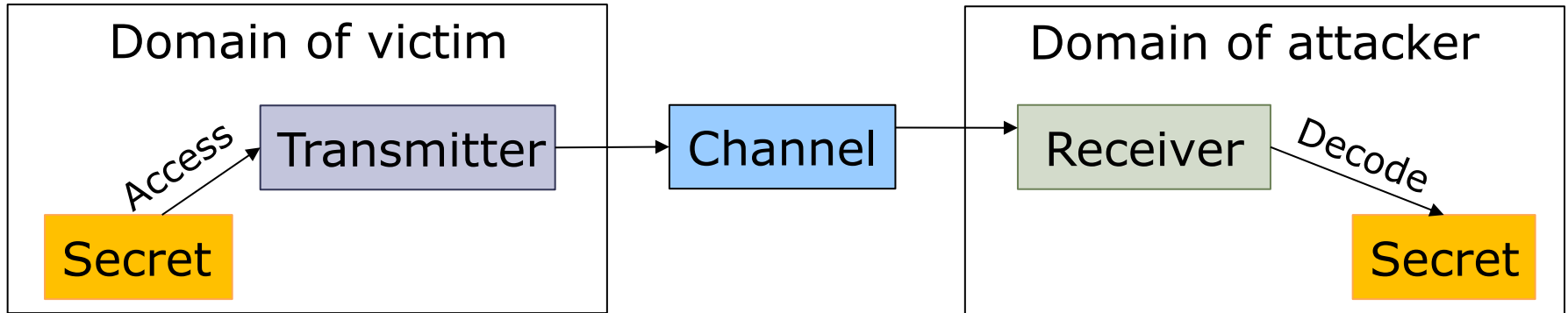
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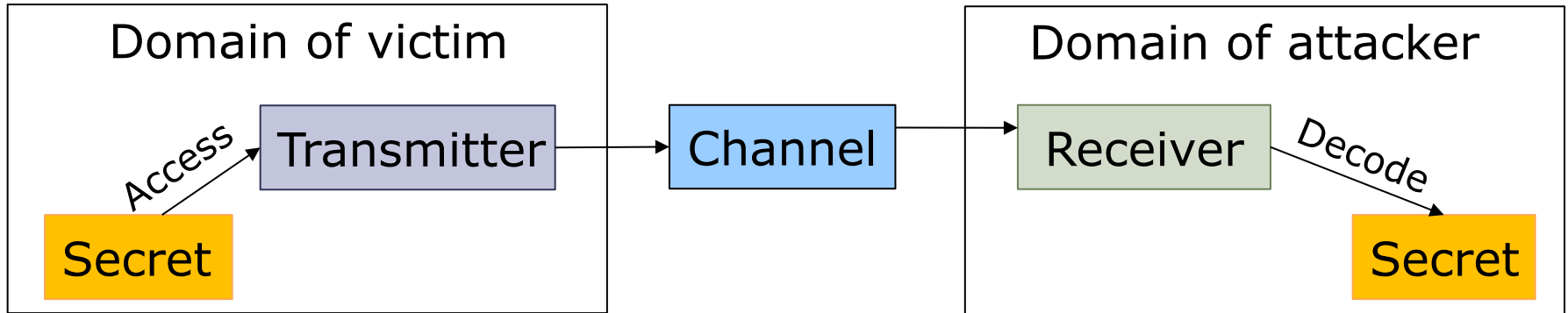
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Note this requires an "active" receiver

Communication w/ Active Receiver

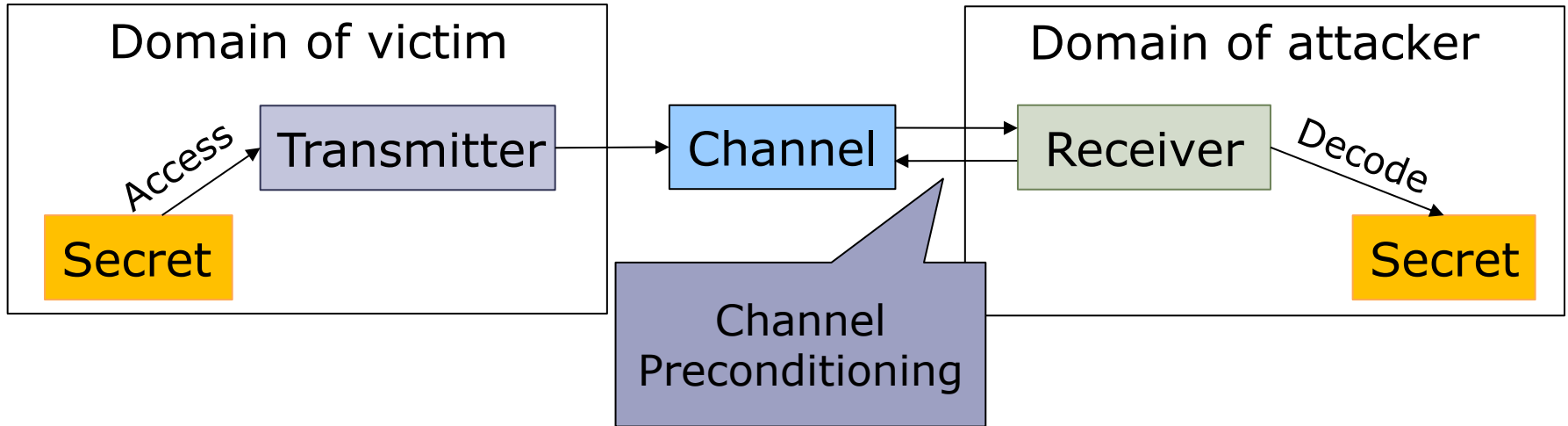


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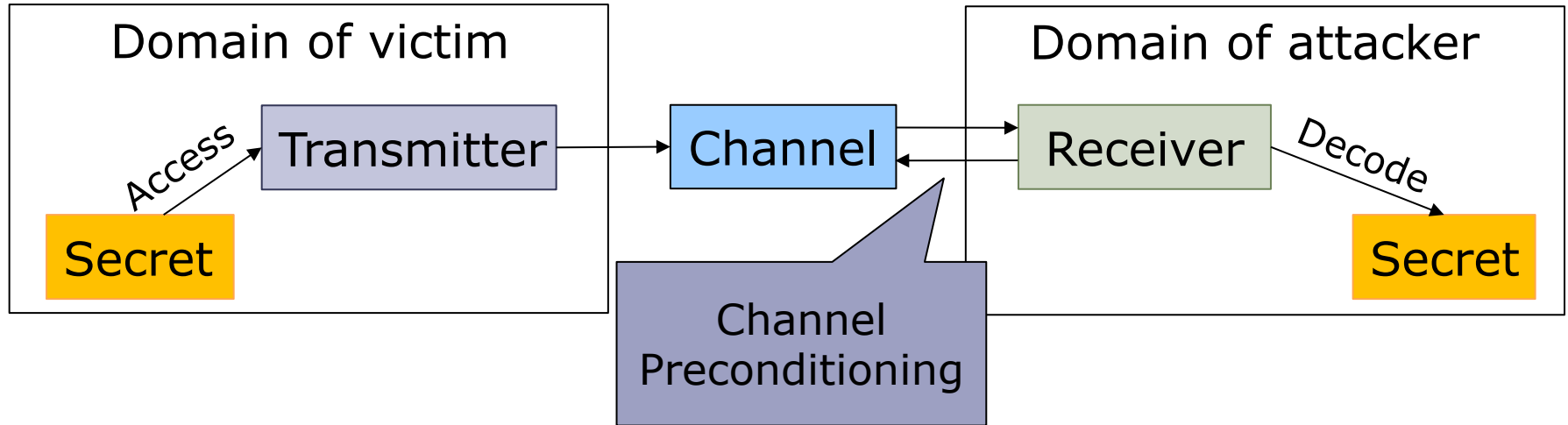
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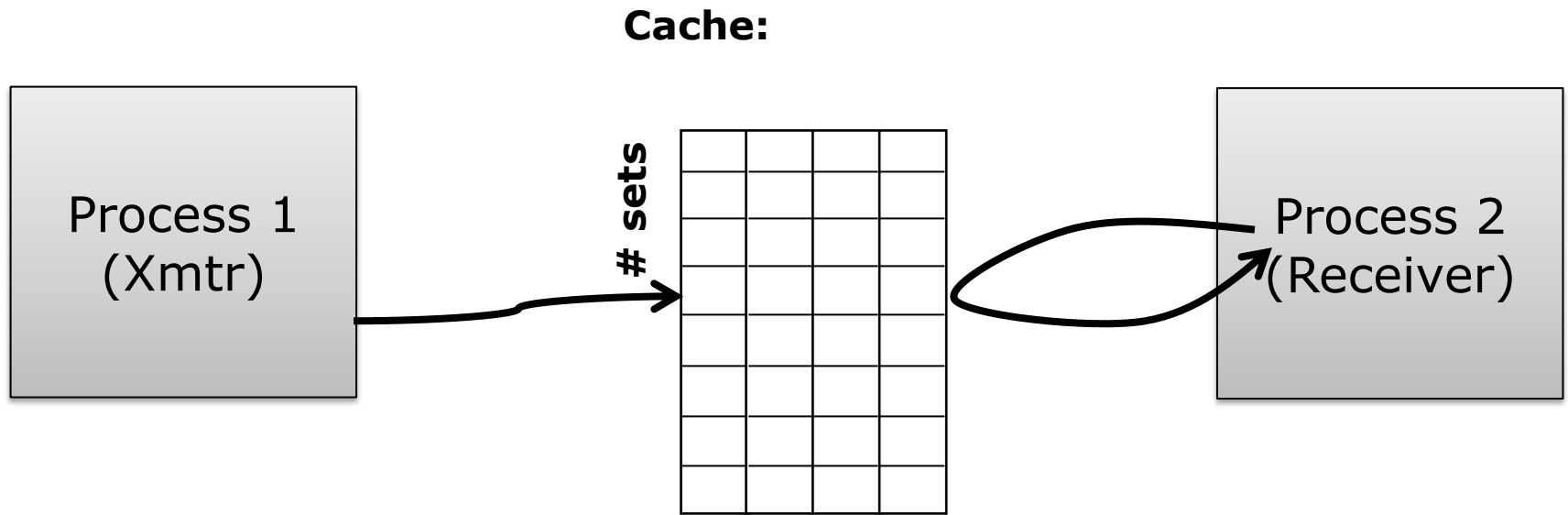
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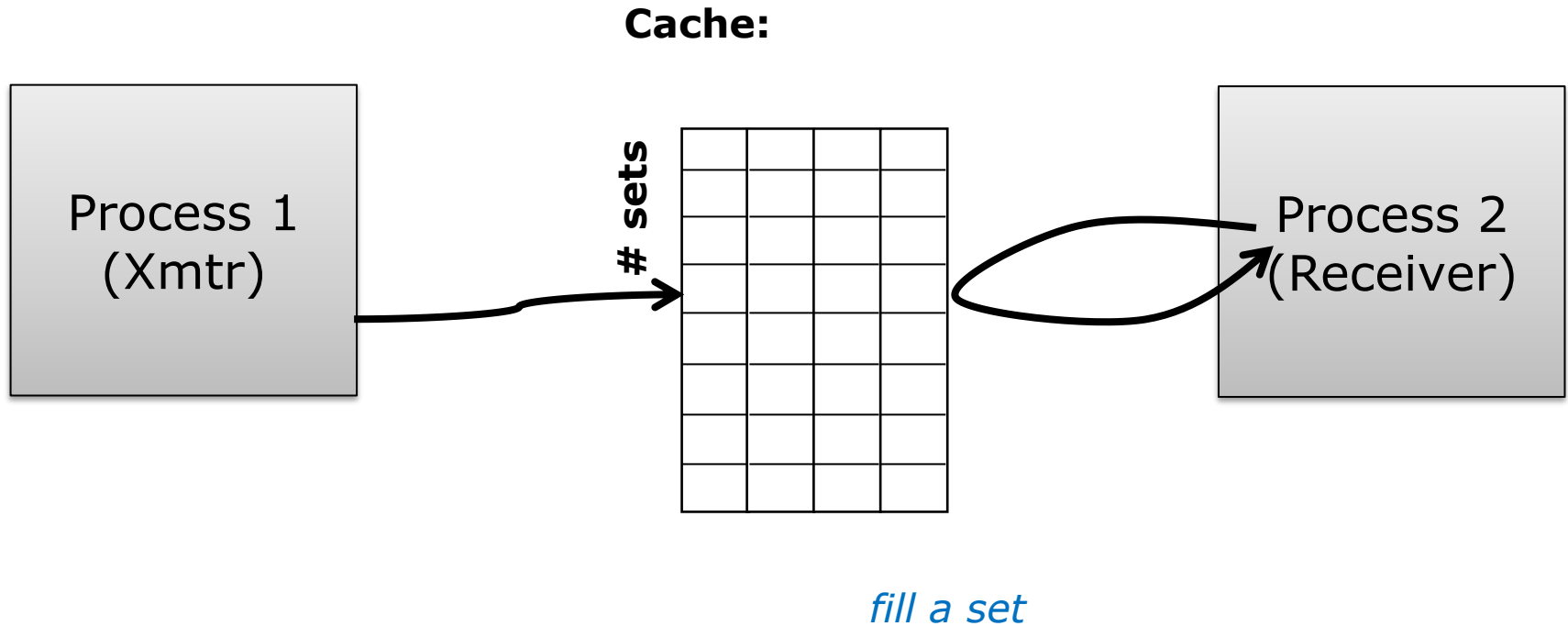


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2. An active receiver also needs to deal with synchronization of transmission (modulation) activity with reception (demodulation) activity.

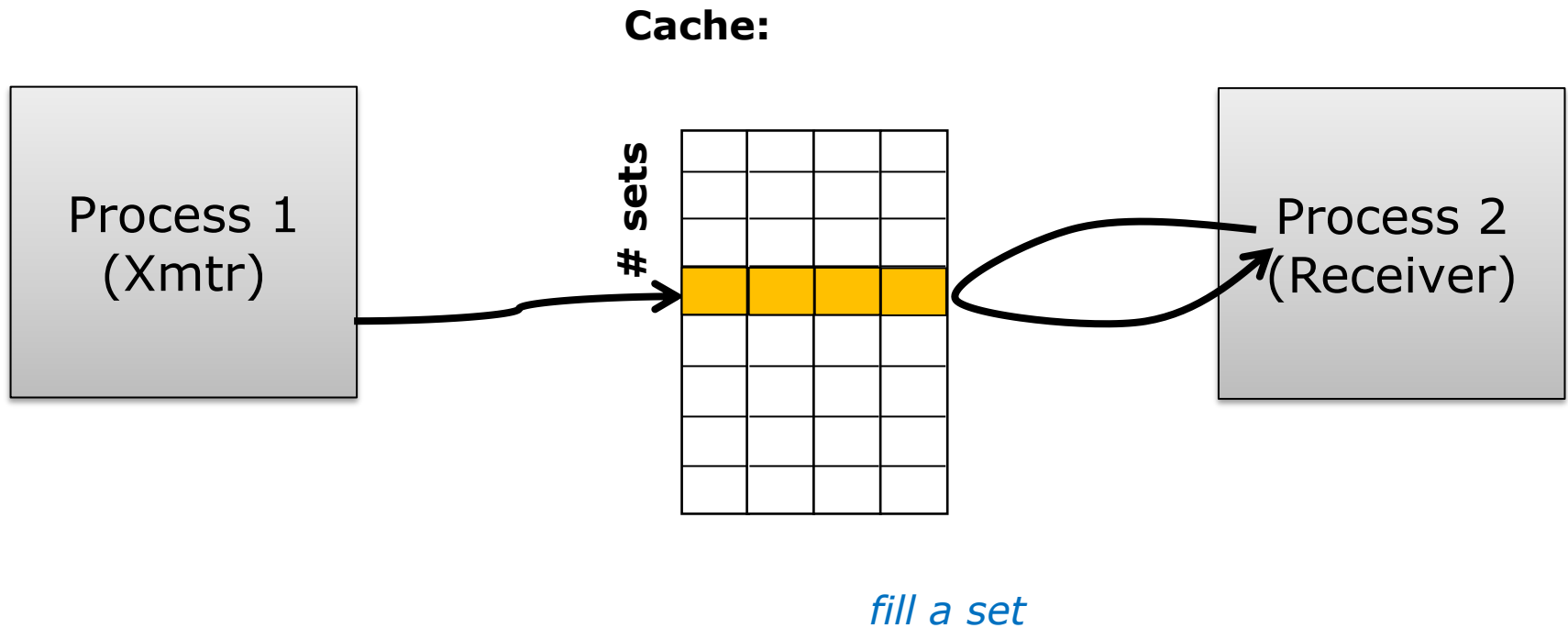
A Multi-way Cache-based Channel



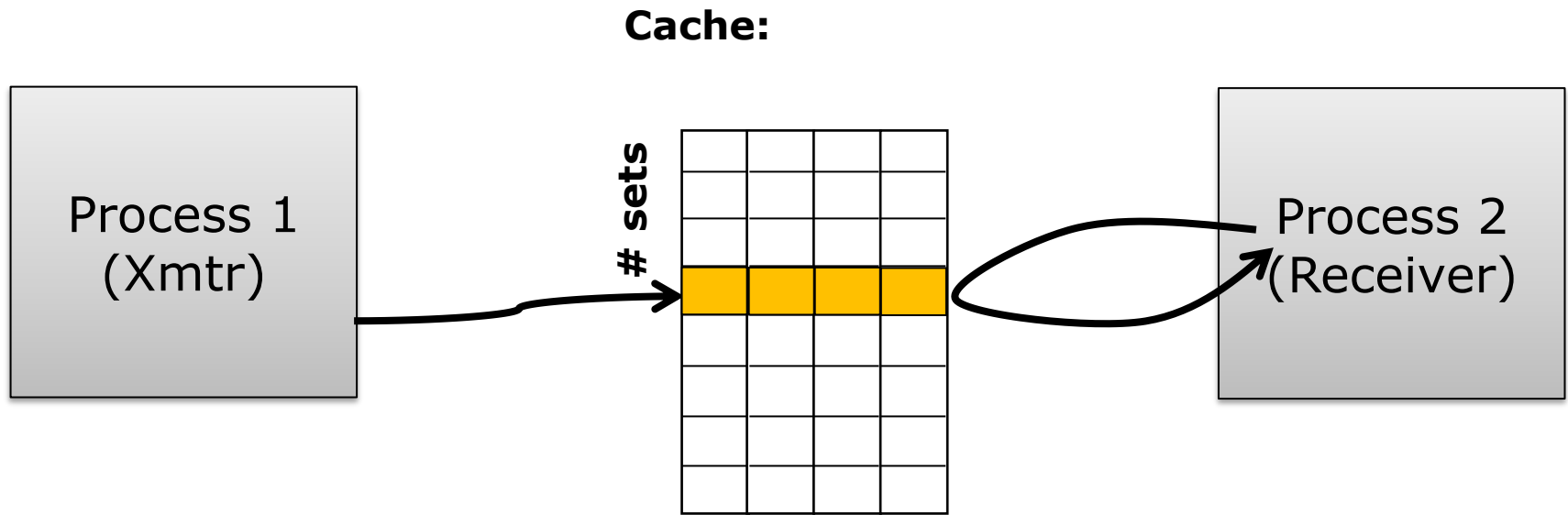
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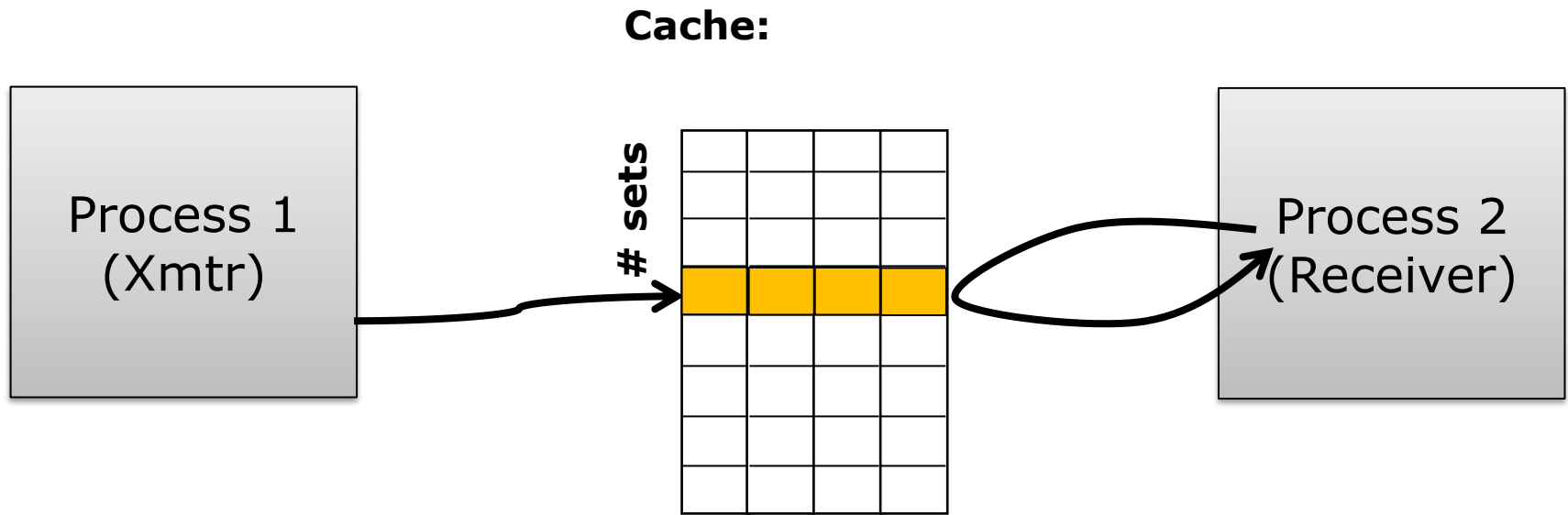
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fill a set

A Multi-way Cache-based Channel



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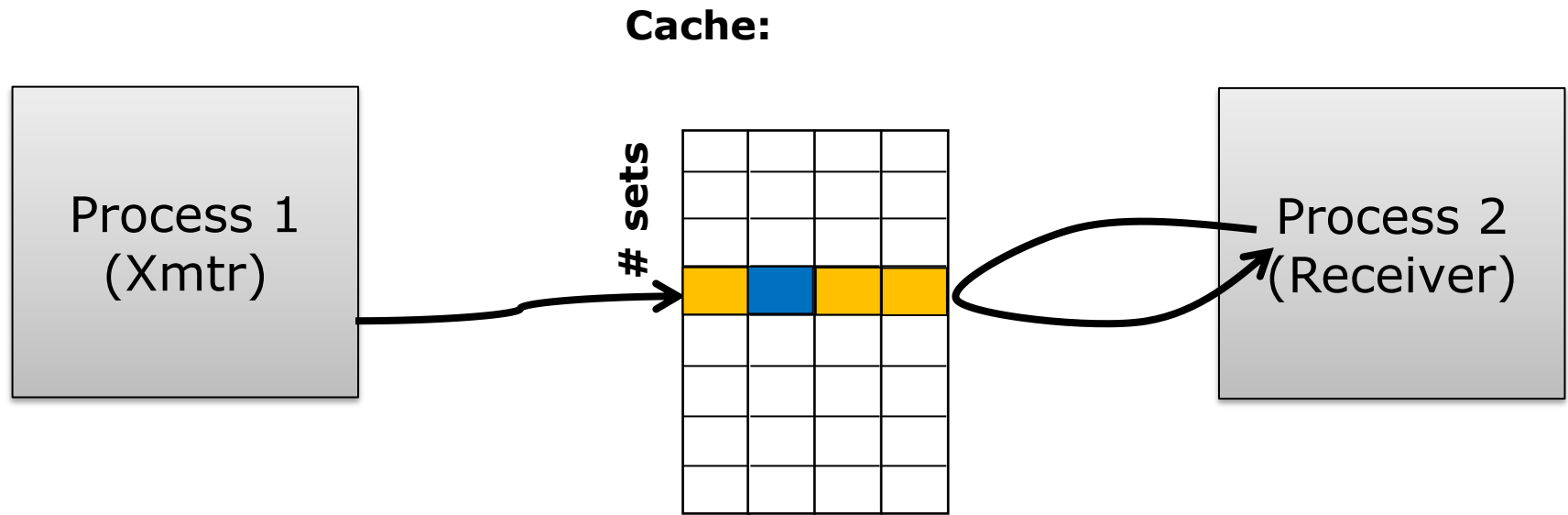
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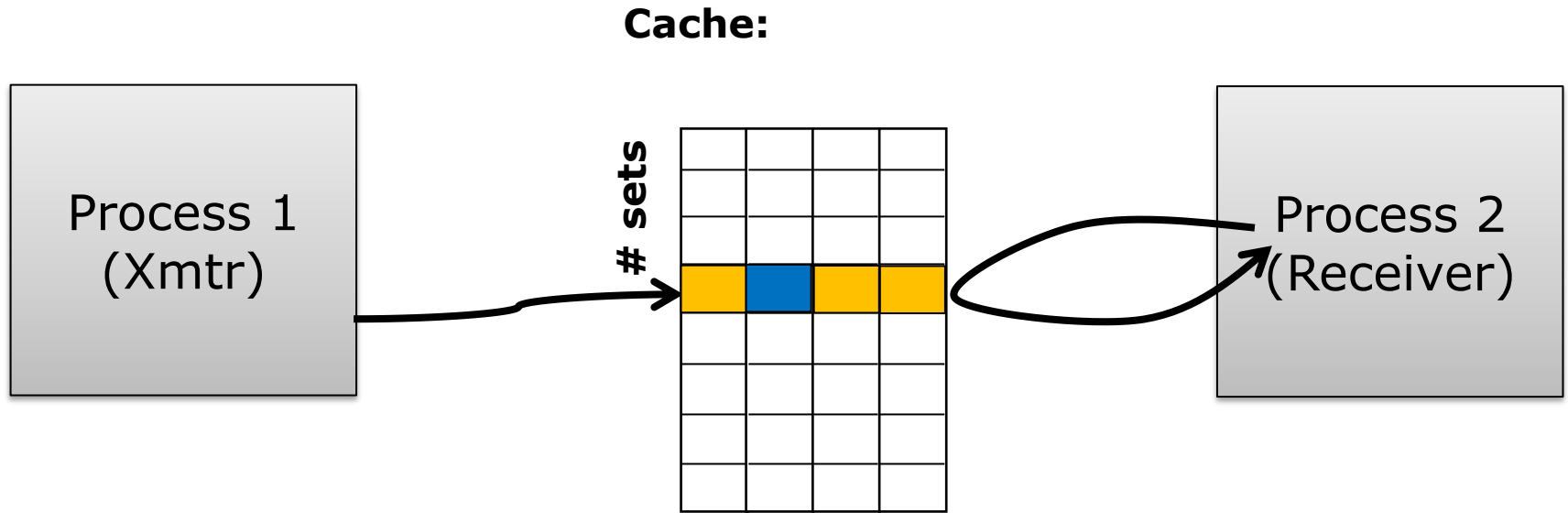
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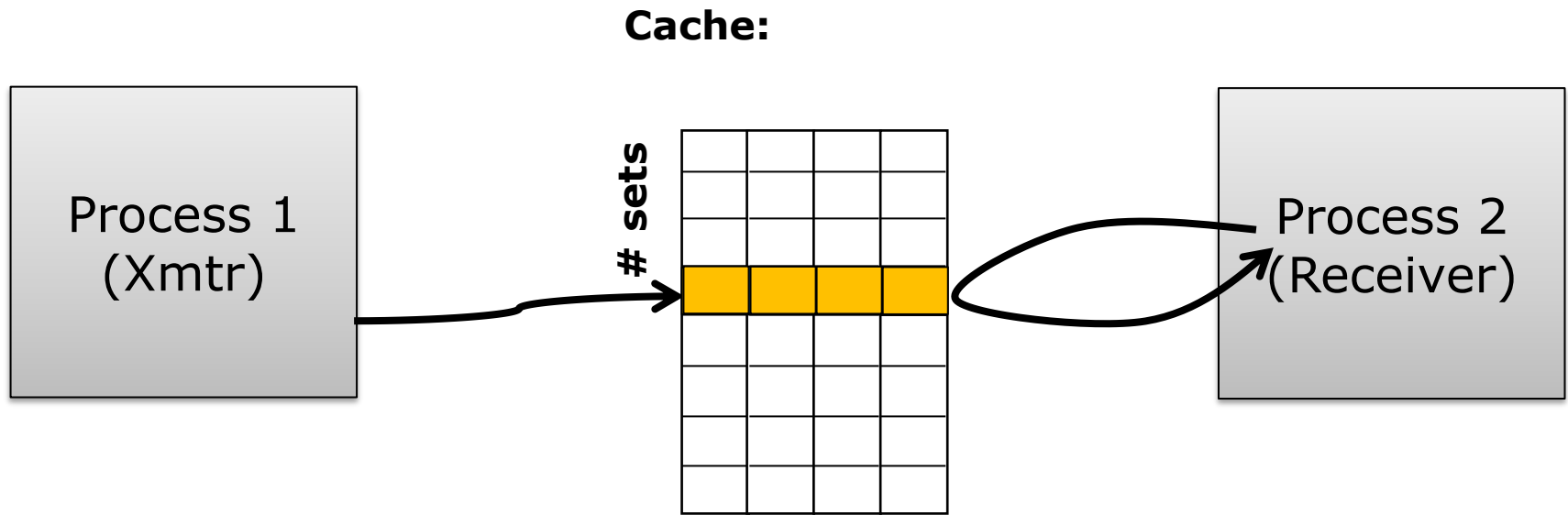
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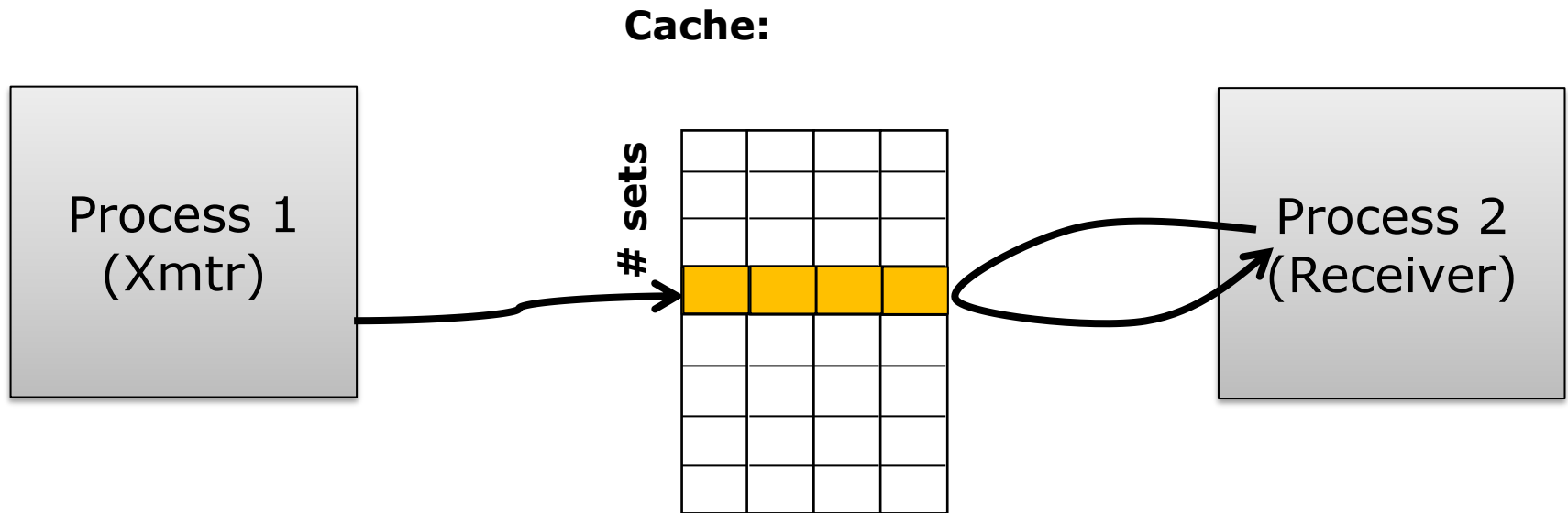
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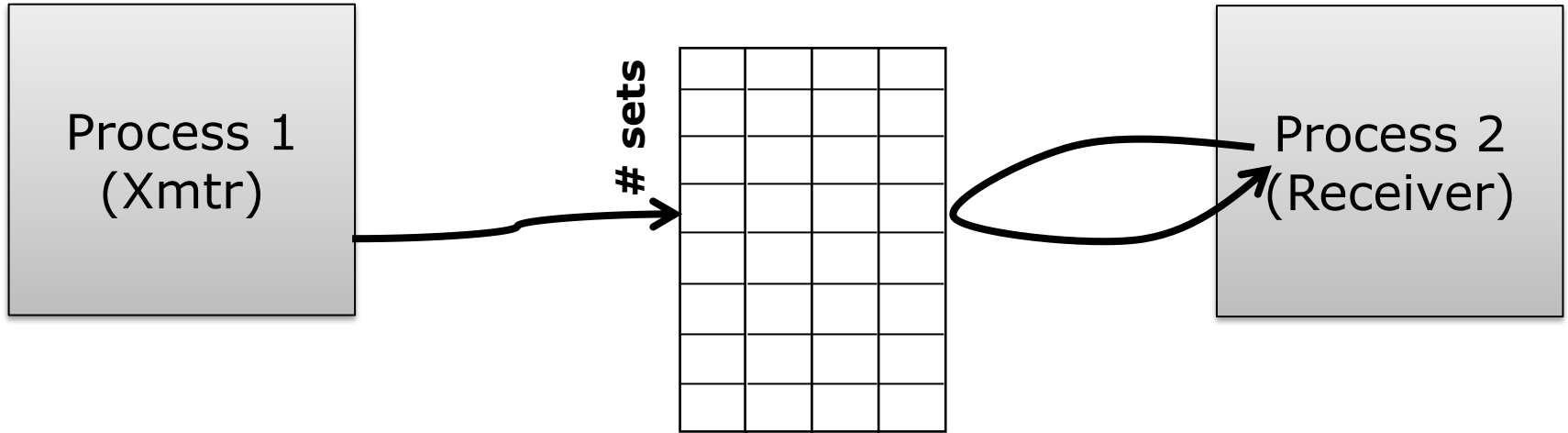
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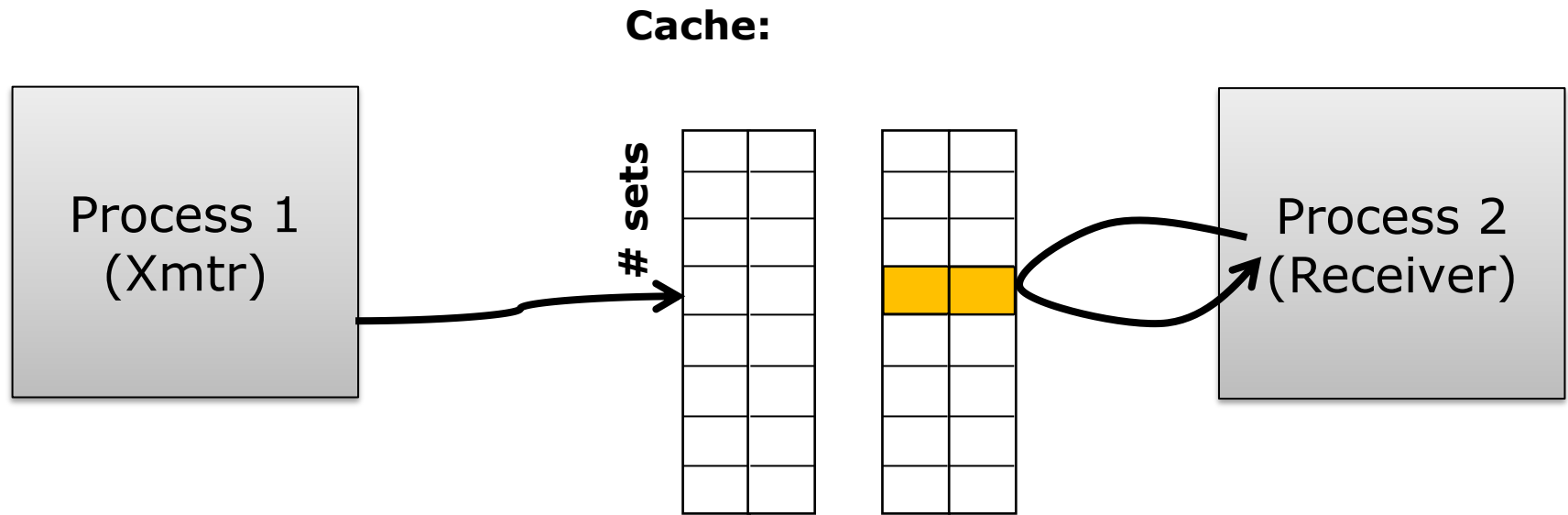
 decode '0'

Disrupting Communication

Cache:

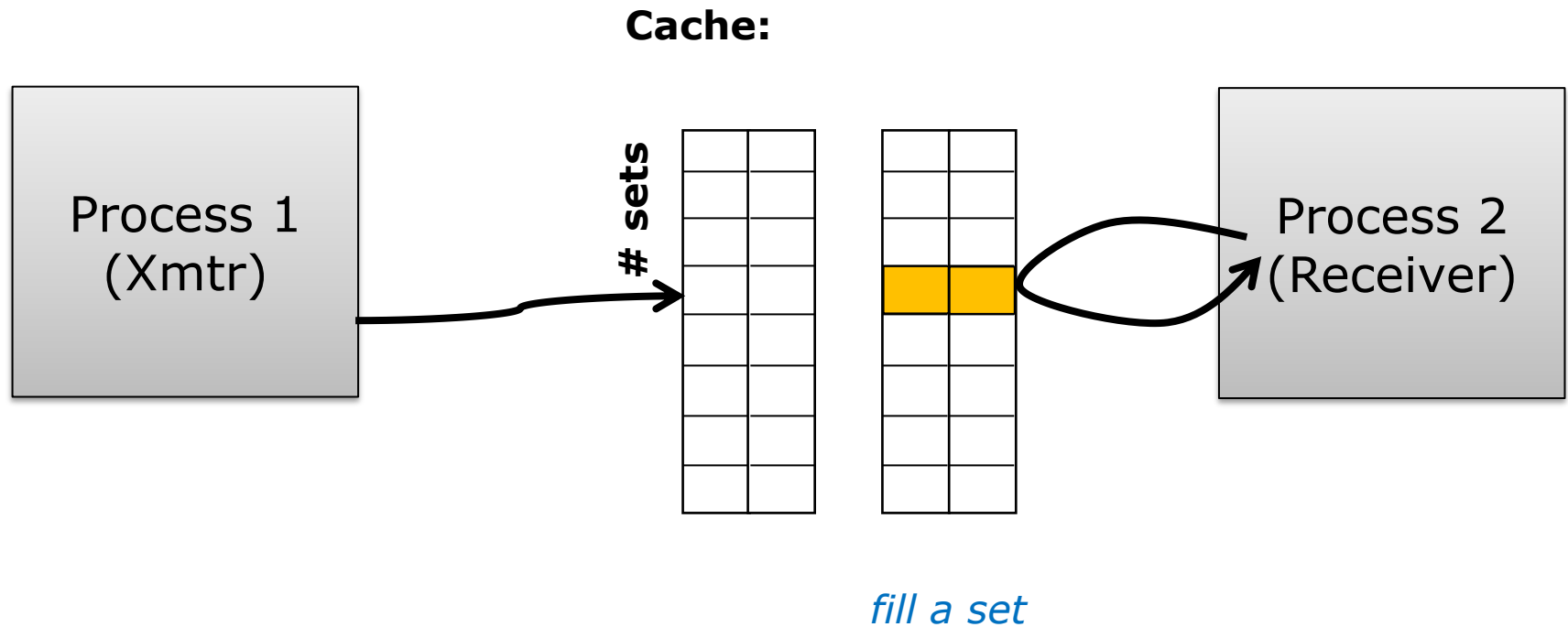


Disrupting Communication



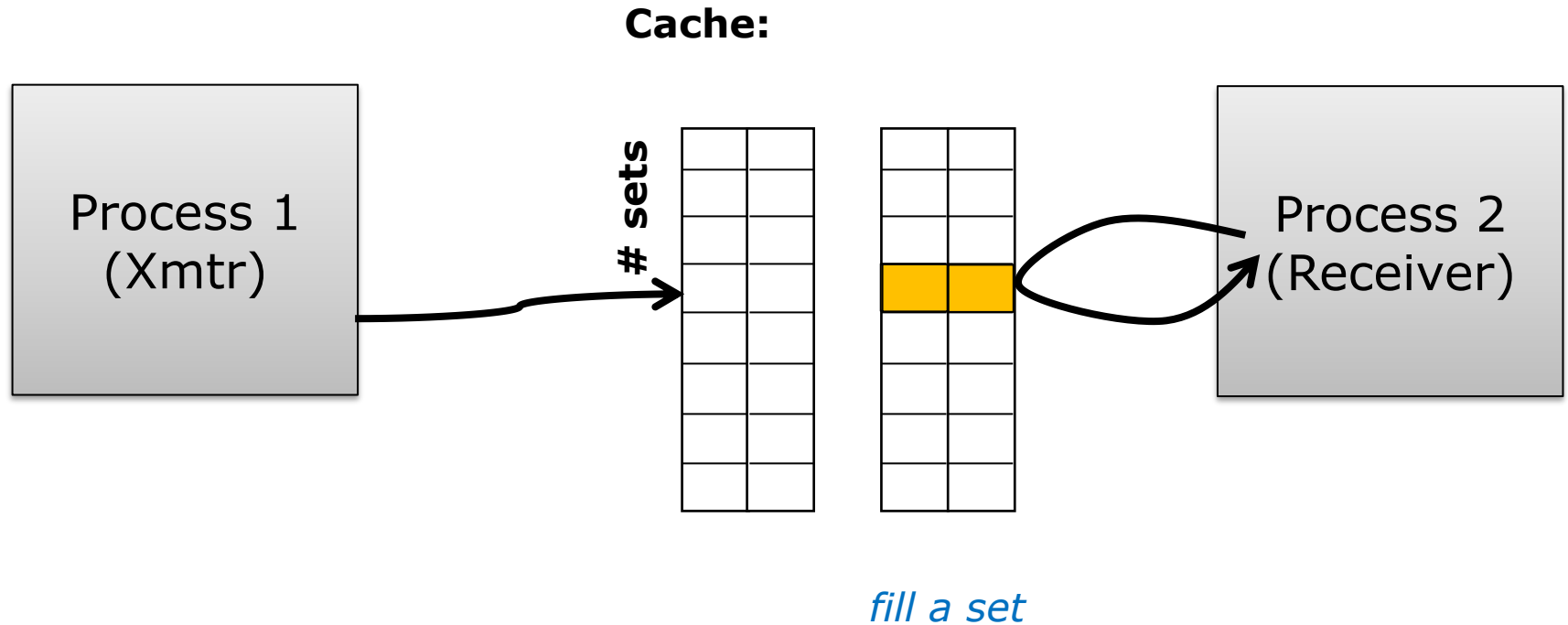
Kirianski et. al. Dawg, Micro'18

Disrupting Communication



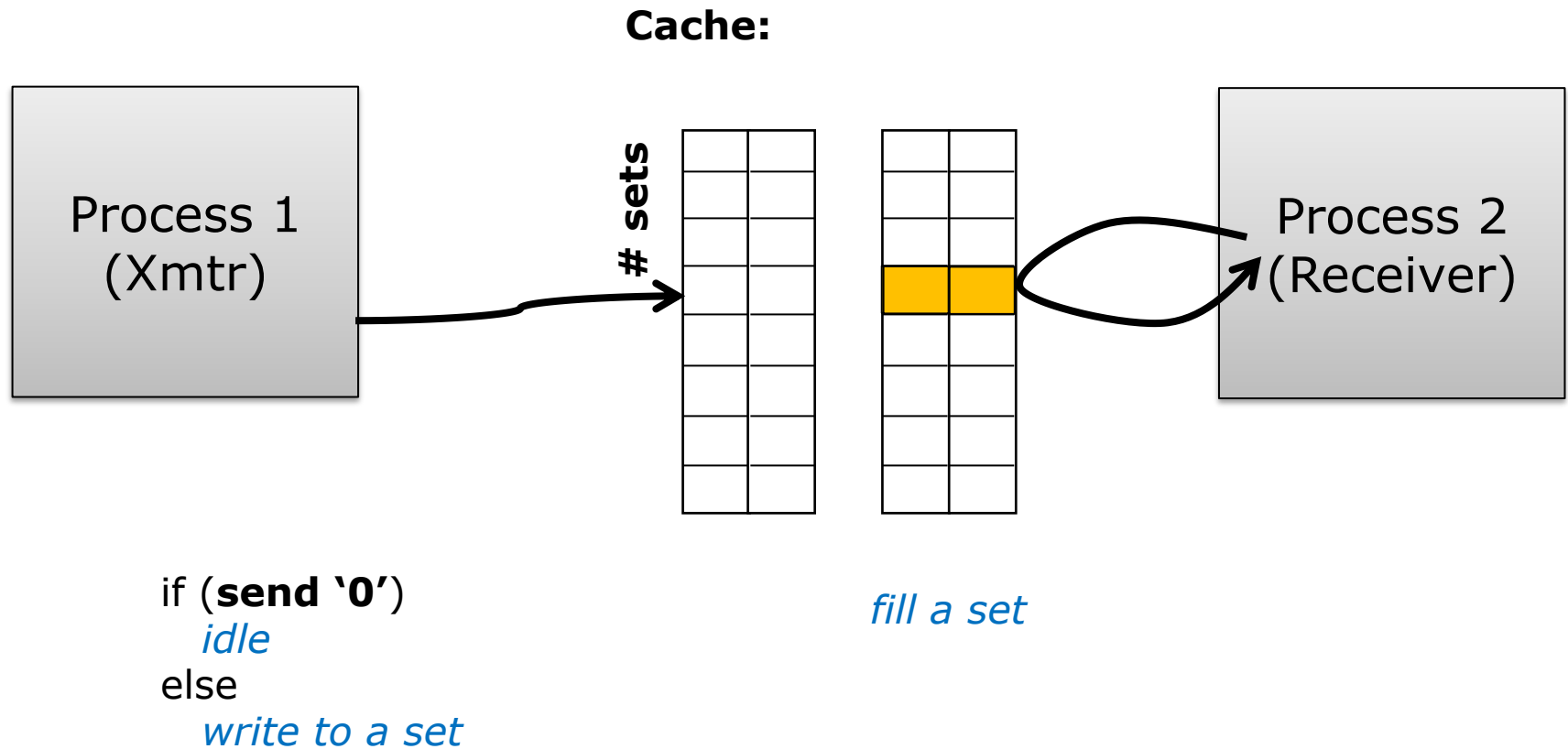
Kirianski et. al. Dawg, Micro'18

Disrupting Communication



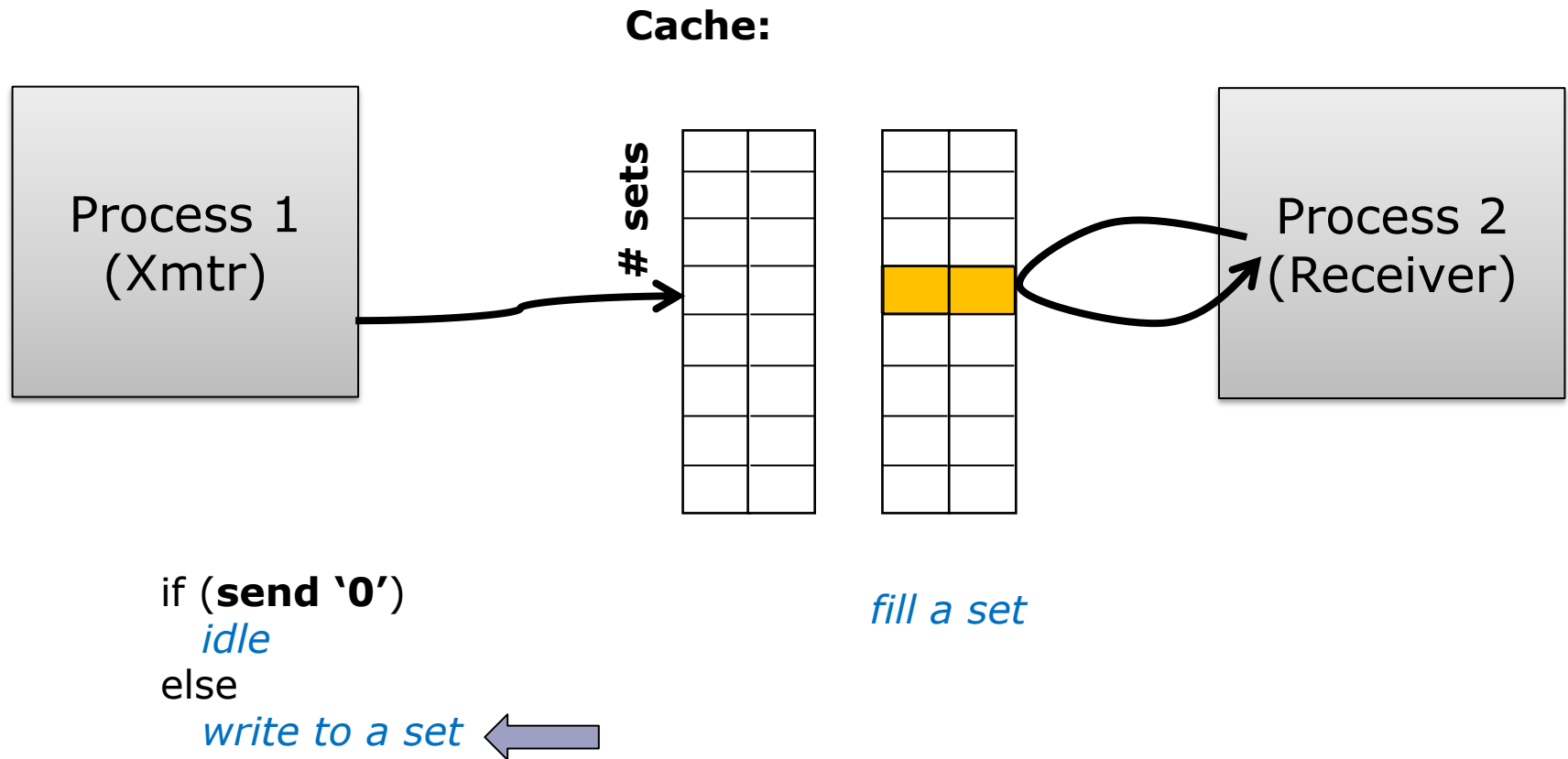
Kirianski et. al. Dawg, Micro'18

Disrupting Communication



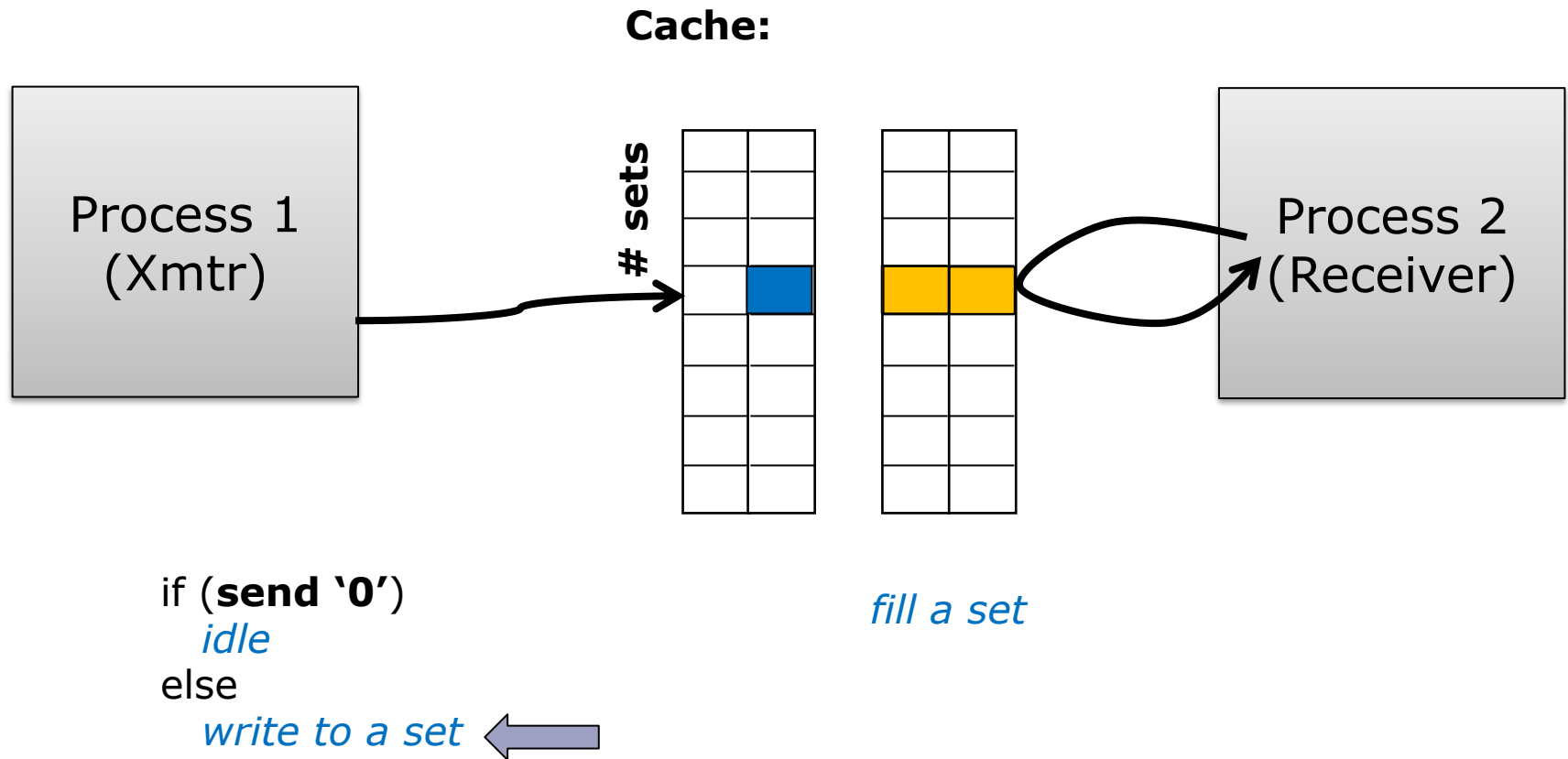
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Disrupting Communication



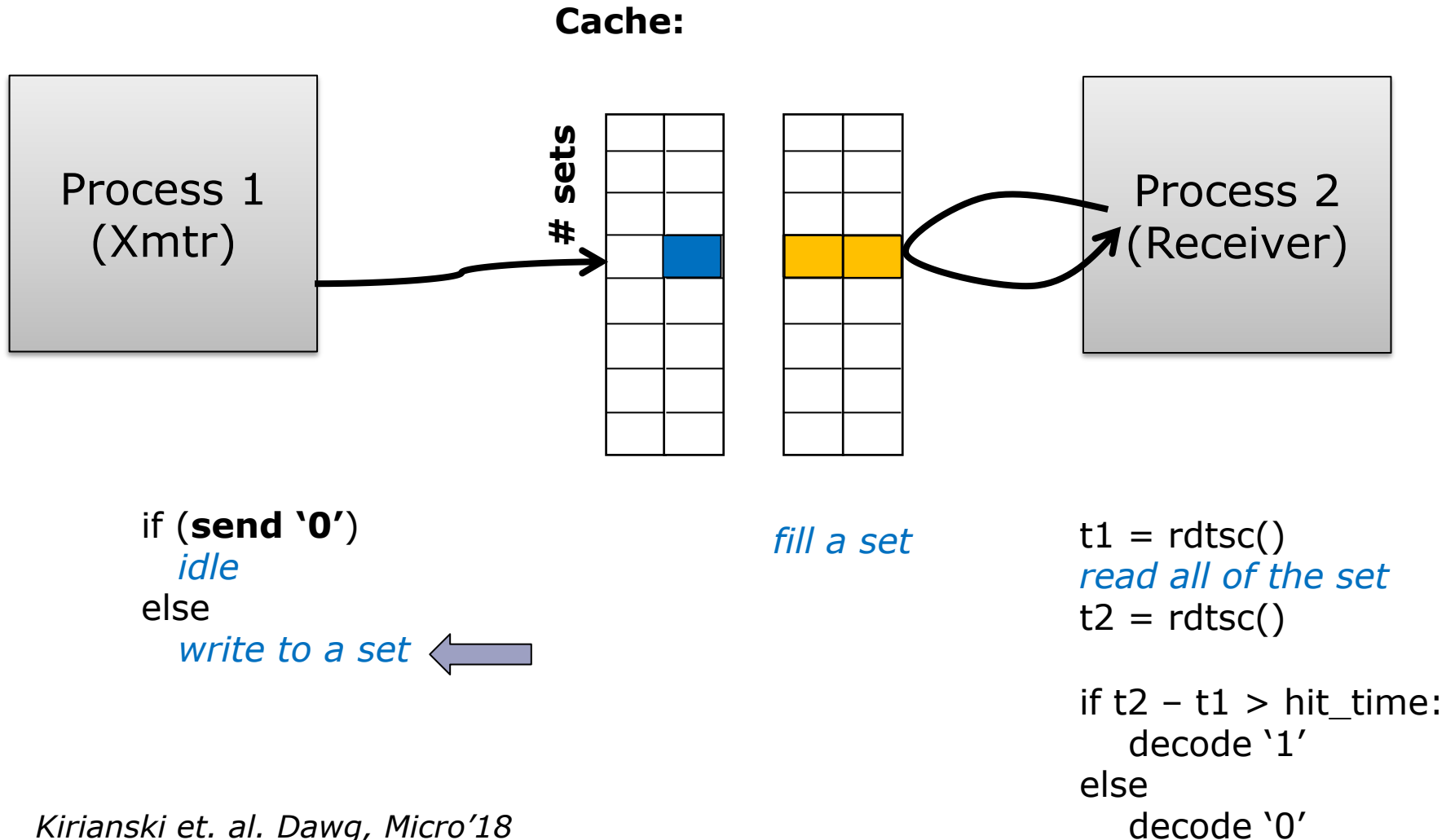
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Disrupting Communication



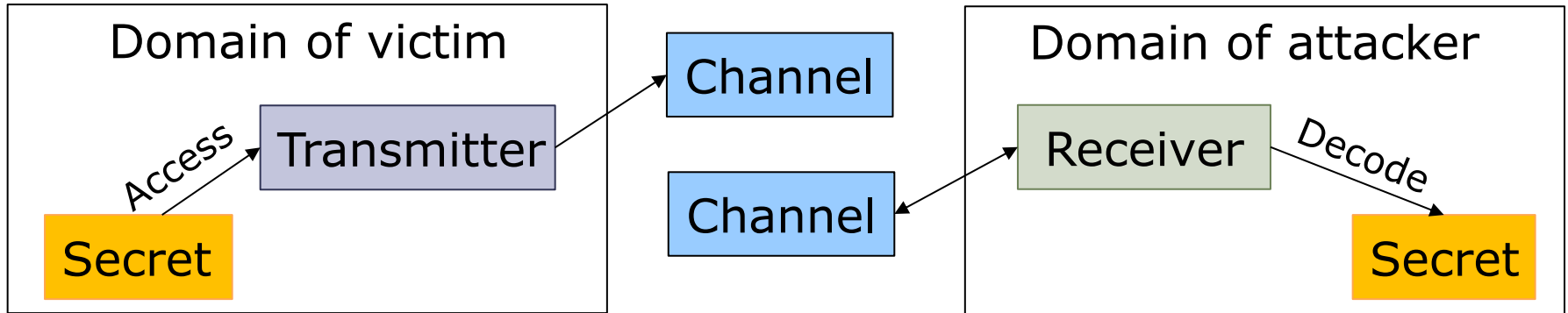
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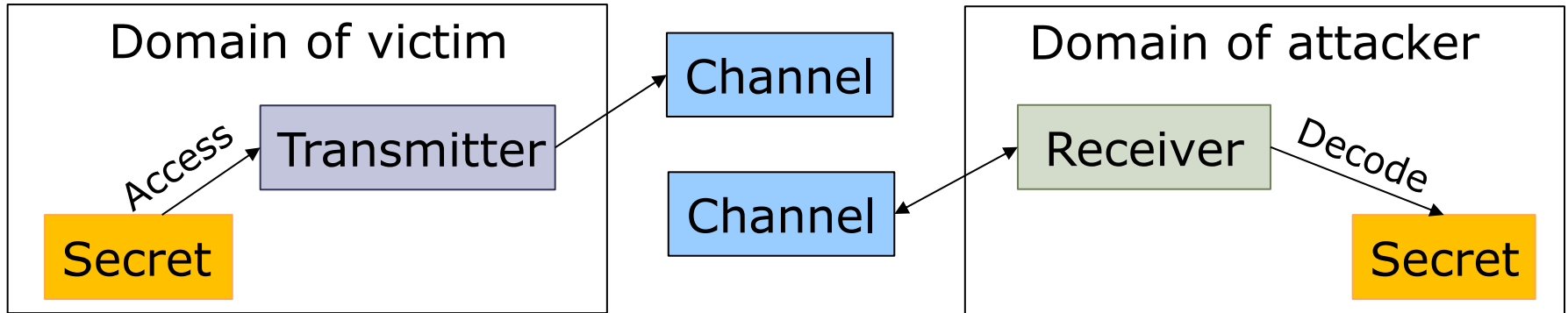


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Disjoint Channels

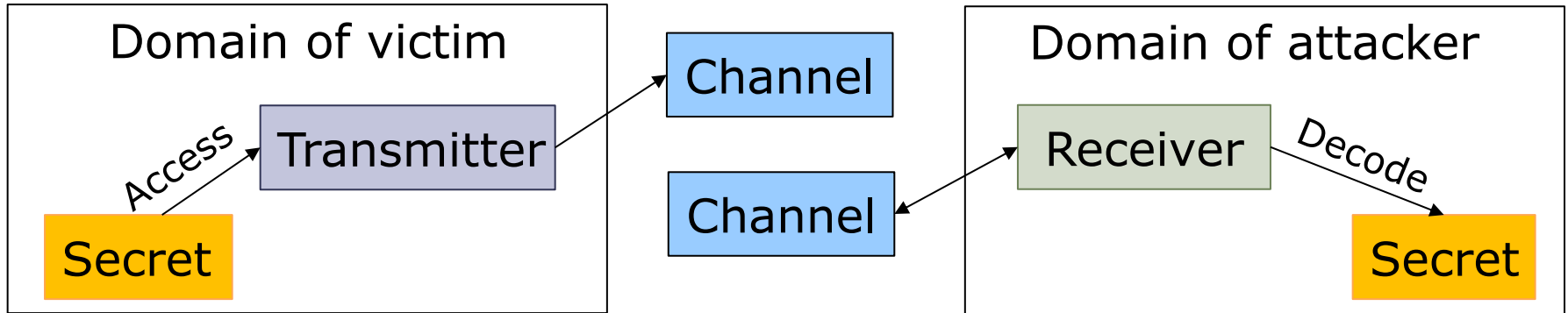


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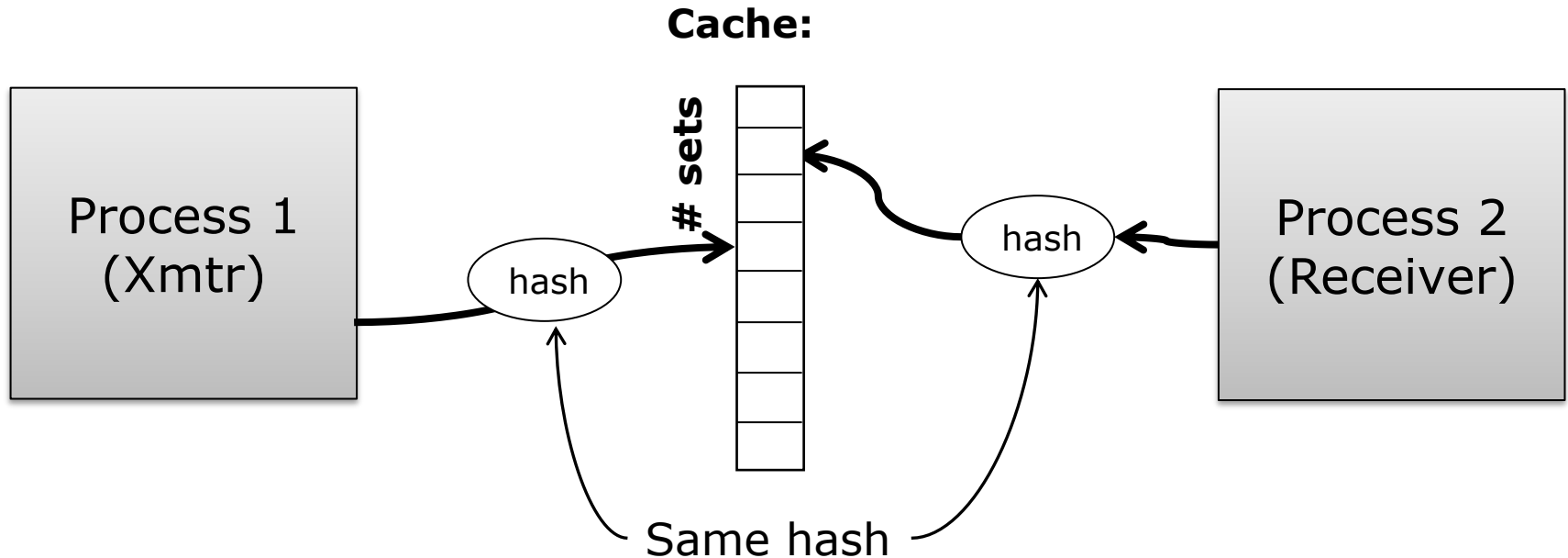
1. Making disjoint channels makes communication impossible.

Disjoint Channels



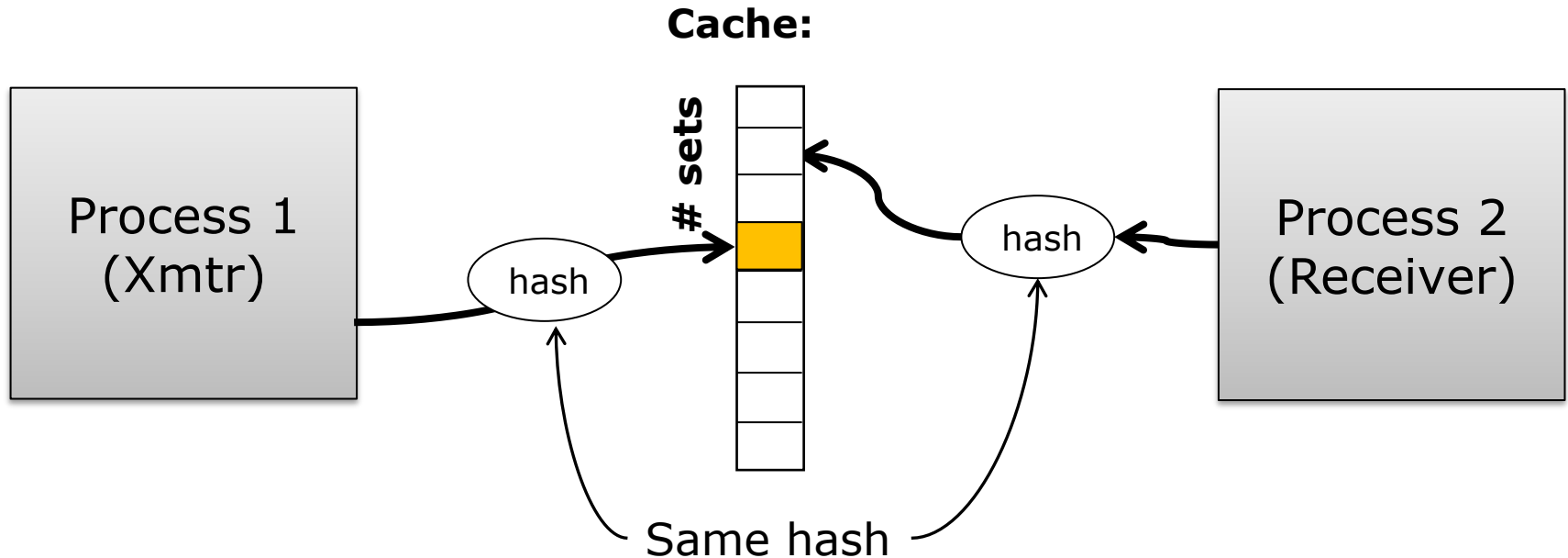
1. Making disjoint channels makes communication impossible.
2. Channel can be allocated by "domain" and will need to be "cleaned" as processes enter and leave running state, so next process cannot see any "modulation" on the channel.

Obfuscating the channel (1)



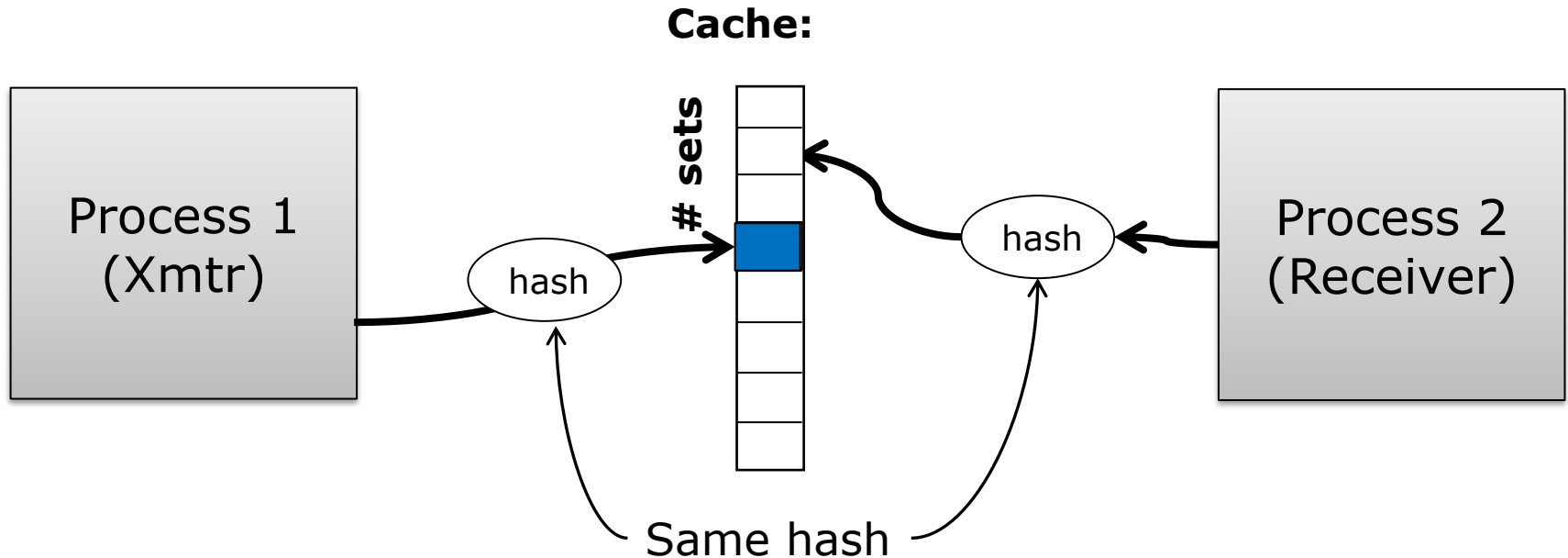
- Adding a single hash makes it difficult for the receiver to craft an address that monitors a specific set because addresses in each process will not match one-to-one.

Obfuscating the channel (1)



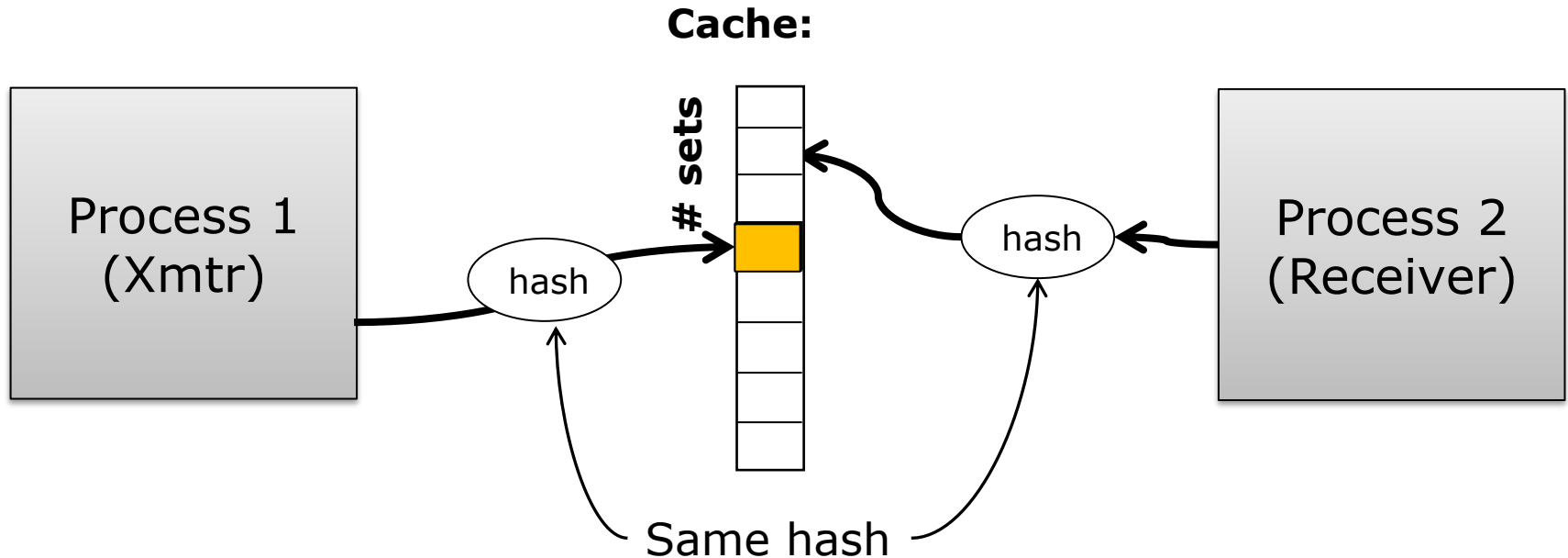
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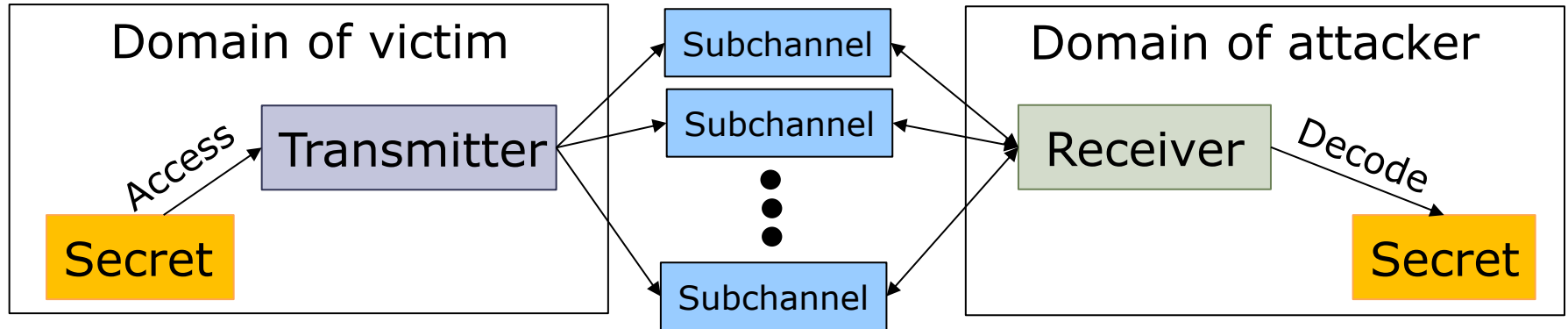
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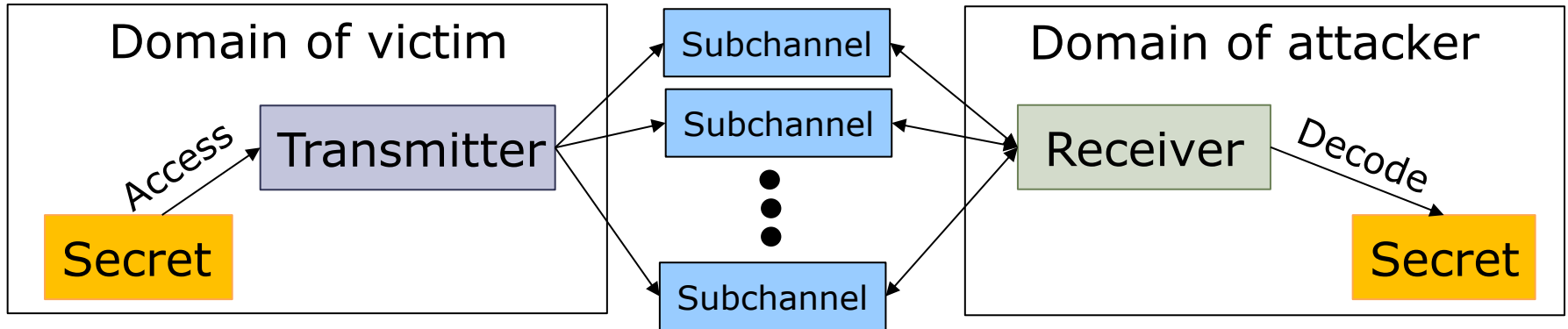


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Communication with subchannels

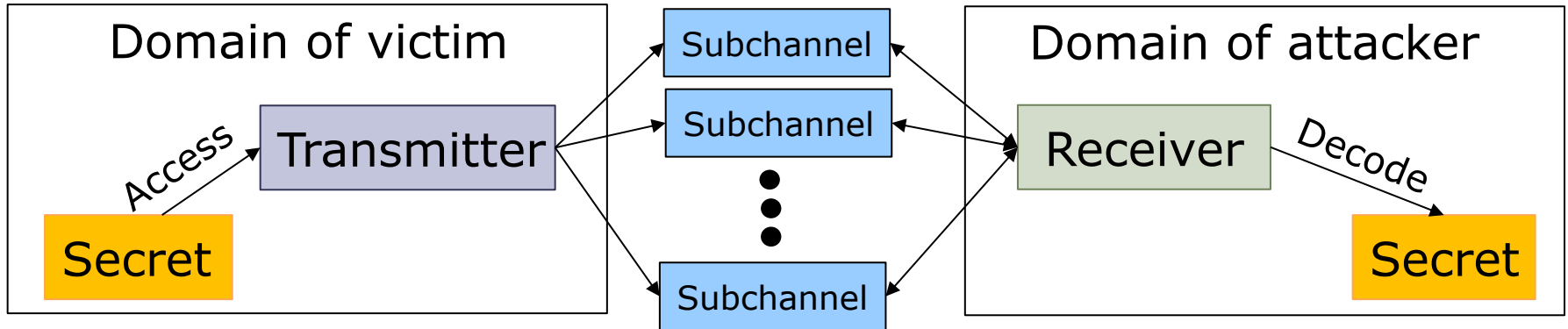


Communication with subchannels



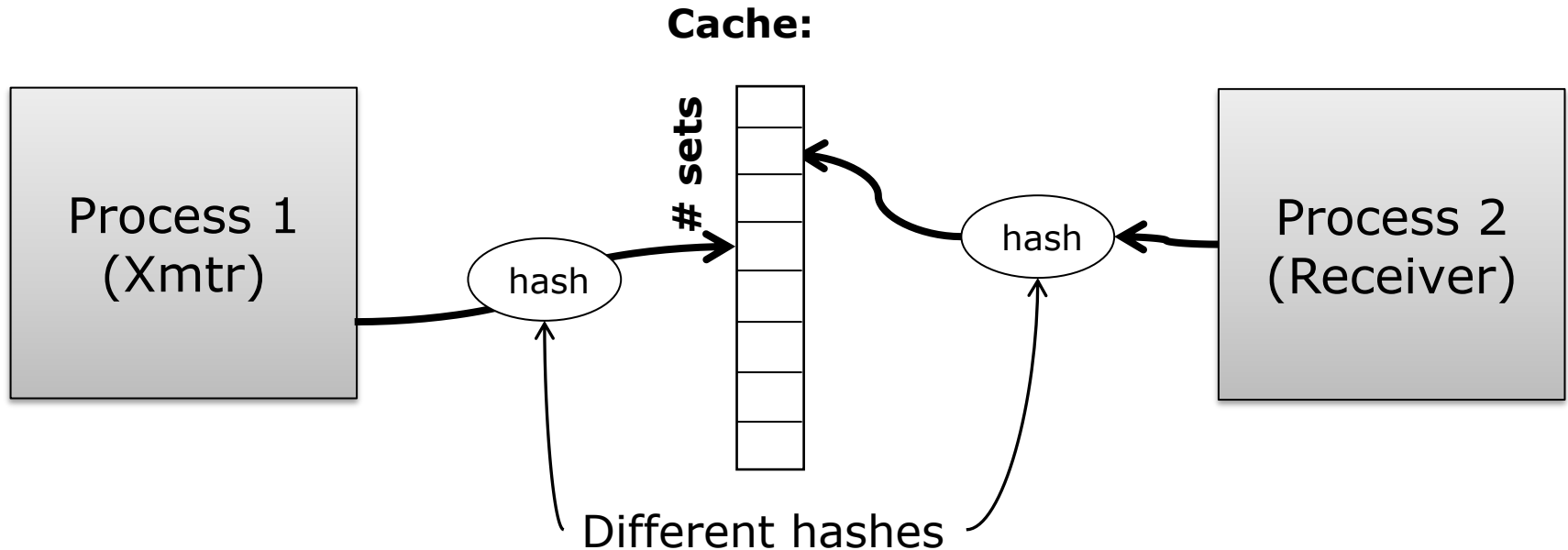
1. Transmissions may now occur on one of many subchannels

Communication with subchannels



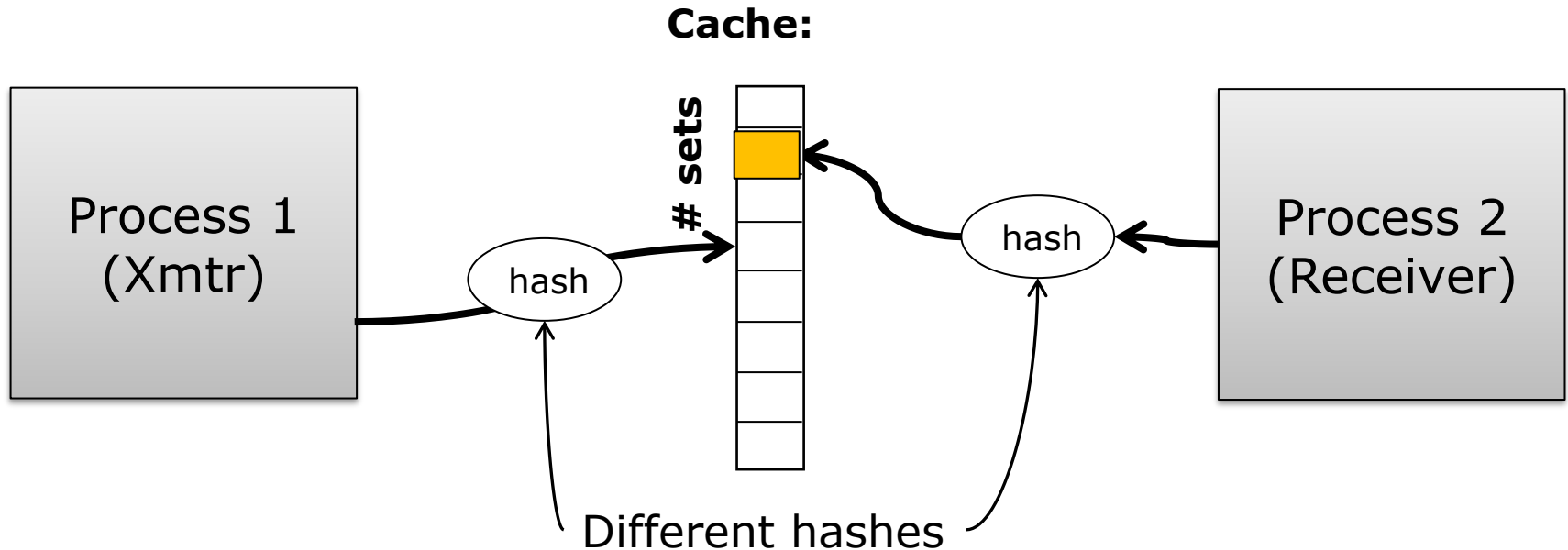
1. Transmissions may now occur on one of many subchannels
2. With a single hash, analysis by the receiver can, however, figure out which subchannel will be modulated.

Obfuscating the channel (2)



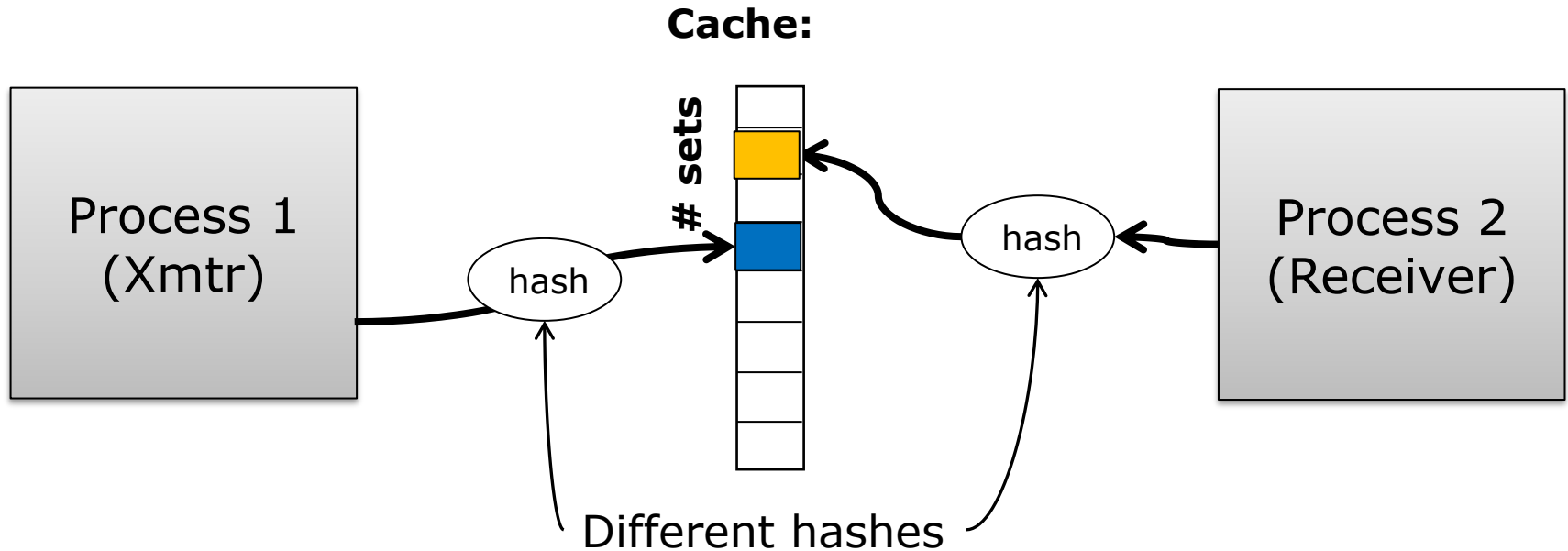
- Adding a process dependent hash makes the needed cache collision probabilistic.
- Now the receiver needs an extra step to find a way to probe a variety of “channels” to detect modulation.

Obfuscating the channel (2)



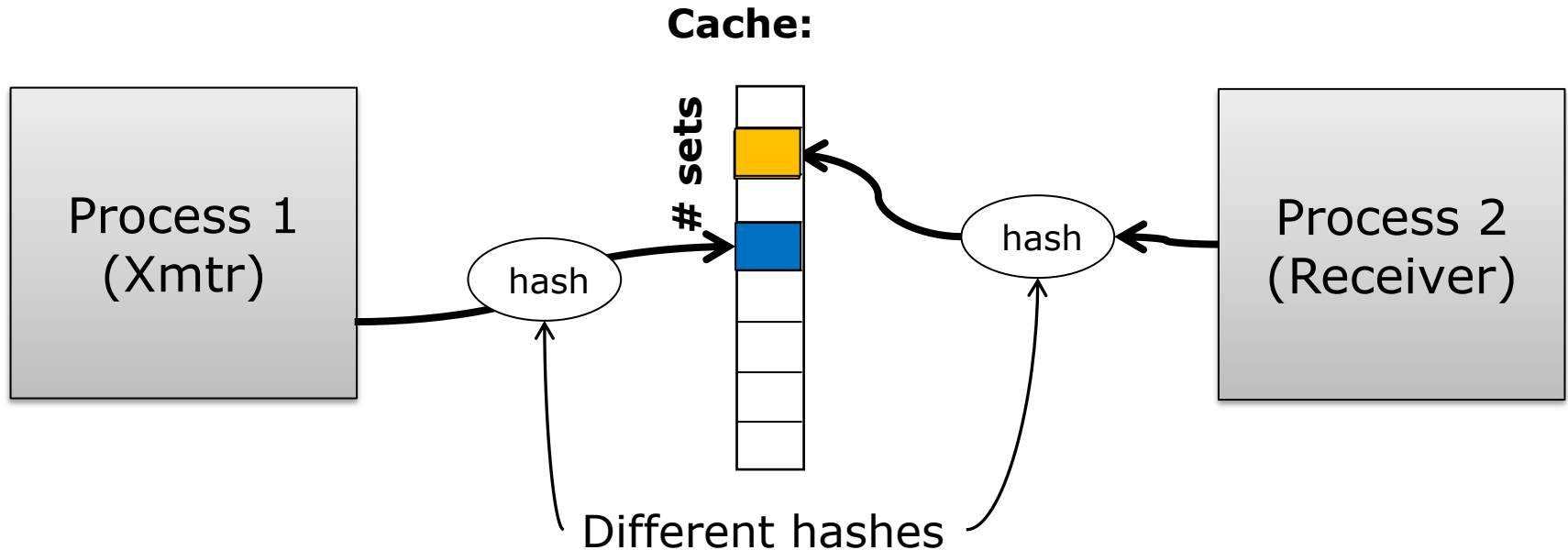
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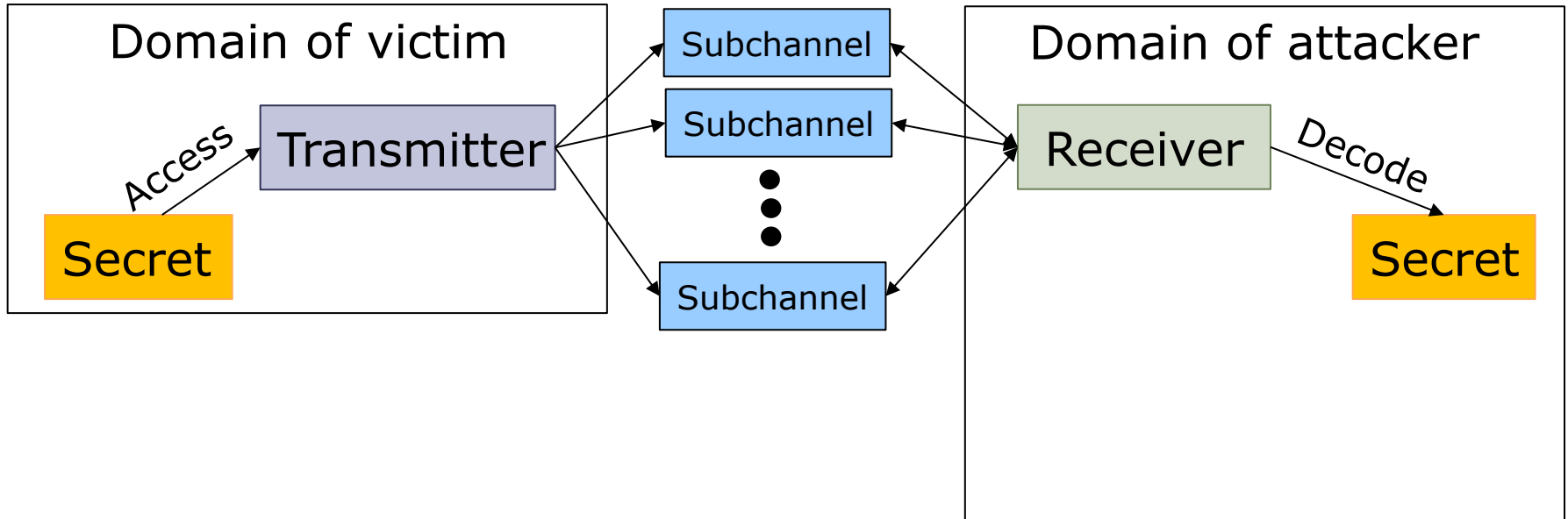
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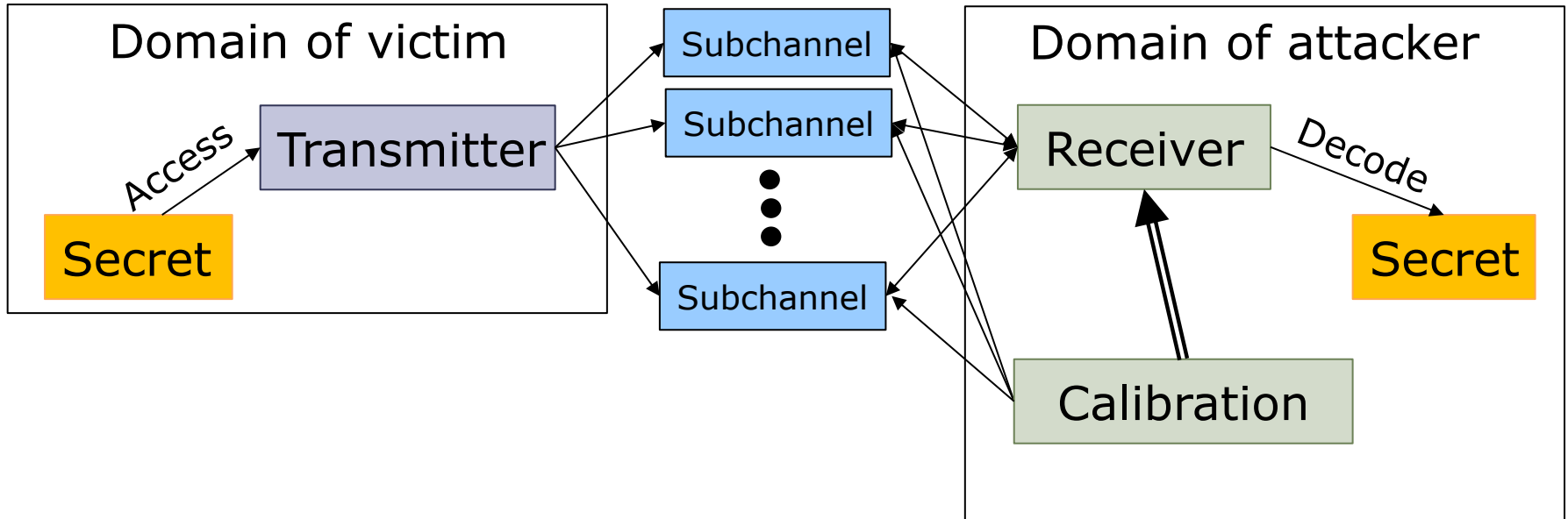


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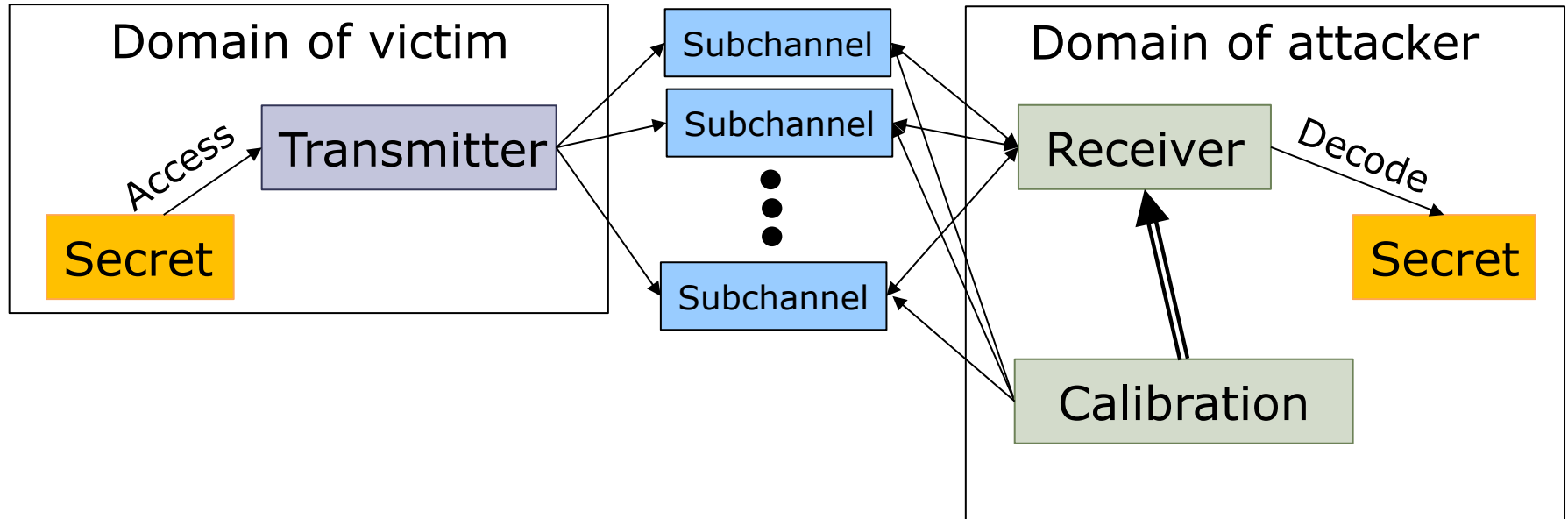
Receiver Calibration



Receiver Calibration

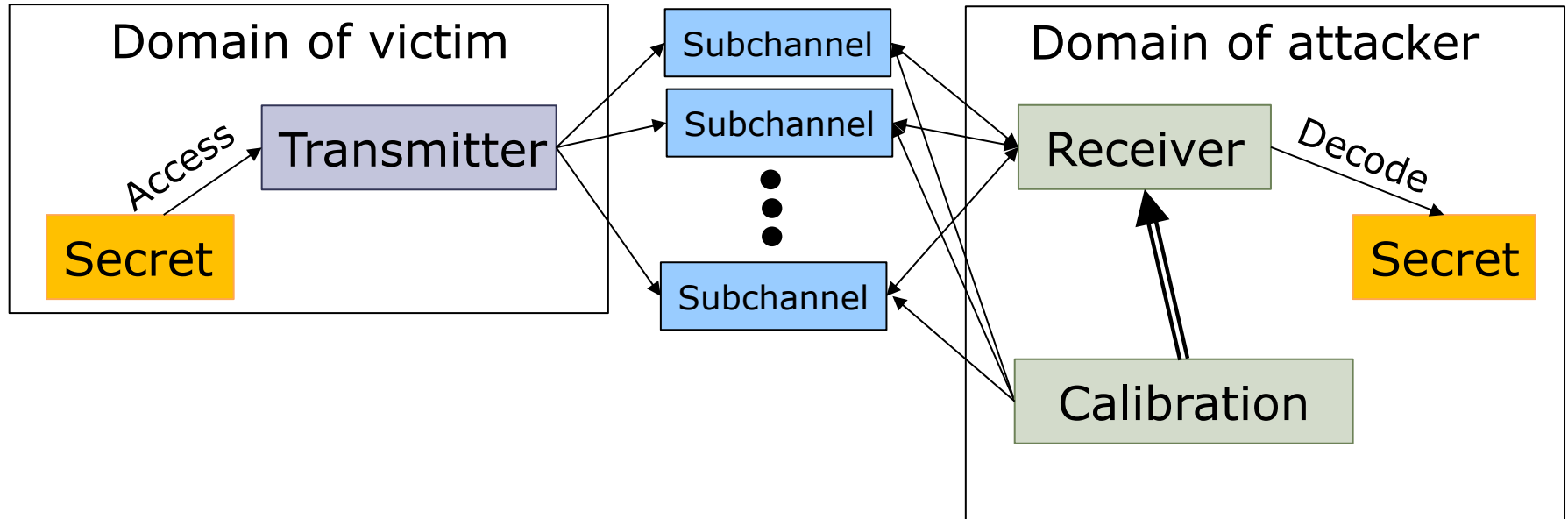


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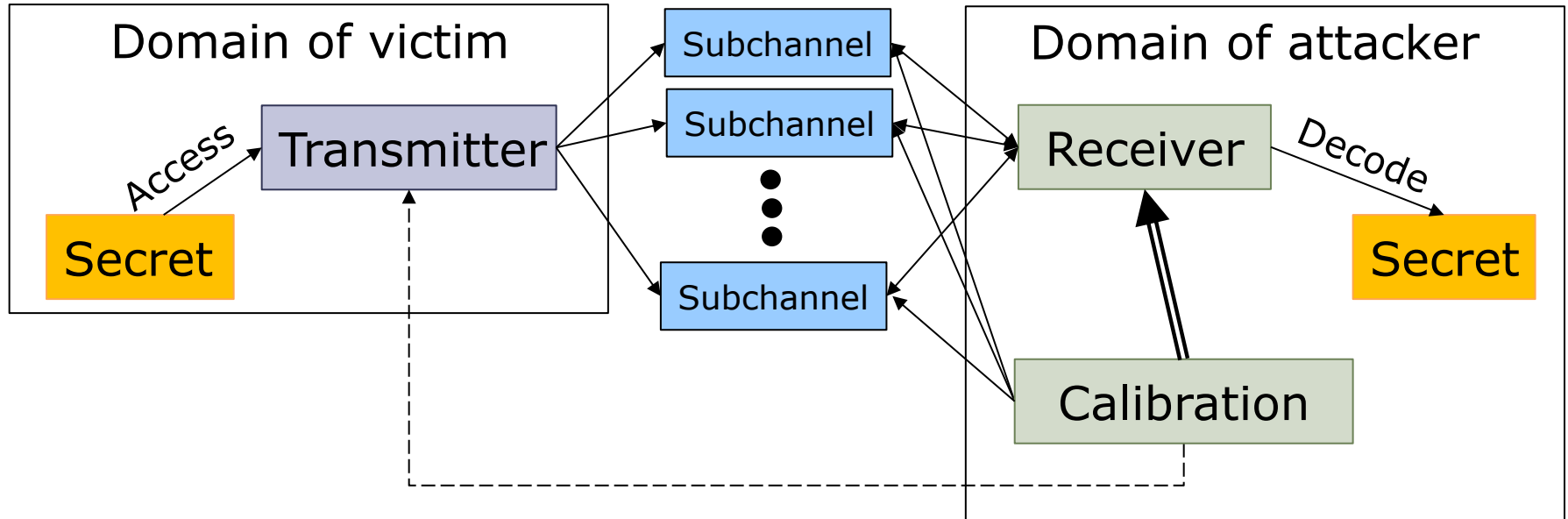
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1. The calibration unit determines which subchannels (addresses) the receiver needs to use to detect modulation by a transmission
2. The receiver may just observe known transmissions by the transmitter to determine the subchannels to monitor
3. Or, the receiver may provoke the transmitter to make a particular transmission..

Hashing* variations

- Nature of hash
 - Well-known
 - Secret
 - Cryptographic (per machine key)

*Hash -> address to set index mapping

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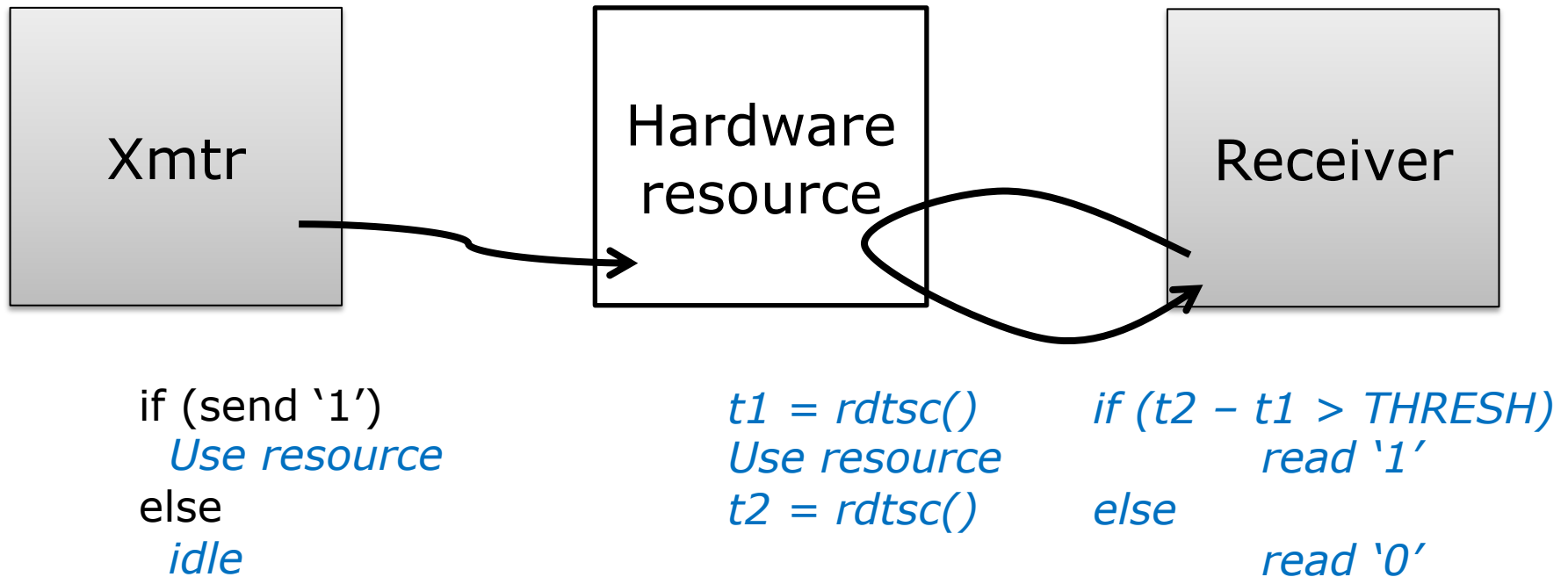
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 - Fixed interval in accesses (all sets at once or subset of sets)
 - Random interval (all sets at once or subset of sets)
- Hashes per address
 - Single or multiple

*Hash -> address to set index mapping

Generalizes to Other Resources



Types of State-based Channels

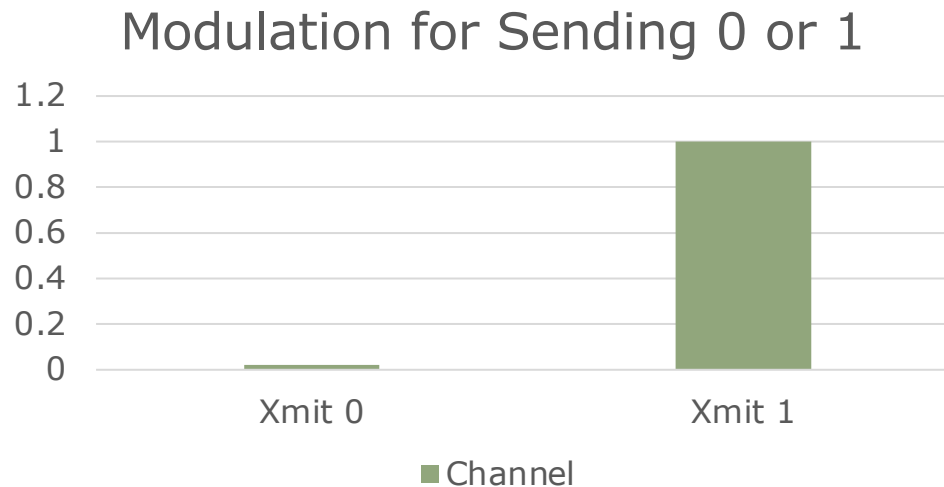
Resource	Shared by
Private cache (L1, L2)	Intra-core
Shared cache (LLC)	On-socket cross core
Cache directory	Cross socket
DRAM row buffer	Cross socket
TLB (private/shared)	Intra-core/Inter-core
Branch Predictor	Intra-core
....	...

Simple Transmitter

```
secret = oneof(0..1)  
if secret == 1:  
    x = channel
```

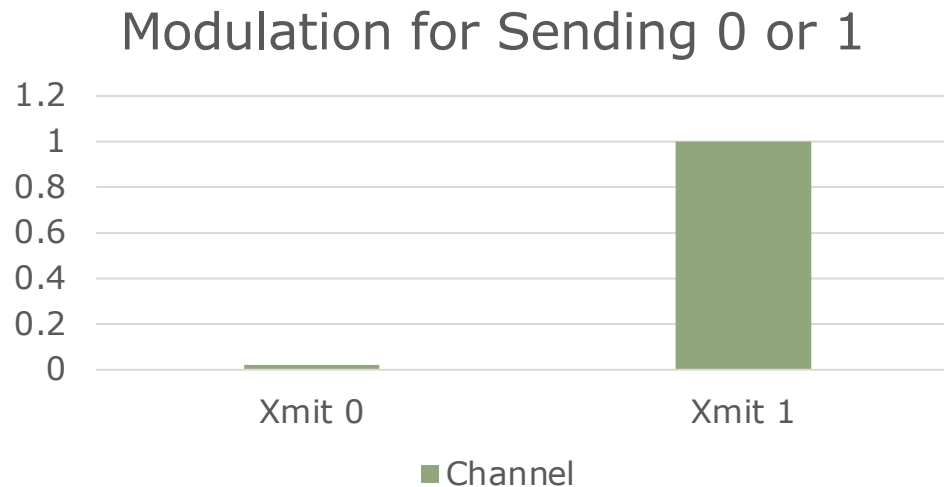
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Like an amplitude modulated (AM) radio transmission

"AM" Transmitter in RSA

[Percival 2005]

- Assume square-and-multiply based exponentiation

```
Input : base b, modulo  $m$ ,  
         exponent e =  $(e_{n-1} \dots e_0)_2$   
Output:  $b^e \bmod m$   
 $r = 1$   
for  $i = n-1$  down to 0 do  
     $r = \text{sqrt}(r)$   
     $r = \text{mod}(r, m)$   
    if  $e_i == 1$  then  
         $r = \text{mul}(r, \mathbf{b})$   
         $r = \text{mod}(r, m)$   
    end  
end  
return  $r$ 
```

"AM" Transmitter in RSA

[Percival 2005]

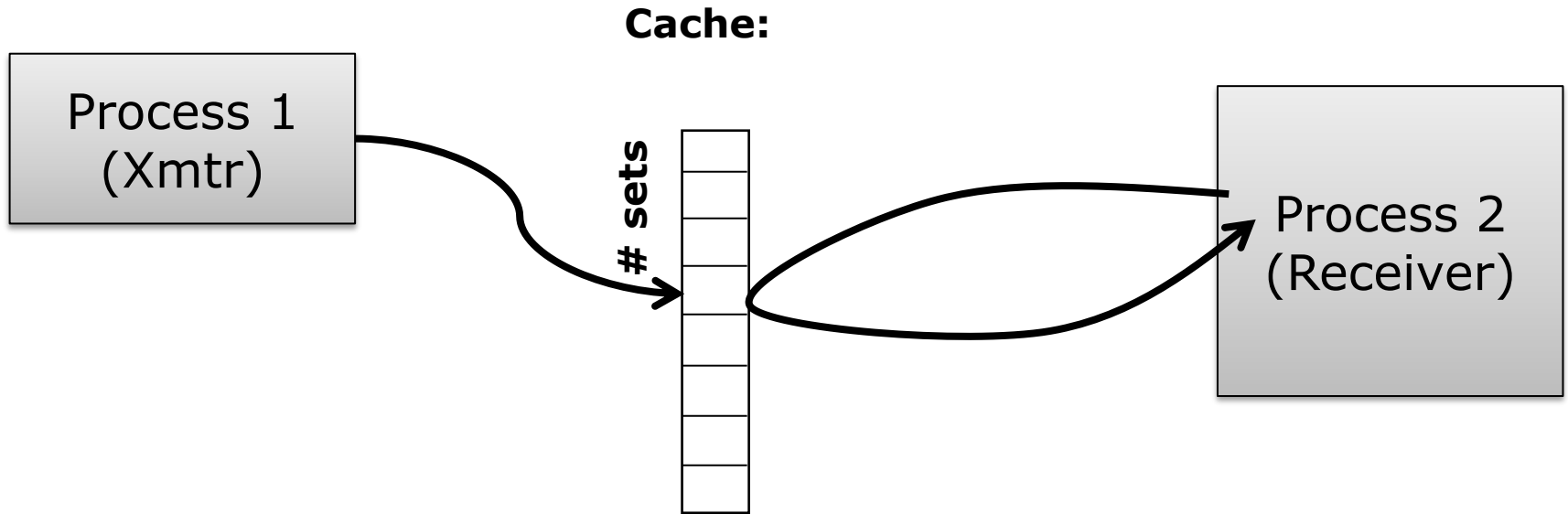
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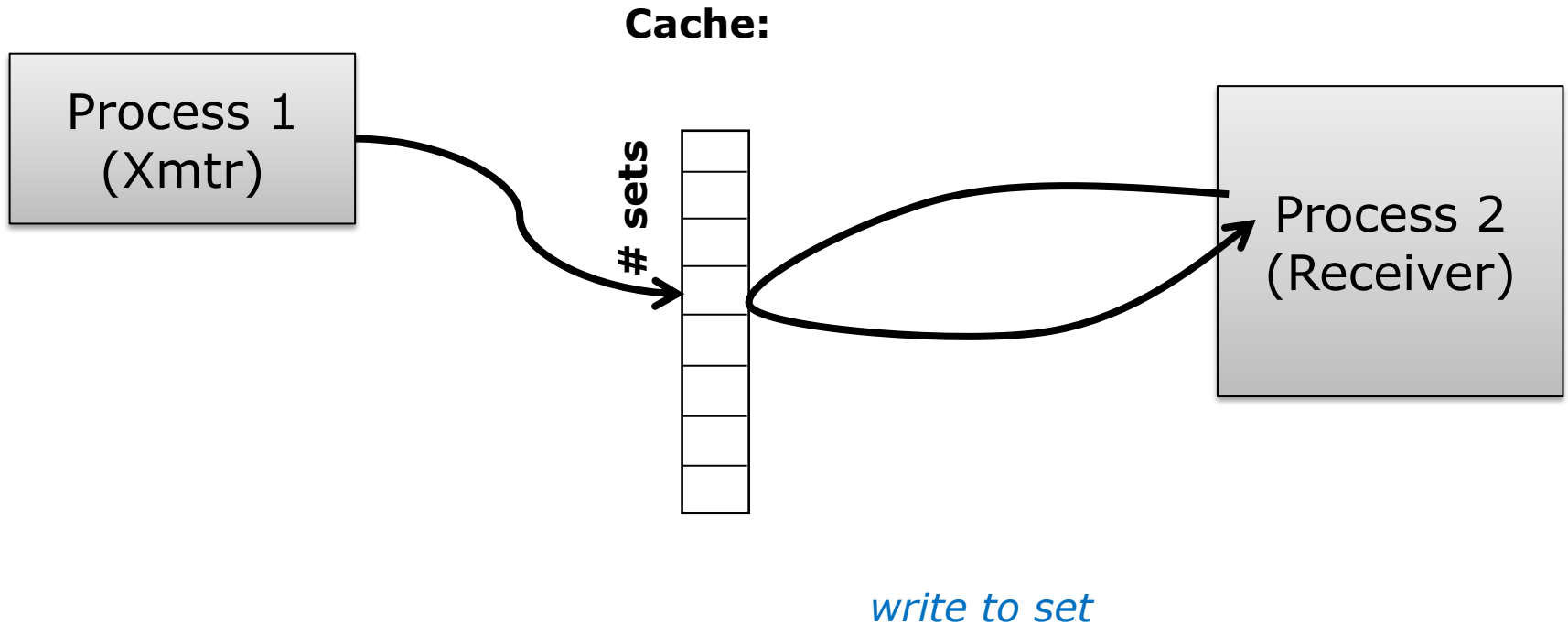
Secret-dependent
memory access →
transmitter



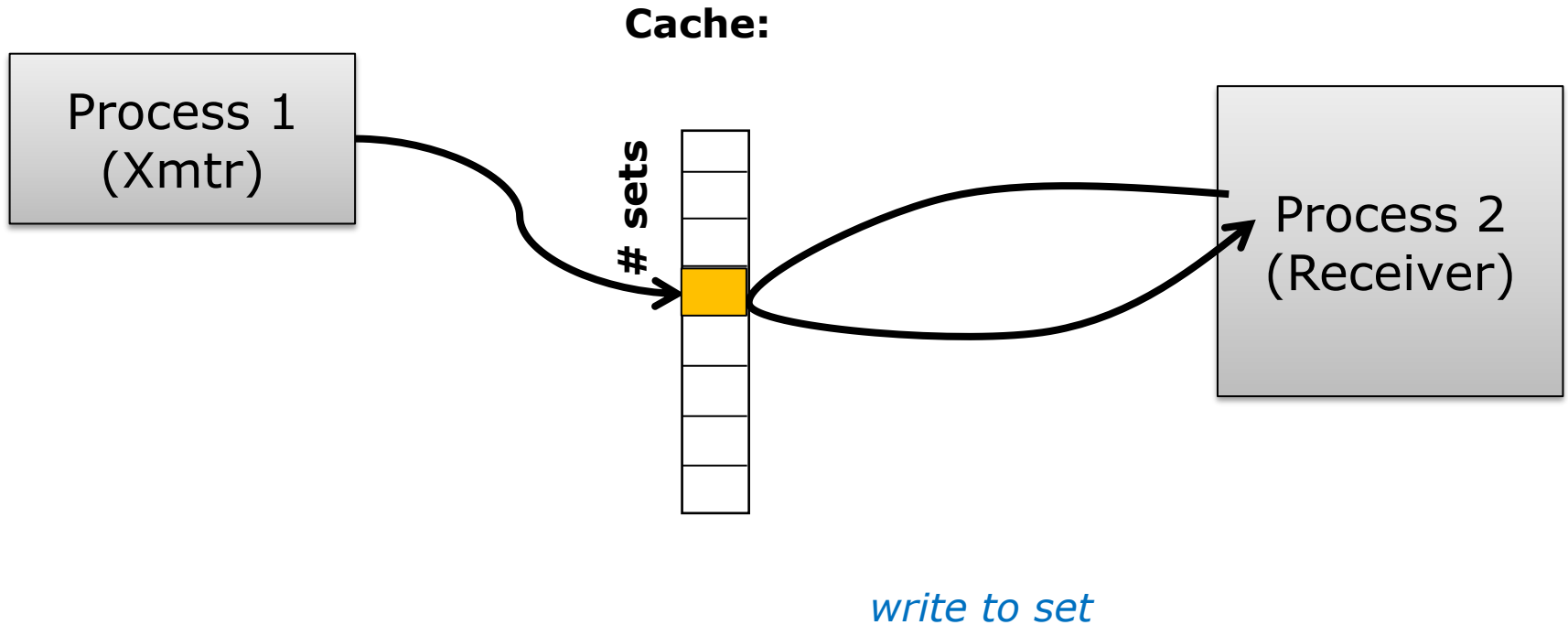
Noise in the channel



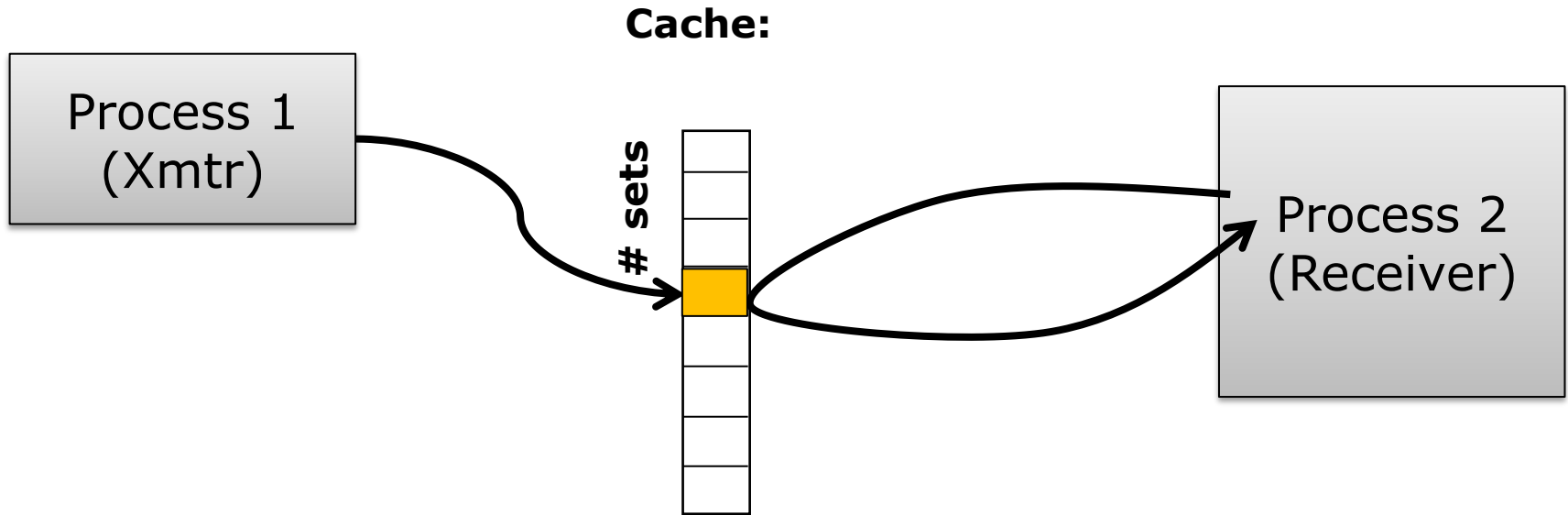
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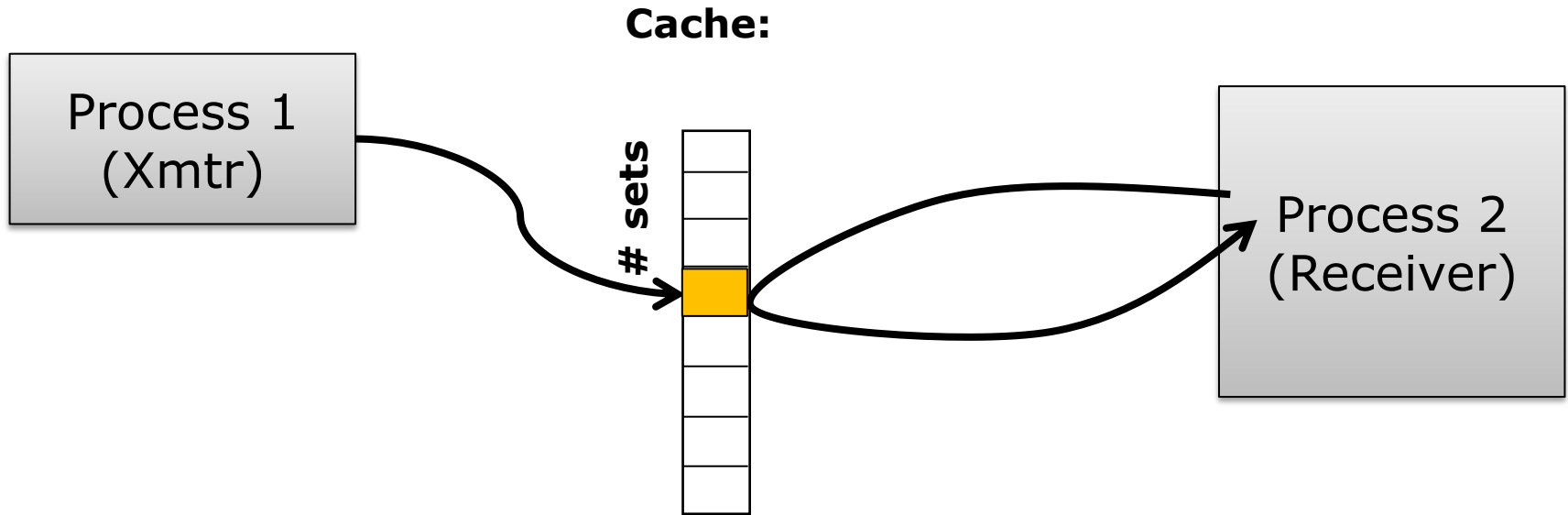
Noise in the channel



```
if (send '0')  
  idle  
else  
  write to a set
```

write to set

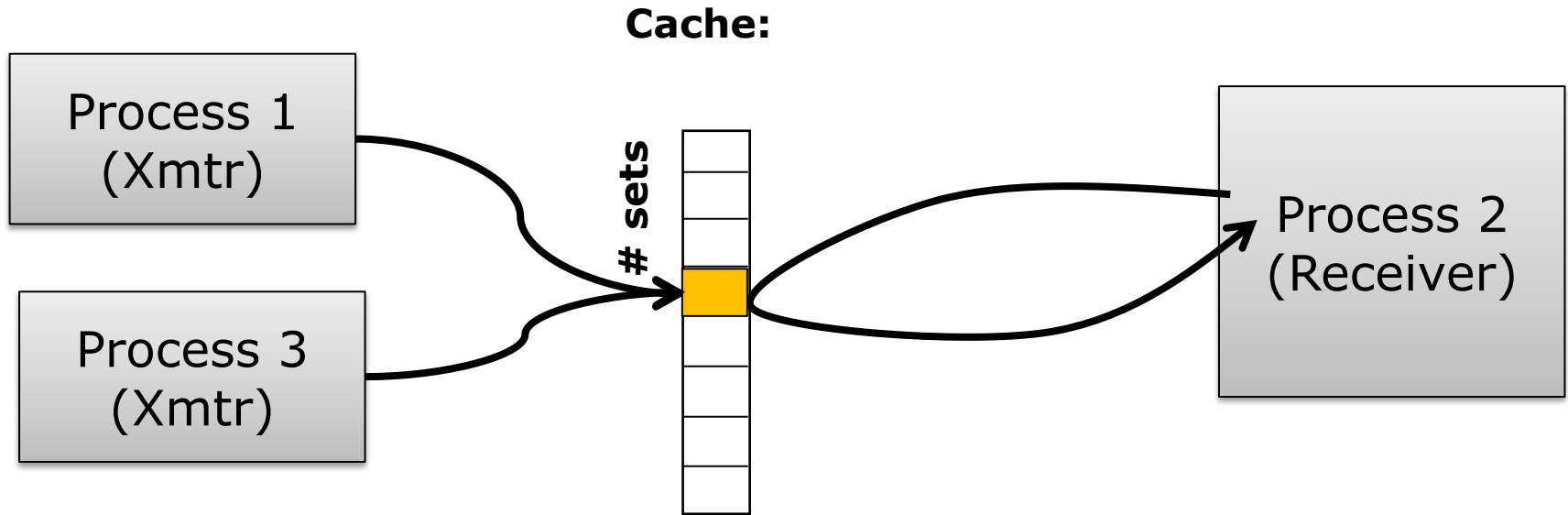
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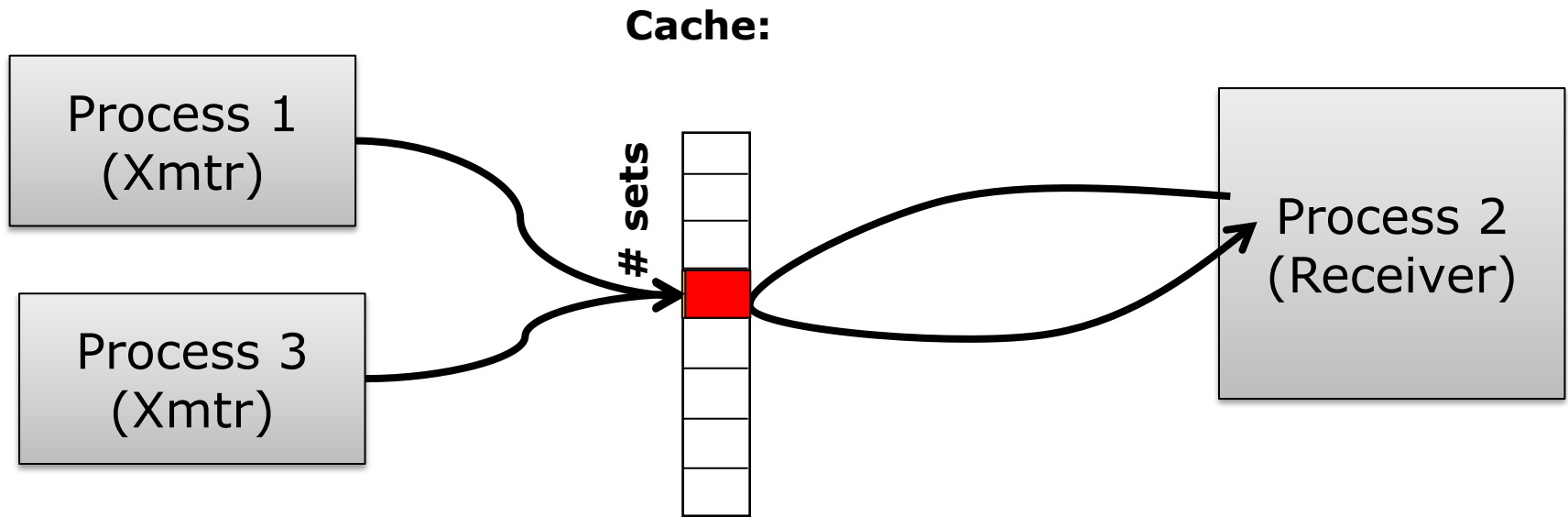
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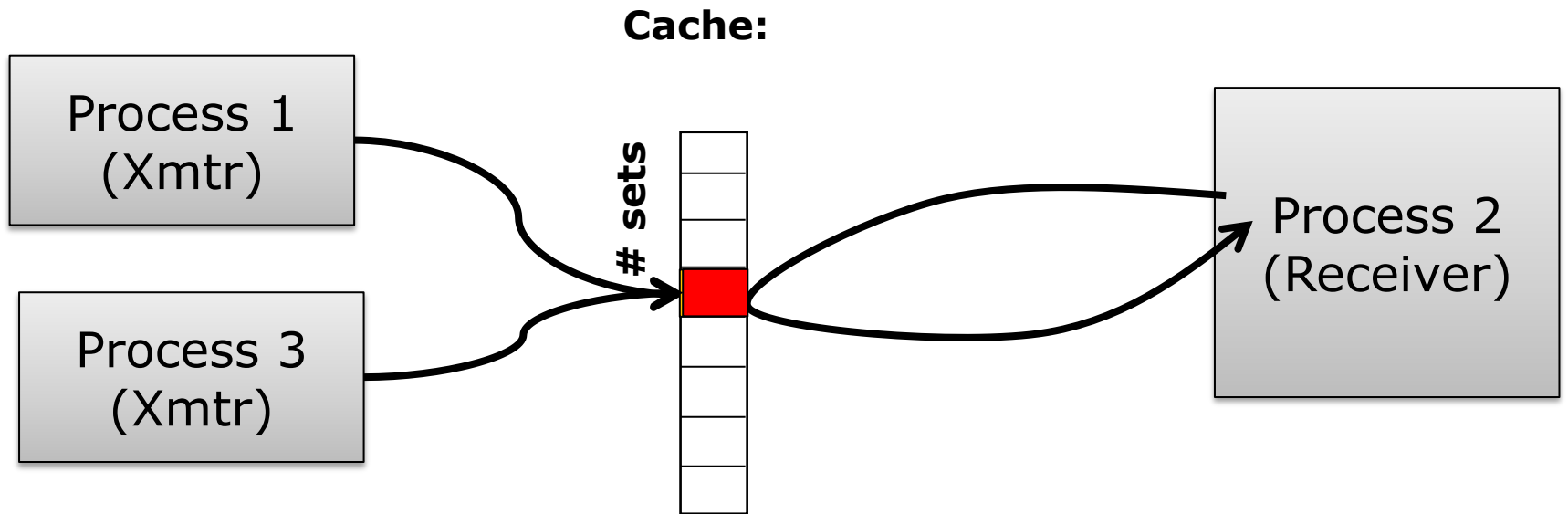
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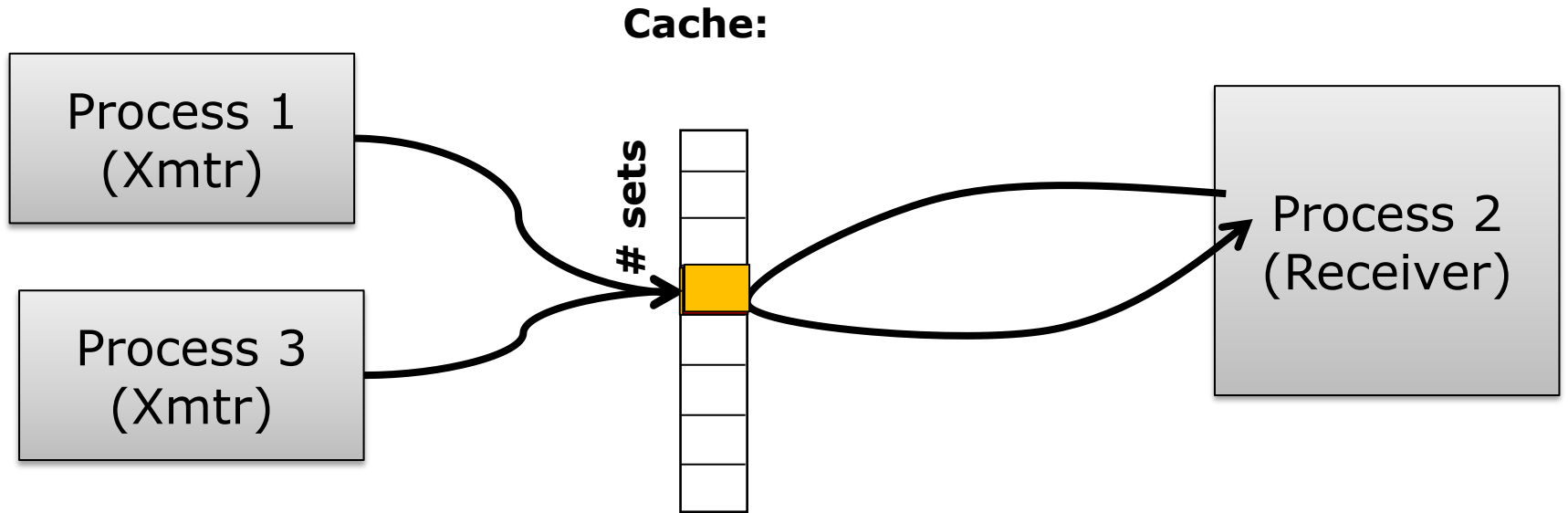


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t2 = rdtsc()
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Noise in the channel

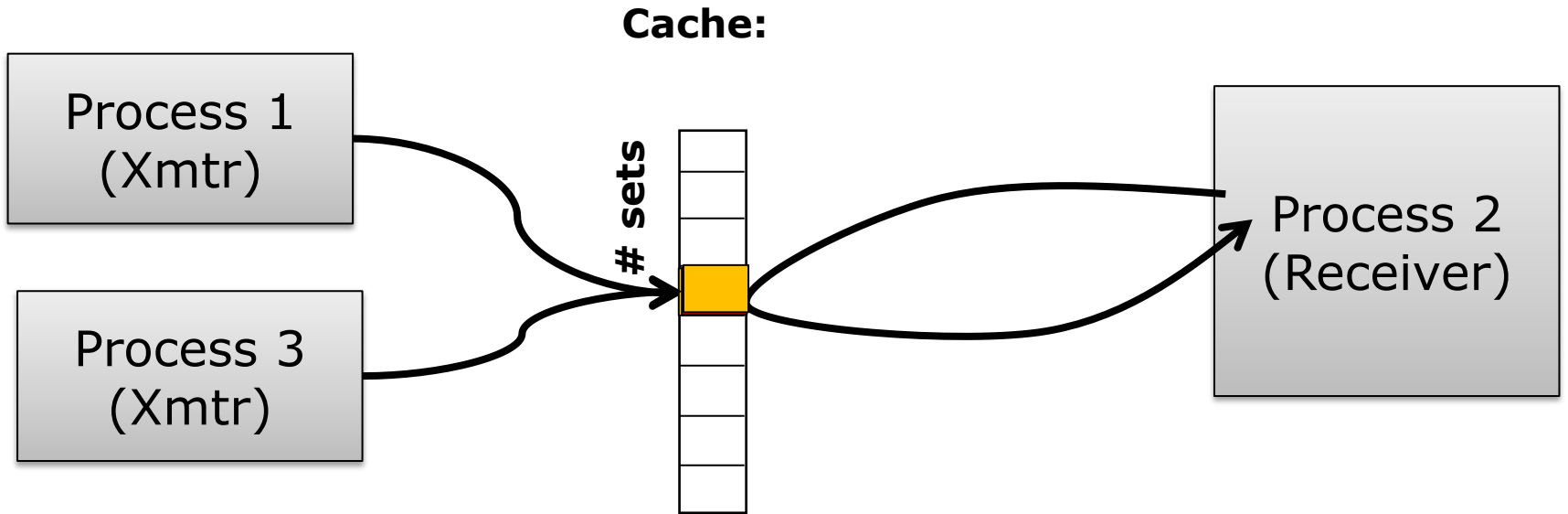


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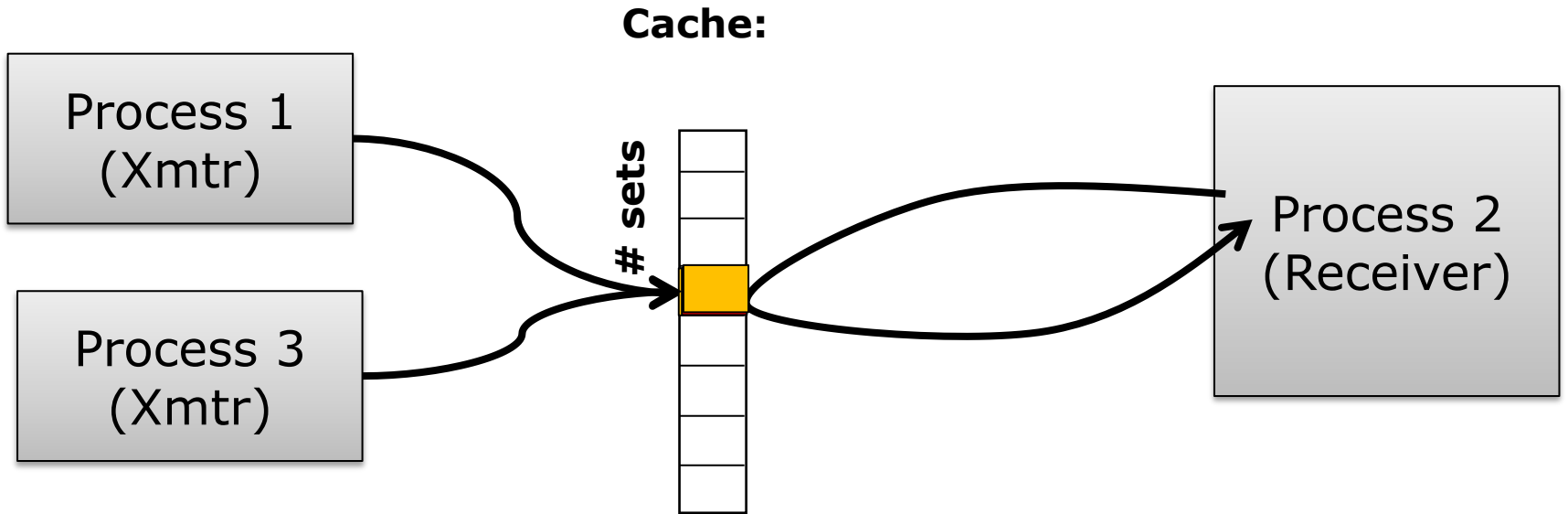
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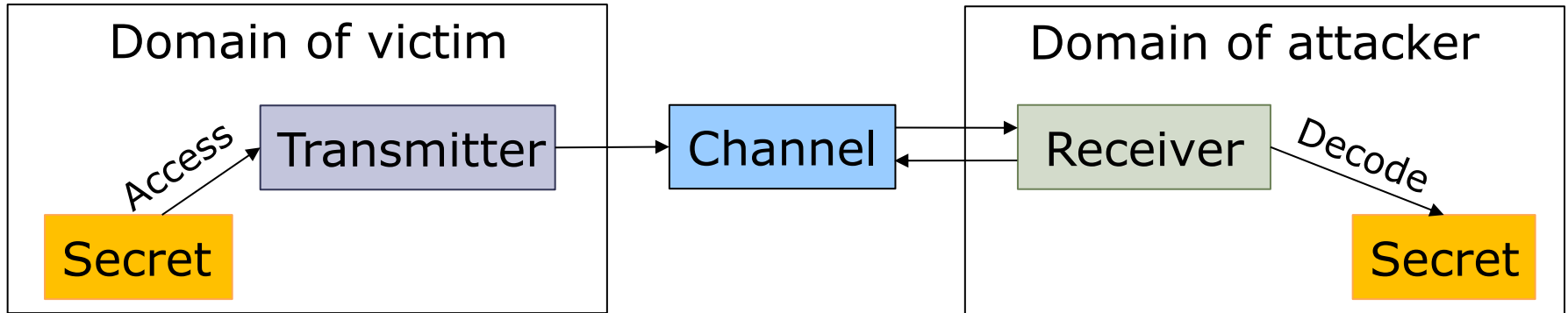
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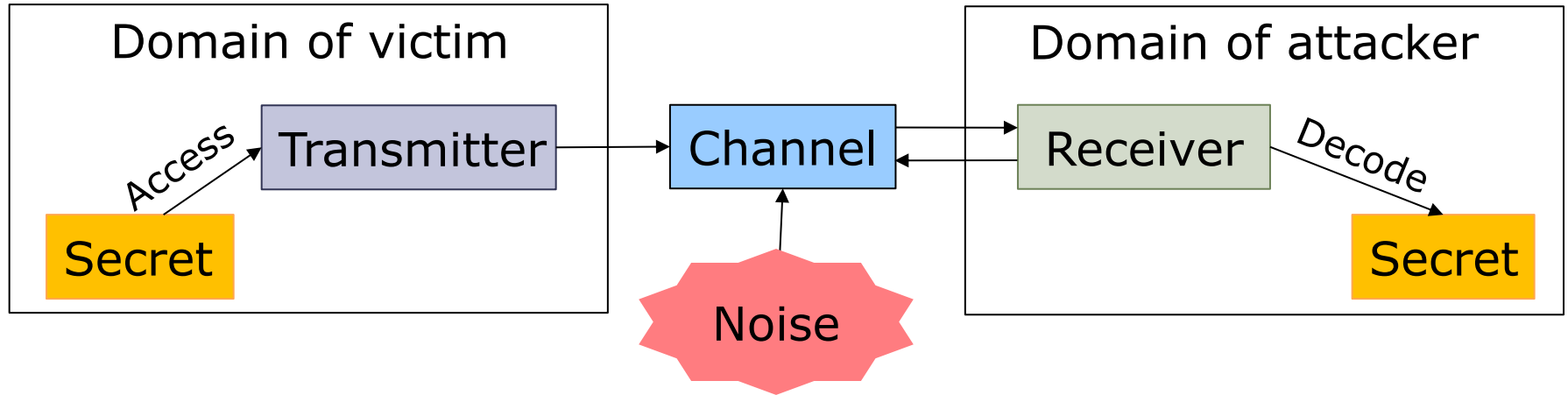
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Receiver interprets "noise" as a signal!

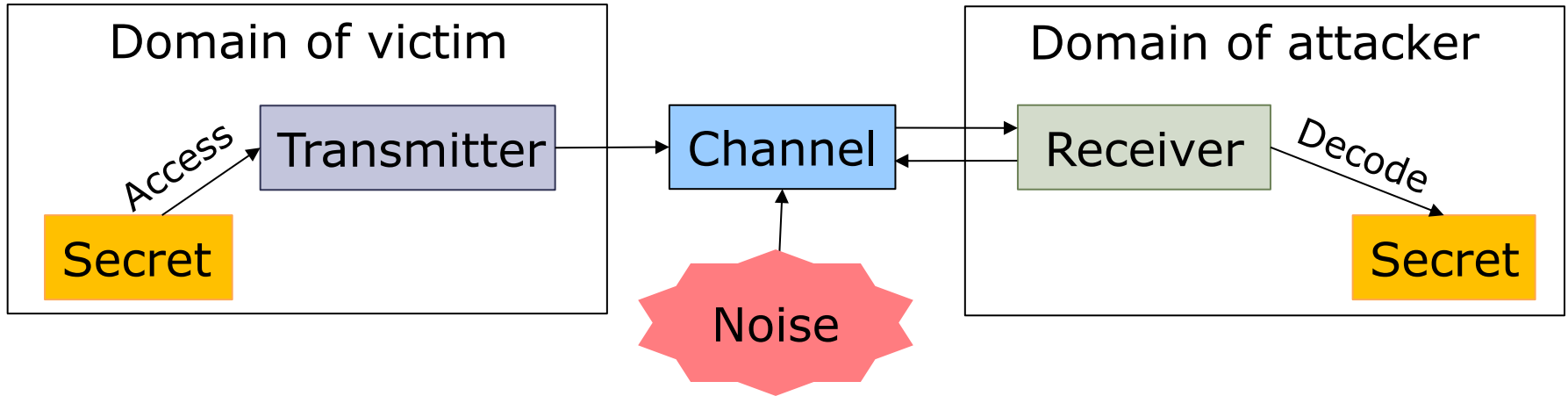
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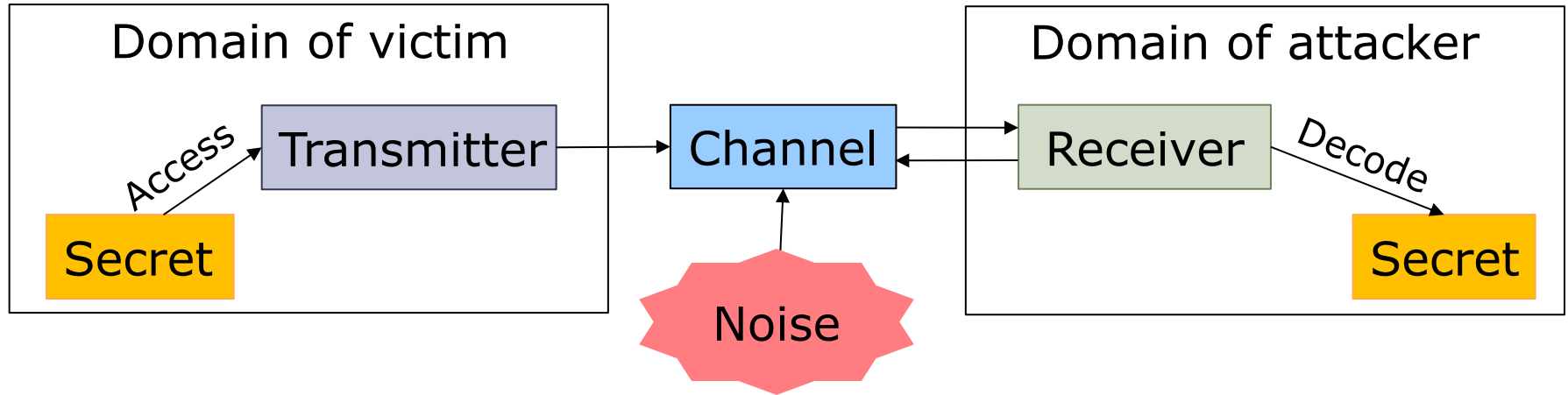


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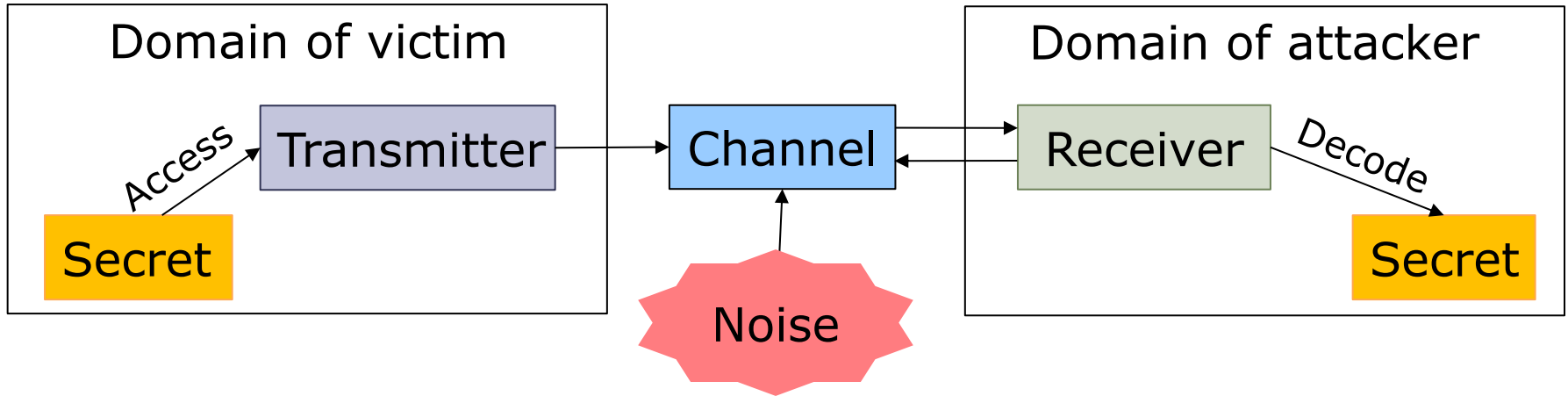
1. Another (or the same) transmitter may introduce changes of state (noise) into the channel which will confound the receiver

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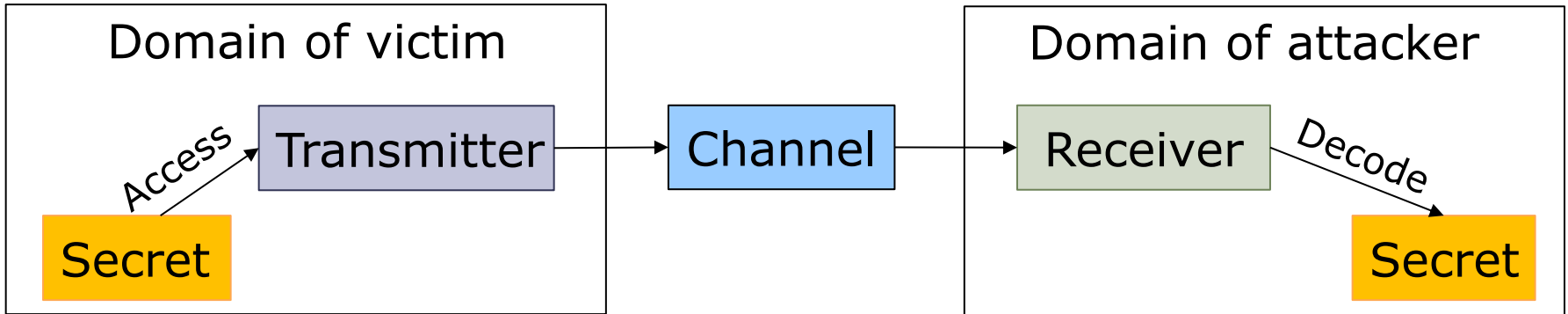
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2. Reception now becomes probabilistic, and a stochastic analysis is needed for the receiver to decode the modulation it sees in the channel.
3. Increases in reliability of reception can be improved by improved message encoding, e.g., by repeating the message.

Types of Transmitters



- Types of transmitter:
 1. Pre-existing so victim itself leaks secret, (e.g., RSA keys)

Another Transmitter

secret = ***oneof(0..3)***

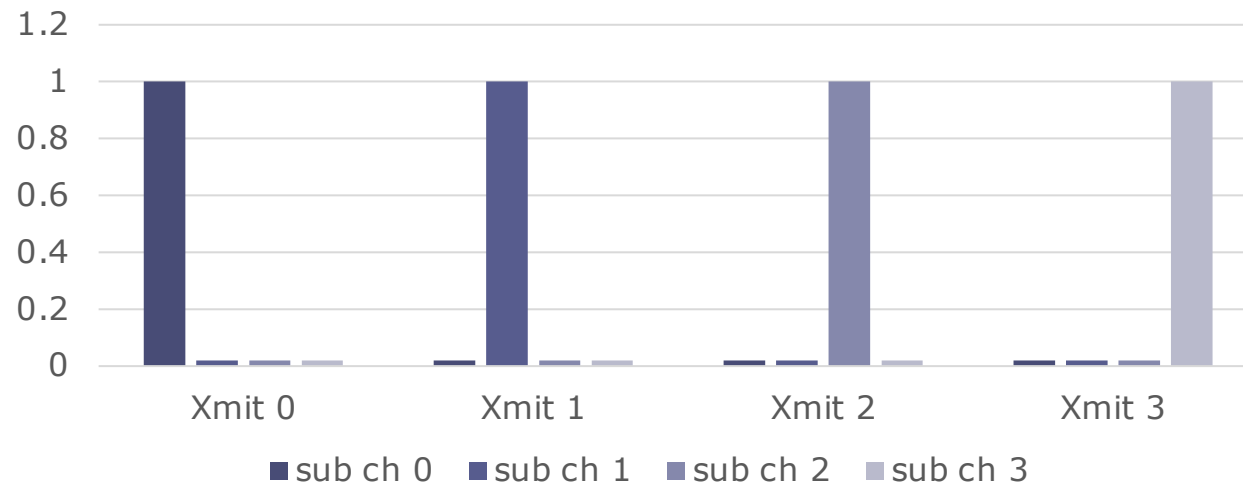
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Modulation for sending 0..3

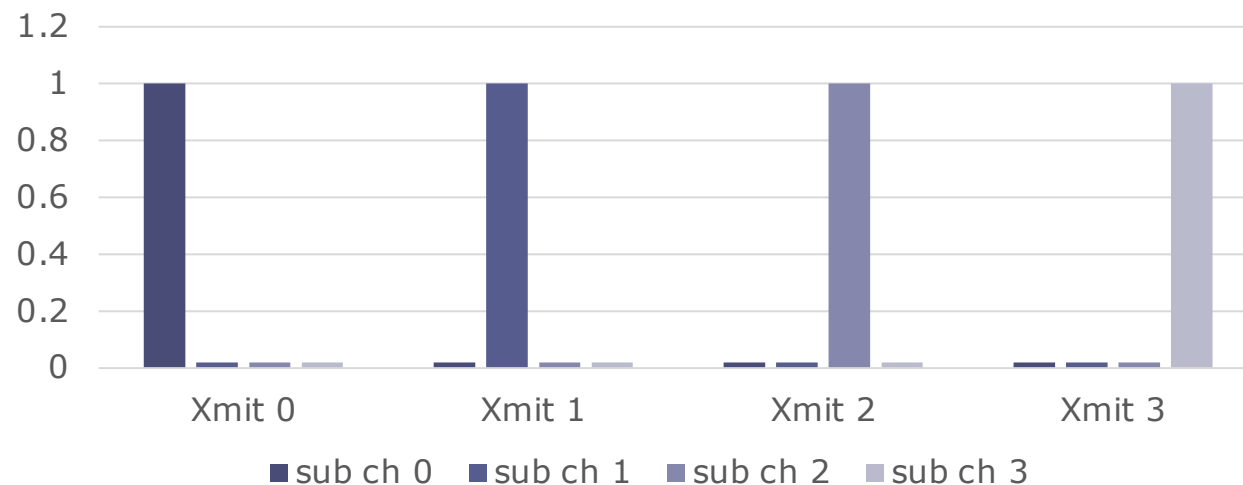


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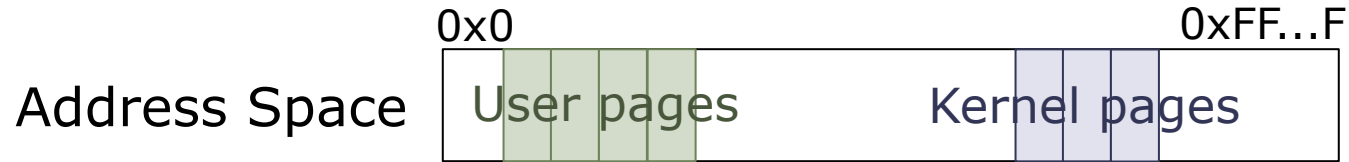
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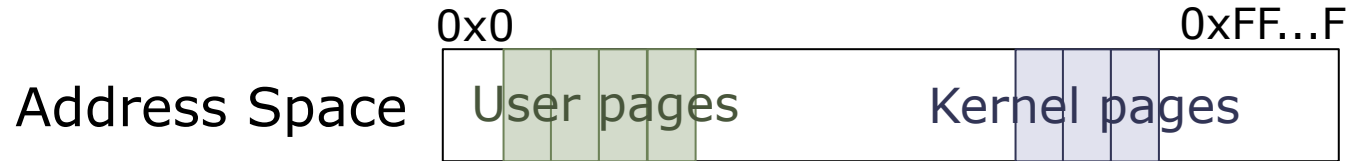


Like a frequency modulated (FM) radio transmission

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 - This avoids switching page tables on context switches, but
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- So what does the following code do when run in user mode do?

```
val = *kernel_address;
```
- Causes a protection fault, but data at "kernel_address" is speculatively read and loaded into val!

“FM” Transmitter - Meltdown

[Lipp et al. 2018]

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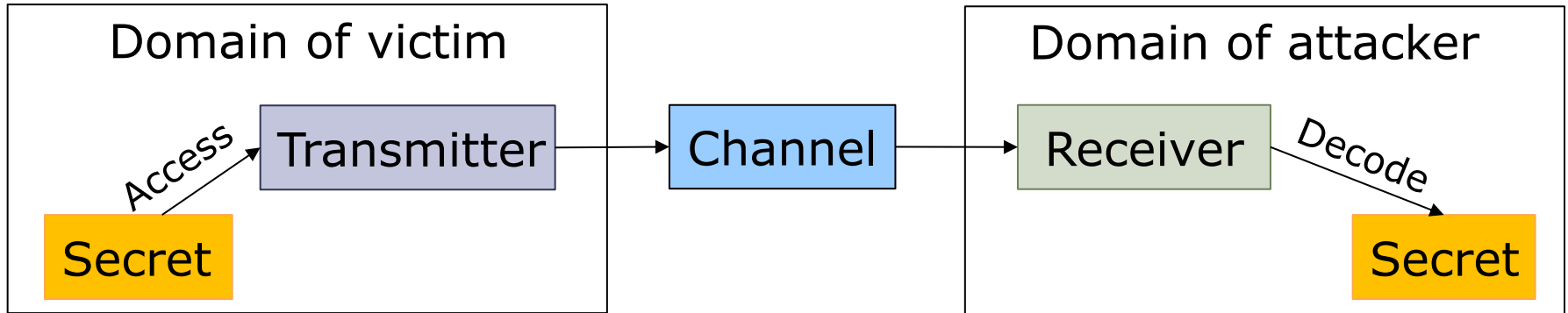
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- Result: Attacker can read arbitrary kernel data!
 - For higher performance, use transactional memory (protection fault aborts transaction on exception instead of invoking kernel)
 - Mitigation: Do not map kernel data in user page tables

Types of Transmitters



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 1. Pre-existing so victim itself leaks secret, (e.g., RSA keys)
 2. Programmed and invoked by attacker (e.g., Meltdown)

Spectre variant 2

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- Consider a situation where there is some kernel code that looks like the following:

```
xmit: uint8_t index = *kernel_address;  
       random_array[index] = 1;
```

- Interpret that code as an FM transmitter:

```
xmit: uint8_t secret = *kernel_address;  
       subchannels[secret] = 1;
```

- But that is kernel code that we cannot execute directly, so if only we could make the kernel jump to "xmit" we could invoke the transmitter...

Spectre variant 2

[Kocher et al. 2018]

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- Note since most BTBs store partial tags **and targets** it can be hard to get the BTB to jump to an arbitrary address, so Spectre uses the indirect jump predictor.

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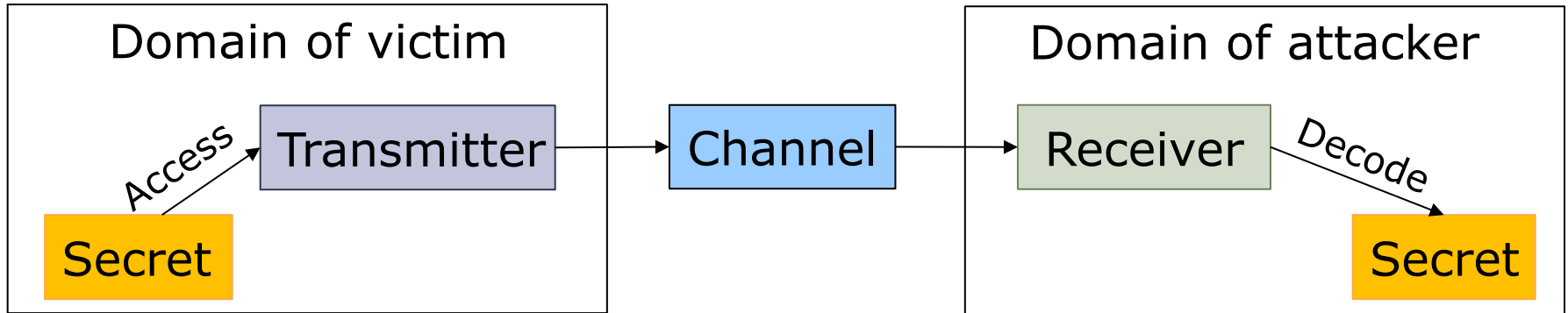
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- Now assume there is another bit of code in that kernel routine that we can force to be executed looks like:

```
abc: br xyz
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Types of Transmitters



- Types of transmitter:

1. Pre-existing so victim itself leaks secret, (e.g., RSA keys)
2. Programmed and invoked by attacker (e.g., Meltdown)
3. Synthesized from existing victim code and invoked by attacker (e.g., Spectre V2)

Spectre variant 1

[Kocher et al. 2018]

- Consider the following kernel code, e.g., in a system call

```
if (x < array1_size)
    y = array2[array1[x] * 4096];
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3. Receive: Attacker probes cache to infer which line of $array2$ was fetched, learns data at kernel address
 - $array2$ may or may not be accessible to attacker (can use prime+probe)

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- Long-term mitigations:
 - Disabling speculation?
 - Closing side channels?

Coming Spring 2022...

Learn to attack processors...

Side channel attacks

Transient/ speculative execution attacks

Row-hammer attacks

SGX Enclave Design

Hardware support for memory safety

And more!

And learn to defend them!

Take 6.888 This Spring!



Mengjia Yan
mengjia@csail.mit.edu

Graduate-Level/ AUS

12 Units (3-0-9)

MW 1:00 - 2:30

Thank you!