Hardwired, Non-pipelined ISA Implementation

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M.I.T.

Administrivia

- TA: Ryan Lee
- Contact: 6823-tas@lists.csail.mit.edu
  or hrlee@csail.mit.edu
- Please use Piazza extensively for questions!
- Office Hours: Wed. 4-5:30pm, 32-G725 or by appointment
- Tutorials every week (optional)
  - First two will cover background materials
  - Cover lab tools (Intel Pin, Murphi)
  - Go over problem sets, quiz prep
  - Two sessions will be reserved for Quizzes. Do not miss them!

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- Today: single-cycle implementation of a processor

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rest of this lecture →

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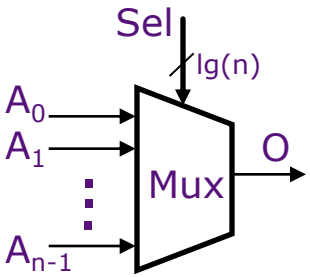

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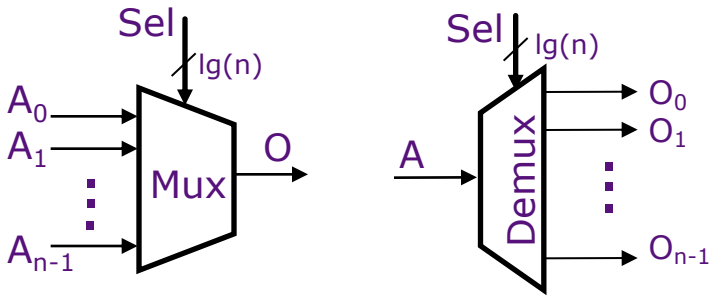

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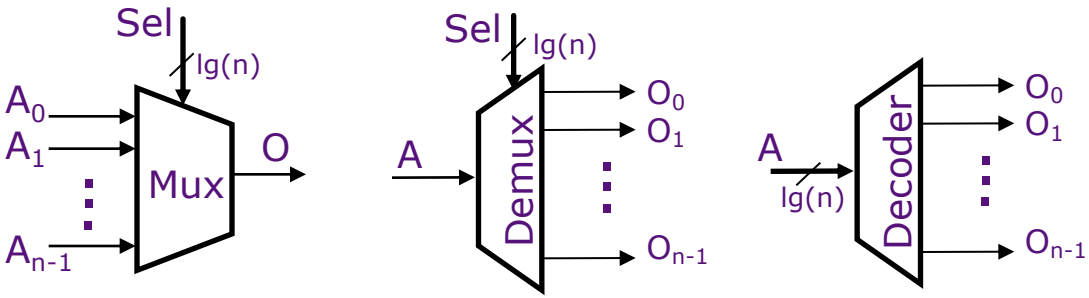

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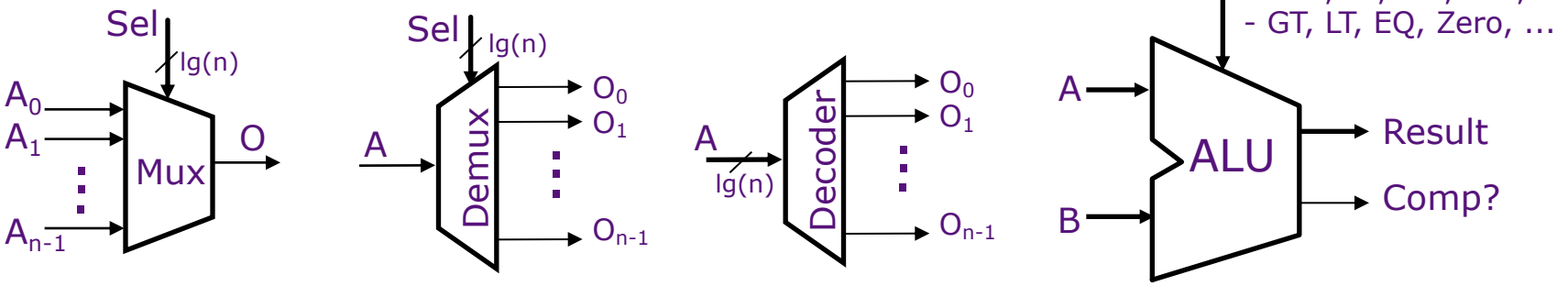

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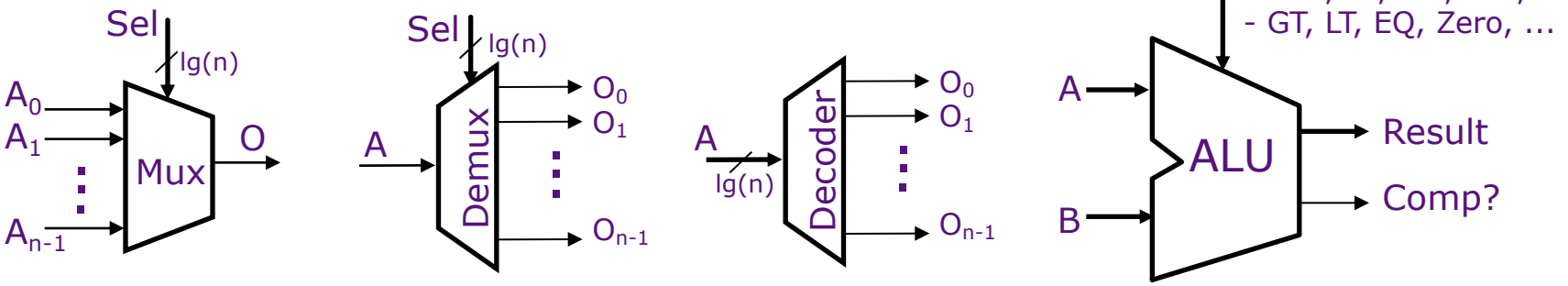

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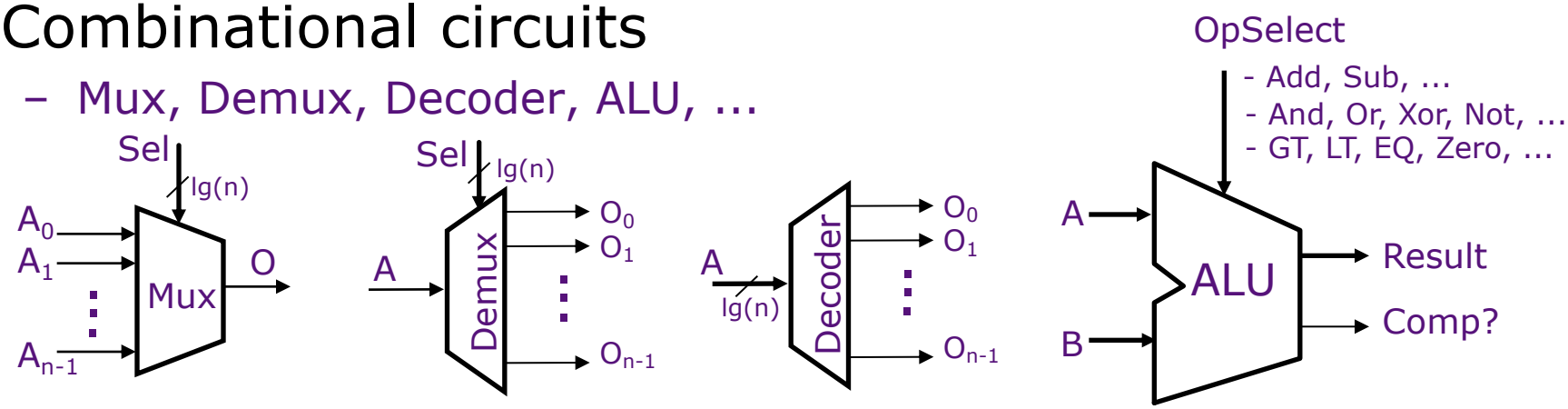

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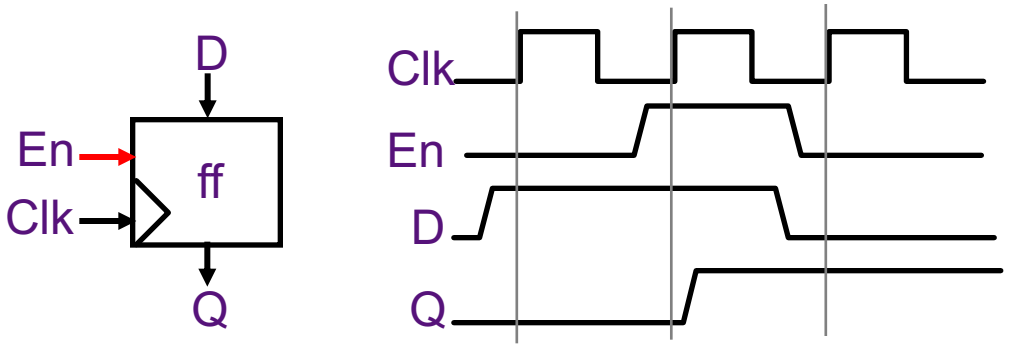

Edge-triggered: Data is sampled at the rising edge

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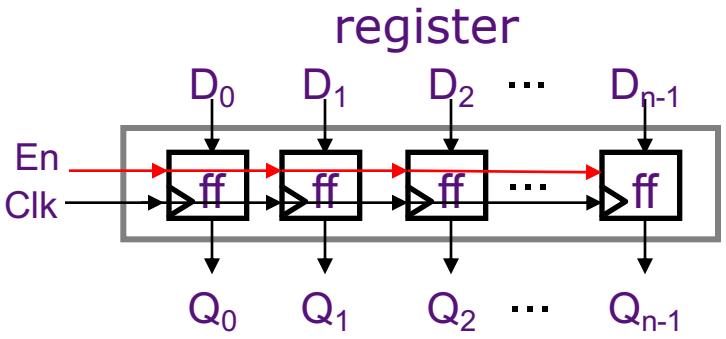

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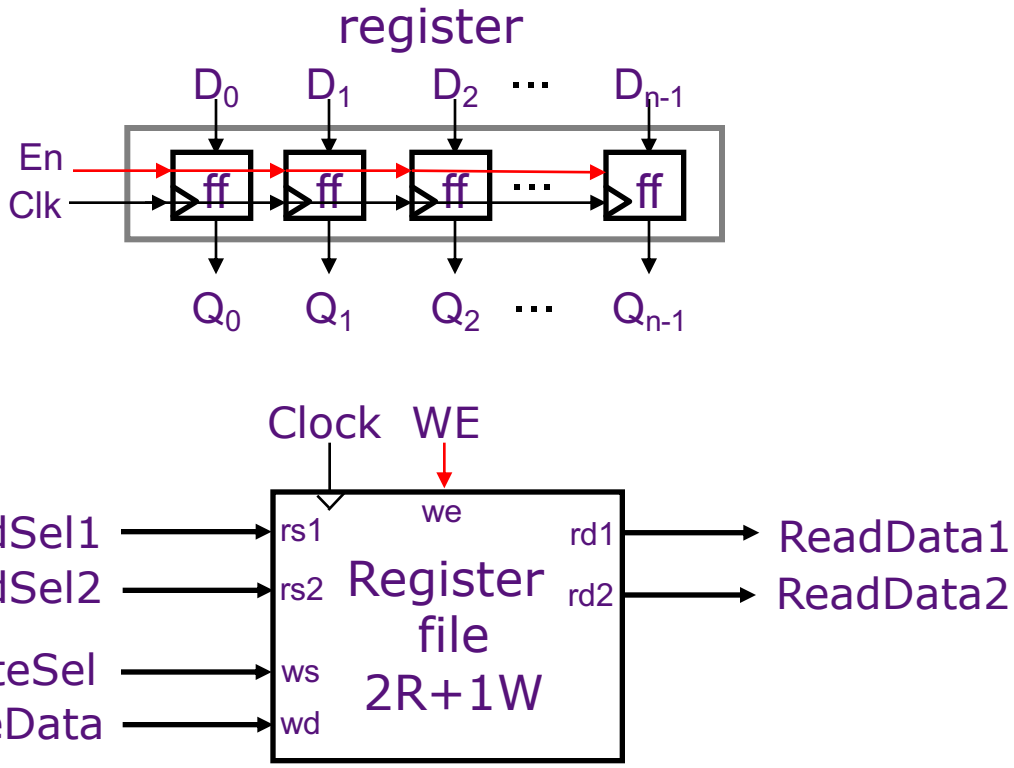

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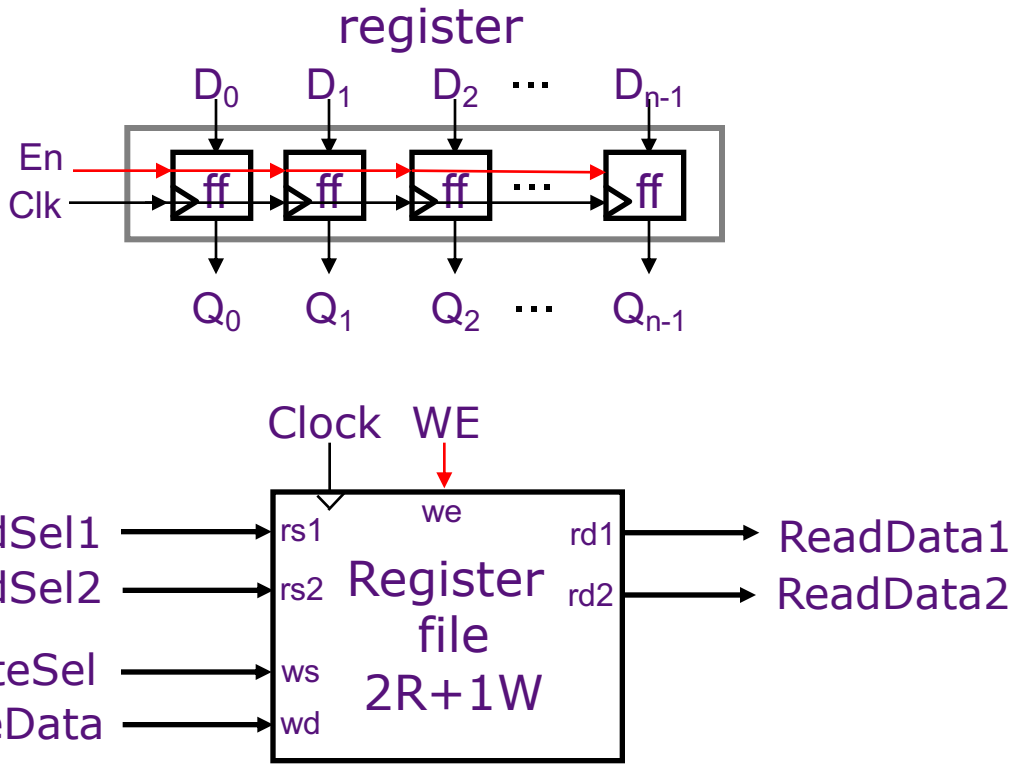
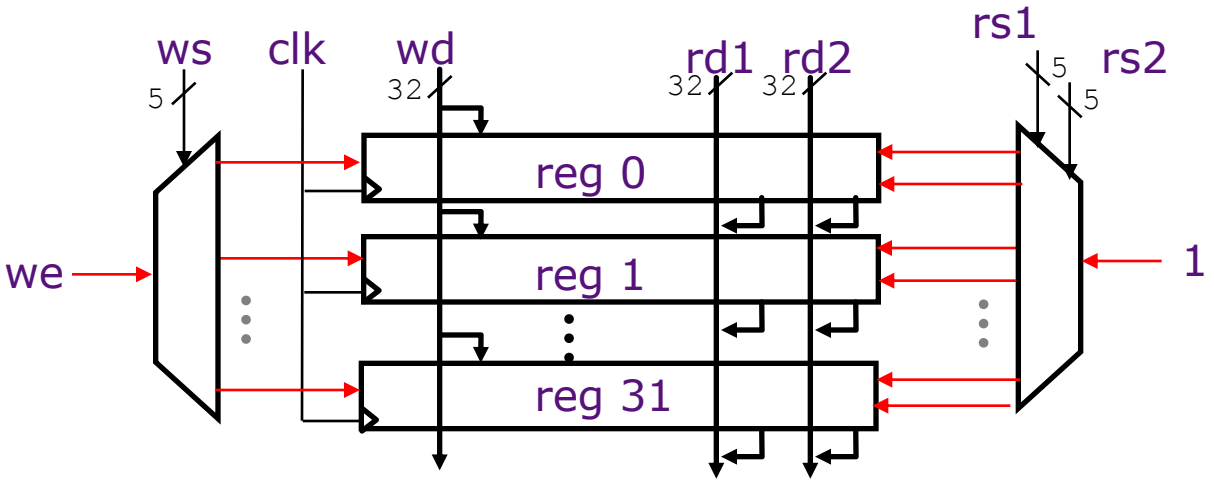


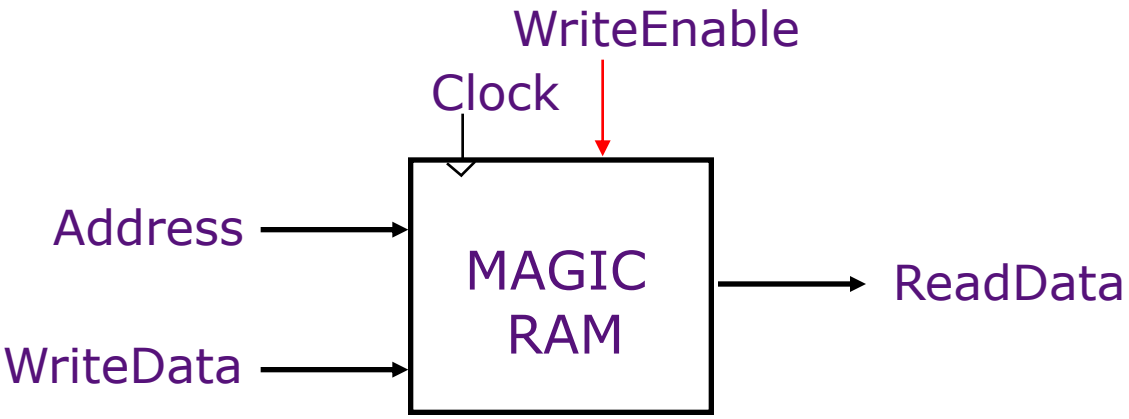
No timing issues when reading and writing the same register (writes happen at the end of the cycle)

Register File Implementation



- Register files with a large number of ports are difficult to design
  - Area scales with ports^2
  - Almost all Alpha instructions have exactly 2 register source operands
  - *Intel's Itanium GPR File has 128 registers with 8 read ports and 4 write ports!!*

A Simple Memory Model



- Reads and writes are always completed in one cycle
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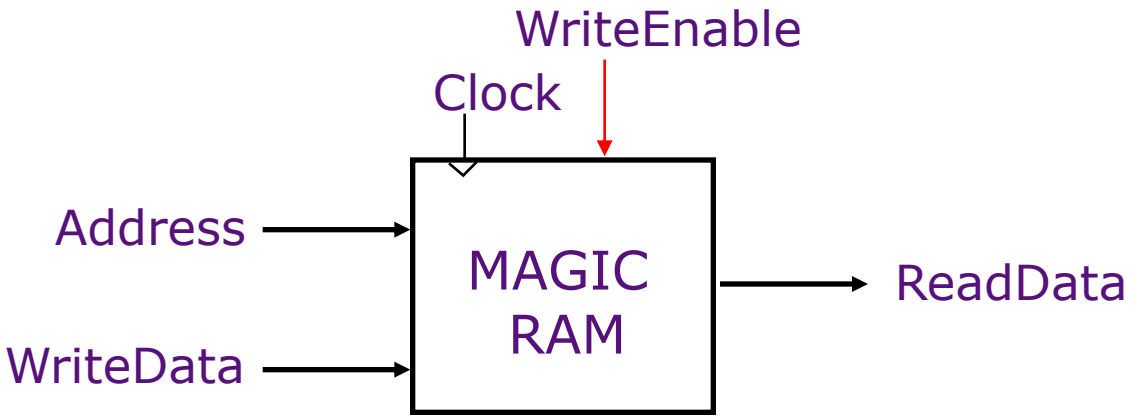

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Later in the course we will present a more realistic model of memory

Implementing MIPS:

Single-cycle per instruction datapath & control logic

The MIPS ISA

Processor State

- 32 32-bit GPRs, R0 always contains a 0
- 32 single precision FPRs, may also be viewed as
  16 double precision FPRs
- FP status register, used for FP compares & exceptions
- PC, the program counter
- Some other special registers

Data types

- 8-bit byte, 16-bit half word
- 32-bit word for integers
- 32-bit word for single precision floating point
- 64-bit word for double precision floating point

Load/Store style instruction set

- Data addressing modes: immediate & indexed
- Branch addressing modes: PC relative & register indirect
- Byte-addressable memory, big-endian mode

All instructions are 32 bits

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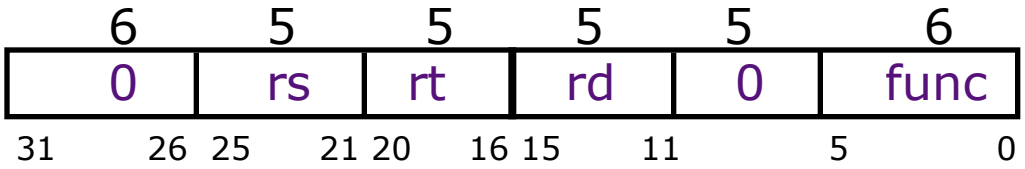
And computing the address of the
next instruction (next PC)

Datapath: Reg-Reg ALU Instructions



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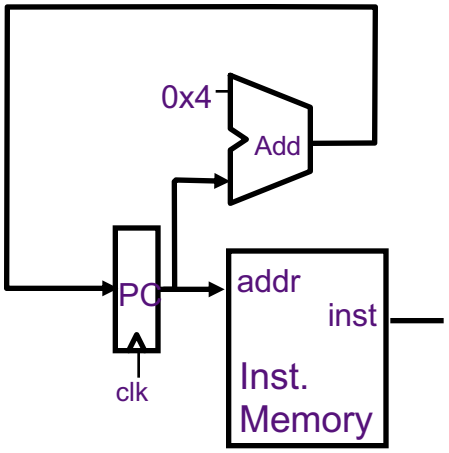

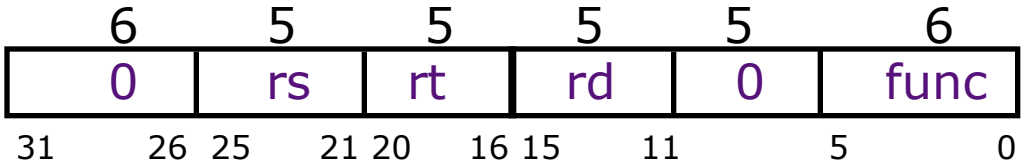

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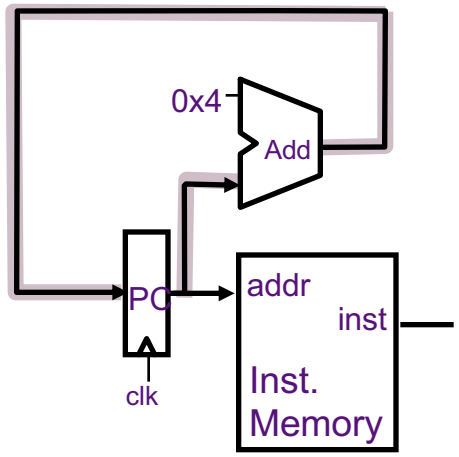

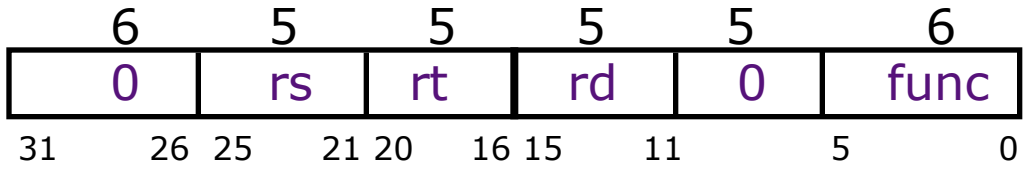

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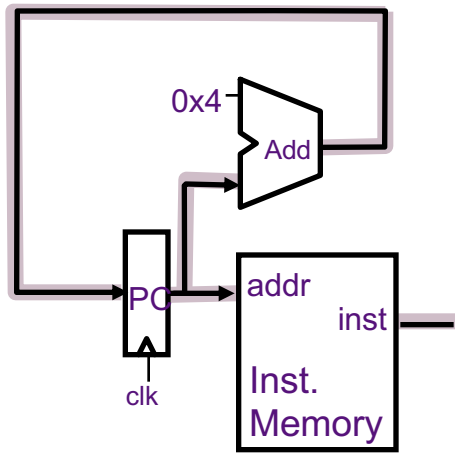

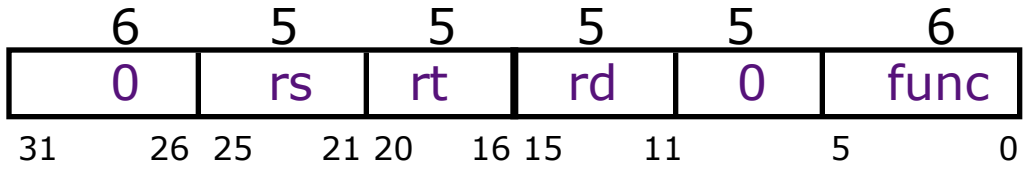

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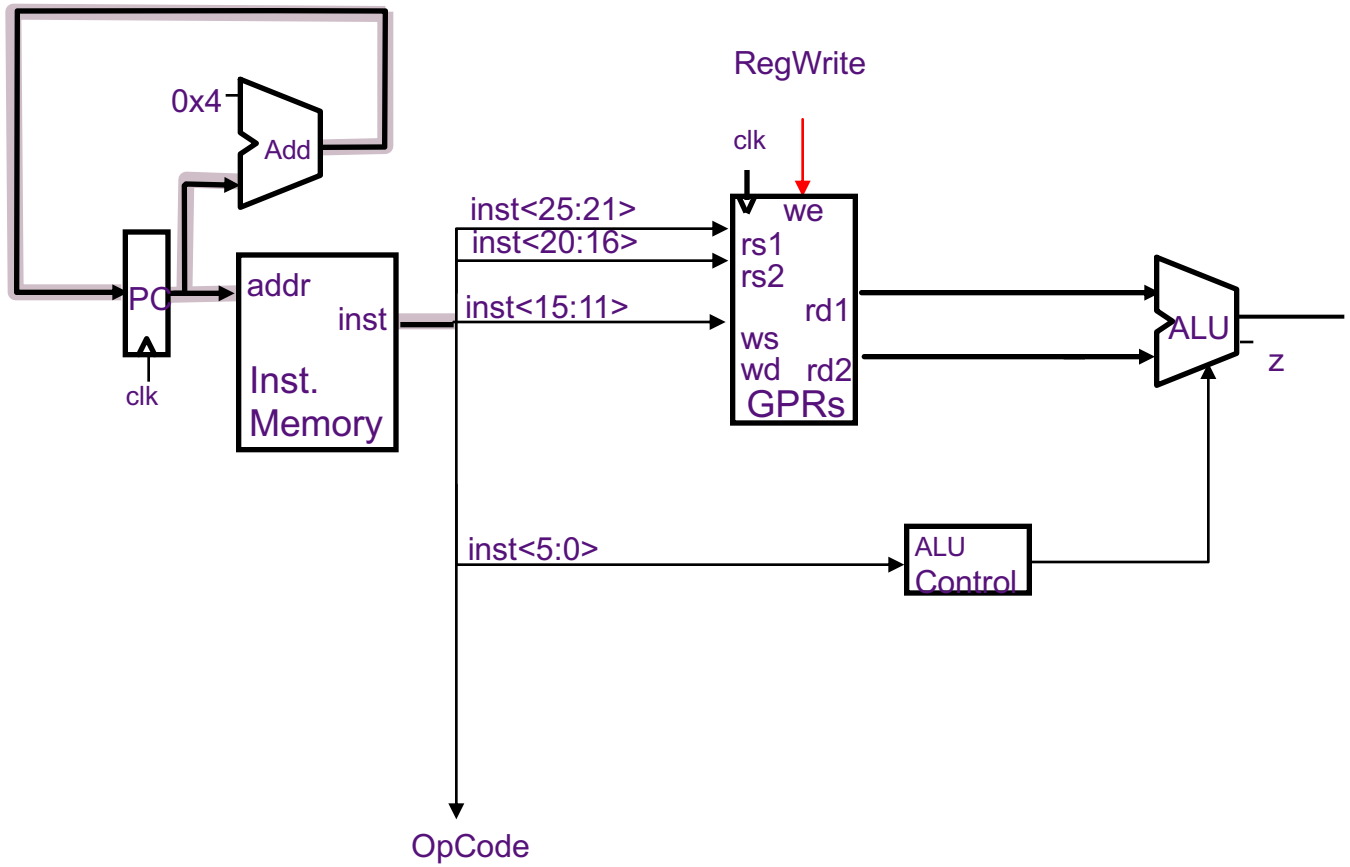

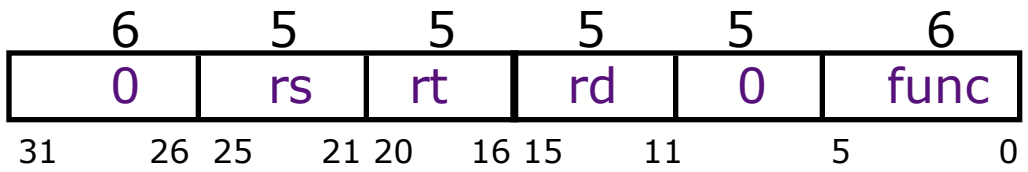

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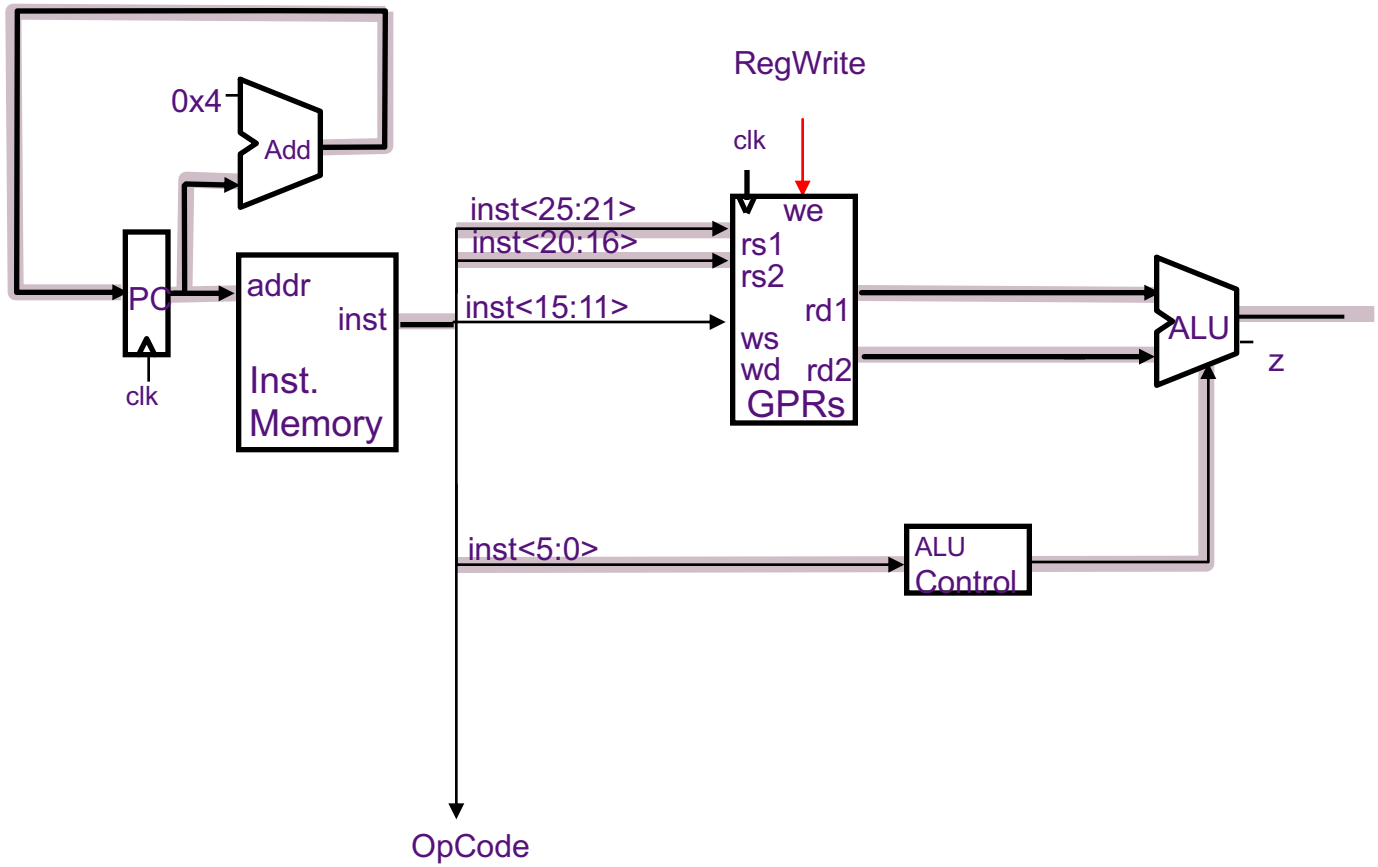

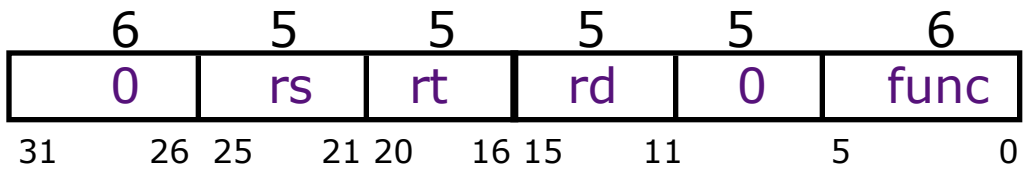

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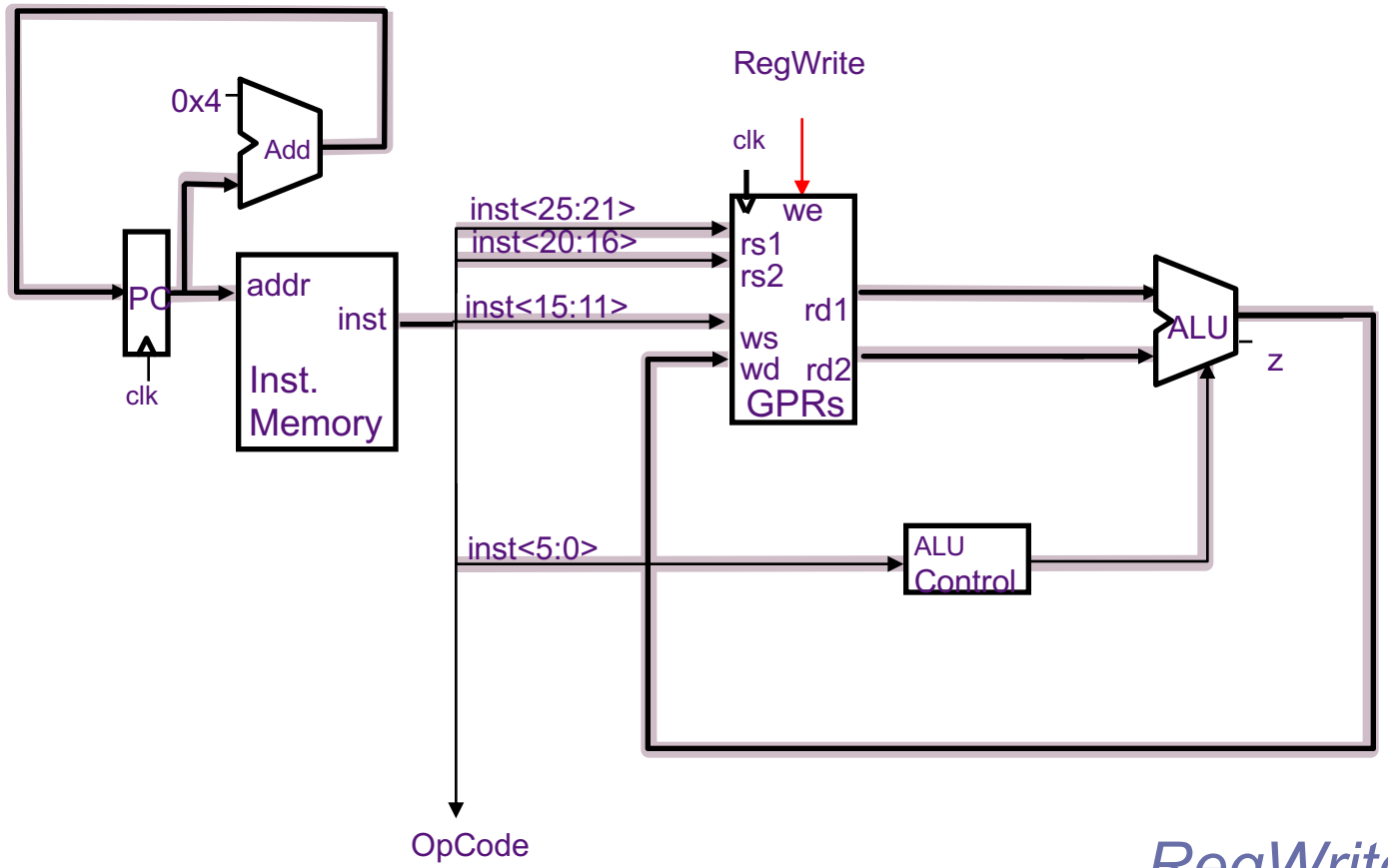

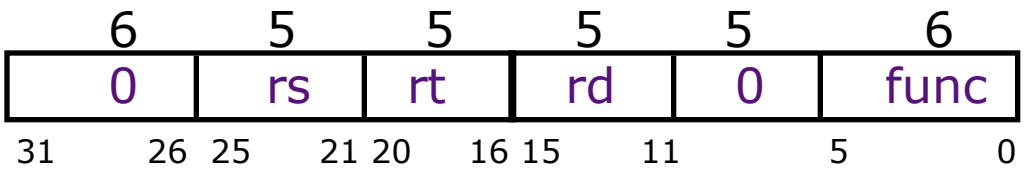

RegWrite Timing?

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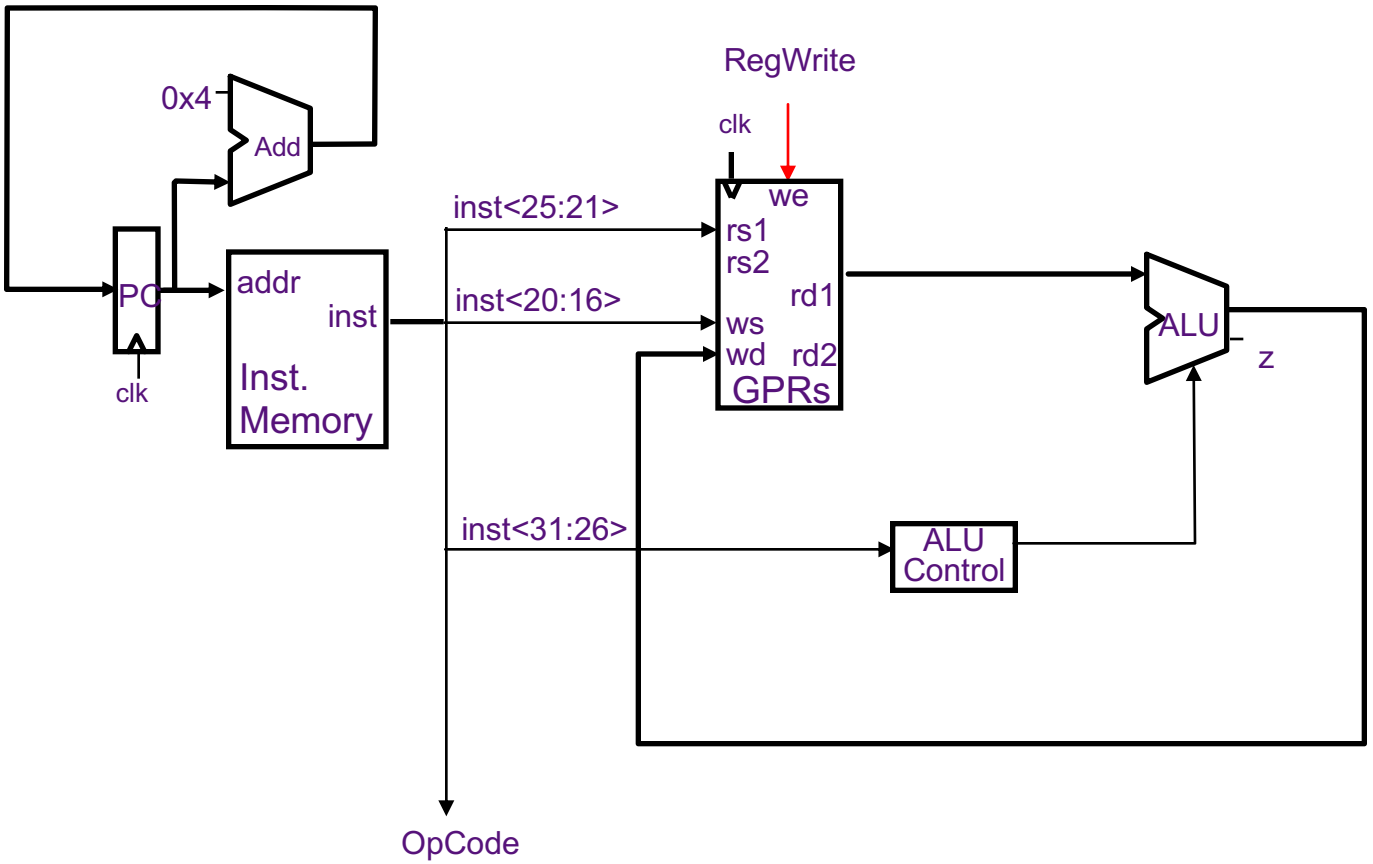

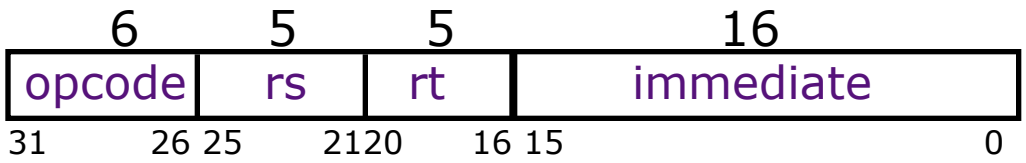

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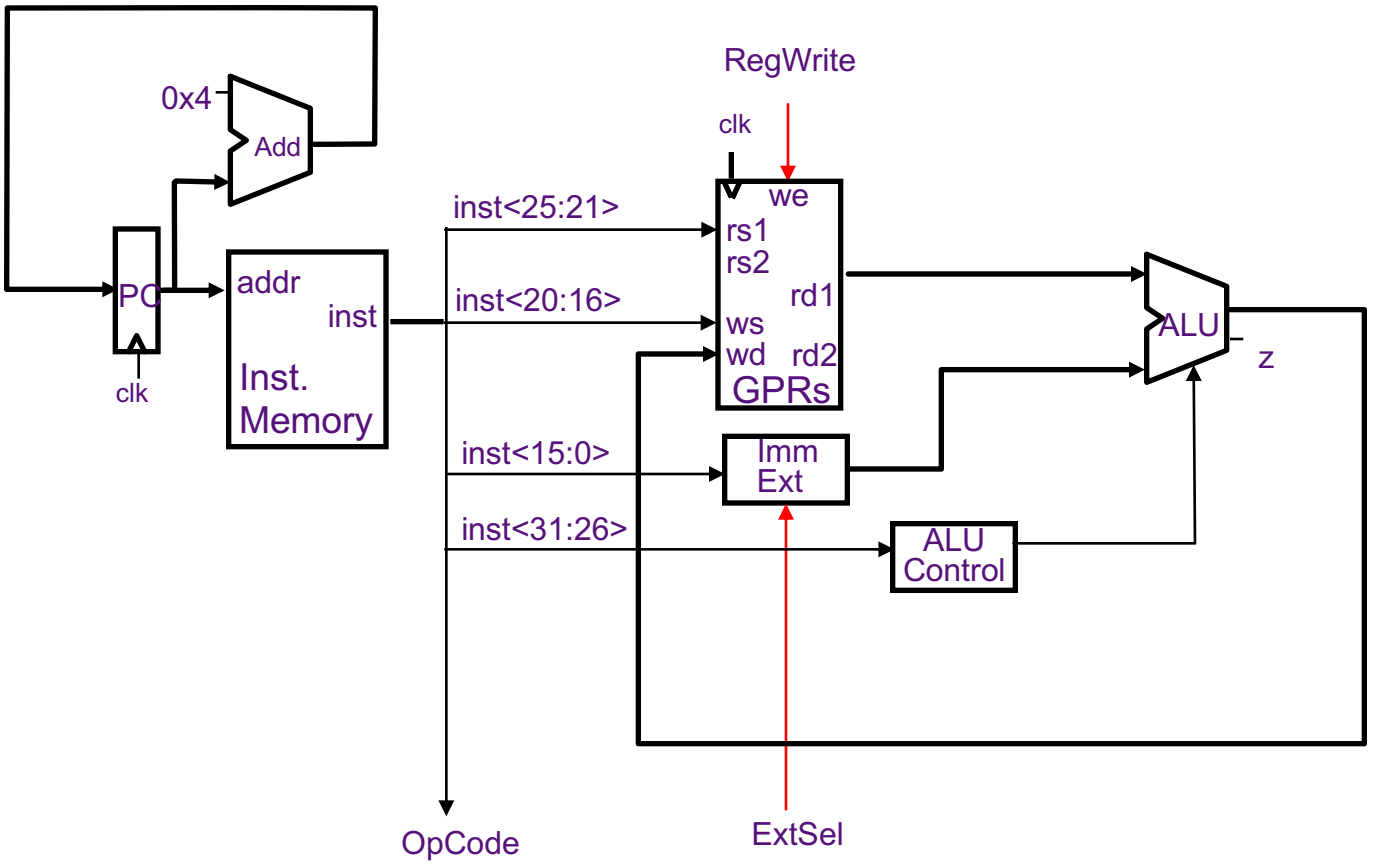

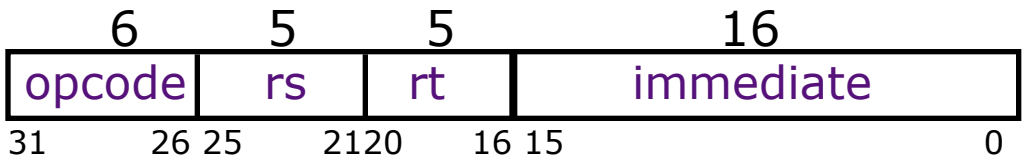

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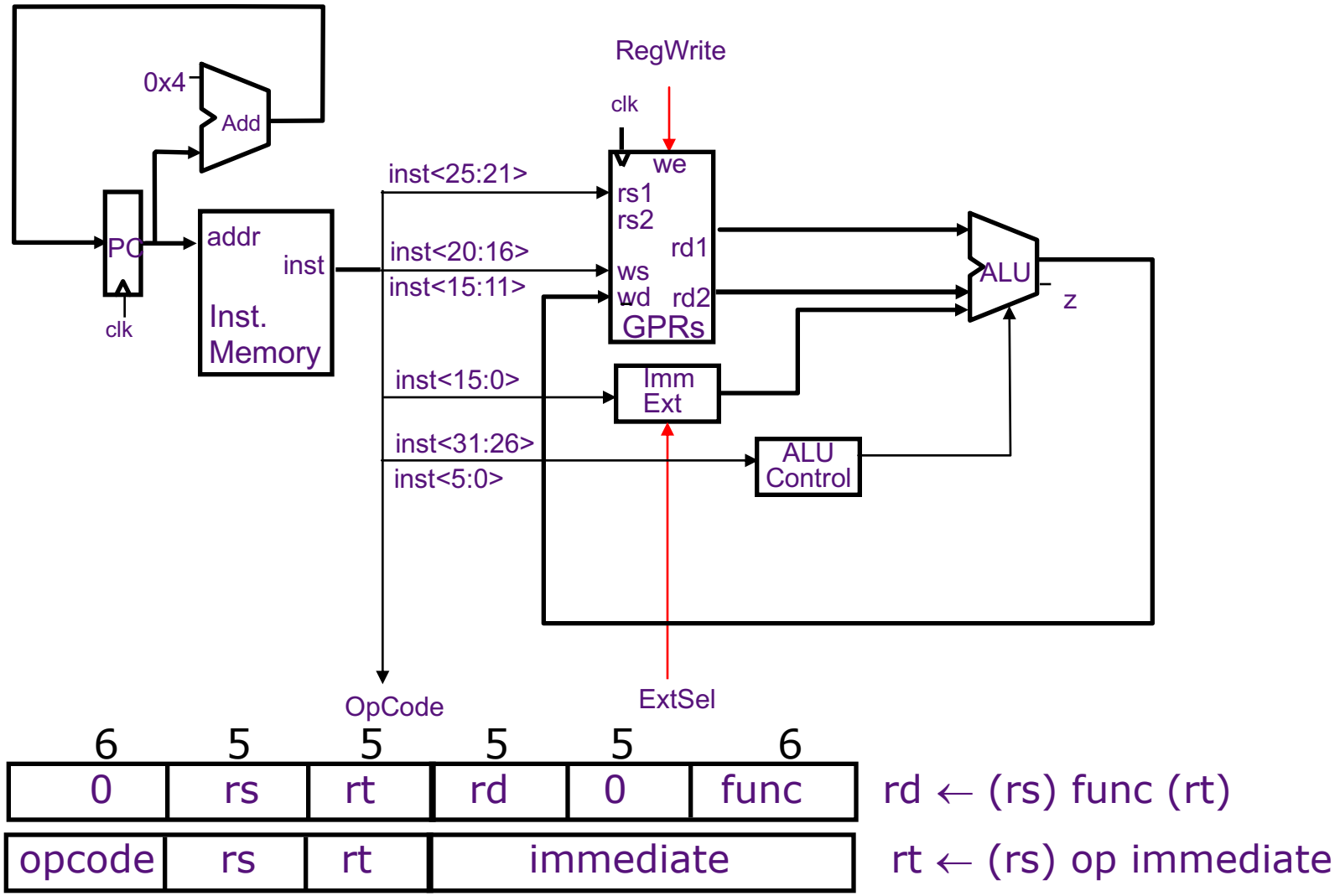

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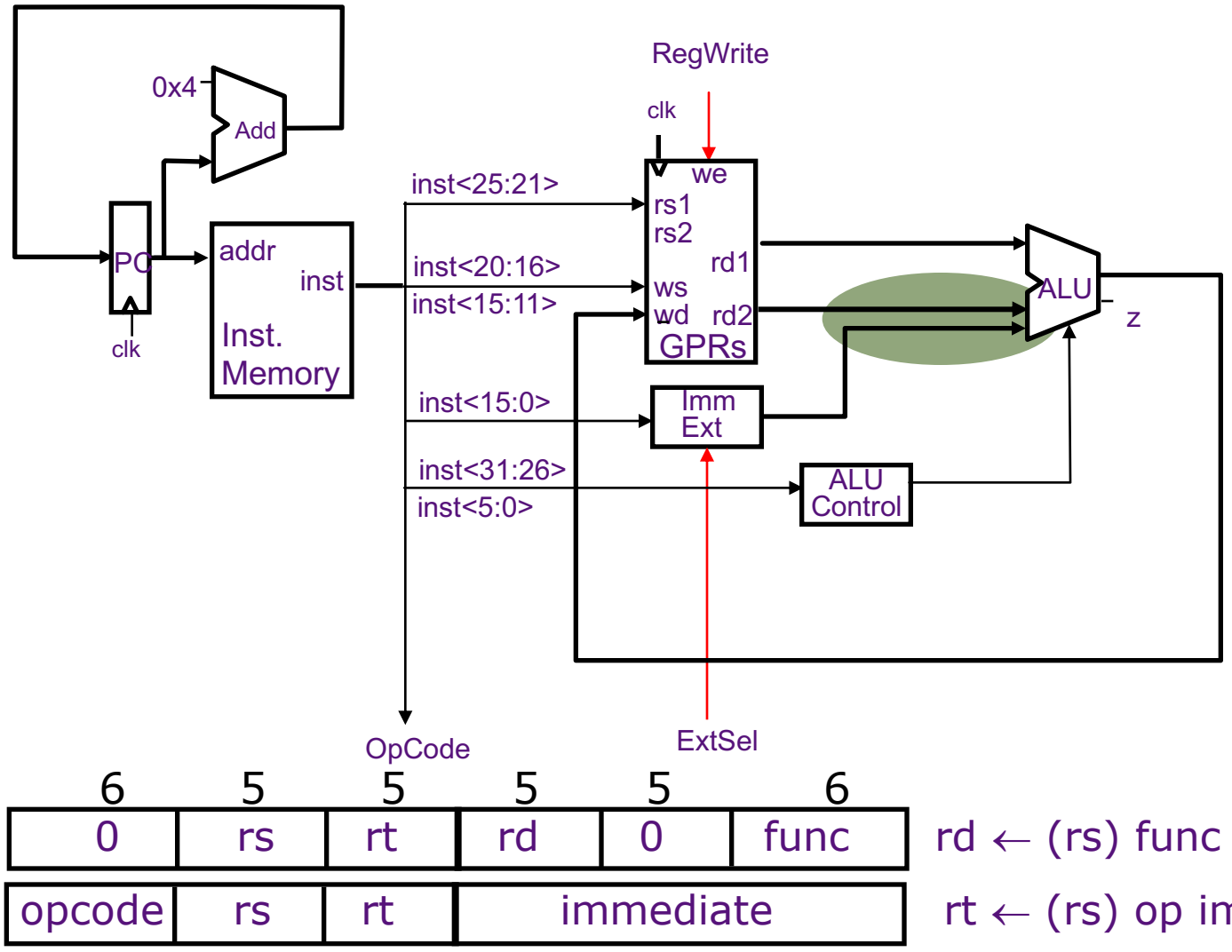

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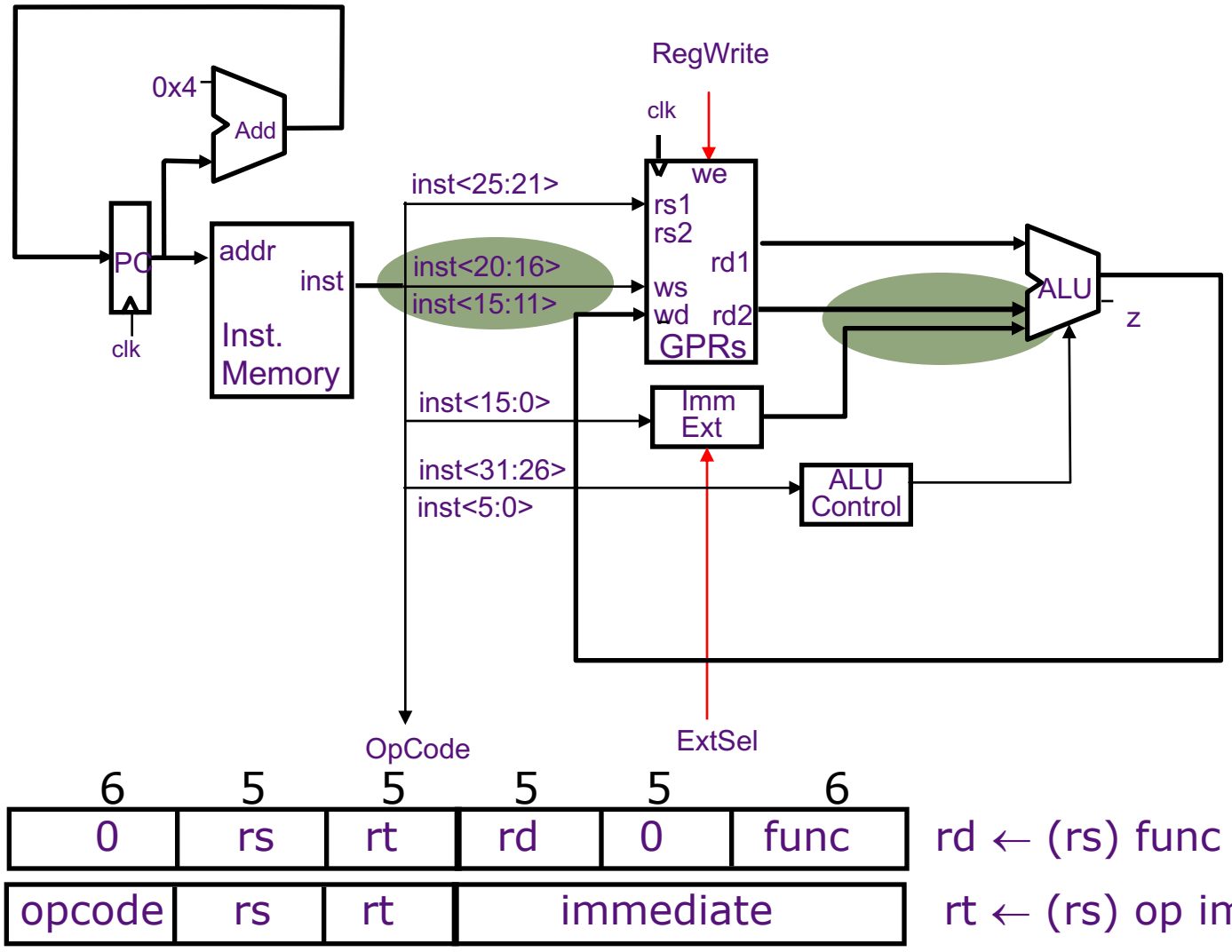

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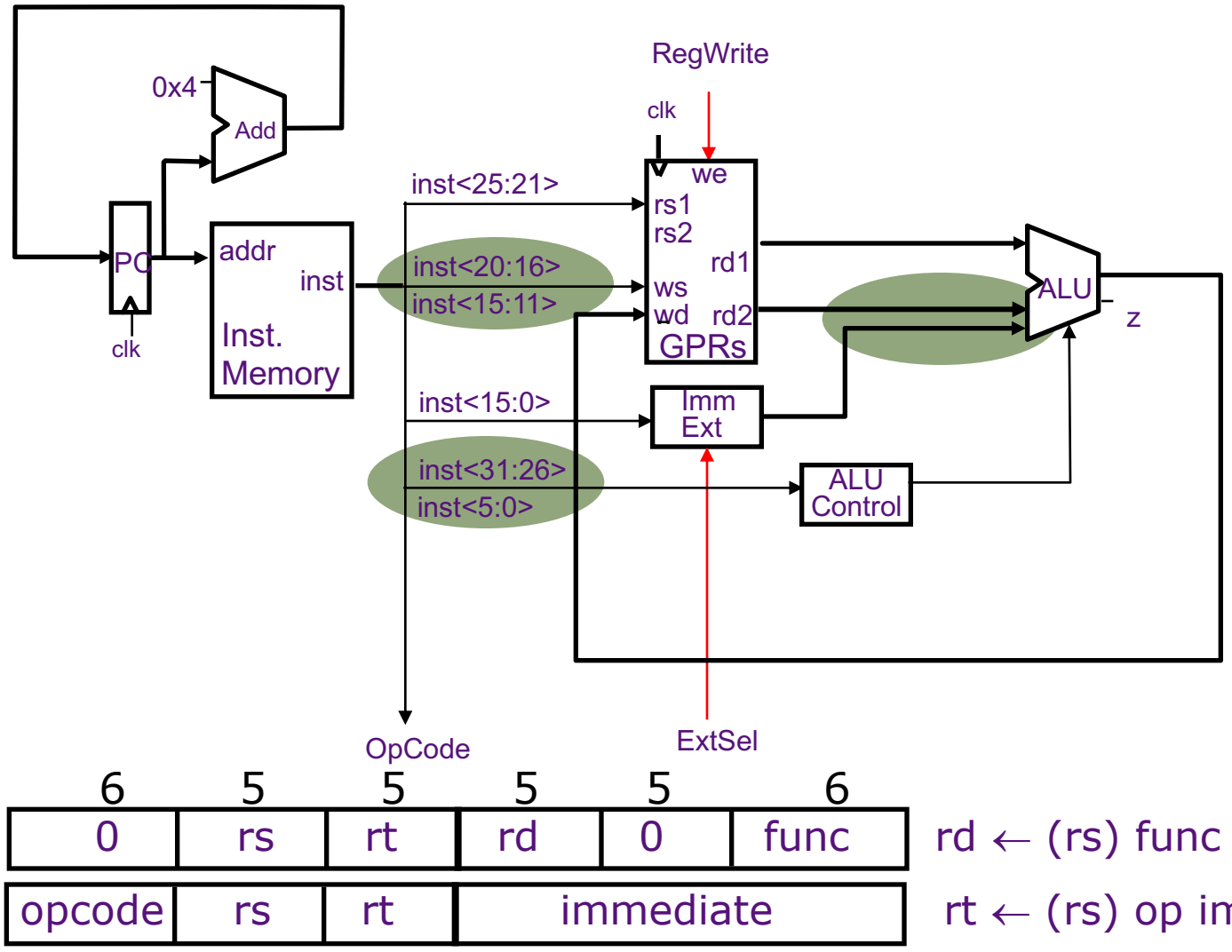

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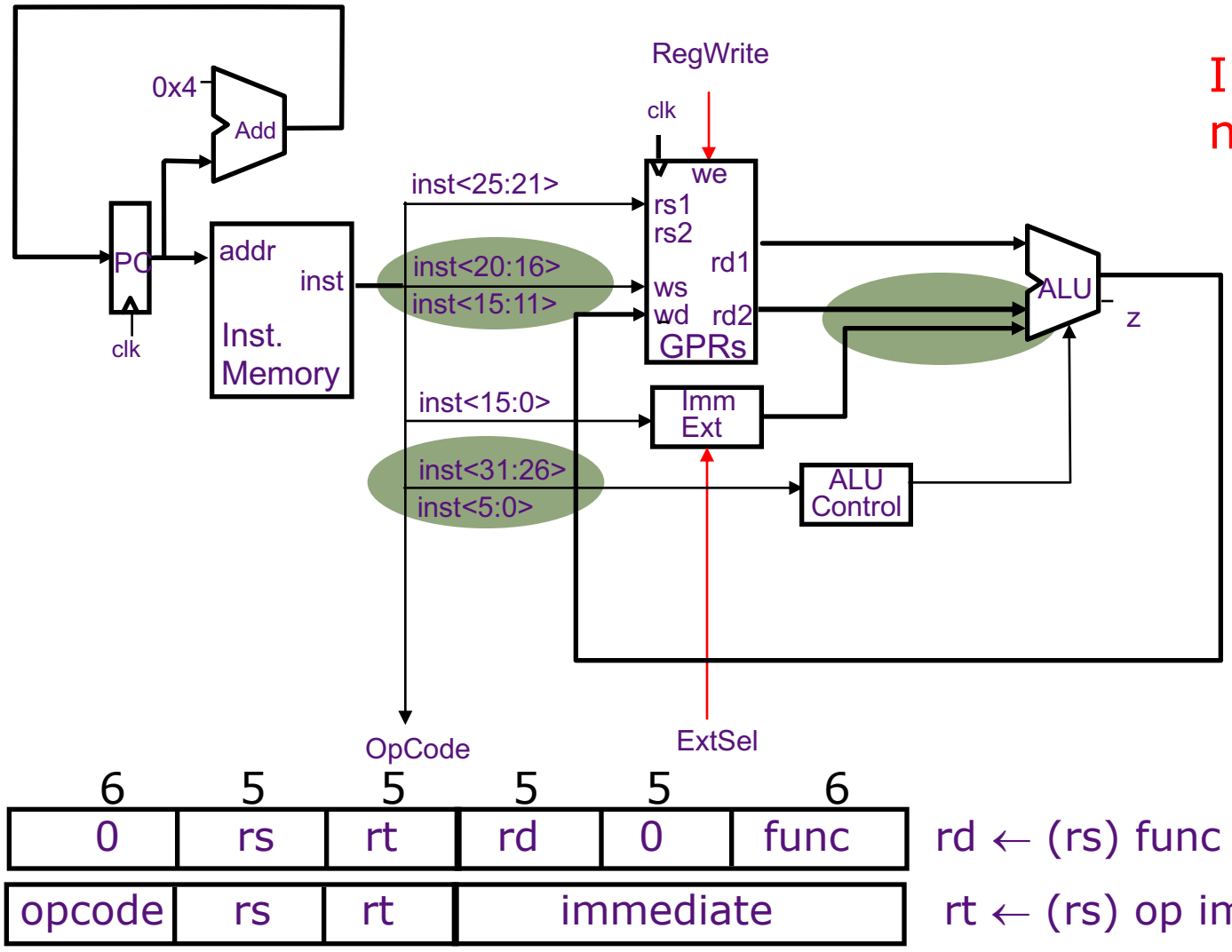

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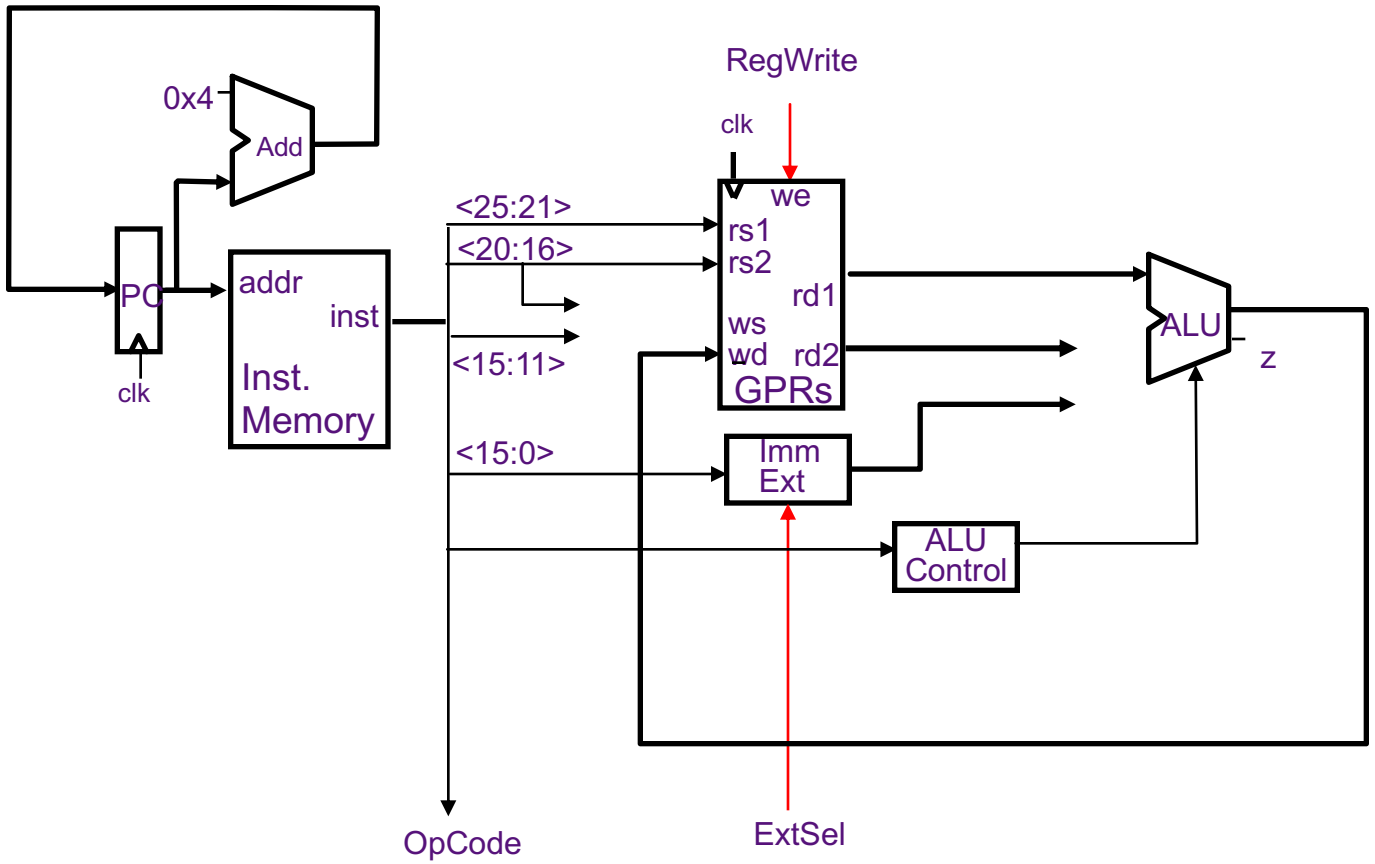

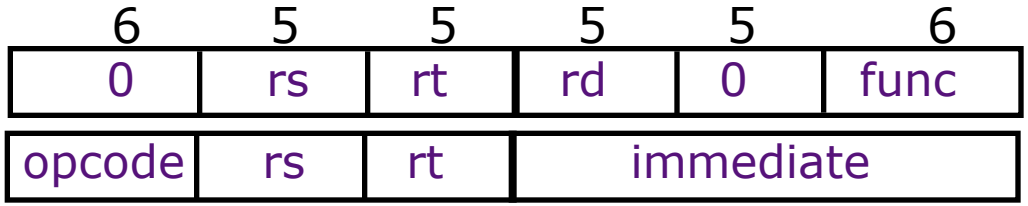

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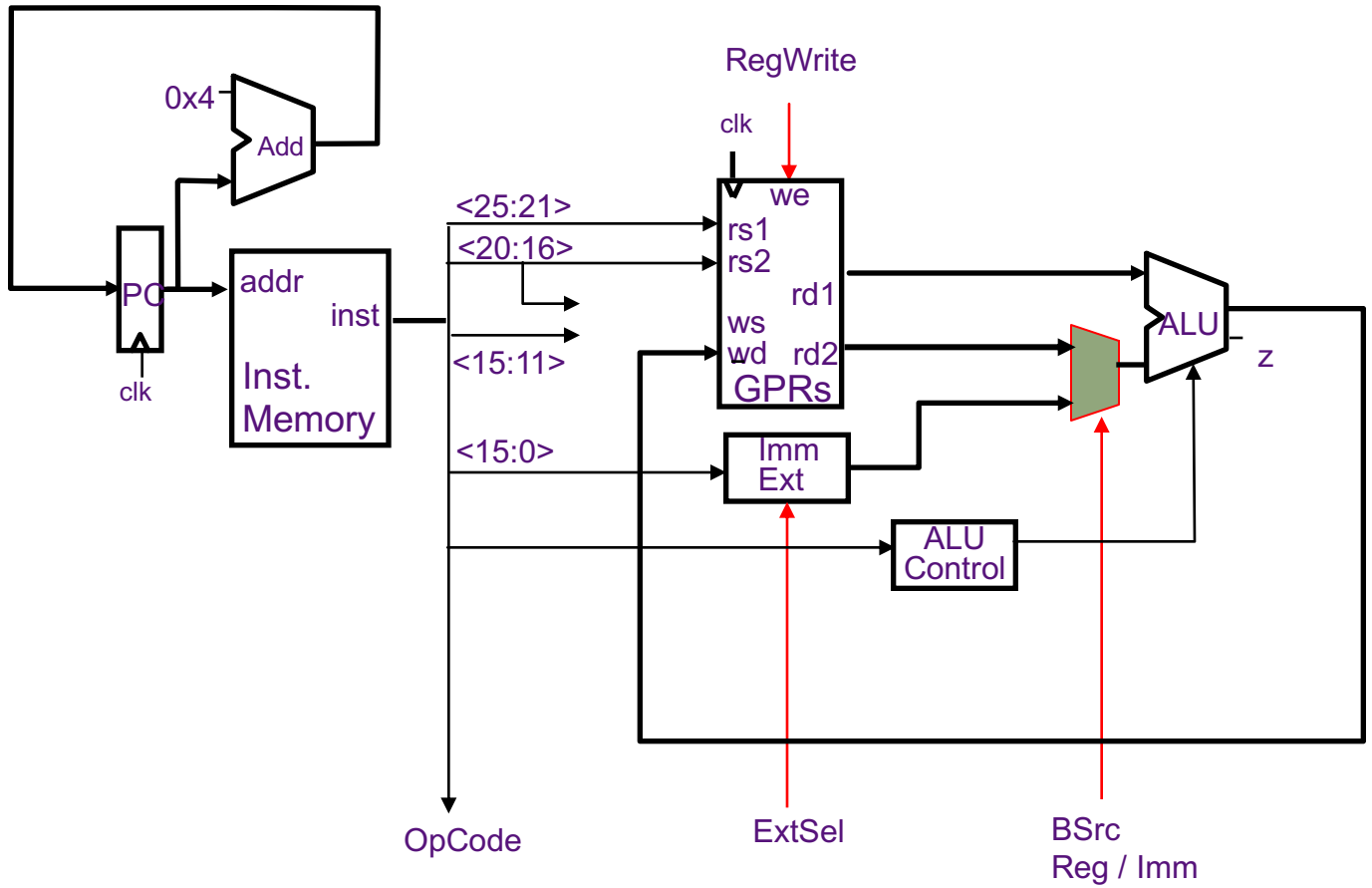

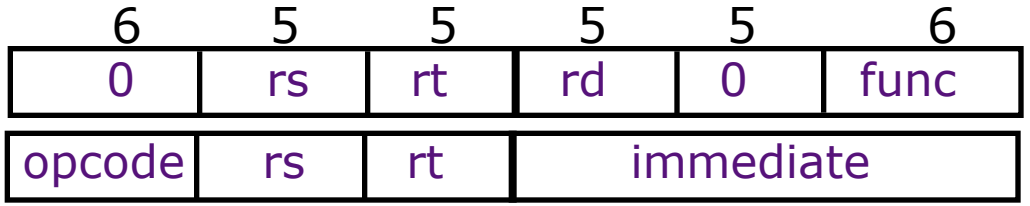

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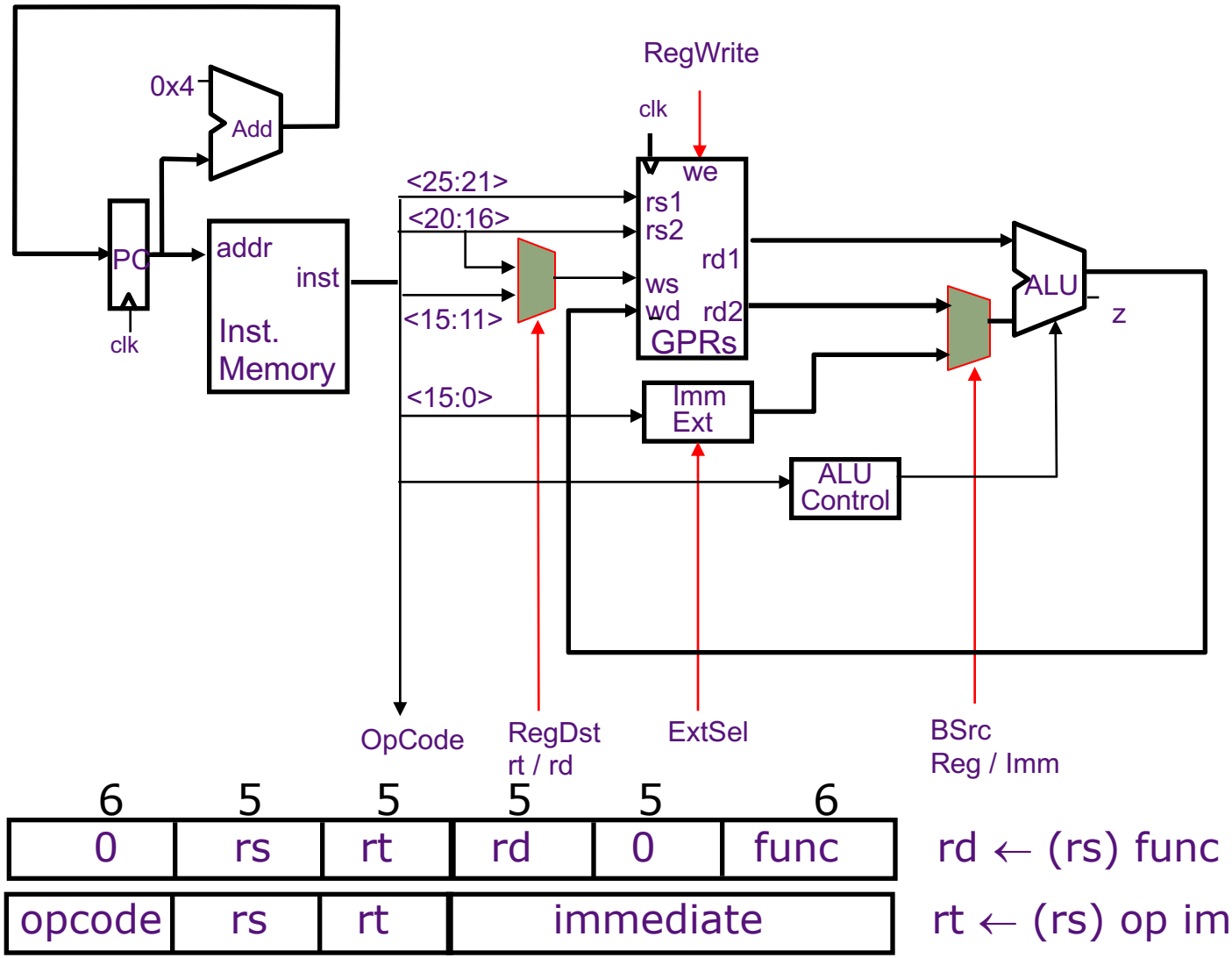

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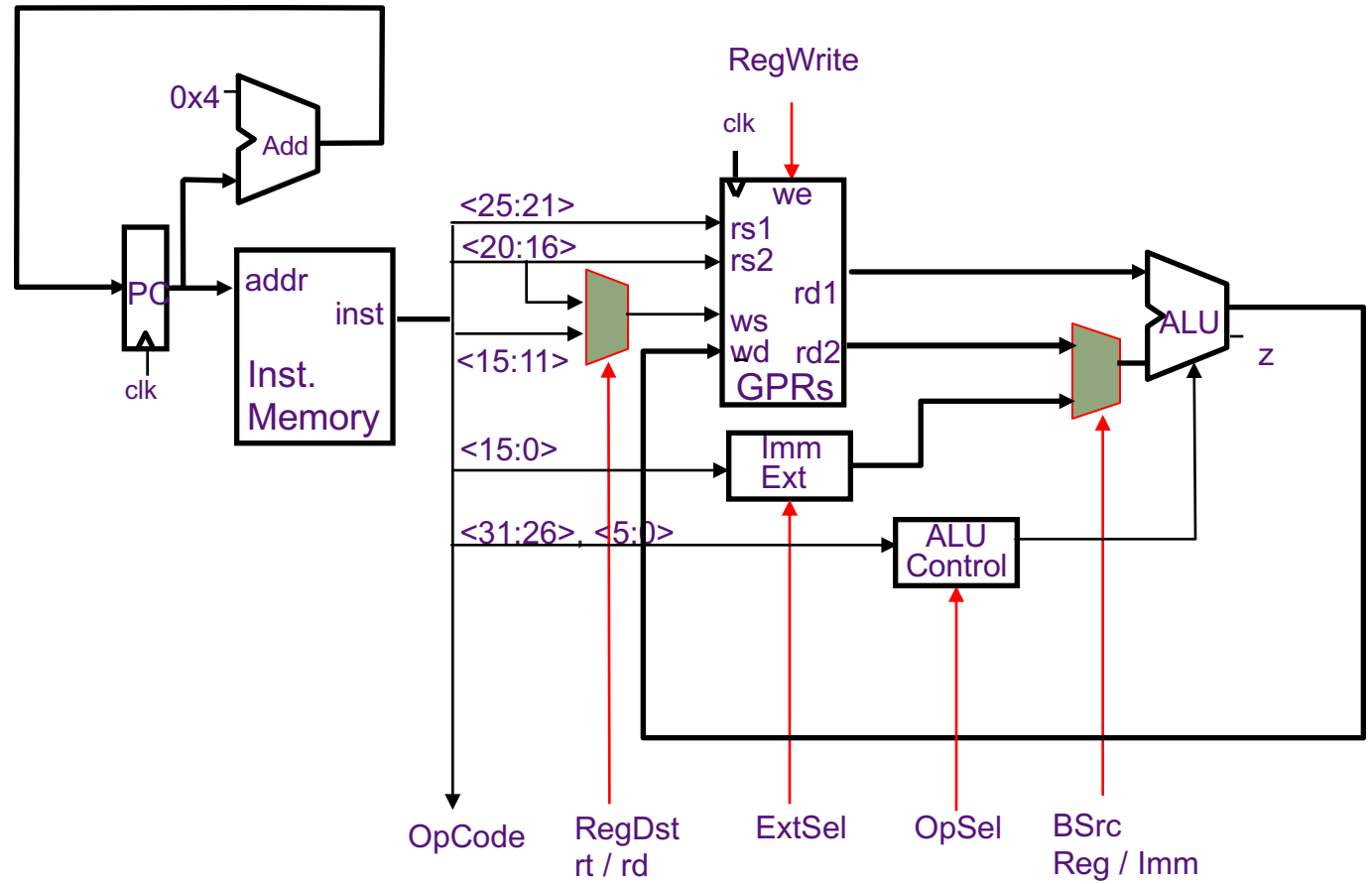

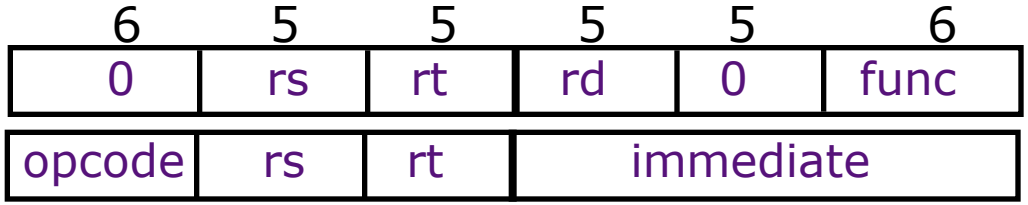

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Should program and data memory be separate?

Harvard style: separate (Aiken and Mark 1 influence)
- read-only program memory
- read/write data memory

Princeton style: the same (von Neumann's influence)
- single read/write memory for program and data

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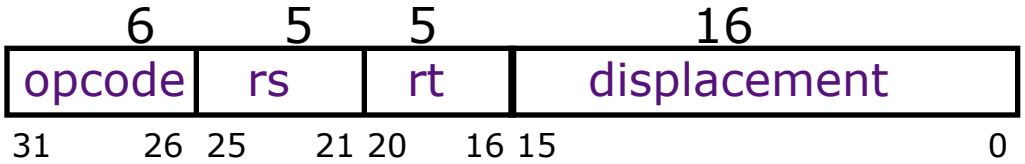
- Note:
  Executing a Load or Store instruction requires accessing the memory more than once

Load/Store Instructions

Harvard Datapath



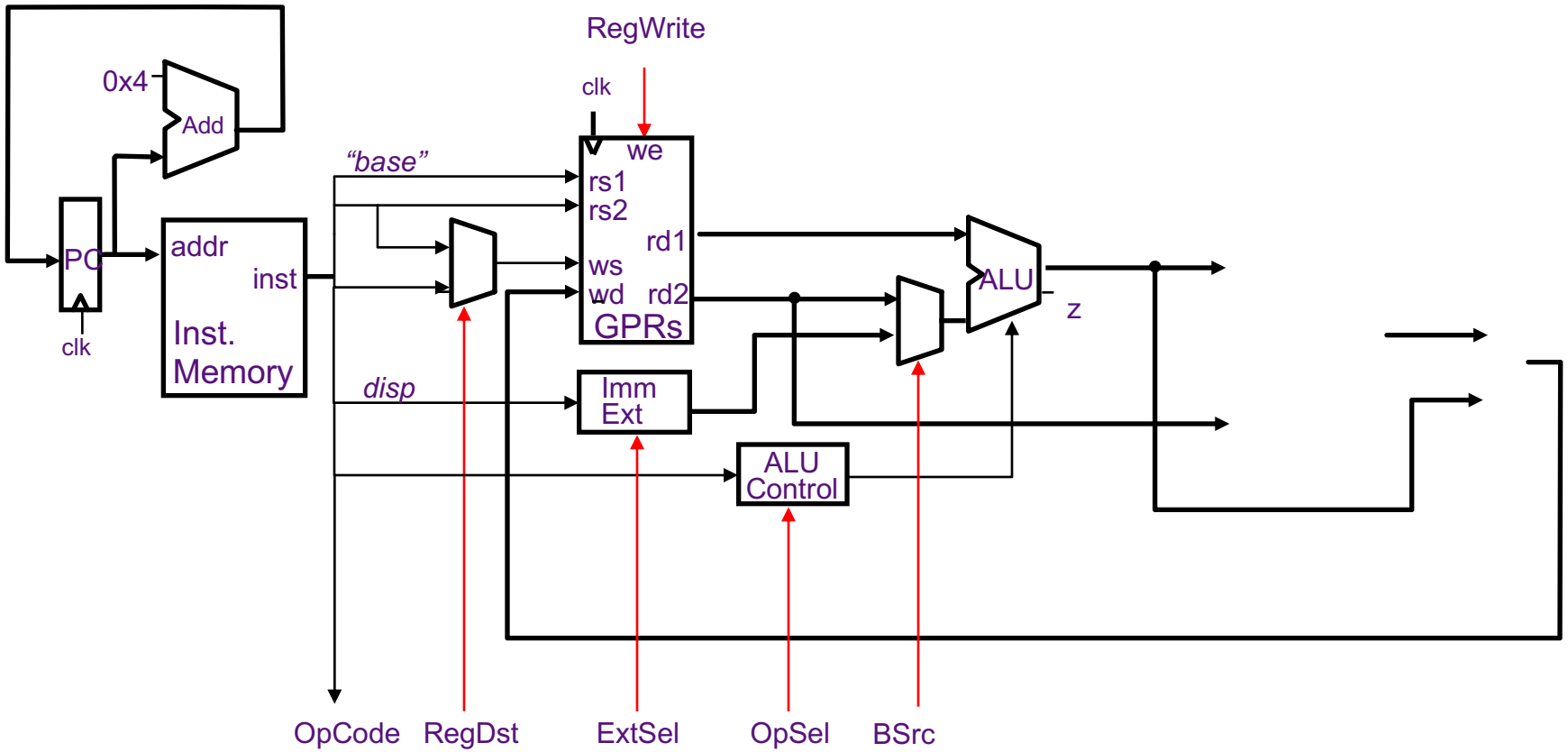
addressing mode
(rs) + displacement

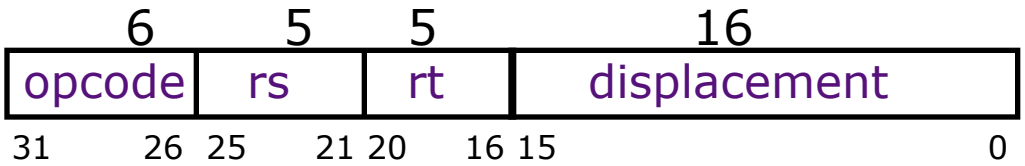
rs is the base register

rt is the destination of a Load or the source for a Store

Load/Store Instructions

Harvard Datapath





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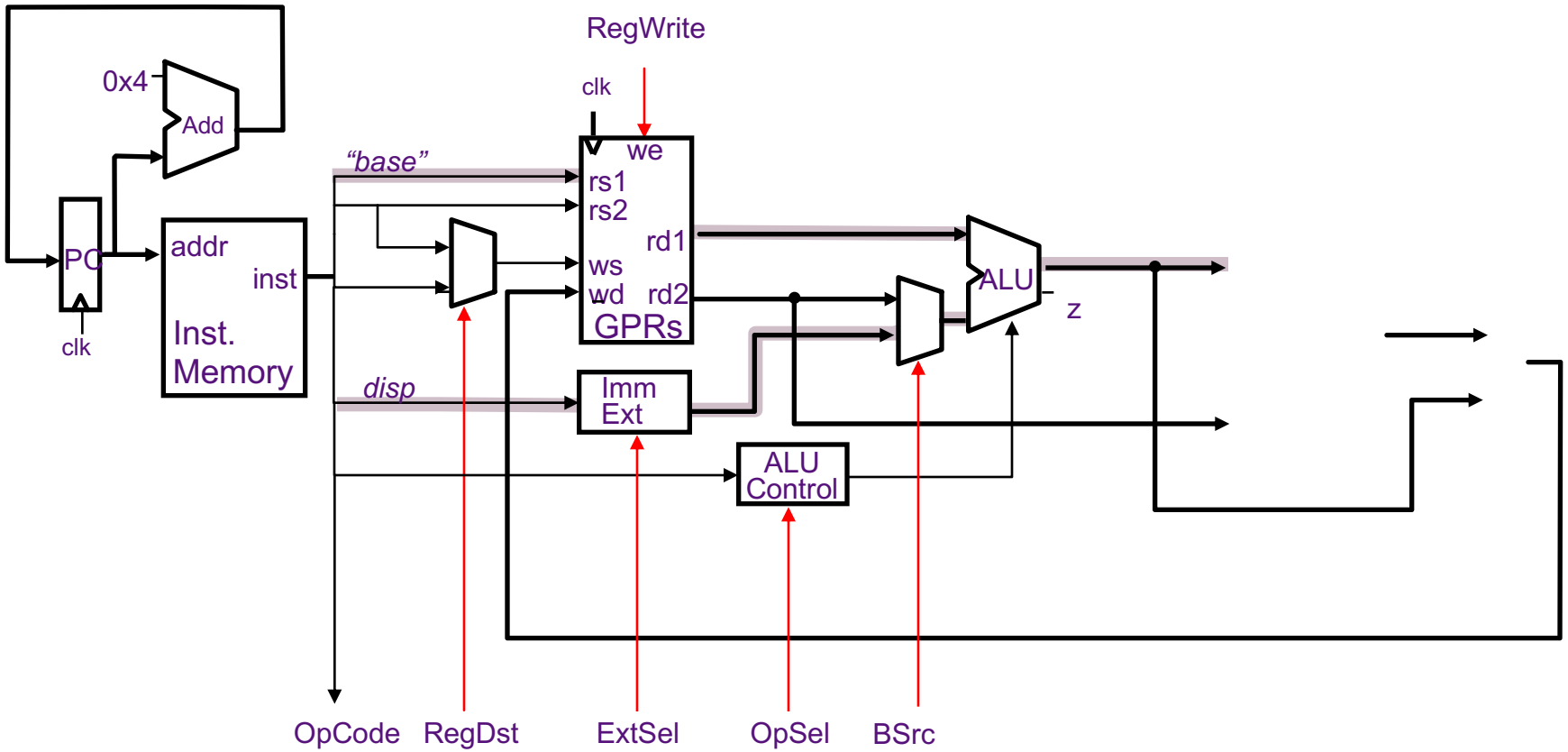
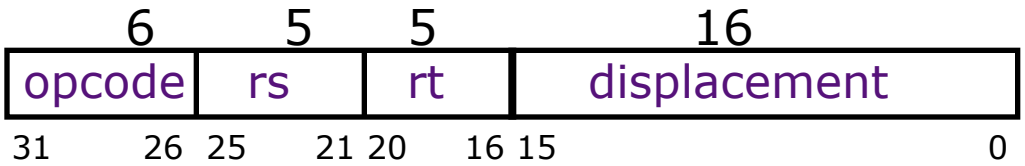
Load/Store Instructions

Harvard Datapath





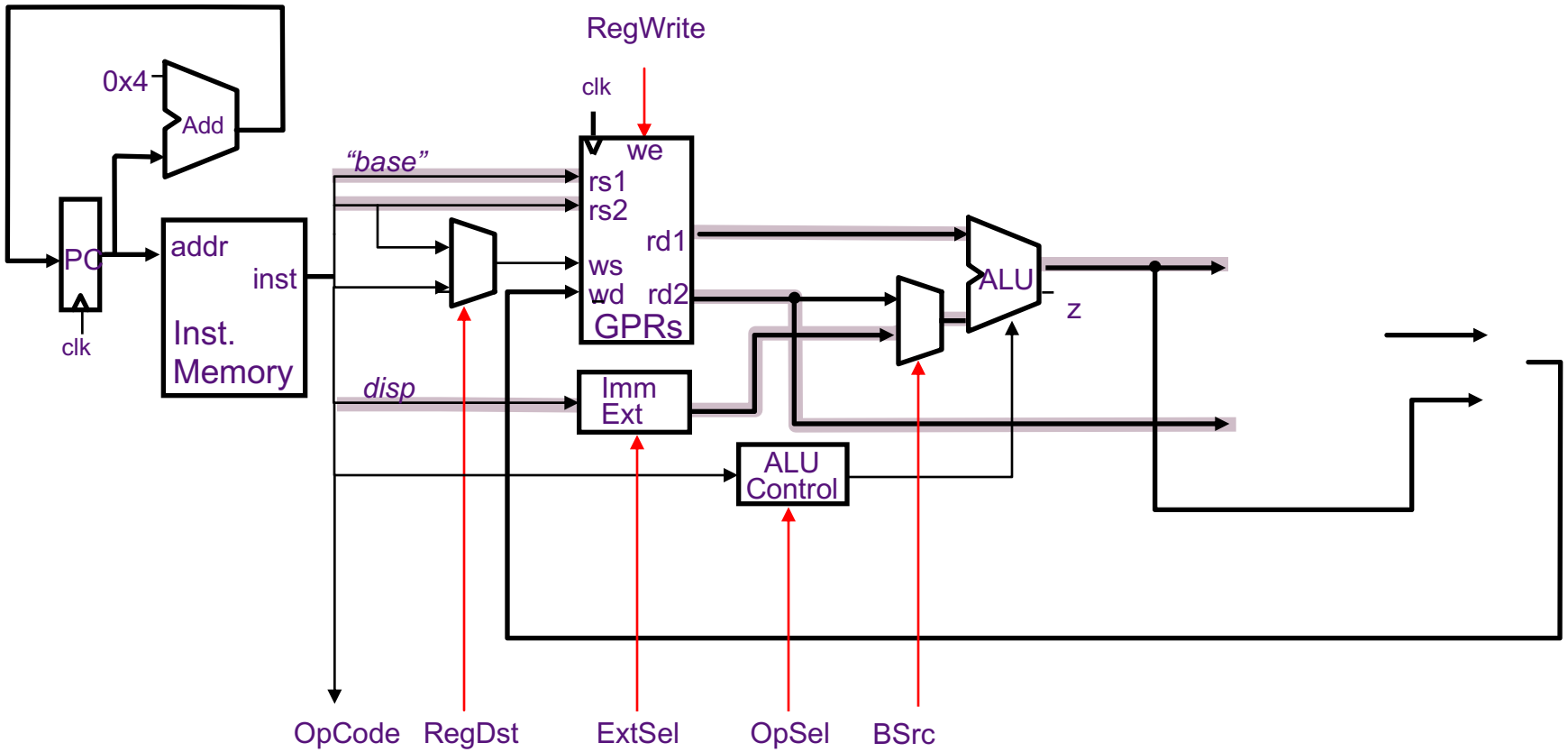
addressing mode
(rs) + displacement

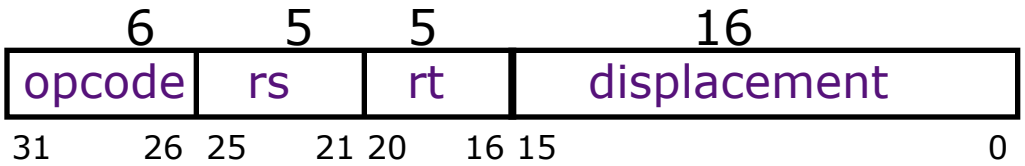
rs is the base register

rt is the destination of a Load or the source for a Store

Load/Store Instructions

Harvard Datapath





addressing mode
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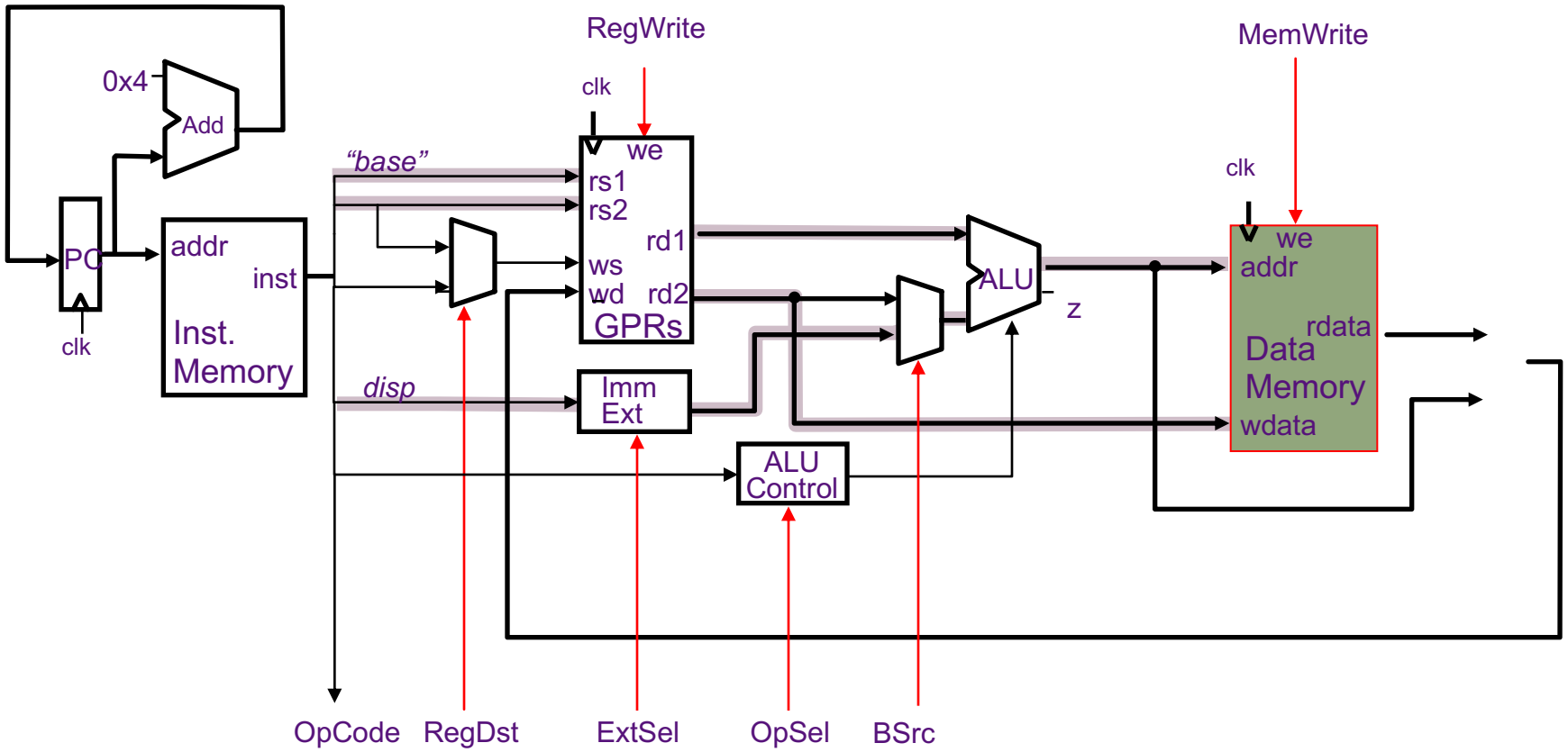
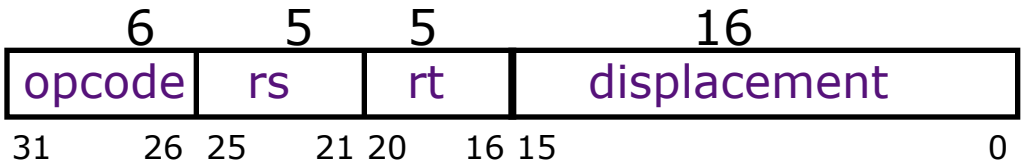
Load/Store Instructions

Harvard Datapath





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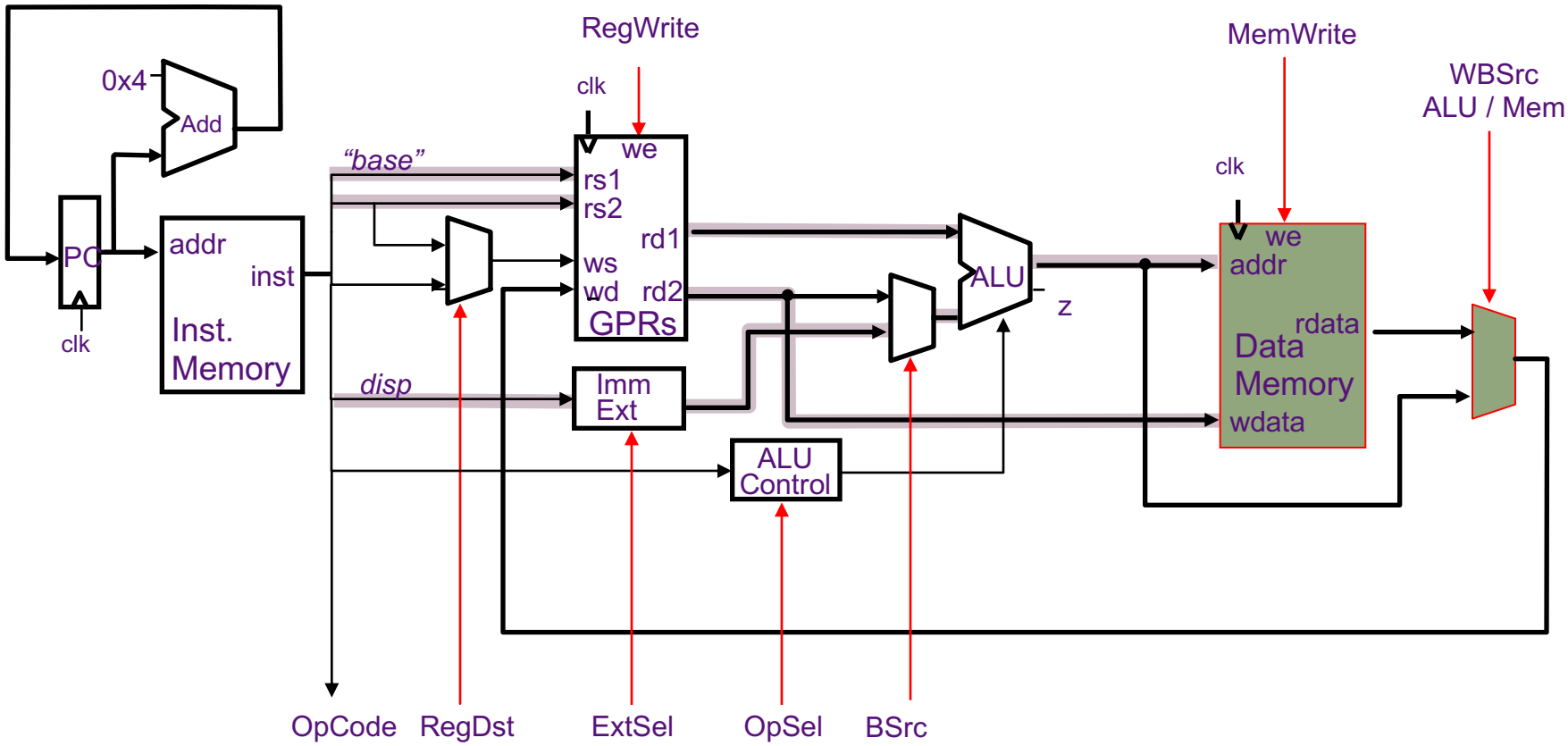
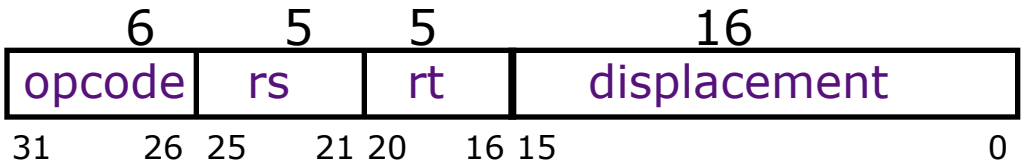
Load/Store Instructions

Harvard Datapath





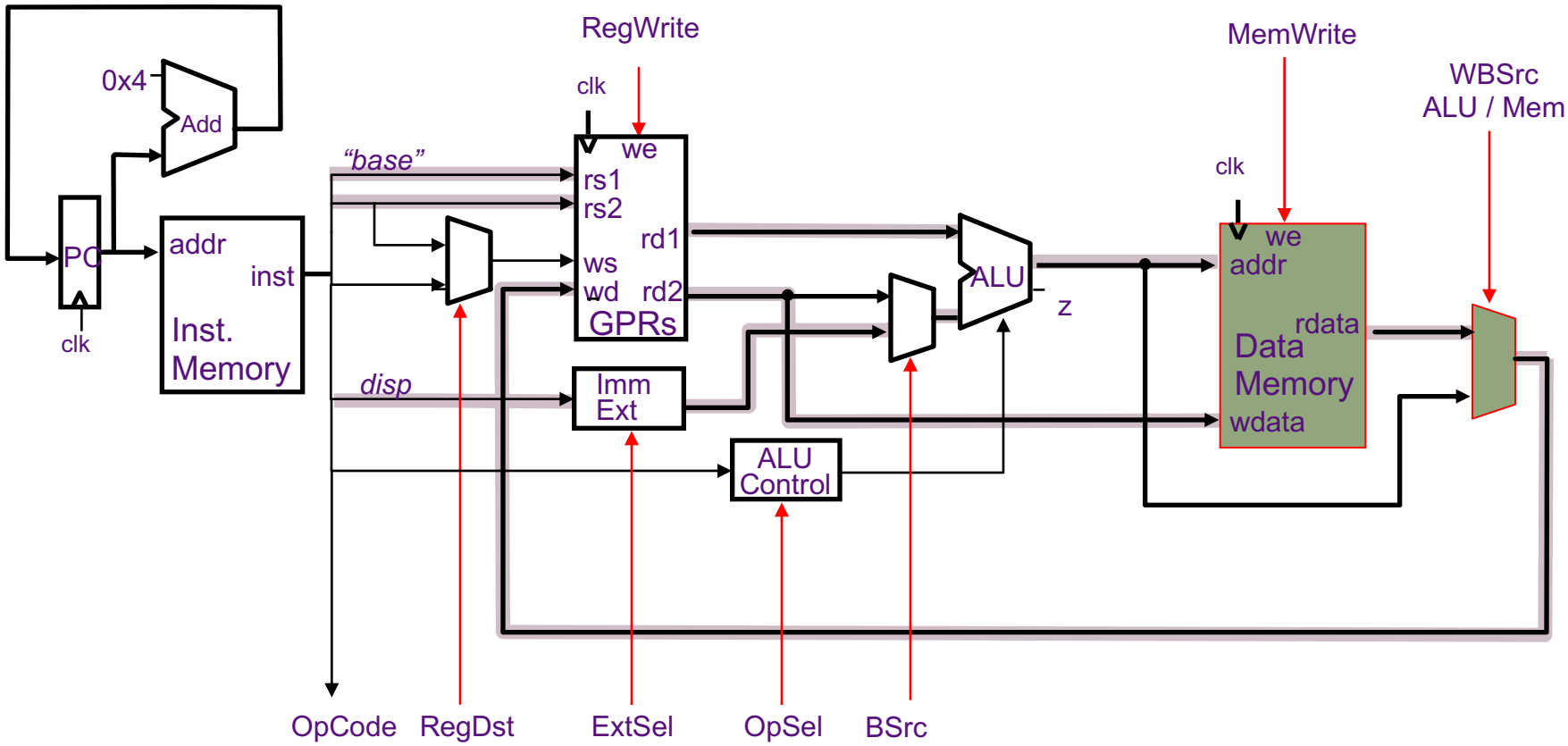
addressing mode
(rs) + displacement

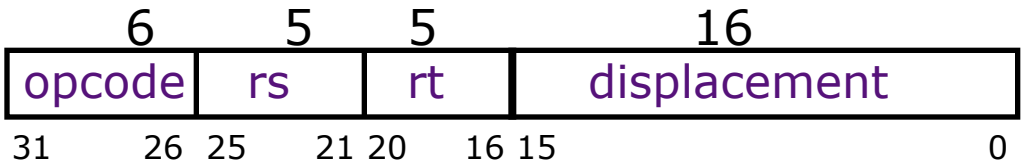
rs is the base register

rt is the destination of a Load or the source for a Store

Load/Store Instructions

Harvard Datapath





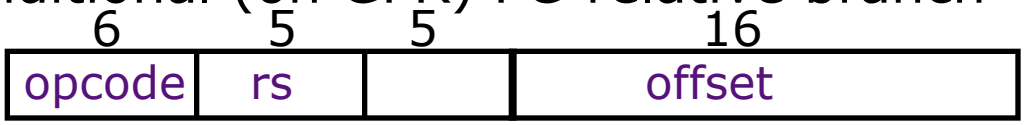
addressing mode
(rs) + displacement

rs is the base register

rt is the destination of a Load or the source for a Store

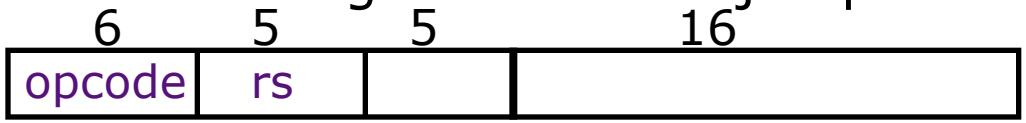
MIPS Control Instructions

Conditional (on GPR) PC-relative branch



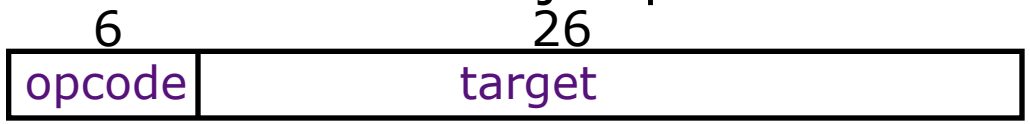
BEQZ, BNEZ

Unconditional register-indirect jumps



JR, JALR

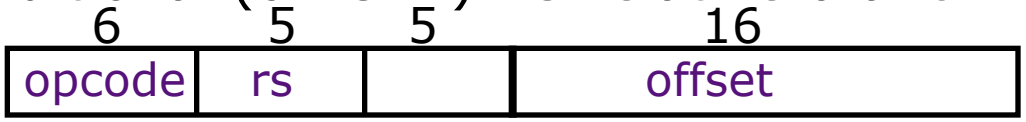
Unconditional absolute jumps



J, JAL

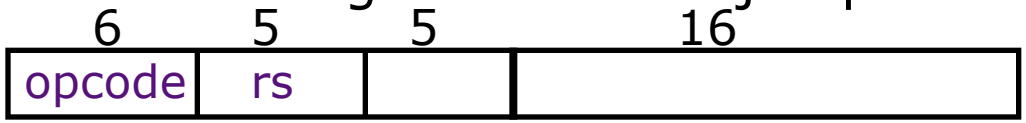
MIPS Control Instructions

Conditional (on GPR) PC-relative branch



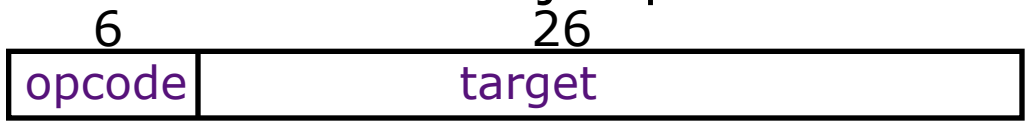
BEQZ, BNEZ

Unconditional register-indirect jumps



JR, JALR

Unconditional absolute jumps



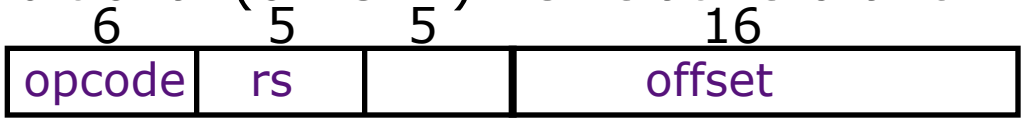
J, JAL

	Target PC	Condition
BEQZ	PC+4+offset*4	(rs)==0
BNEZ		(rs)!=0
JR, JALR	(rs)	Always taken
J, JAL	PC[31:28]|target*4	Always taken

- Jump-&-link stores PC+4 into the link register (R31)

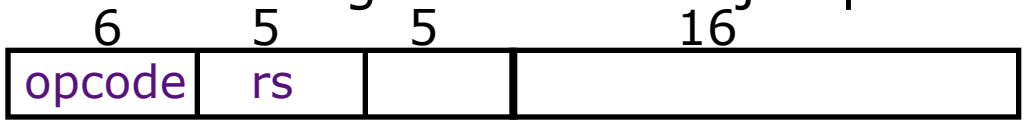
MIPS Control Instructions

Conditional (on GPR) PC-relative branch



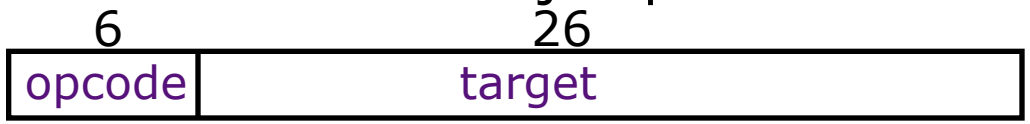
BEQZ, BNEZ

Unconditional register-indirect jumps



JR, JALR

Unconditional absolute jumps

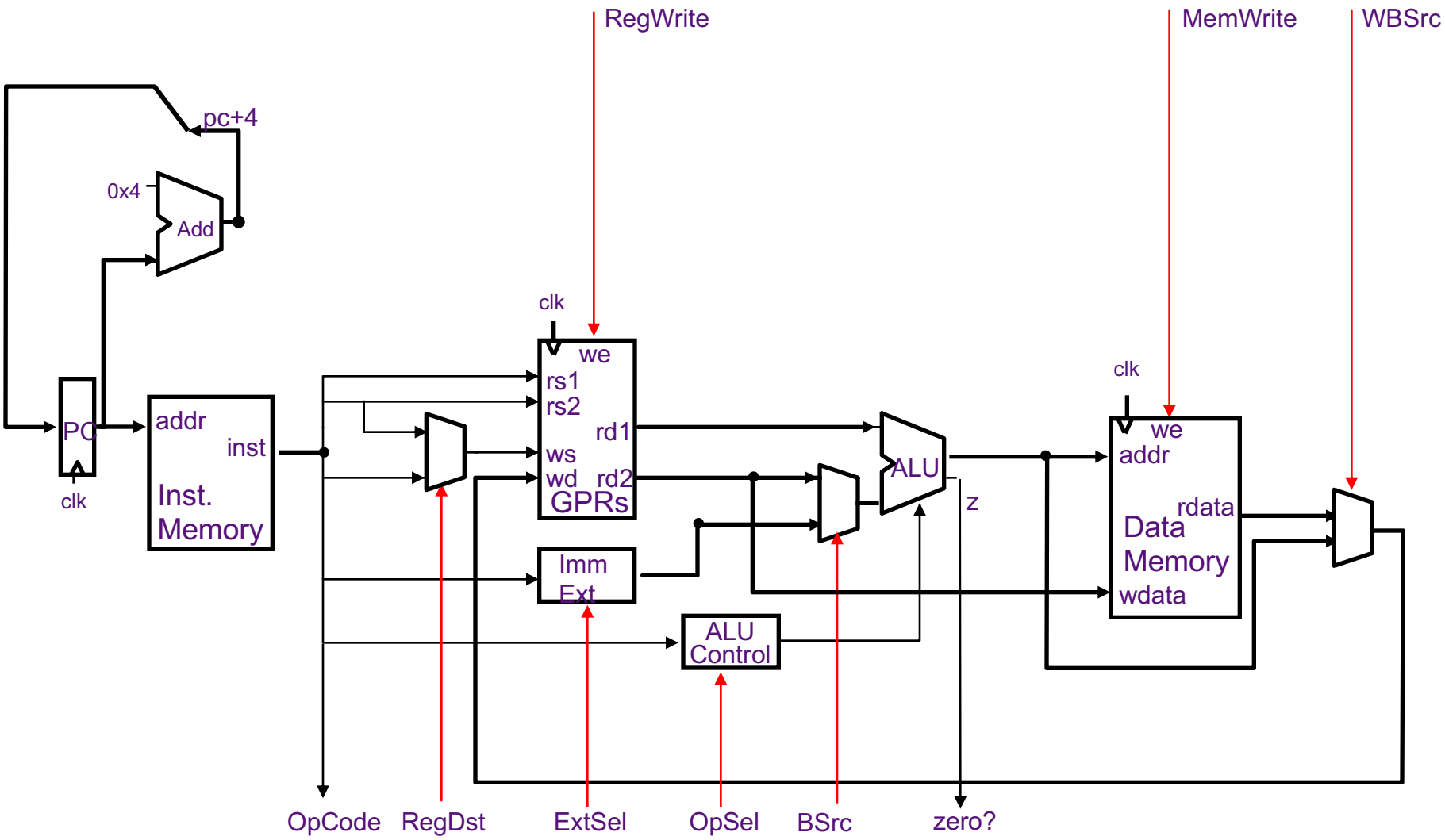


J, JAL

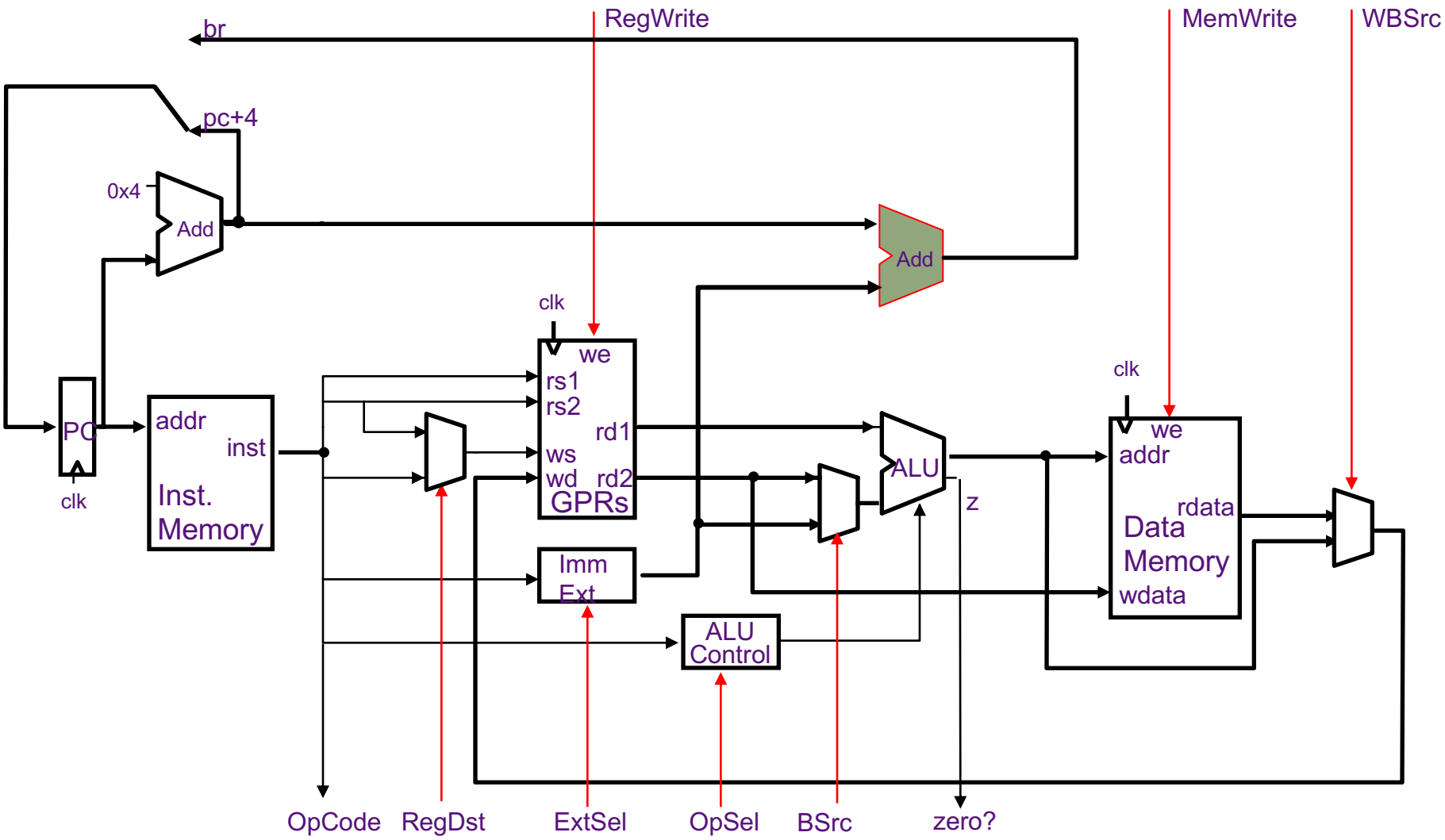
	Target PC	Condition
BEQZ	PC+4+offset*4	(rs)==0
BNEZ		(rs)!=0
JR, JALR	(rs)	Always taken
J, JAL	PC[31:28]|target*4	Always taken

- Jump-&-link stores PC+4 into the link register (R31)
- Control transfers are not delayed
  we will worry about the branch delay slot later

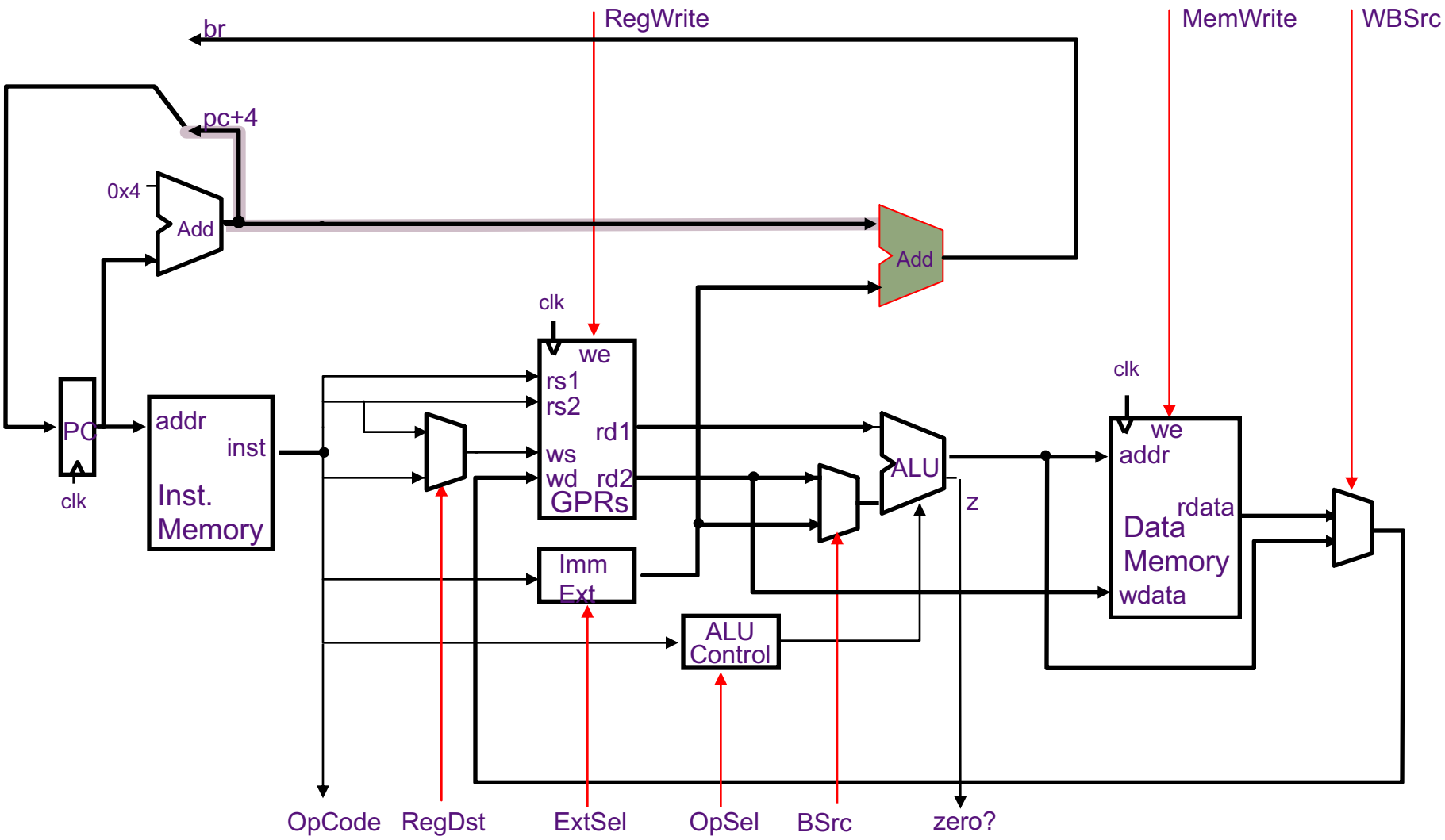
Conditional Branches (BEQZ, BNEZ)



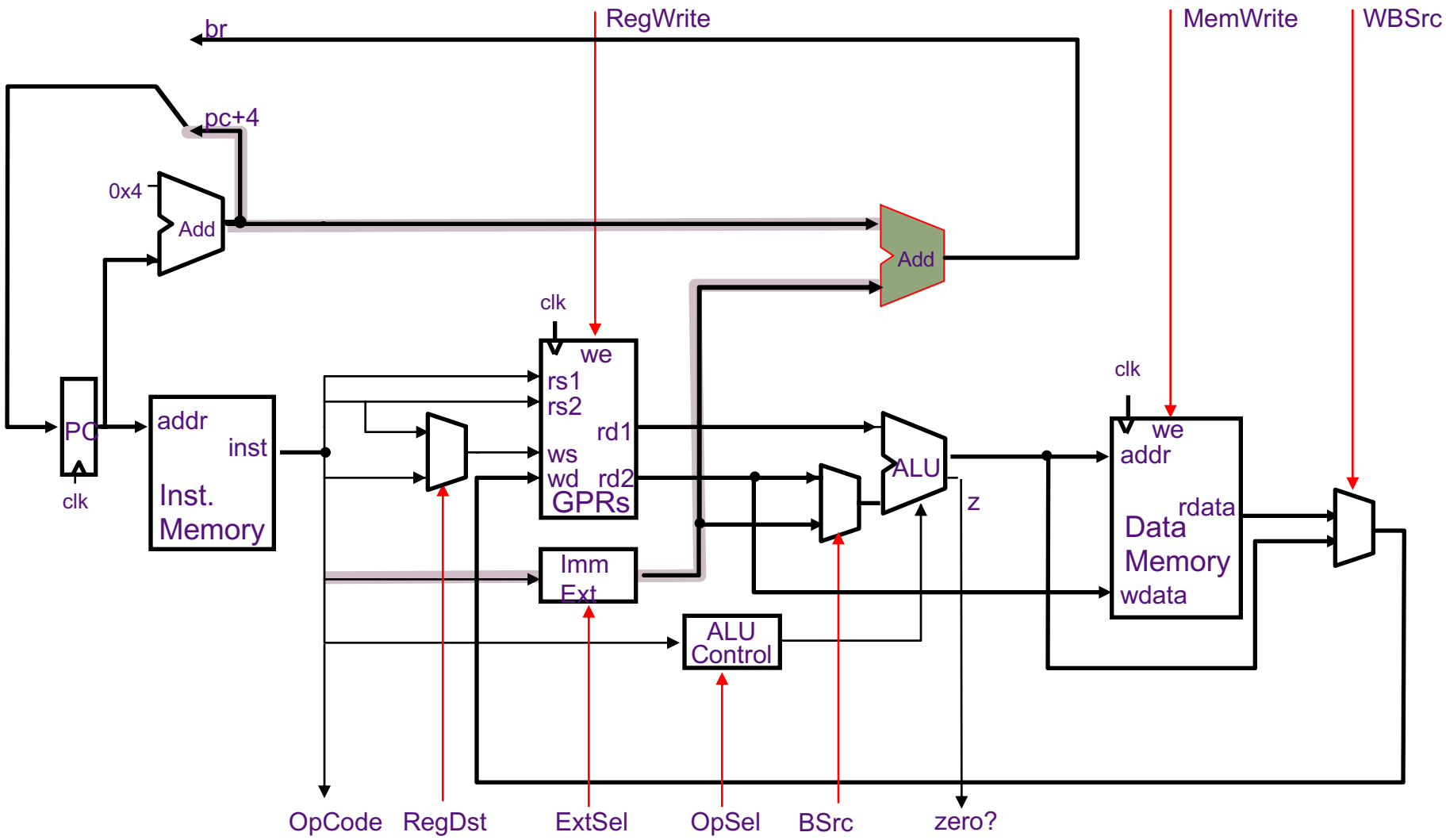
Conditional Branches (BEQZ, BNEZ)



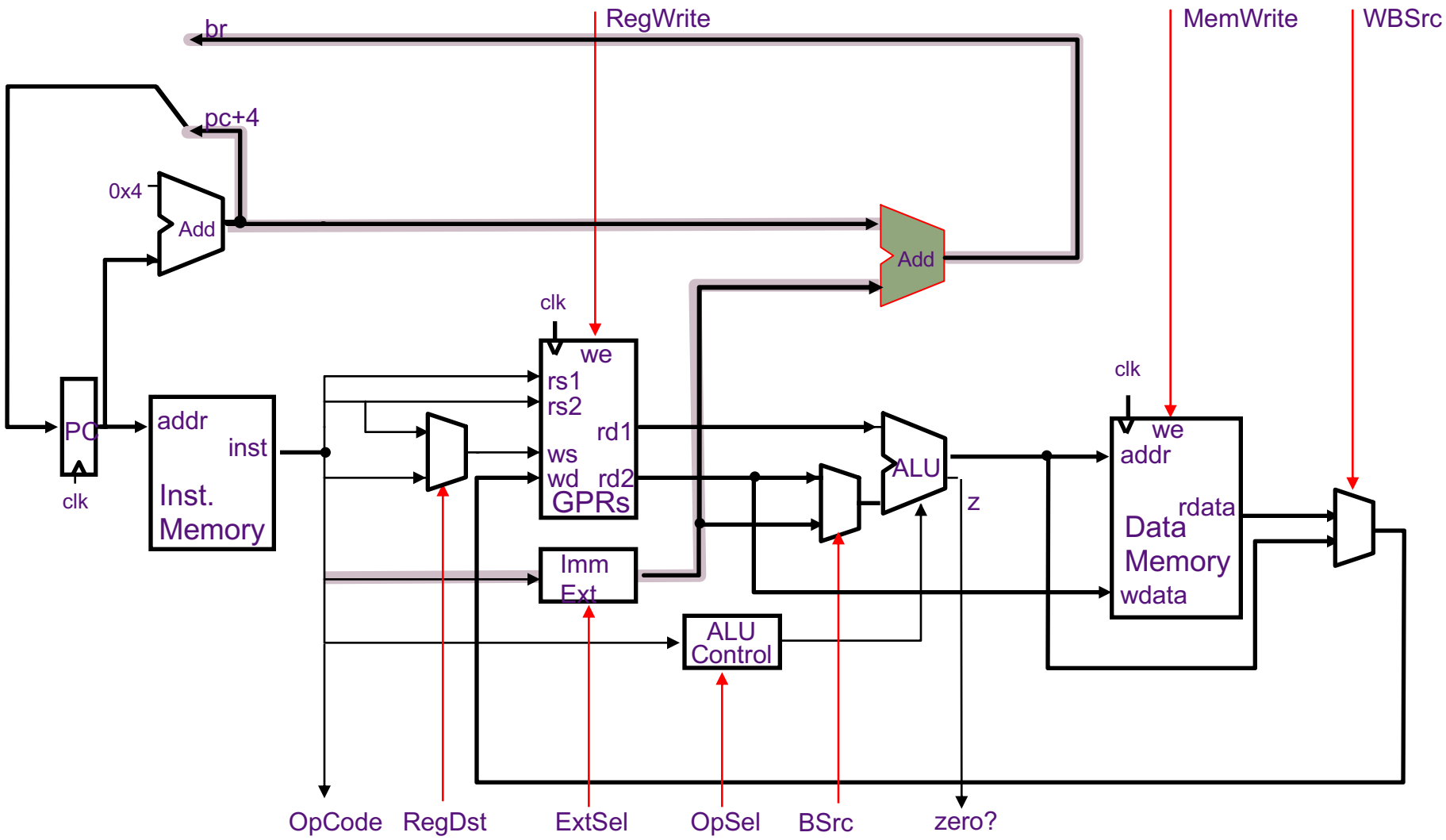
Conditional Branches (BEQZ, BNEZ)



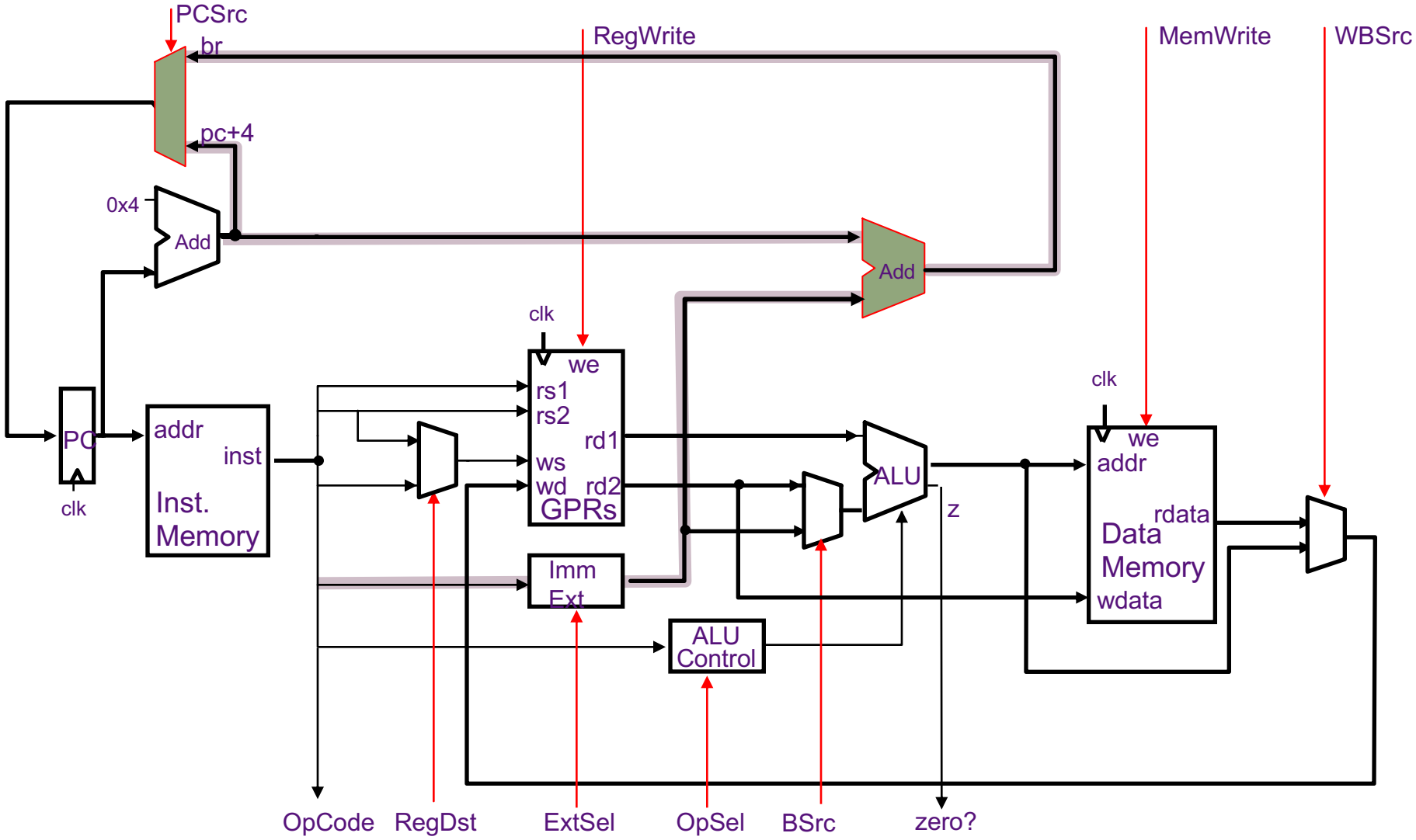
Conditional Branches (BEQZ, BNEZ)



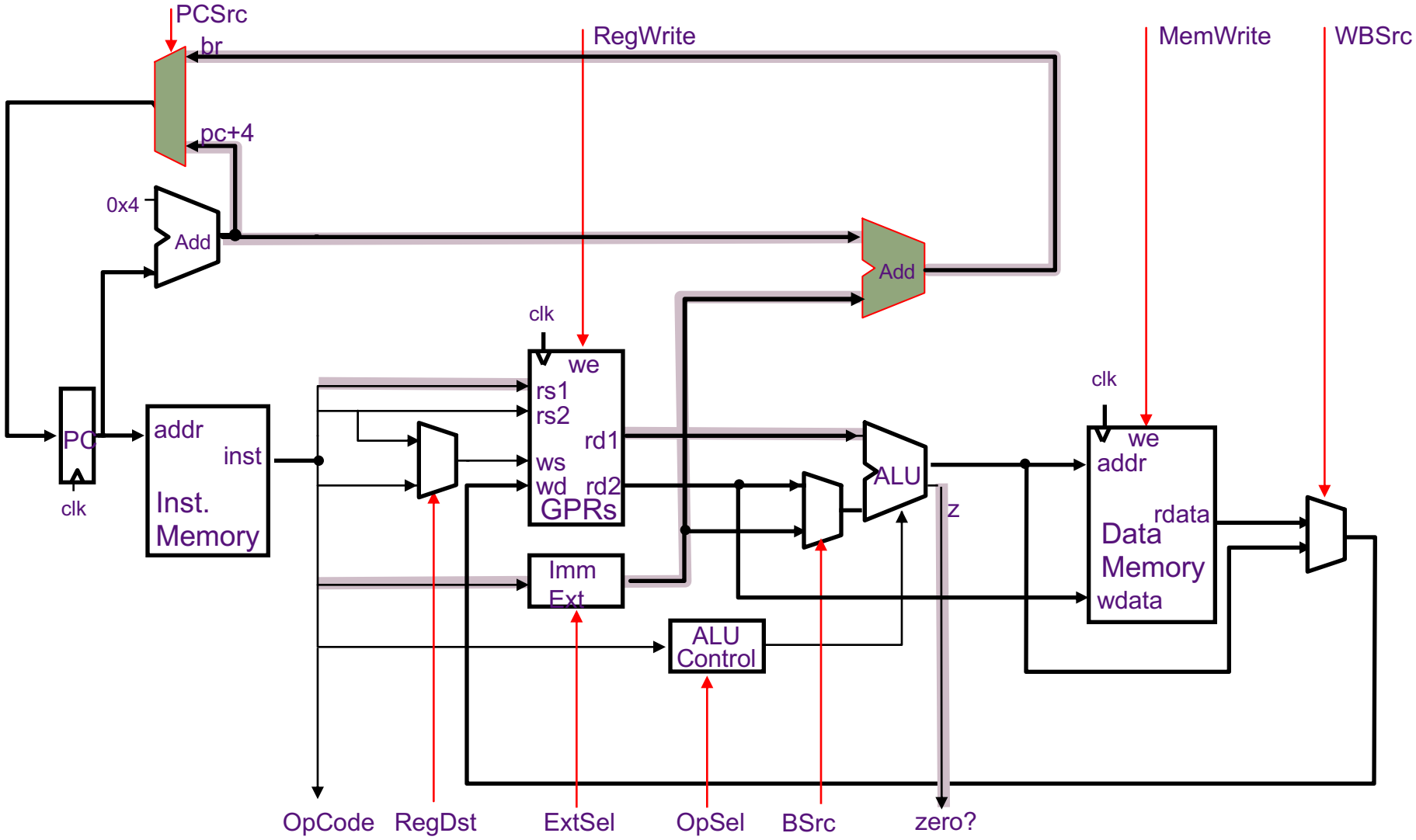
Conditional Branches (BEQZ, BNEZ)



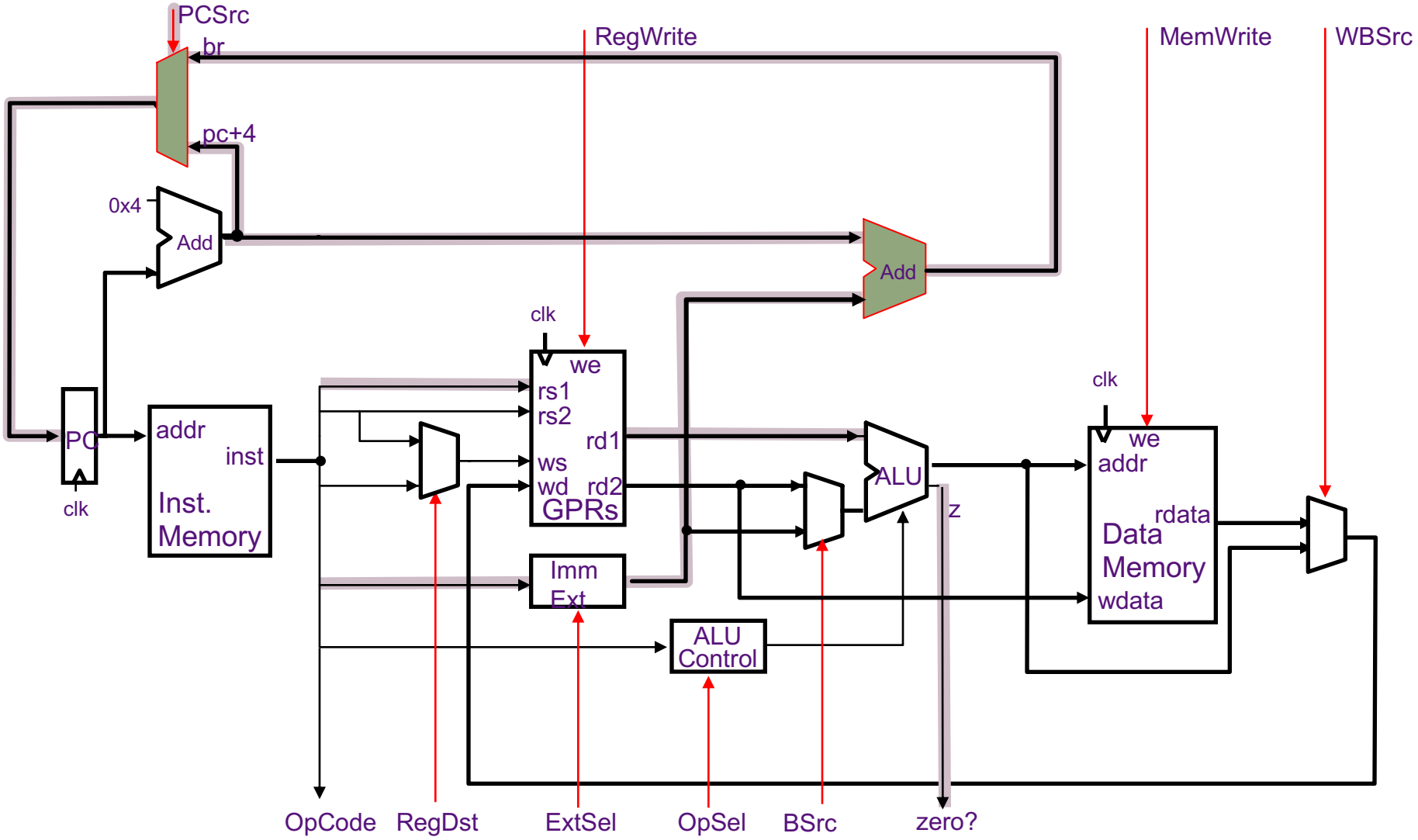
Conditional Branches (BEQZ, BNEZ)



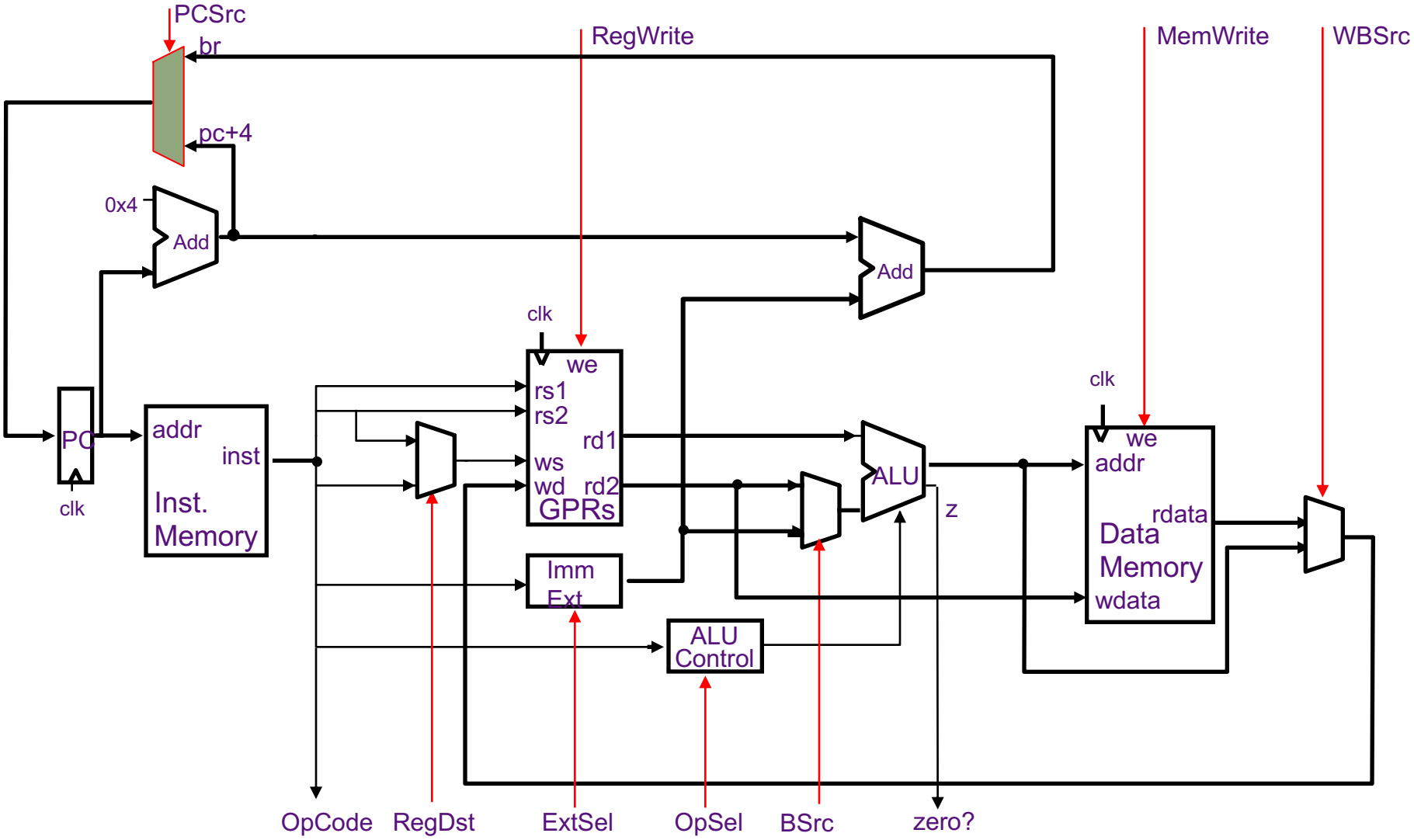
Conditional Branches (BEQZ, BNEZ)



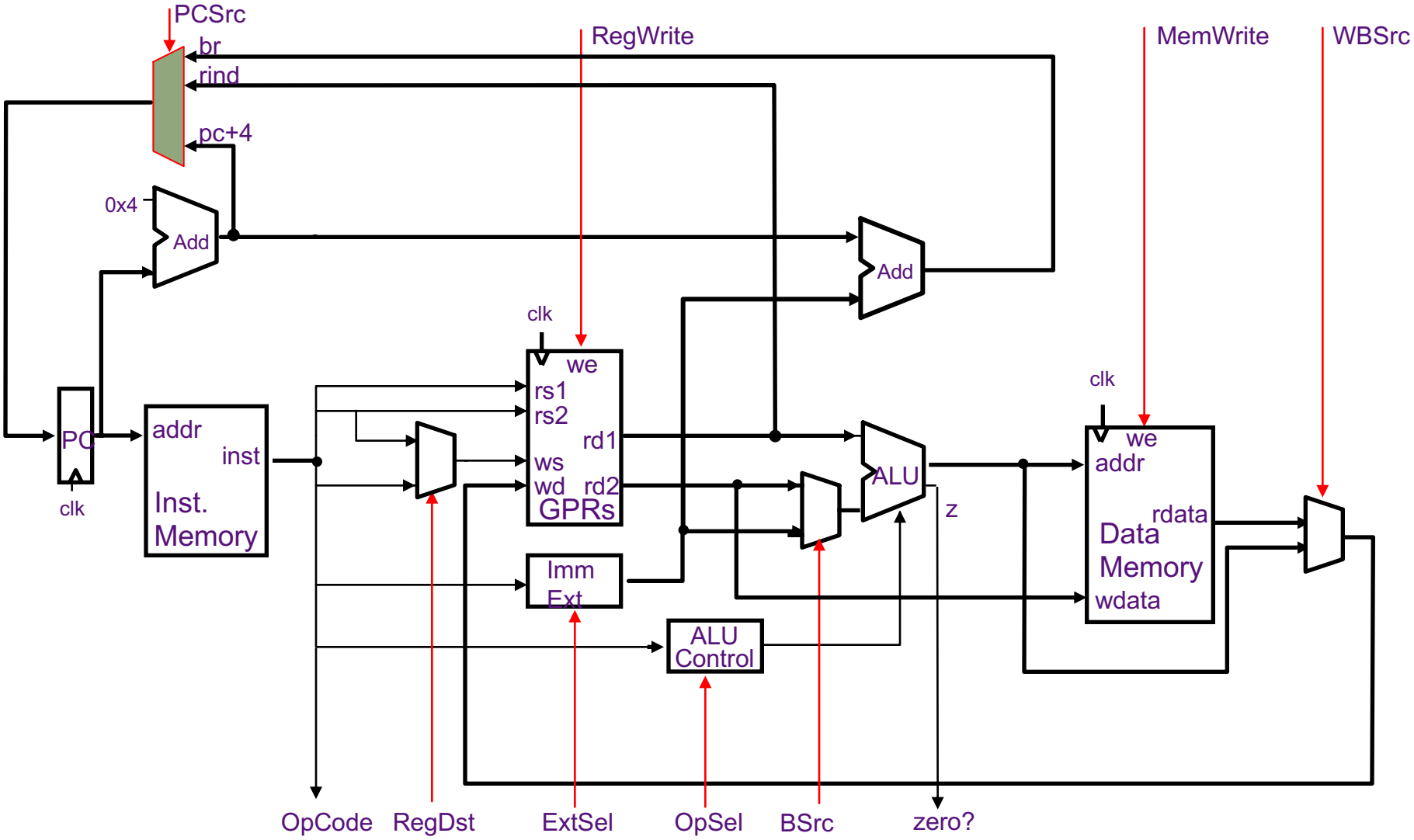
Conditional Branches (BEQZ, BNEZ)



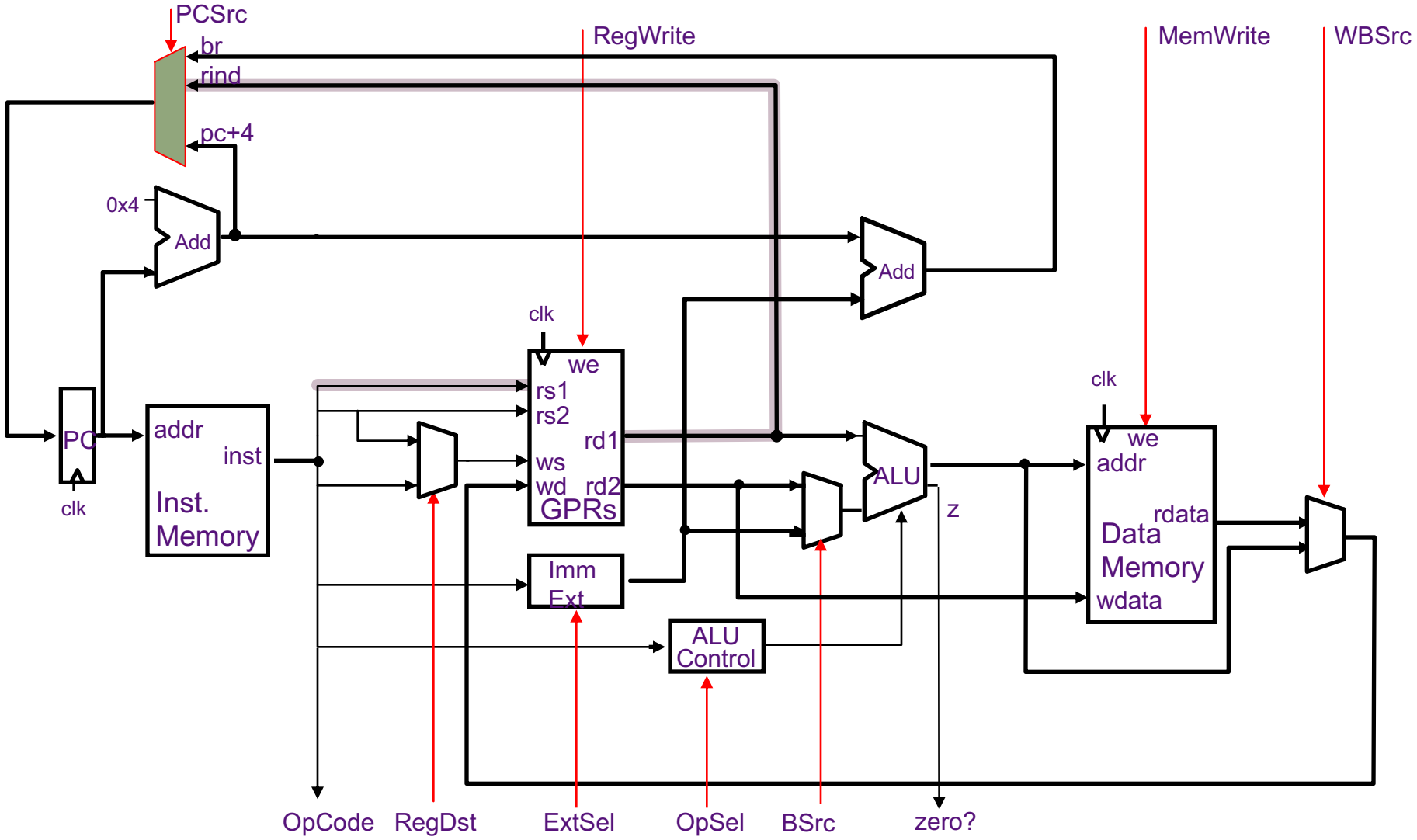
Register-Indirect Jumps (JR)



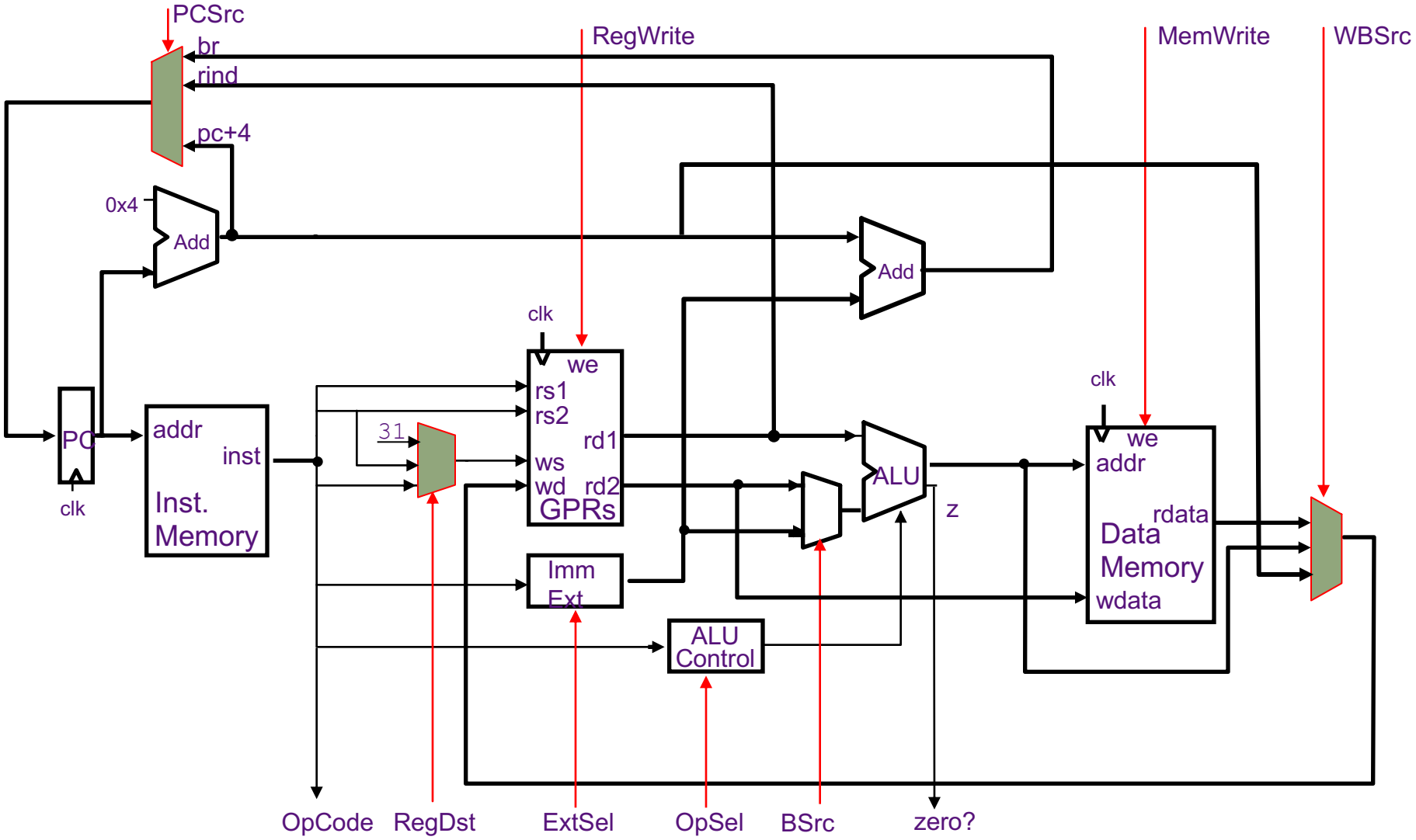
Register-Indirect Jumps (JR)



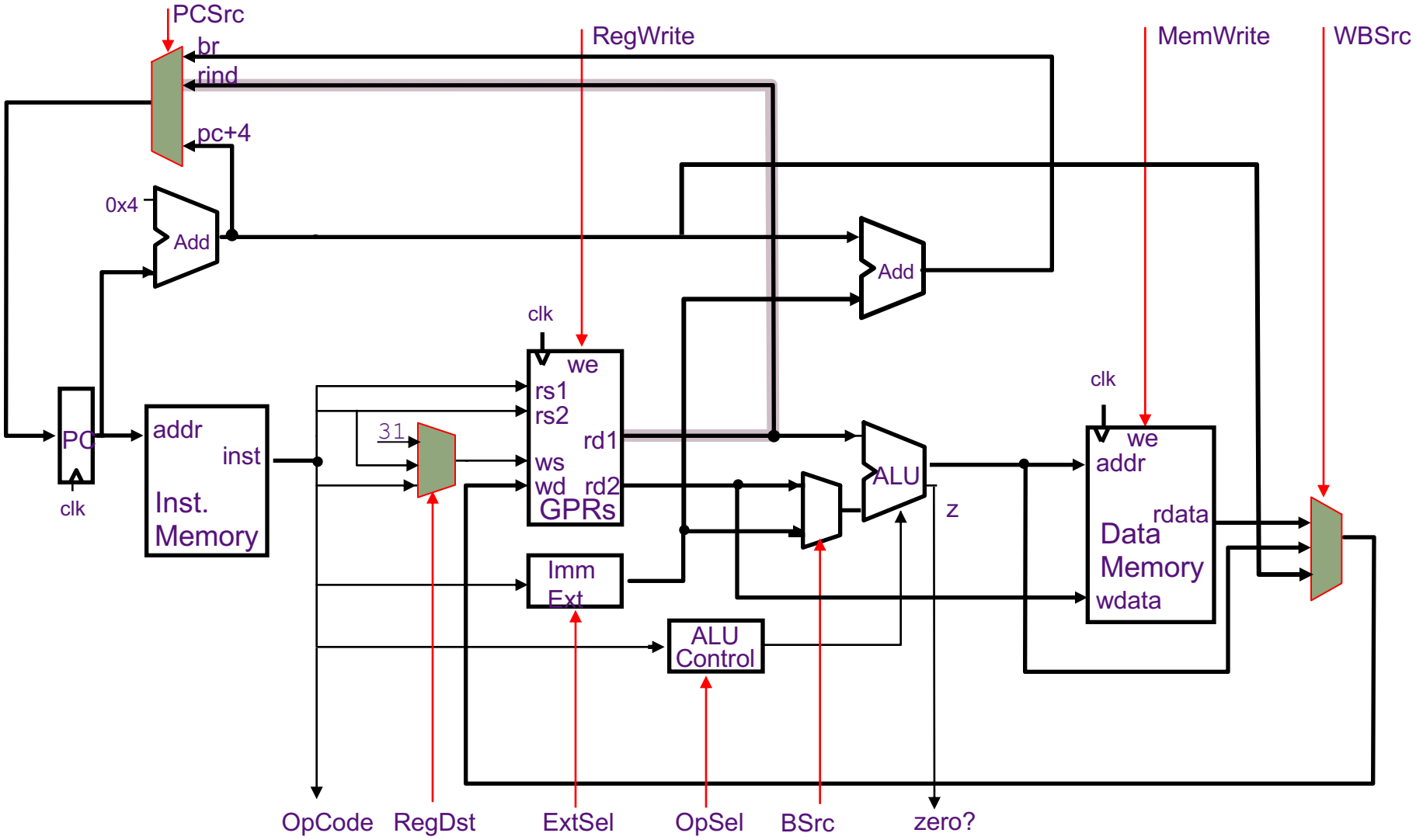
Register-Indirect Jumps (JR)



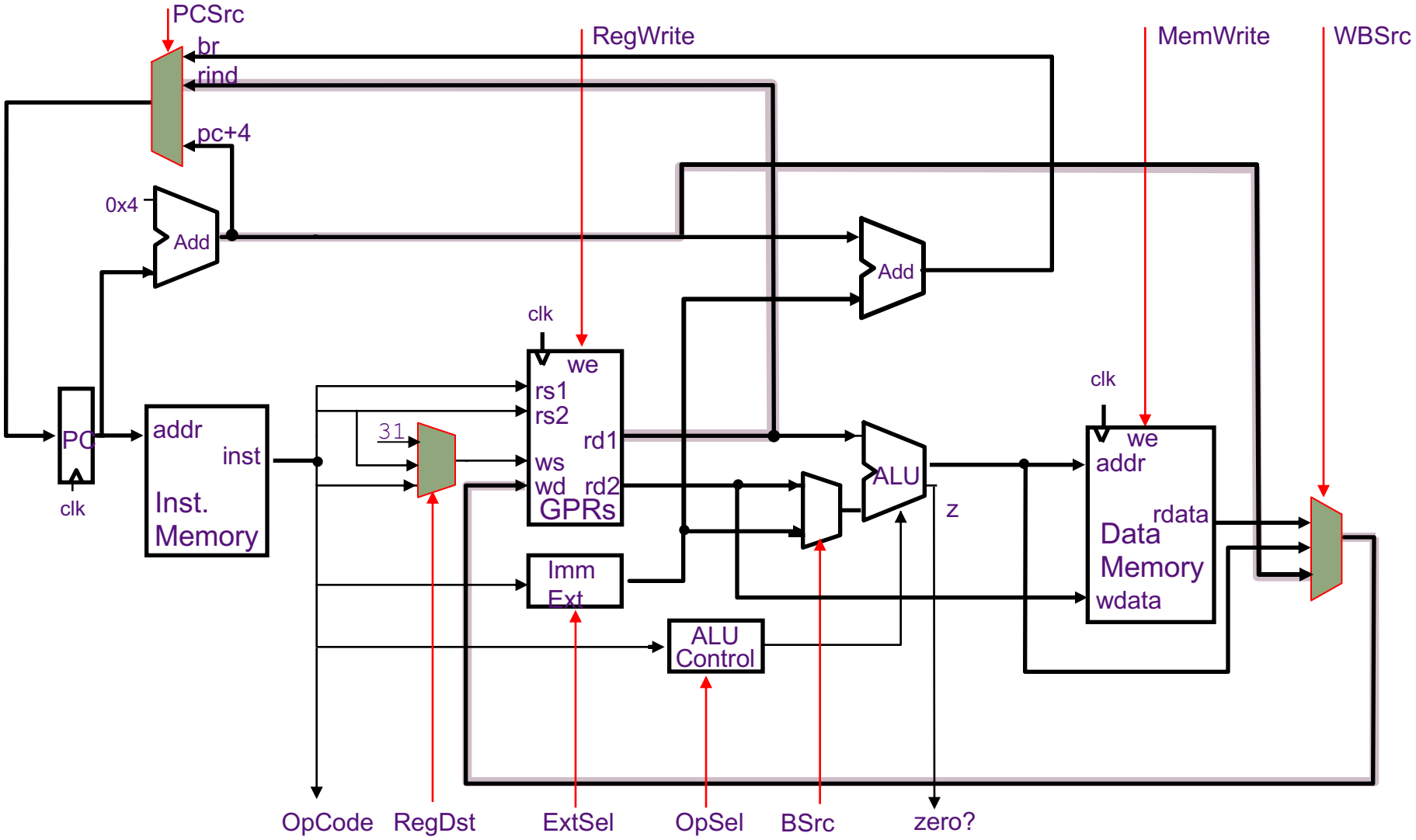
Register-Indirect Jump-&-Link (JALR)



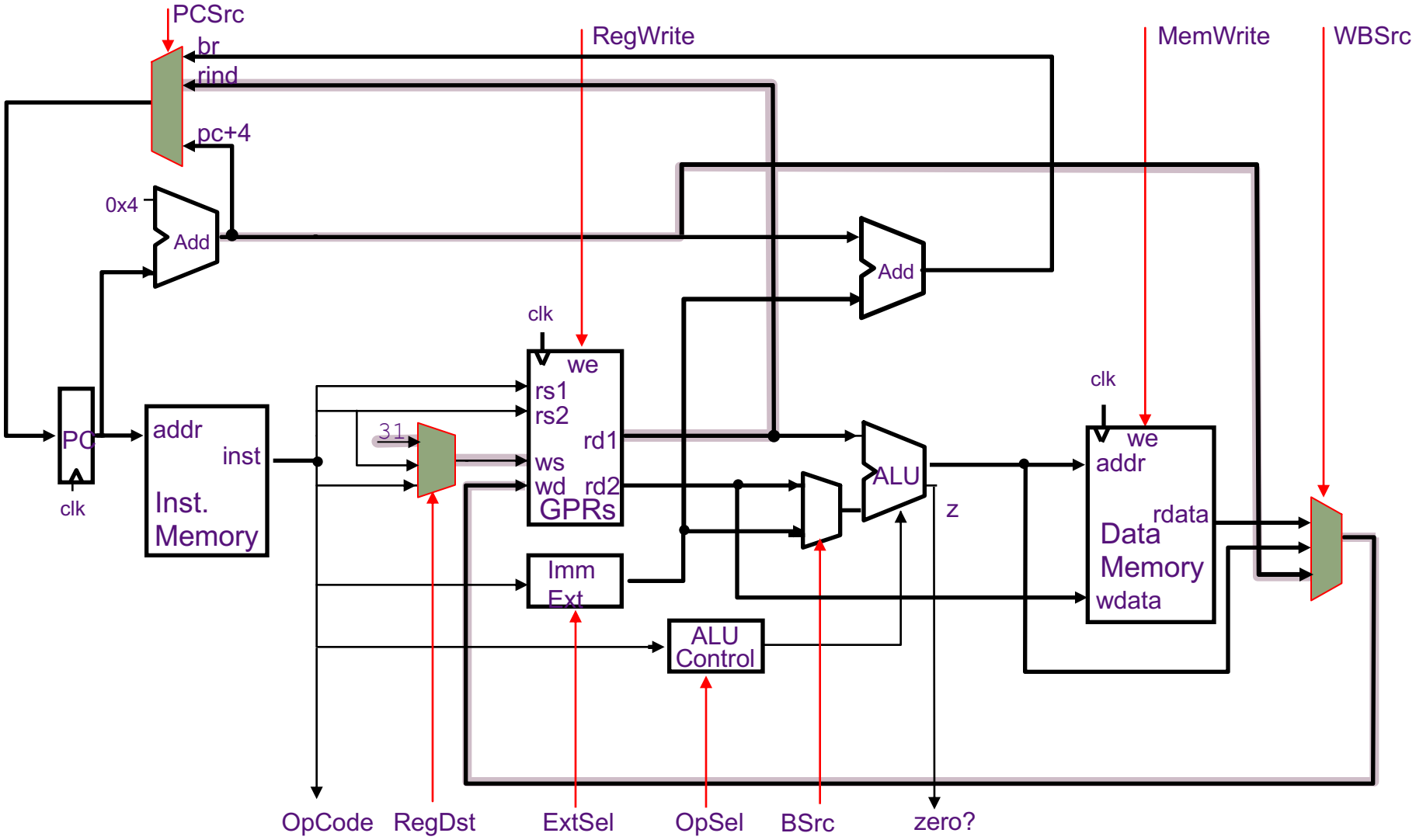
Register-Indirect Jump-&-Link (JALR)



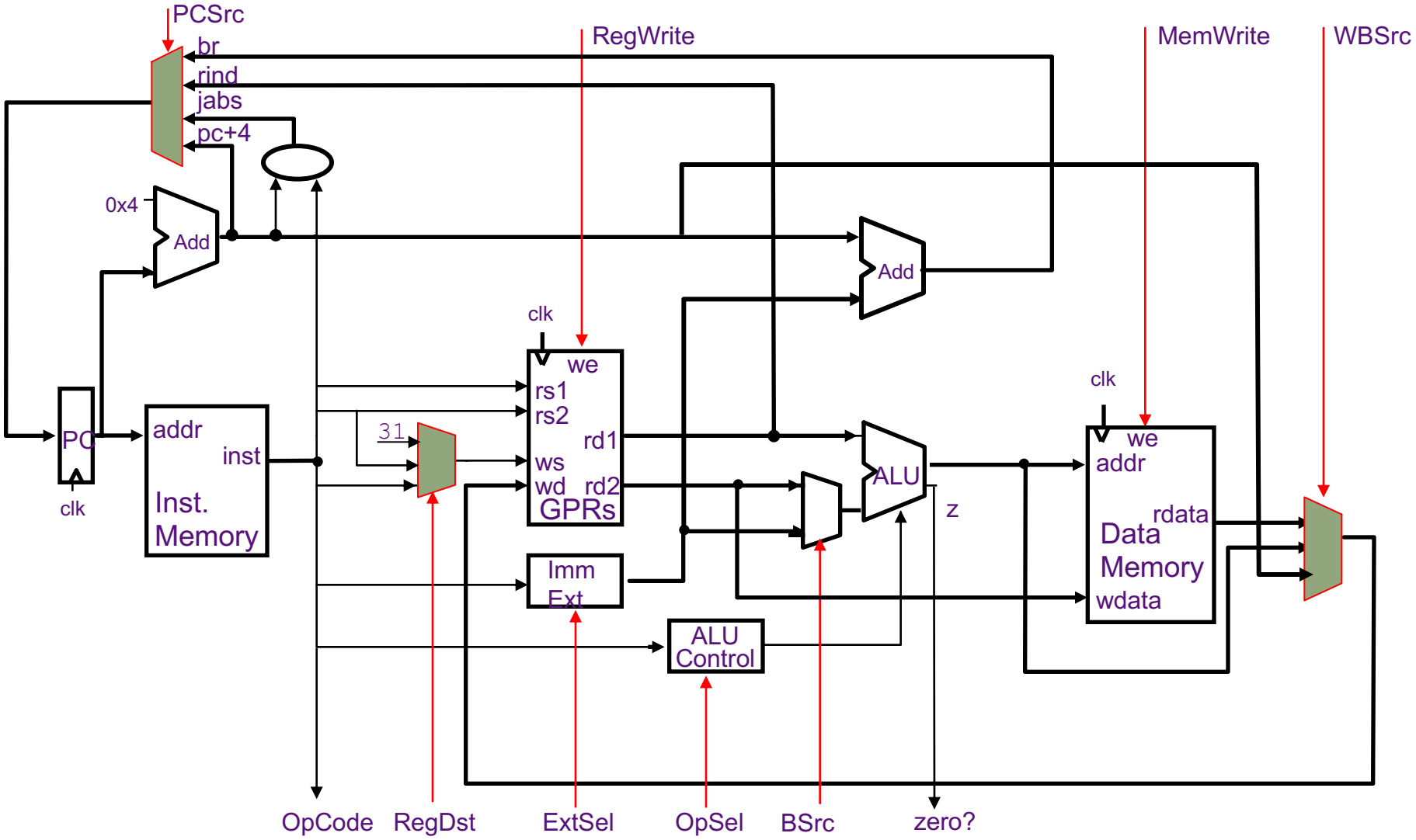
Register-Indirect Jump-&-Link (JALR)



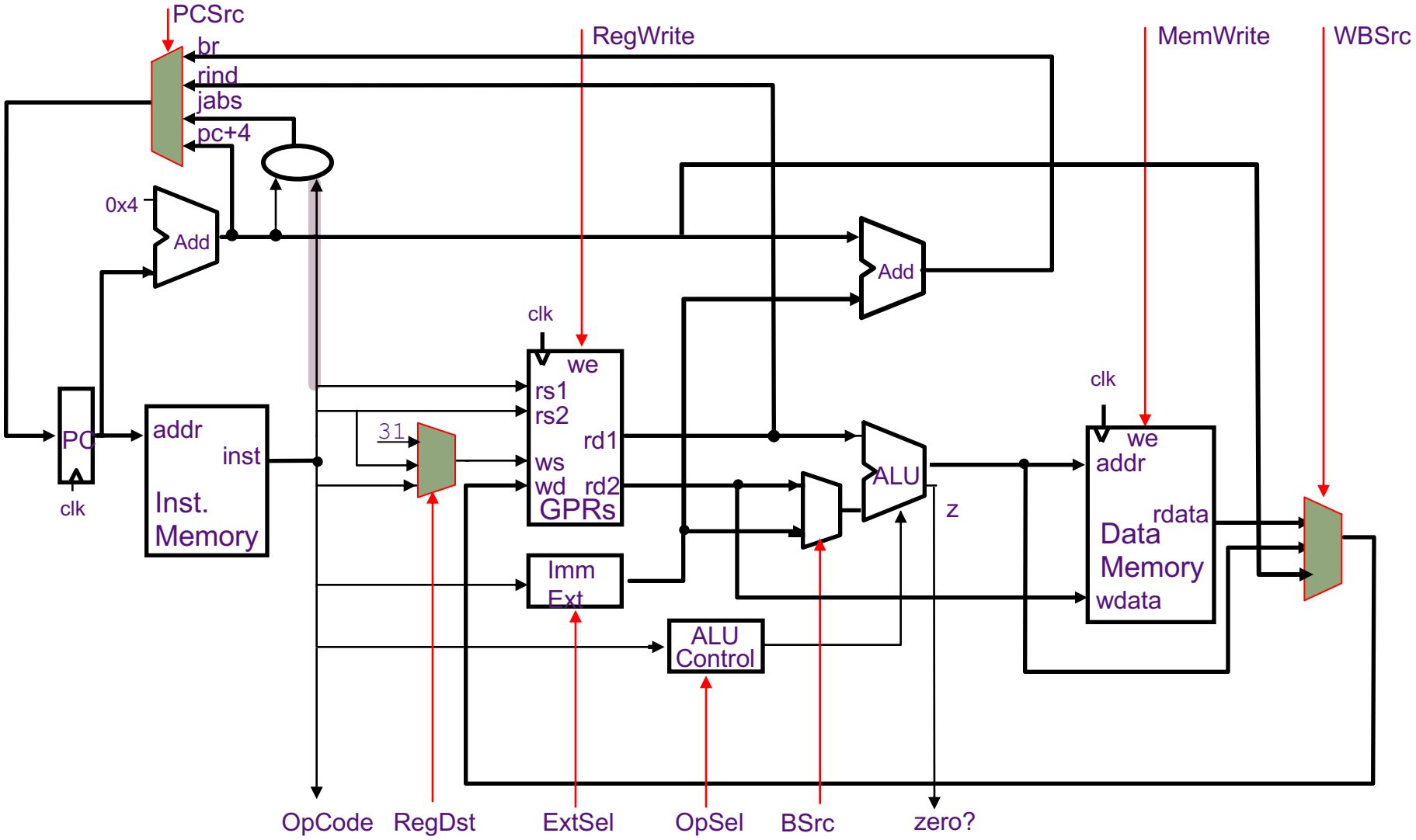
Register-Indirect Jump-&-Link (JALR)



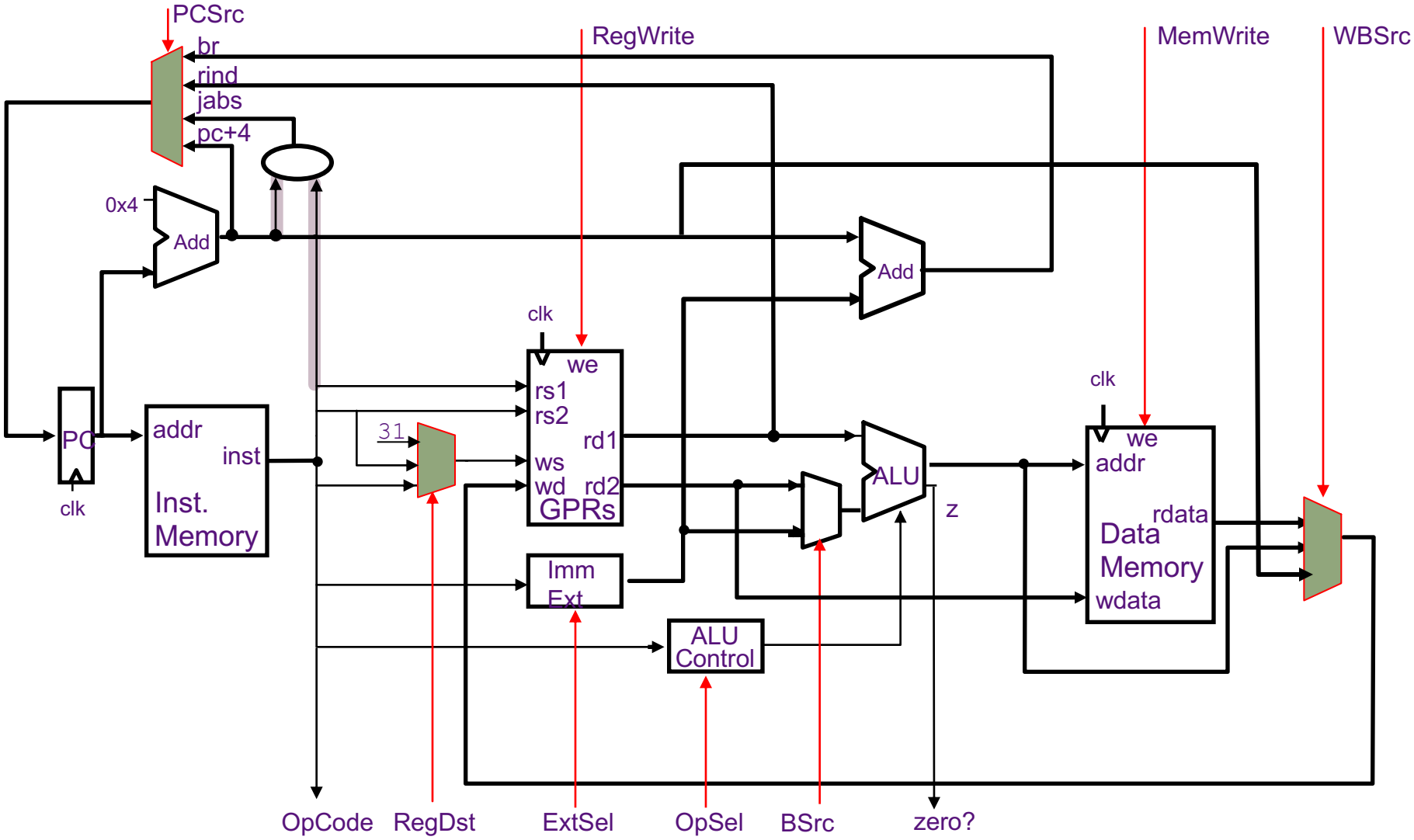
Absolute Jumps (J, JAL)



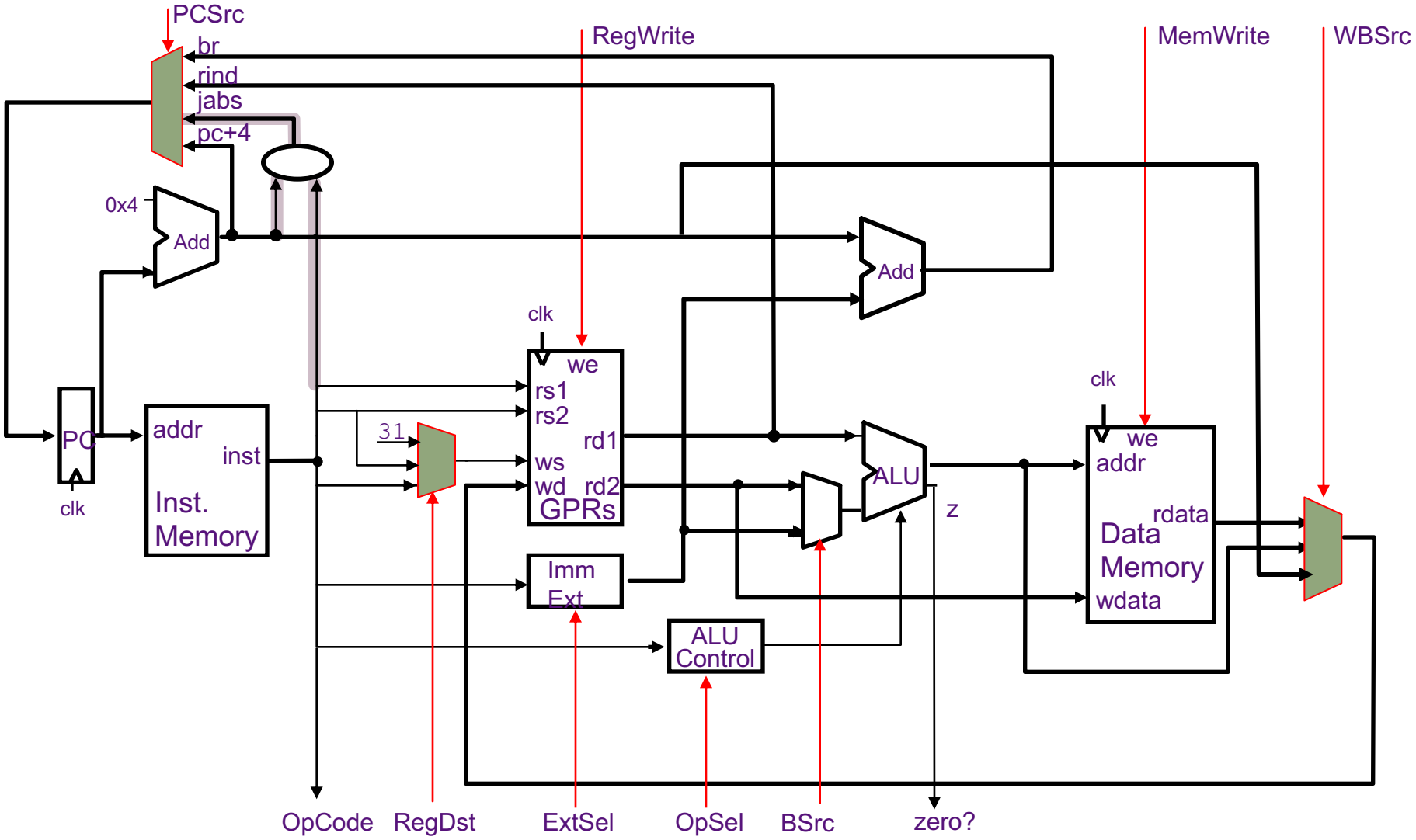
Absolute Jumps (J, JAL)



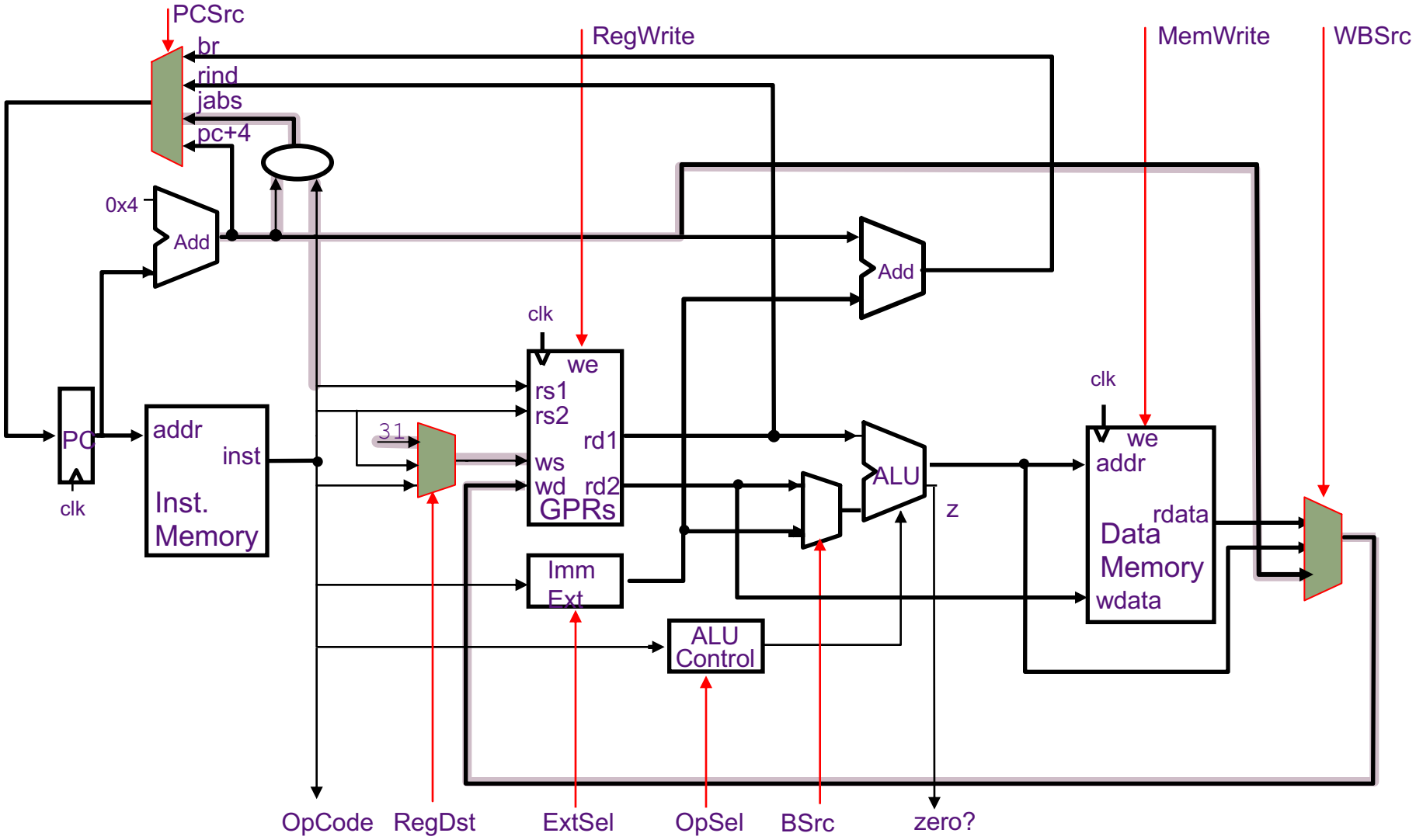
Absolute Jumps (J, JAL)



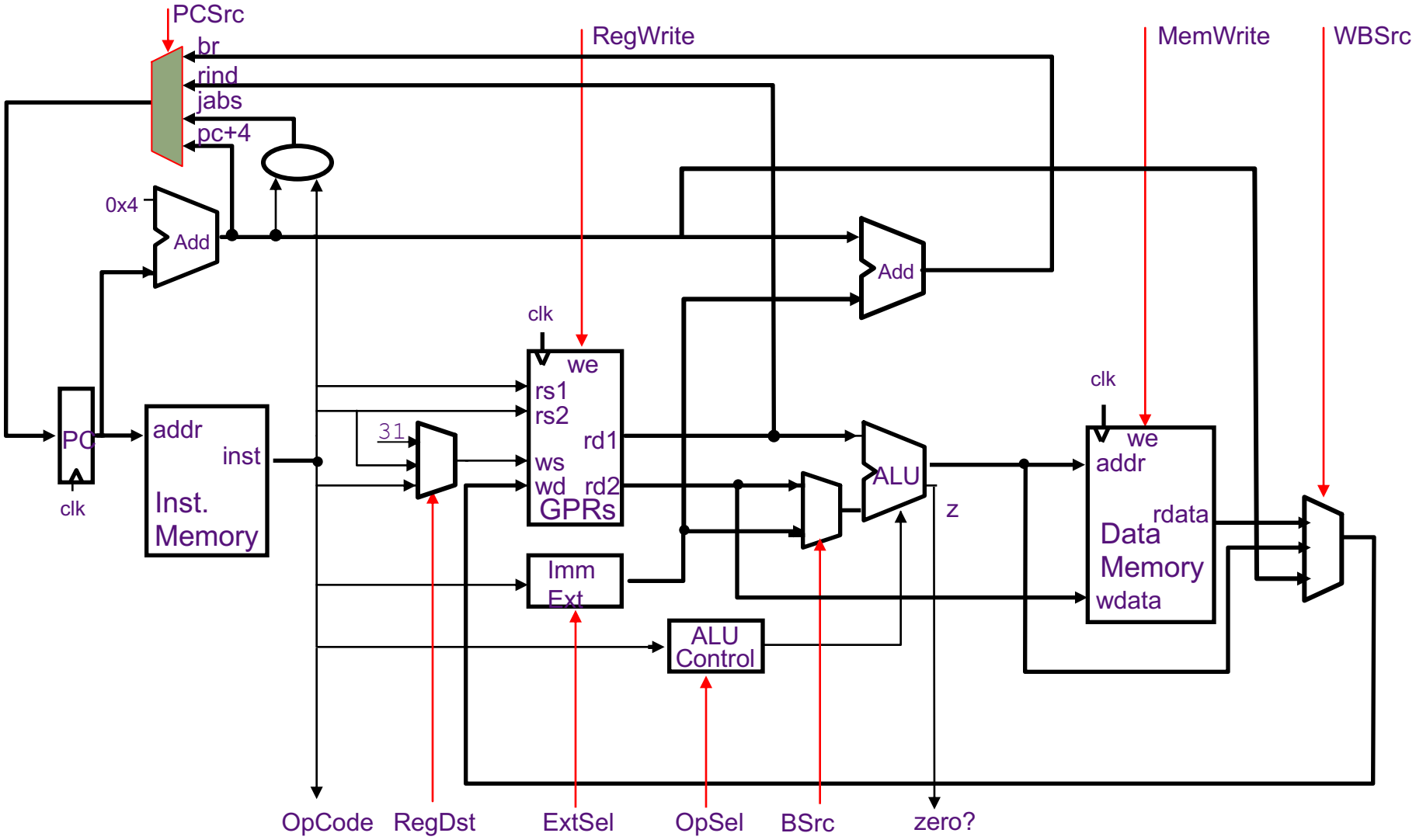
Absolute Jumps (J, JAL)



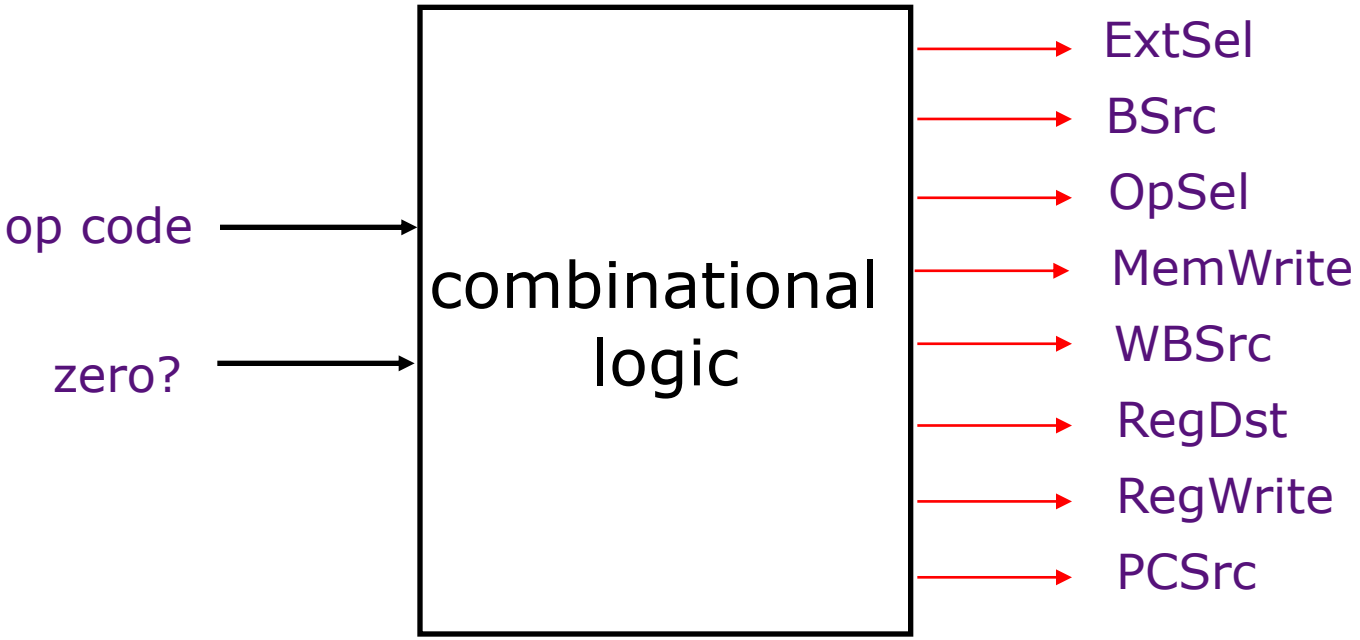
Absolute Jumps (J, JAL)



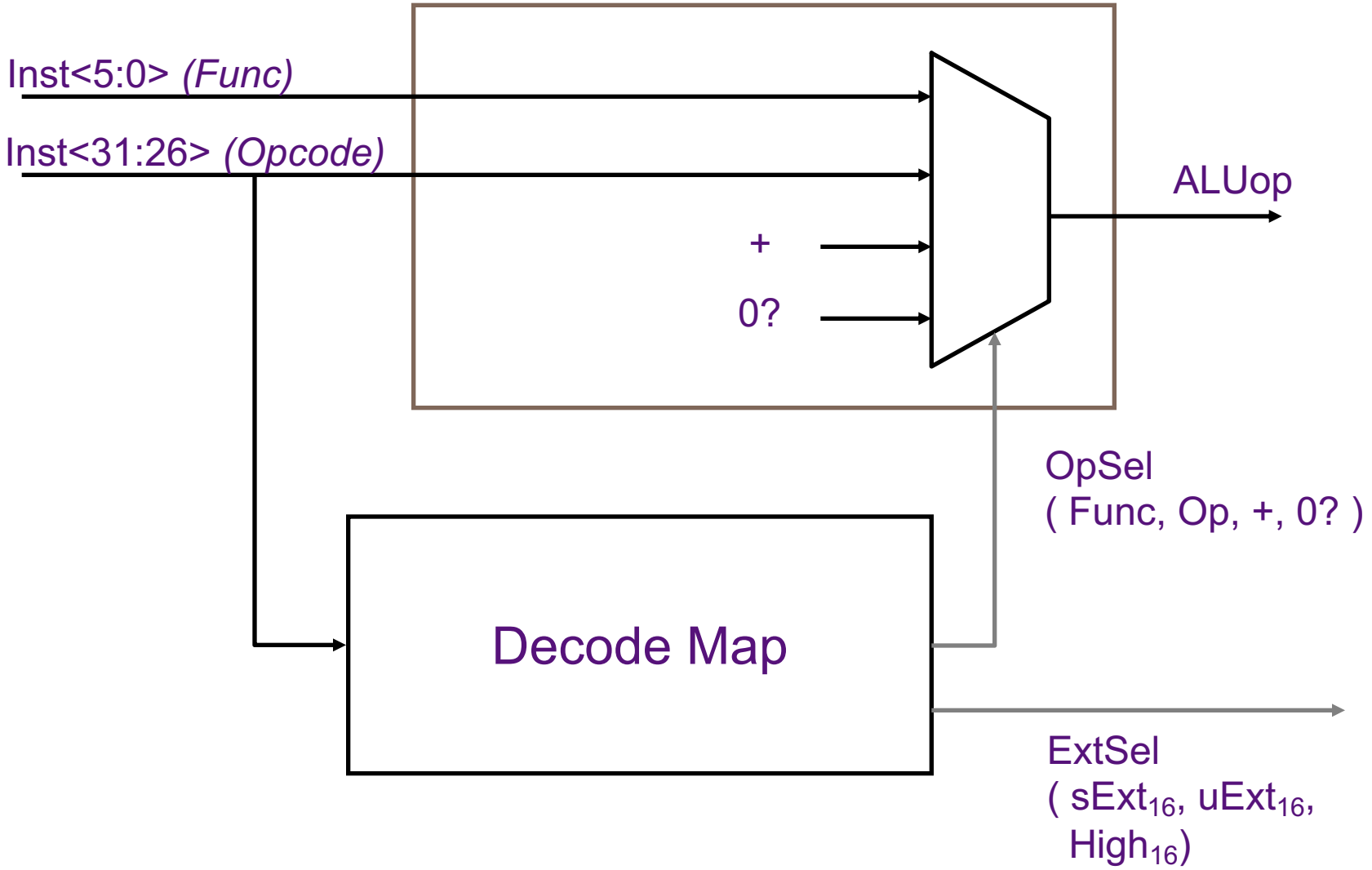
Harvard-Style Datapath for MIPS



Hardwired Control is pure Combinational Logic



ALU Control & Immediate Extension



Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU								
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*							
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg						
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func					
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no				
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no	yes			
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no	yes	ALU		
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no	yes	ALU	rd	
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no	yes	ALU	rd	pc+4
ALUi								
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
$BEQZ_{z=1}$								
J								
JAL								
JR								
JALR								

BSrc = Reg / Imm
RegDst = rt / rd / R31

WBSrc = ALU / Mem / PC
PCSrc = pc+4 / br / rind / jabs

Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no	yes	ALU	rd	pc+4
ALUi	$sExt_{16}$							
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
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ALU	*	Reg	Func	no	yes	ALU	rd	pc+4
ALUi	$sExt_{16}$	Imm						
ALUiu								
LW								
SW								
$BEQZ_{z=0}$								
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SW								
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LW	$sExt_{16}$	Imm	+	no				
SW								
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SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
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SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*						
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LW	$sExt_{16}$	Imm	+	no	yes	Mem	rt	pc+4
SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?					
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SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	
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LW	$sExt_{16}$	Imm	+	no	yes	Mem	rt	pc+4
SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
$BEQZ_{z=1}$								
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LW	$sExt_{16}$	Imm	+	no	yes	Mem	rt	pc+4
SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	
J								
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SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
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SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
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J	*	*	*					
JAL								
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$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	
JAL								
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$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL								
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SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL	*	*	*	no				
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$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL	*	*	*	no	yes			
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$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL	*	*	*	no	yes	PC		
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$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL	*	*	*	no	yes	PC	R31	
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$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL	*	*	*	no	yes	PC	R31	jabs
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Hardwired Control Table

Opcode	ExtSel	BSrc	OpSel	MemW	RegW	WBSrc	RegDst	PCSrc
ALU	*	Reg	Func	no	yes	ALU	rd	pc+4
ALUi	$sExt_{16}$	Imm	Op	no	yes	ALU	rt	pc+4
ALUiu	$uExt_{16}$	Imm	Op	no	yes	ALU	rt	pc+4
LW	$sExt_{16}$	Imm	+	no	yes	Mem	rt	pc+4
SW	$sExt_{16}$	Imm	+	yes	no	*	*	pc+4
$BEQZ_{z=0}$	$sExt_{16}$	*	0?	no	no	*	*	br
$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL	*	*	*	no	yes	PC	R31	jabs
JR	*	*	*					
JALR								

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JAL	*	*	*	no	yes	PC	R31	jabs
JR	*	*	*	no	no	*	*	
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$BEQZ_{z=1}$	$sExt_{16}$	*	0?	no	no	*	*	pc+4
J	*	*	*	no	no	*	*	jabs
JAL	*	*	*	no	yes	PC	R31	jabs
JR	*	*	*	no	no	*	*	rind
JALR	*	*	*	no	yes	PC	R31	rind

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Single-Cycle Hardwired Control:
Harvard architecture

We will assume

- Clock period is sufficiently long for all of the following steps to be "completed":

1. instruction fetch
2. decode and register fetch
3. ALU operation
4. data fetch if required
5. register write-back setup time

$$\Rightarrow\ t_C > t_{IFetch} + t_{RFetch} + t_{ALU} + t_{DMem} + t_{RWB}$$

- At the rising edge of the following clock, the PC, the register file and the memory are updated

Princeton challenge

- What problem arises if instructions and data reside in the same memory?

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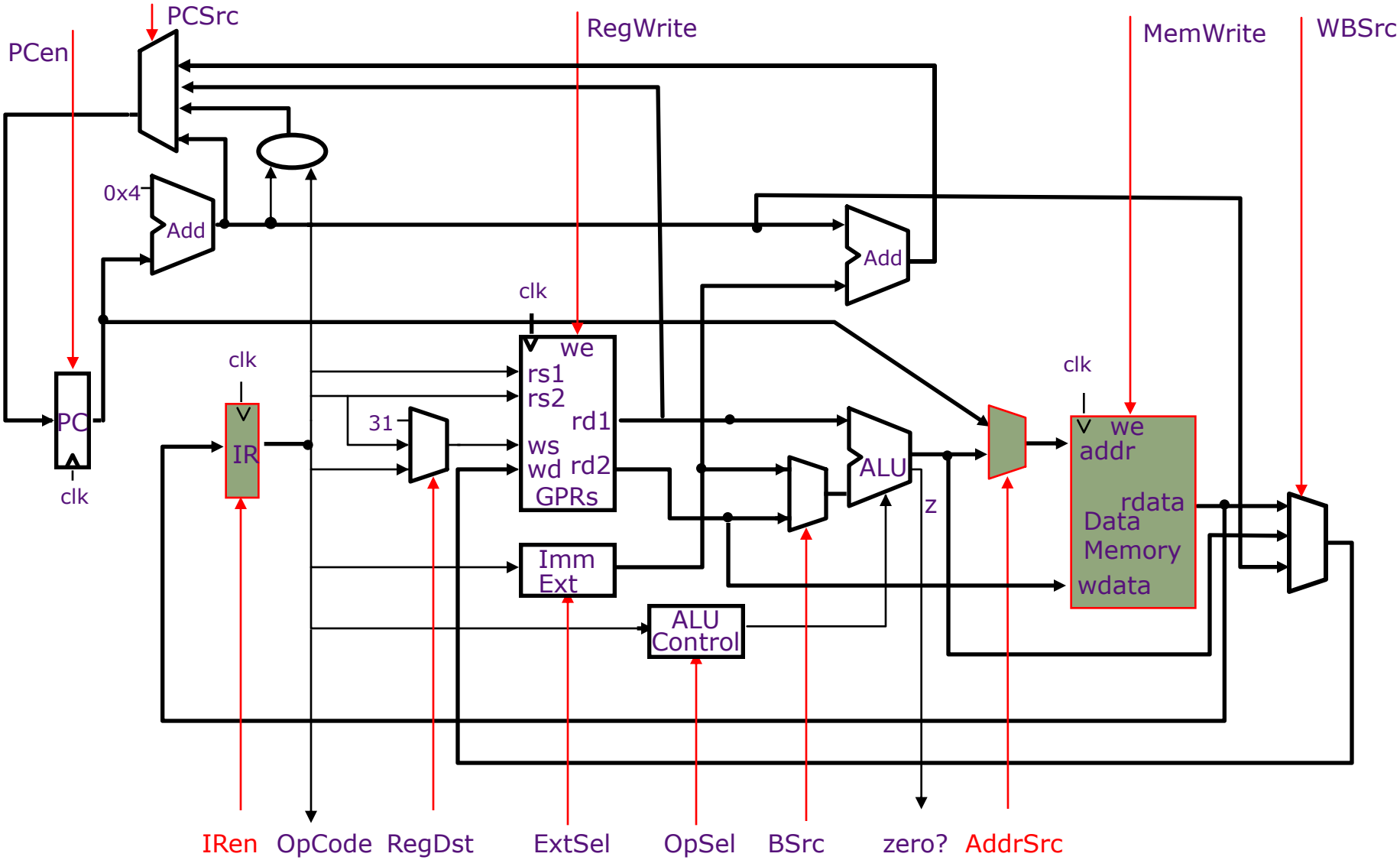
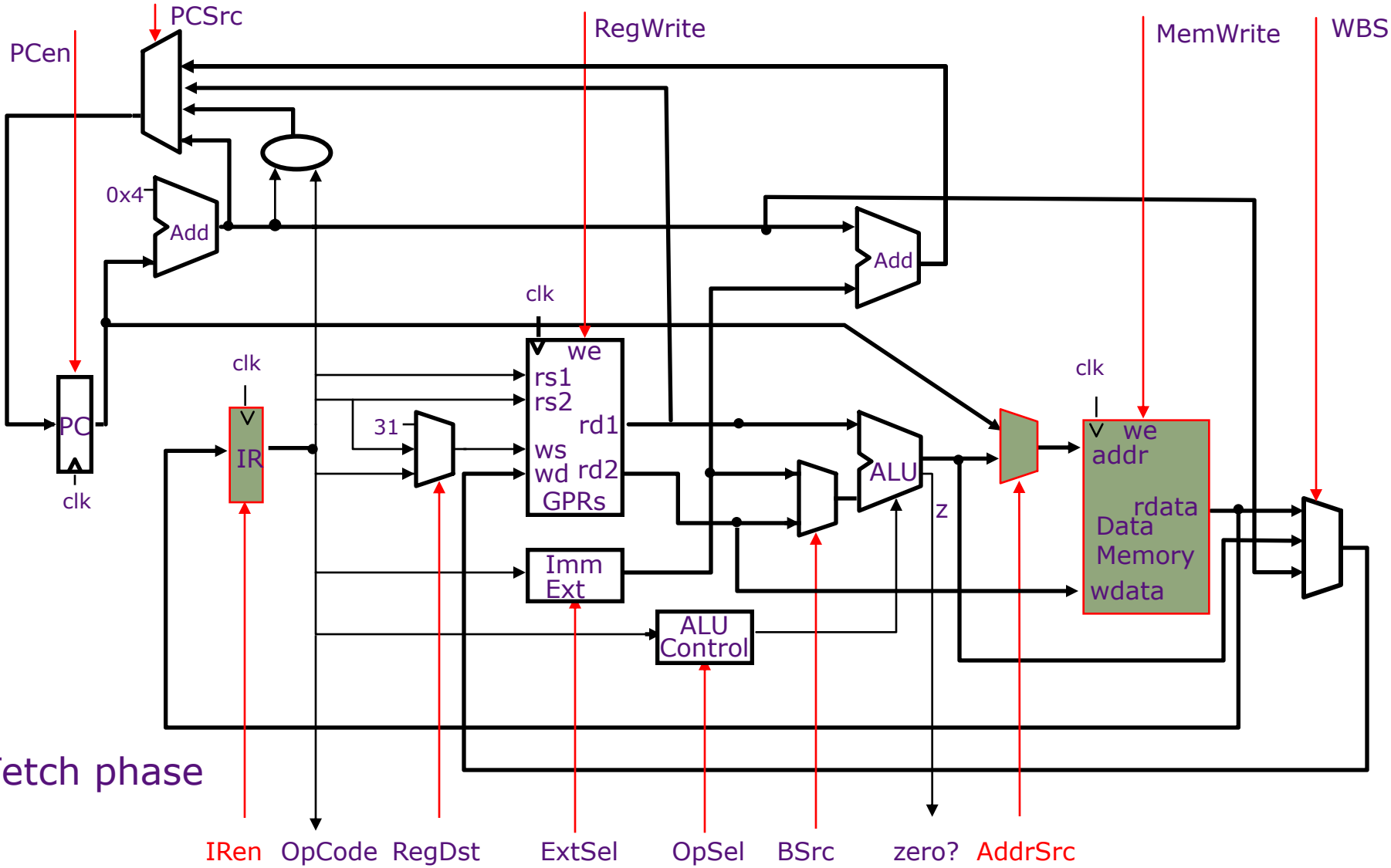
Structural hazard

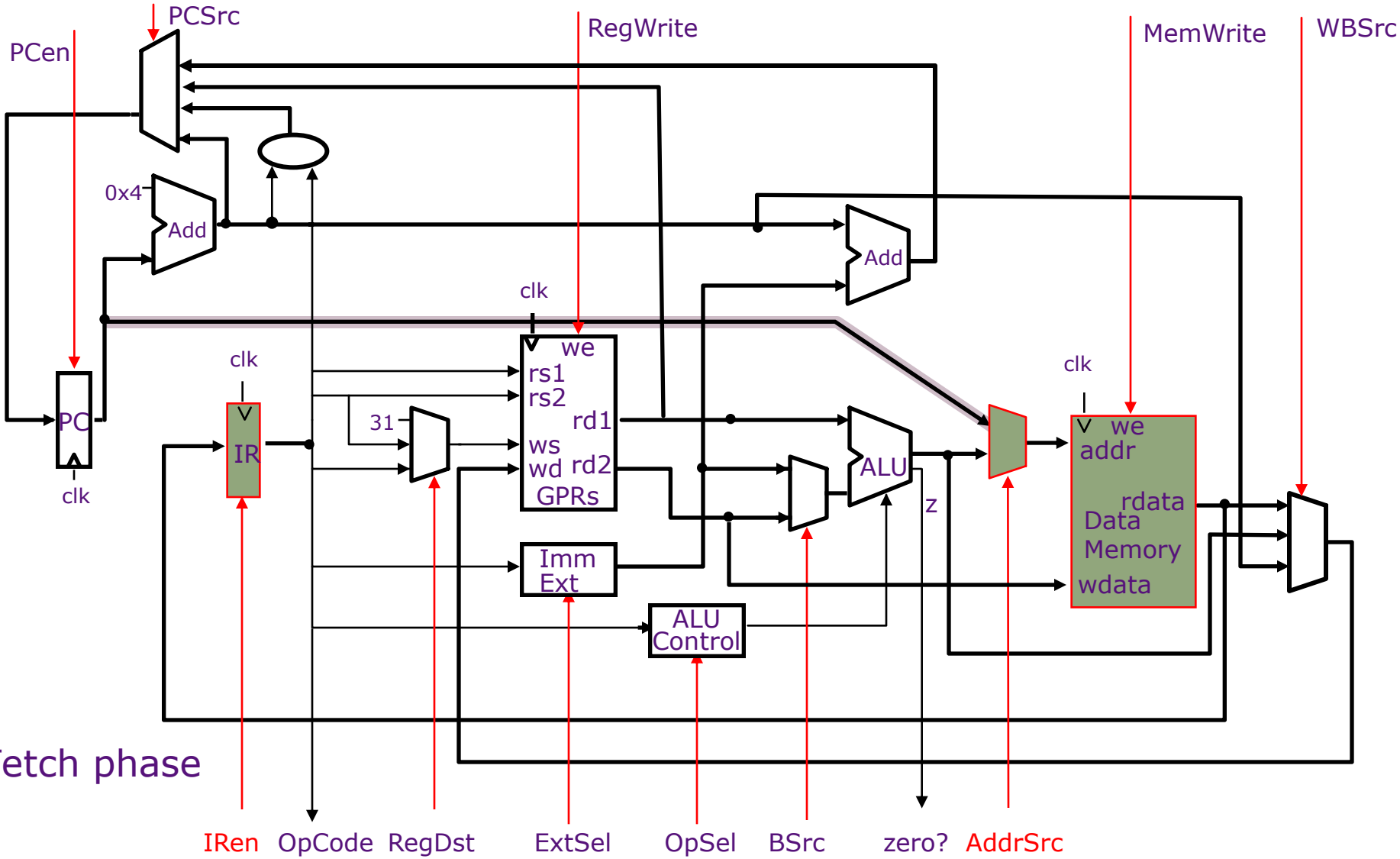
Princeton Microarchitecture
Datapath & Control



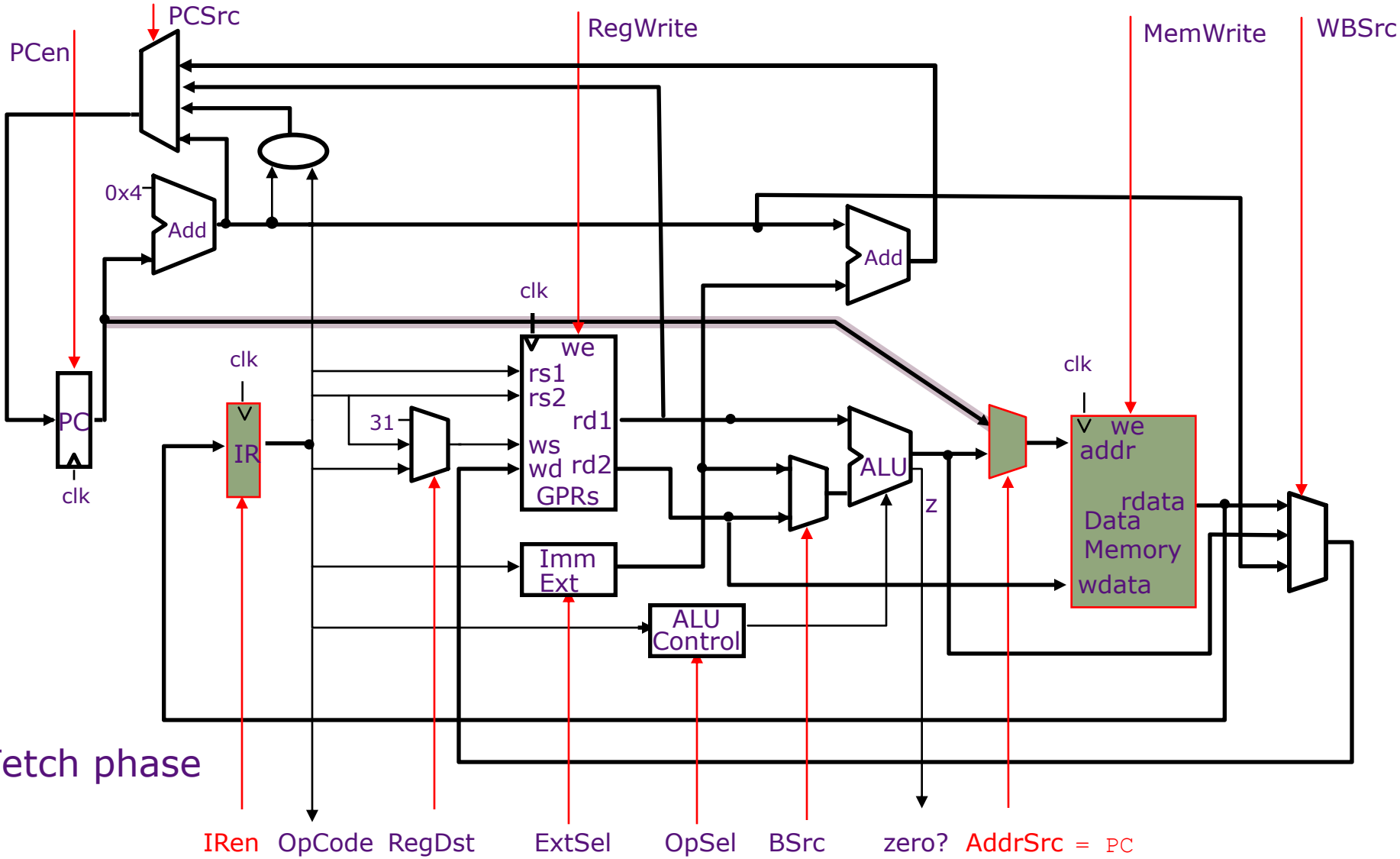
Princeton Microarchitecture
Datapath & Control



Princeton Microarchitecture
Datapath & Control



Princeton Microarchitecture
Datapath & Control



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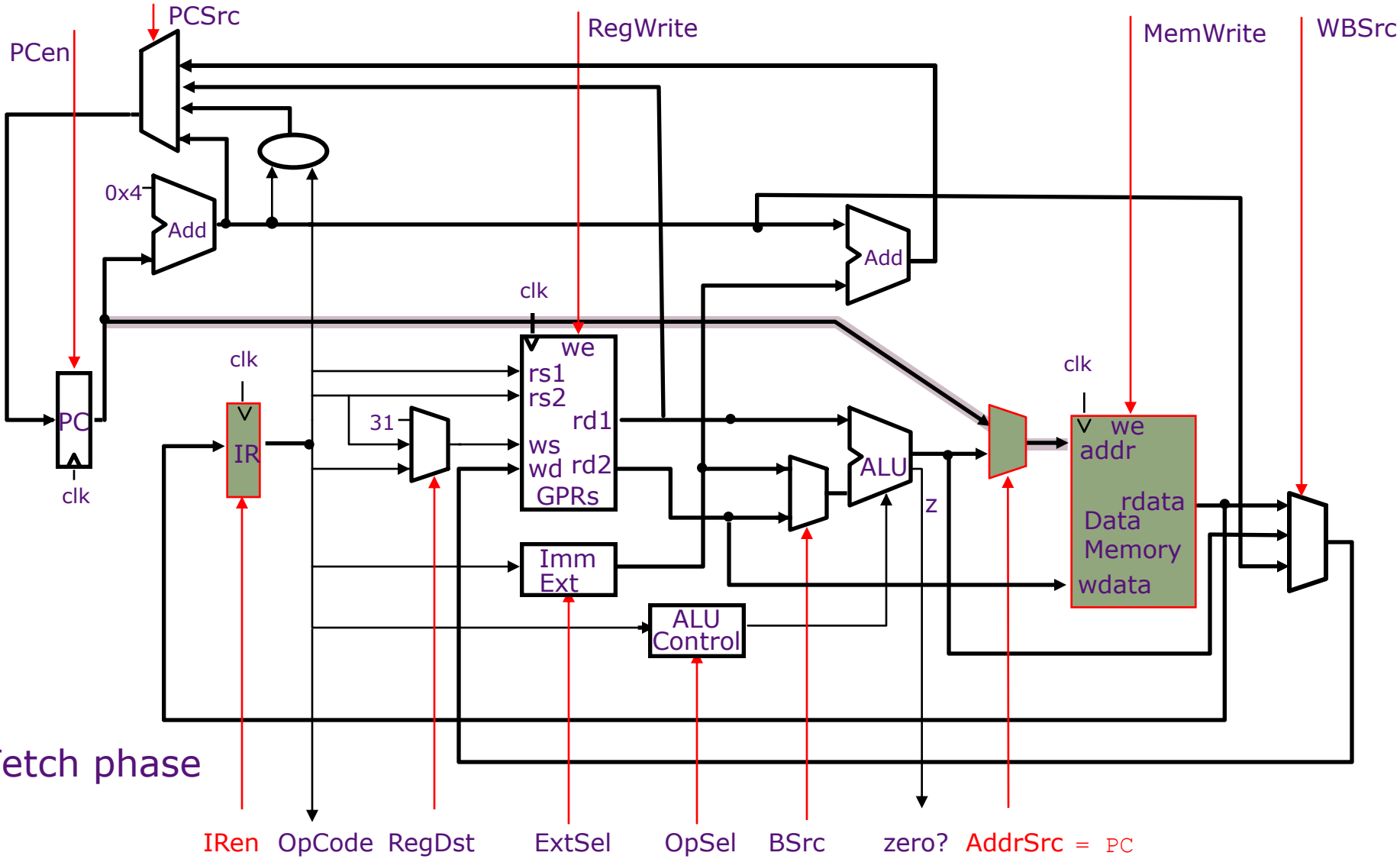
Datapath & Control



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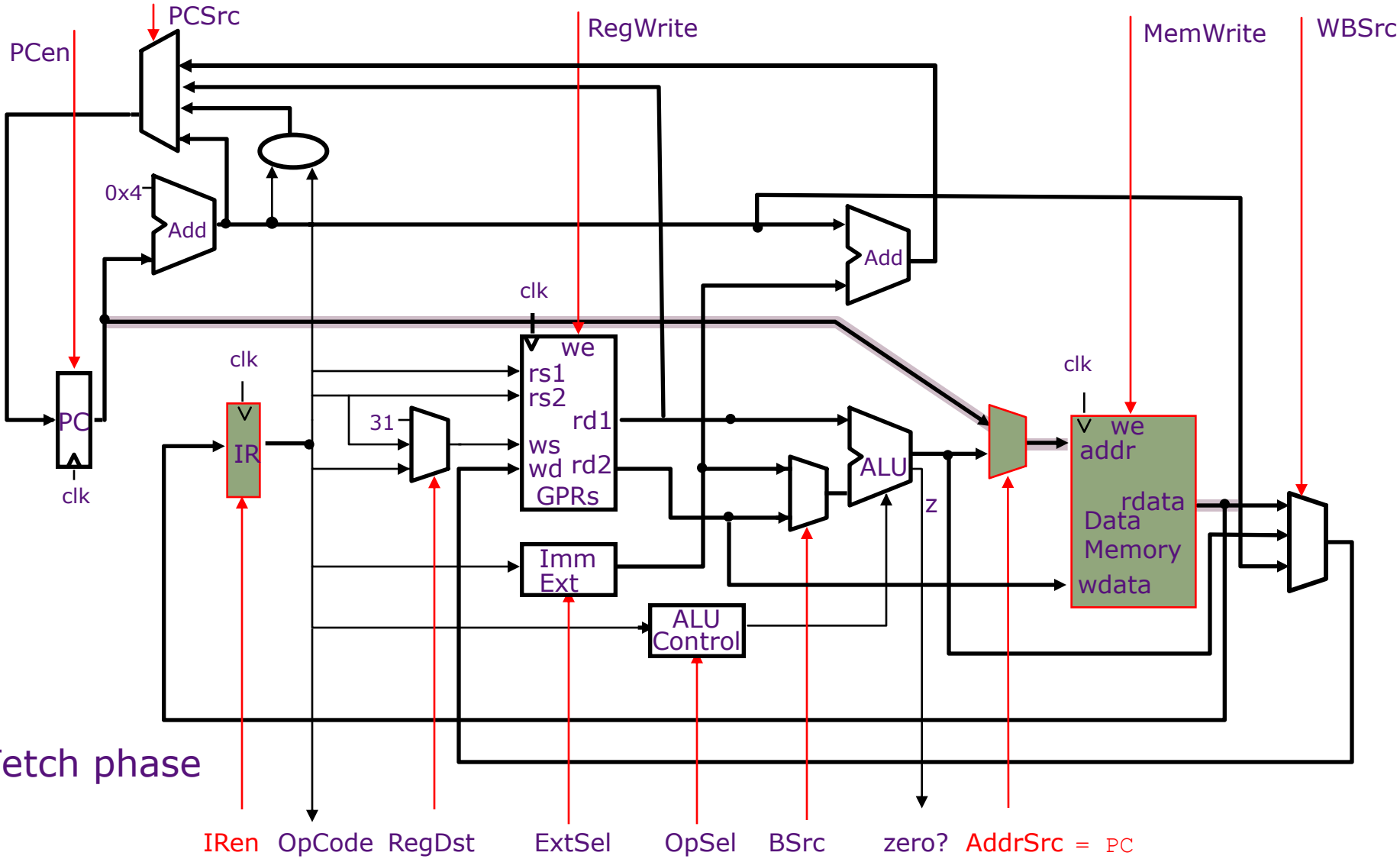
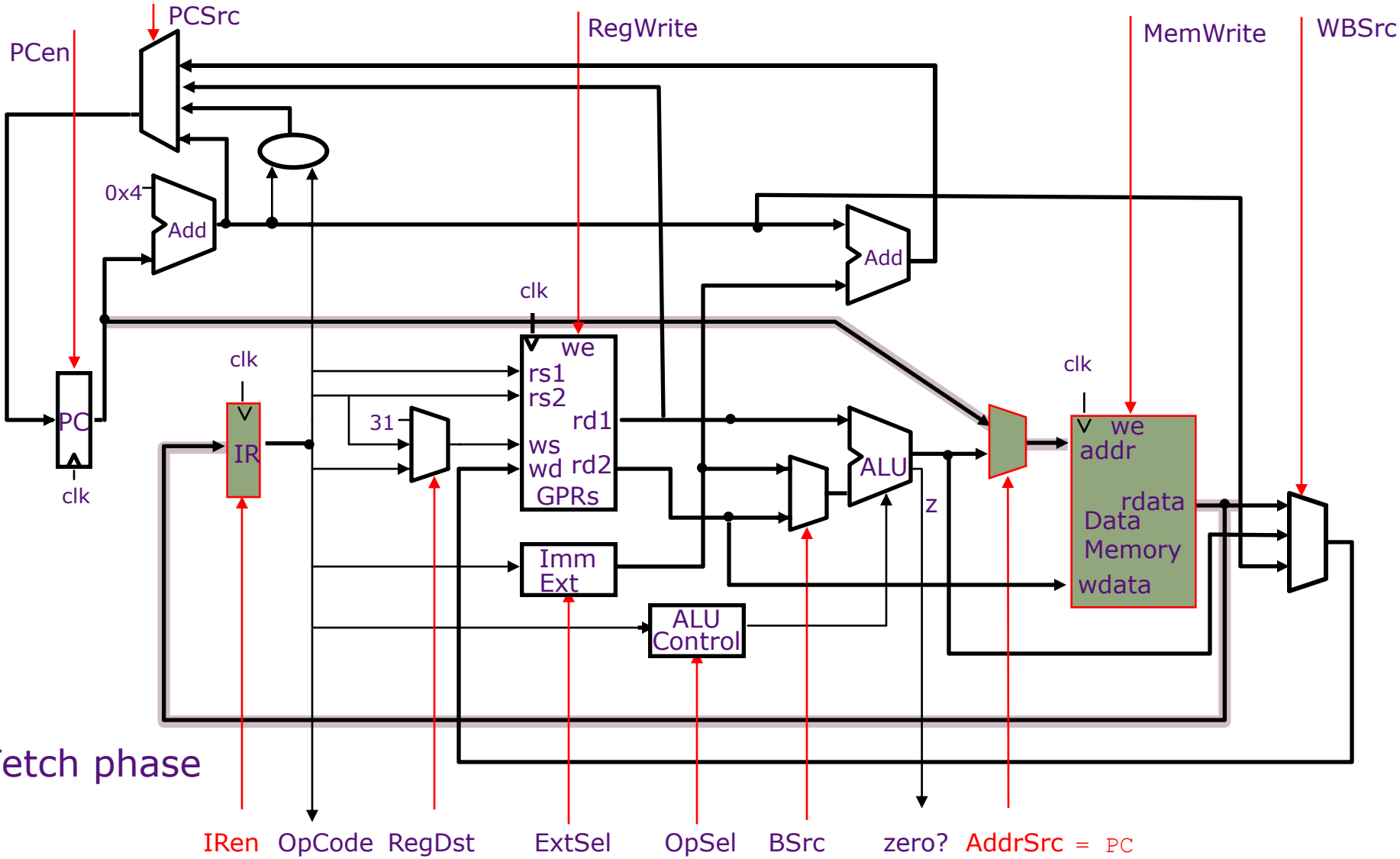


Princeton Microarchitecture
Datapath & Control



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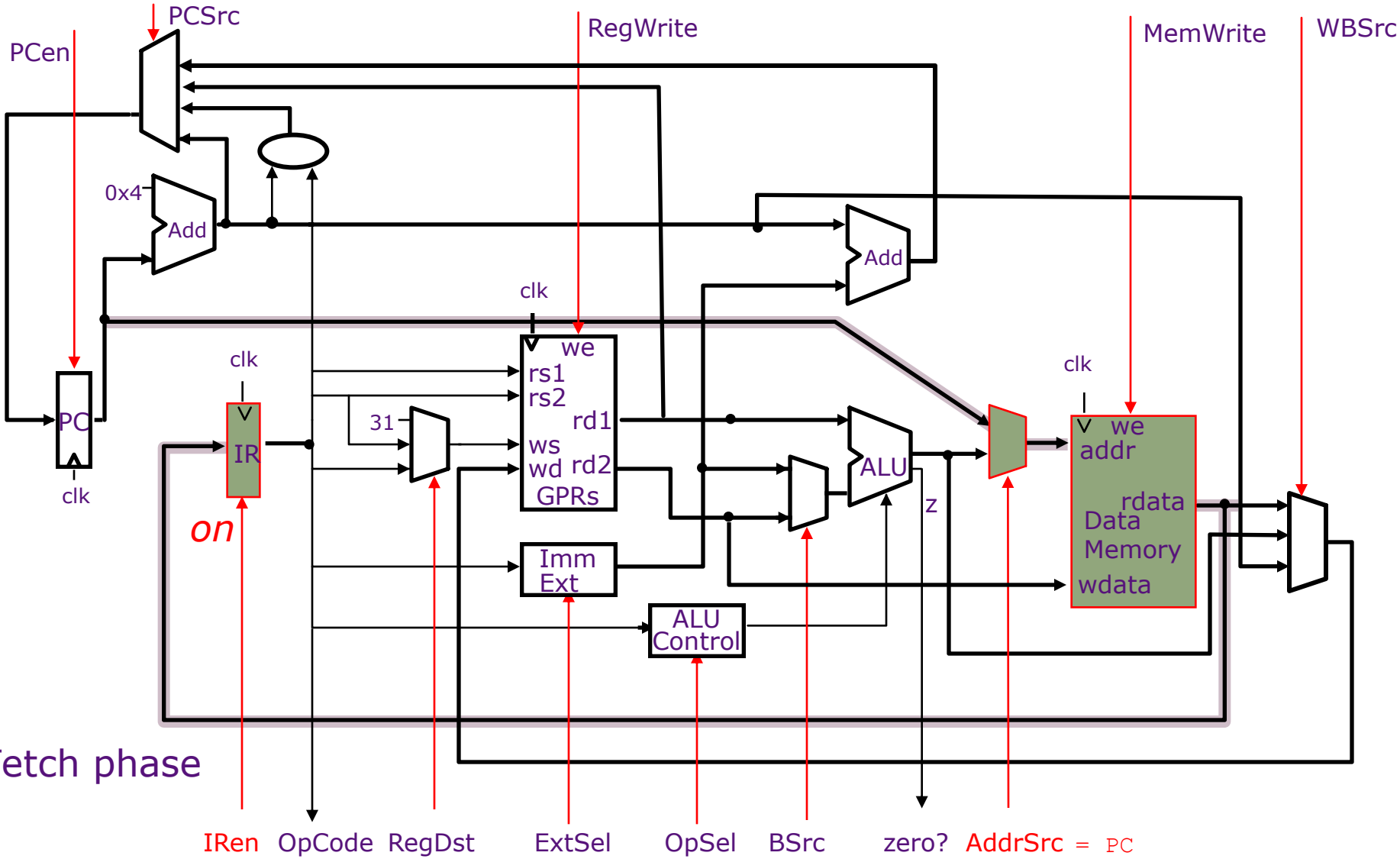
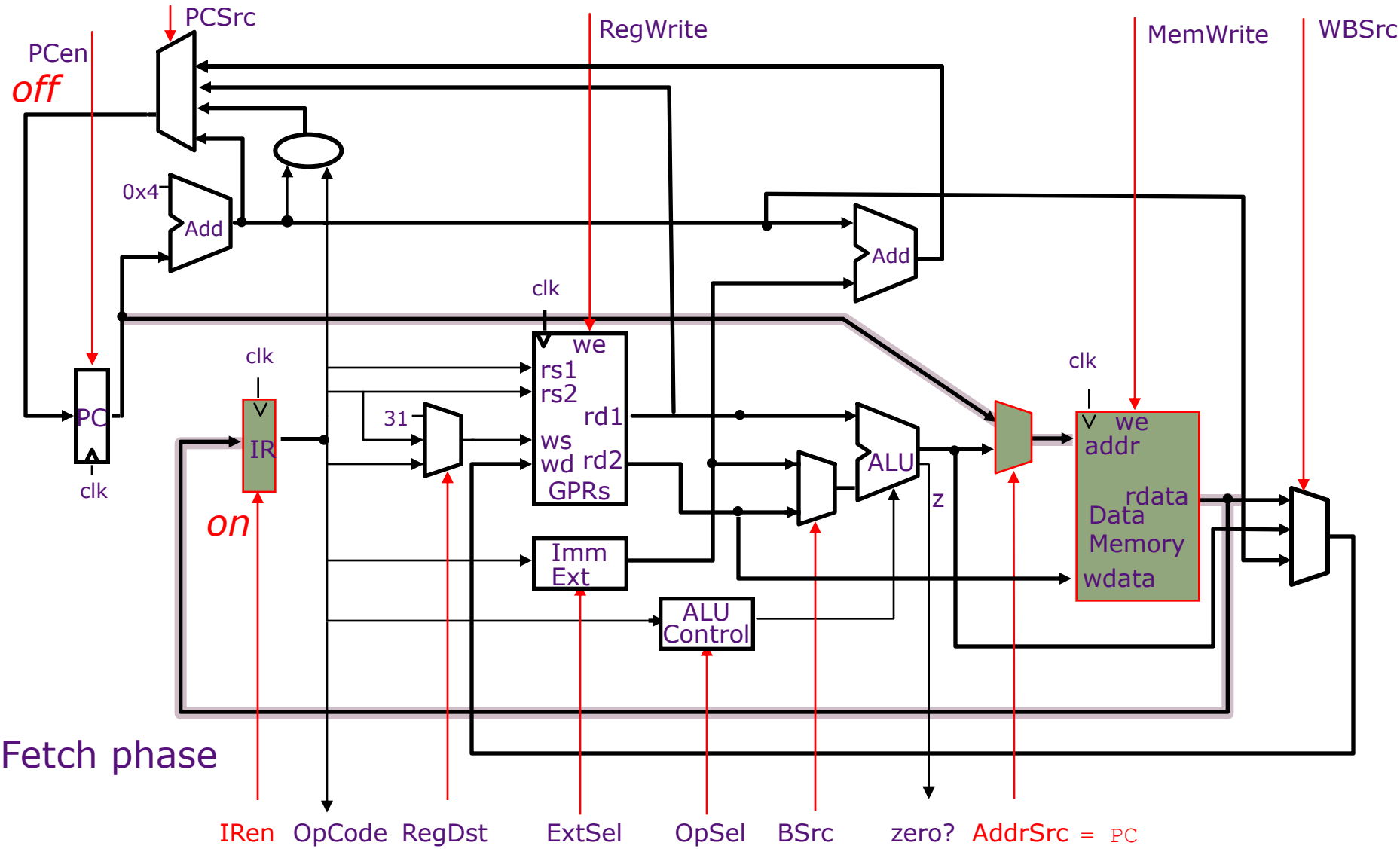


Princeton Microarchitecture
Datapath & Control



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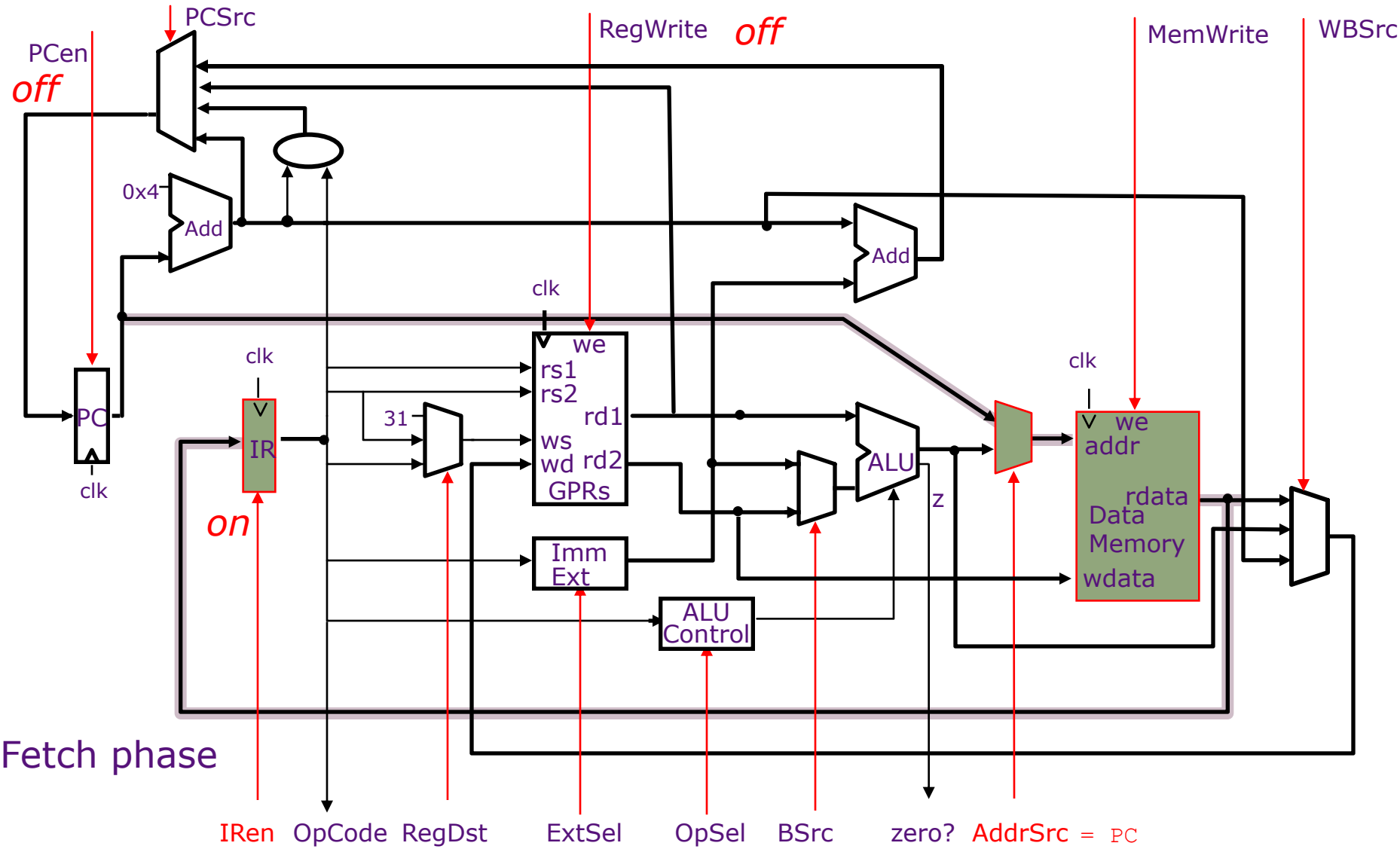

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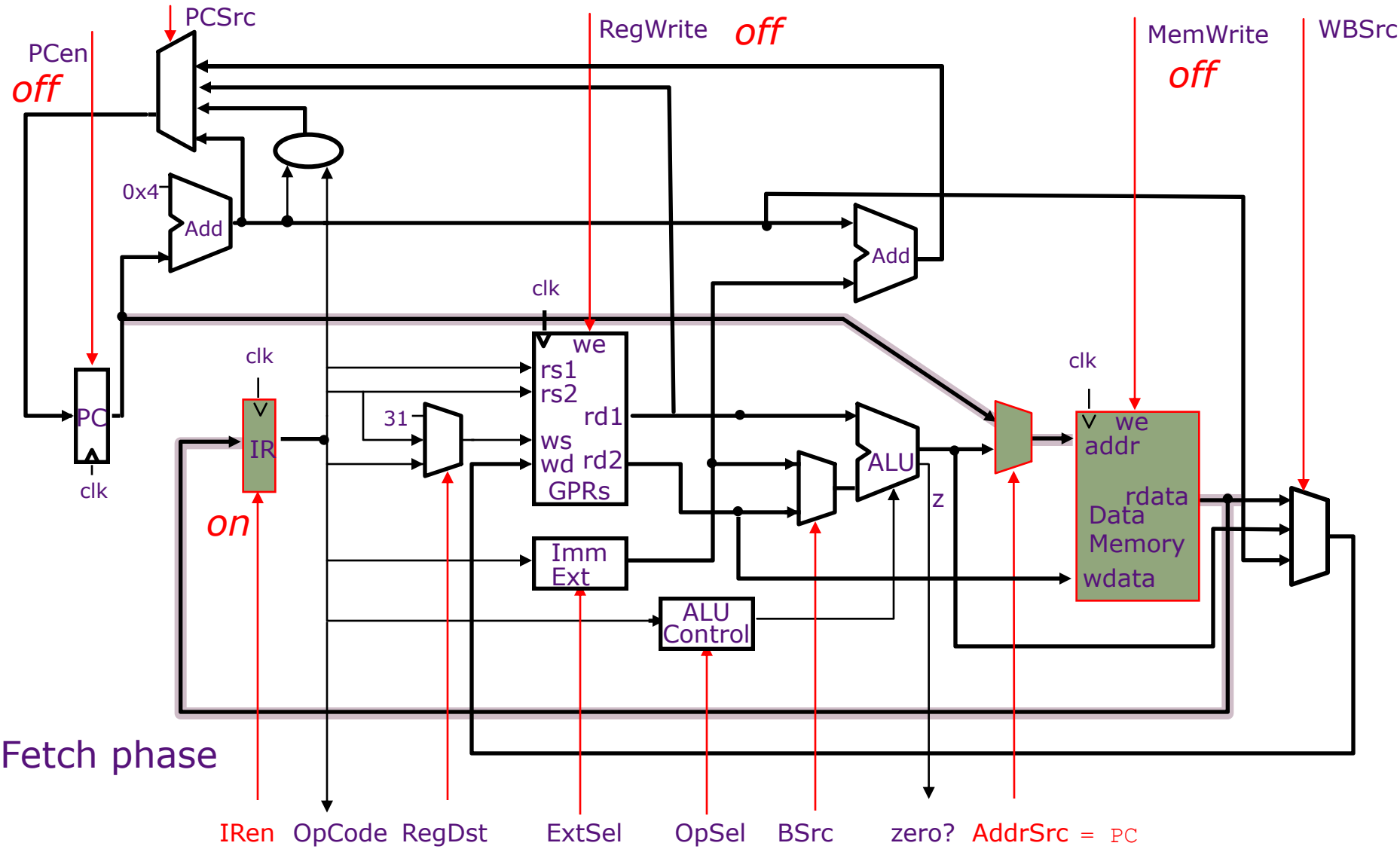
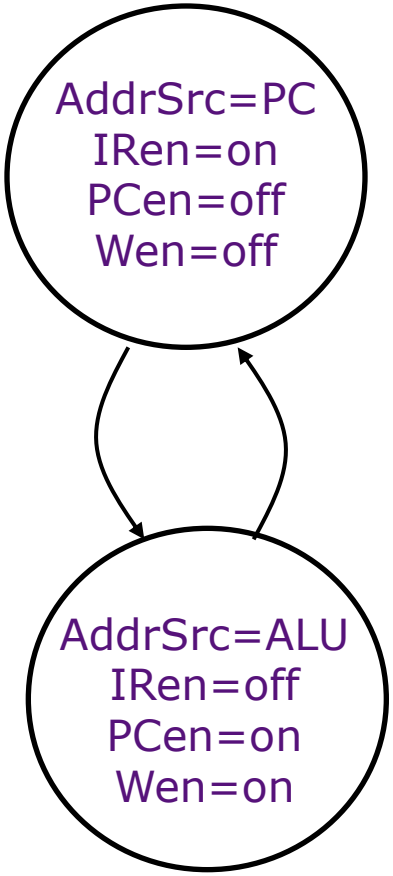


Two-State Controller:
Princeton Architecture

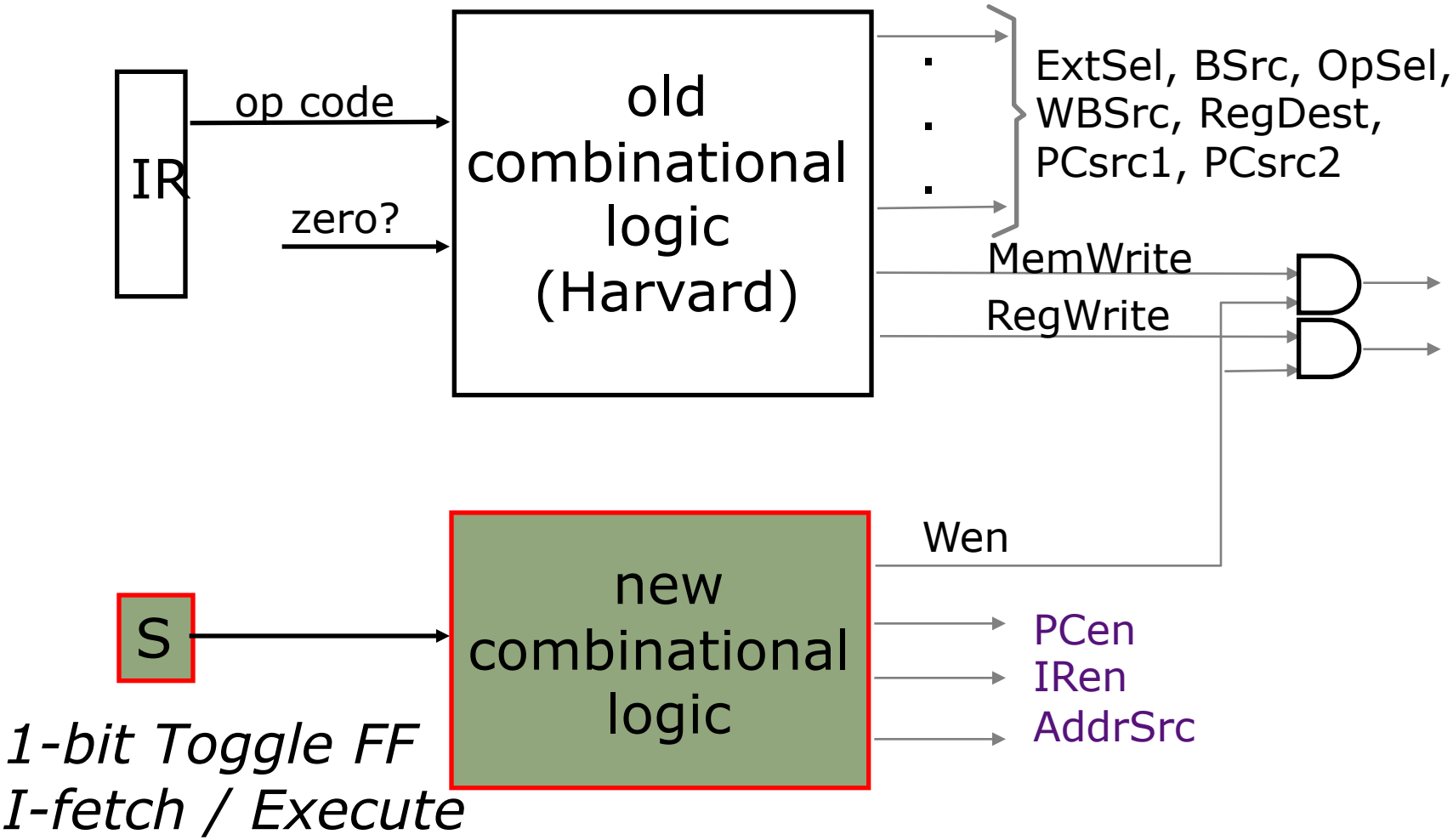
fetch phase

execute phase



A flipflop can be used to remember the phase

Hardwired Controller:
Princeton Architecture



Clock Rate vs CPI

$t_{C\text{-}Princeton} > \max \{t_M , t_{RF} + t_{ALU} + t_M + t_{WB}\}$

$t_{C\text{-}Princeton} > t_{RF} + t_{ALU} + t_M + t_{WB}$

$t_{C\text{-}Harvard} > t_M + t_{RF} + t_{ALU} + t_M + t_{WB}$

Suppose $t_M >> t_{RF} + t_{ALU} + t_{WB}$

$t_{C\text{-}Princeton} = 0.5 * t_{C\text{-}Harvard}$

$CPI_{Princeton} = 2$

$CPI_{Harvard} = 1$

No difference in performance!

Is it possible to design a controller for the Princeton architecture with CPI < 2 ?

CPI = Clock cycles Per Instruction

Stay tuned!