Influence of Technology and Software on Instruction Sets:
Up to the dawn of IBM 360

Daniel Sanchez
Computer Science and Artificial Intelligence Laboratory
M.I.T.

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http://www.csg.csail.mit.edu/6.823
Administrivia

• We’ve moved!
  – Lectures in 2-105
  – Recitations and quizzes in 37-212

• Second TA: Mark Seifter

• Self-assessment test due today
• Lab 0 due Wed
And then there was IBM 701

IBM 701 -- 30 machines were sold in 1953-54

IBM 650 -- a cheaper, drum based machine, more than 120 were sold in 1954 and there were orders for 750 more!

Users stopped building their own machines.

Why was IBM late getting into computers?

IBM was making too much money!
Even without computers, IBM revenues were doubling every 4 to 5 years in 40’s and 50’s.
Computers in mid 50’s

- Hardware was expensive
- Stores were small (1000 words)
  \[\Rightarrow\] No resident system-software!
- Memory access time was 10 to 50 times slower than the processor cycle
  \[\Rightarrow\] Instruction execution time was totally dominated by the memory reference time.
- The ability to design complex control circuits to execute an instruction was the central design concern as opposed to the speed of decoding or an ALU operation
- Programmer’s view of the machine was inseparable from the actual hardware implementation
Accumulator-based computing

- **Single Accumulator**
  - Calculator design carried over to computers

Why?

Registers expensive
## The Earliest Instruction Sets

**Burks, Goldstein & von Neumann ~1946**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOAD x</td>
<td></td>
<td>AC ← M[x]</td>
</tr>
<tr>
<td>STORE x</td>
<td></td>
<td>M[x] ← (AC)</td>
</tr>
<tr>
<td>ADD x</td>
<td></td>
<td>AC ← (AC) + M[x]</td>
</tr>
<tr>
<td>SUB x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MUL x</td>
<td></td>
<td>Involved a quotient register</td>
</tr>
<tr>
<td>DIV x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHIFT LEFT</td>
<td></td>
<td>AC ← 2 × (AC)</td>
</tr>
<tr>
<td>SHIFT RIGHT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>JUMP x</td>
<td></td>
<td>PC ← x</td>
</tr>
<tr>
<td>JGE x</td>
<td></td>
<td>if (AC) ≥ 0 then PC ← x</td>
</tr>
<tr>
<td>LOAD ADR x</td>
<td></td>
<td>AC ← Extract address field(M[x])</td>
</tr>
<tr>
<td>STORE ADR x</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Typically less than 2 dozen instructions!*
Programming: Single Accumulator Machine

Cᵢ ← Aᵢ + Bᵢ, 1 ≤ i ≤ n

<table>
<thead>
<tr>
<th>LOOP</th>
<th>LOAD</th>
<th>N</th>
</tr>
</thead>
<tbody>
<tr>
<td>JGE</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td>ADD</td>
<td>ONE</td>
<td></td>
</tr>
<tr>
<td>STORE</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>F1</td>
<td>LOAD</td>
<td>A</td>
</tr>
<tr>
<td>F2</td>
<td>ADD</td>
<td>B</td>
</tr>
<tr>
<td>F3</td>
<td>STORE</td>
<td>C</td>
</tr>
<tr>
<td>JUMP</td>
<td>LOOP</td>
<td></td>
</tr>
<tr>
<td>DONE</td>
<td>HLT</td>
<td></td>
</tr>
</tbody>
</table>

Problem?

How to modify the addresses A, B and C?

How to modify the addresses A, B and C?
## Self-Modifying Code

<table>
<thead>
<tr>
<th>LOOP</th>
<th>LOAD</th>
<th>N</th>
<th>JGE</th>
<th>DONE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADD</td>
<td></td>
<td></td>
<td>ONE</td>
</tr>
<tr>
<td></td>
<td>STORE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F1</td>
<td>LOAD</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F2</td>
<td>ADD</td>
<td>B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F3</td>
<td>STORE</td>
<td>C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Each iteration involves the following:

- **total instruction fetches**: 17
- **book-keeping instruction fetches**: 14
- **operand fetches**: 10
- **stores**: 5

Most of the executed instructions are for book-keeping!

C\_i \leftarrow A\_i + B\_i, \ 1 \leq i \leq n

modify the program for the next iteration

In addition to the code:

<table>
<thead>
<tr>
<th>LOOP</th>
<th>LOAD ADR</th>
<th>F1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADD</td>
<td>ONE</td>
</tr>
<tr>
<td></td>
<td>STORE ADR</td>
<td>F1</td>
</tr>
<tr>
<td></td>
<td>LOAD ADR</td>
<td>F2</td>
</tr>
<tr>
<td></td>
<td>ADD</td>
<td>ONE</td>
</tr>
<tr>
<td></td>
<td>STORE ADR</td>
<td>F2</td>
</tr>
<tr>
<td></td>
<td>LOAD ADR</td>
<td>F3</td>
</tr>
<tr>
<td></td>
<td>ADD</td>
<td>ONE</td>
</tr>
<tr>
<td></td>
<td>STORE ADR</td>
<td>F3</td>
</tr>
<tr>
<td></td>
<td>JUMP</td>
<td>LOOP</td>
</tr>
<tr>
<td>DONE</td>
<td>HLT</td>
<td></td>
</tr>
</tbody>
</table>
Processor-Memory Bottleneck: Early Solutions

- **Indexing capability**
  - to reduce book keeping instructions

- **Fast local storage in the processor**
  - 8-16 registers as opposed to one accumulator
  - to save on loads/stores

- **Complex instructions**
  - to reduce instruction fetches

- **Compact instructions**
  - implicit address bits for operands
  - to reduce instruction fetch cost
Index Registers

Tom Kilburn, Manchester University, mid 50’s

One or more specialized registers to simplify address calculation

Modify existing instructions

LOAD x, IX AC ← M[x + (IX)]
ADD x, IX AC ← (AC) + M[x + (IX)]
...

Add new instructions to manipulate index registers

JZi x, IX if (IX)=0 then PC ← x
else IX ← (IX) + 1
LOADi x, IX IX ← M[x] (truncated to fit IX)
...

Index registers have accumulator-like characteristics
Using Index Registers

\[ C_i \leftarrow A_i + B_i, \quad 1 \leq i \leq n \]

- **Program does not modify itself**
- **Efficiency has improved dramatically (ops / iter)**
  
  \[
  \begin{array}{ll}
  \text{instruction fetch} & 5 (2) \quad 17 (14) \\
  \text{operand fetch} & 2 \quad 10 (8) \\
  \text{store} & 1 \quad 5 (4)
  \end{array}
  \]
- **Costs?**
  - Complex control
  - Index register computations (ALU-like circuitry)
  - 1 to 2 bits longer Instructions
Operations on Index Registers

To increment index register by k

\[ \text{AC} \leftarrow (\text{IX}) \]
\[ \text{AC} \leftarrow (\text{AC}) + k \]
\[ \text{IX} \leftarrow (\text{AC}) \]

new instruction

also the AC must be saved and restored

It may be better to increment IX directly

\[ \text{INCI} \quad k, \text{IX} \quad \text{IX} \leftarrow (\text{IX}) + k \]

More instructions to manipulate index register

\[ \text{STOREi} \quad x, \text{IX} \quad M[x] \leftarrow (\text{IX}) \] (extended to fit a word)

... 

IX begins to look like an accumulator

⇒ several index registers

several accumulators

⇒ General Purpose Registers
Support for Subroutine Calls

A special *subroutine jump instruction*

A: JSR F

M[F] ← A + 1 and jump to F + 1

Main Program

<table>
<thead>
<tr>
<th>call F</th>
<th>a1</th>
<th>a2</th>
<th>.</th>
<th>.</th>
</tr>
</thead>
<tbody>
<tr>
<td>call F</td>
<td>b1</td>
<td>b2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Subroutine F

. . .

return
Indirect Addressing and Subroutine Calls

**Indirect addressing**

LOAD (x) means AC ← M[M[x]]

... 

**Events:**

- Execute A
- Execute S1
- Execute S2
- Execute S3

**Subroutine**

F
F+1

- S1: LOAD (F)
- S2: STORE (F)
- S3: JUMP (F)

**Caller**

A
A+3

- JSR F
- arg
- result

Indirect addressing almost eliminates the need to write self-modifying code (location F still needs to be modified)

**Problems? ⇒ recursive procedure calls**

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Recursive Procedure Calls and Reentrant Codes

*Indirect Addressing through a register*

\[ \text{LOAD } R_1, (R_2) \]

Load register \( R_1 \) with the contents of the word whose address is contained in register \( R_2 \).
Evolution of Addressing Modes

1. Single accumulator, absolute address
   LOAD  x

2. Single accumulator, index registers
   LOAD  x, IX

3. Indirection
   LOAD  (x)

4. Multiple accumulators, index registers, indirection
   LOAD  R, IX, x
   or  LOAD  R, IX, (x)
   the meaning?
   R ← M[M[x] + (IX)]
   or R ← M[M[x + (IX)]]

5. Indirect through registers
   LOAD  R_I, (R_J)

6. The works
   LOAD  R_I, R_J, (R_K)
   R_J = index, R_K = base addr
Variety of Instruction Formats

• **Three address formats:** One destination and up to two operand sources per instruction

  \[(\text{Reg op Reg}) \text{ to Reg} \quad R_I \leftarrow (R_j) \text{ op } (R_k)\]
  \[(\text{Reg op Mem}) \text{ to Reg} \quad R_I \leftarrow (R_j) \text{ op } M[x]\]

  - x can be specified directly or via a register
  - effective address calculation for x could include indexing, indirection, ...

• **Two address formats:** the destination is same as one of the operand sources

  \[(\text{Reg op Reg}) \text{ to Reg} \quad R_I \leftarrow (R_I) \text{ op } (R_j)\]
  \[(\text{Reg op Mem}) \text{ to Reg} \quad R_I \leftarrow (R_I) \text{ op } M[x]\]
More Instruction Formats

- **One address formats**: Accumulator machines
  - Accumulator is always other implicit operand

- **Zero address formats**: operands on a stack
  - Stack can be in registers or in memory
    - usually top of stack cached in registers

\[
\begin{align*}
\text{add} & \quad M[sp-1] \leftarrow M[sp] + M[sp-1] \\
\text{load} & \quad M[sp] \leftarrow M[M[sp]]
\end{align*}
\]

Many different formats are possible!
Data Formats and Memory Addresses

Data formats:

- Bytes, Half words, words and double words

Some issues

- **Byte addressing**
  
  Big Endian
  
  vs. Little Endian

- **Word alignment**
  
  Suppose the memory is organized in 32-bit words. Can a word address begin only at 0, 4, 8, .... ?
Some Tradeoffs

• Should all addressing modes be provided for every operand?

  ⇒ regular vs. irregular instruction formats

• Separate instructions to manipulate Accumulators, Index registers, Base registers

  ⇒ large number of instructions

• Instructions contained implicit memory references -- several contained more than one

  ⇒ very complex control

Great variety of instruction sets
The first definition of the Instruction Set Abstraction: IBM 360
The IBM 650 (1953-4)

Magnetic Drum (1,000 or 2,000 10-digit decimal words)

Active instruction (including next program counter)

Digit-serial ALU

20-digit accumulator

[From 650 Manual, © IBM]
Programmer’s view of a machine: IBM 650

A drum machine with 44 instructions

Instruction: 60 1234 1009

- “Load the contents of location 1234 into the distribution; put it also into the upper accumulator; set lower accumulator to zero; and then go to location 1009 for the next instruction.”

- Programmer’s view of the machine was inseparable from the actual hardware implementation

- Good programmers optimized the placement of instructions on the drum to reduce latency!
Compatibility Problem at IBM

By early 60’s, *IBM had 4 incompatible lines of computers!*

<table>
<thead>
<tr>
<th>System 1</th>
<th>System 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>701</td>
<td>7094</td>
</tr>
<tr>
<td>650</td>
<td>7074</td>
</tr>
<tr>
<td>702</td>
<td>7080</td>
</tr>
<tr>
<td>1401</td>
<td>7010</td>
</tr>
</tbody>
</table>

Each system had its own

- Instruction set
- I/O system and Secondary Storage: magnetic tapes, drums and disks
- assemblers, compilers, libraries,...
- market niche
  - business, scientific, real time, ...

⇒ *IBM 360*
IBM 360: Design Premises
Amdahl, Blaauw and Brooks, 1964

The design must lend itself to growth and successor machines

- General method for connecting I/O devices
- Total performance - answers per month rather than bits per microsecond \(\Rightarrow\) programming aids
- Machine must be capable of supervising itself without manual intervention
- Built-in hardware fault checking and locating aids to reduce down time
- Simple to assemble systems with redundant I/O devices, memories etc. for fault tolerance
- Some problems required floating point words larger than 36 bits
Processor State and Data Types

The information held in the processor at the end of an instruction to provide the processing context for the next instruction.

Program Counter, Accumulator, . . .

- The information held in the processor will be interpreted as having data types manipulated by the instructions.

- If the processing of an instruction can be interrupted then the hardware must save and restore the state in a transparent manner.

Programmer’s machine model is a contract between the hardware and software.
Instruction set

The control for changing the information held in the processor are specified by the instructions available in the instruction set architecture or ISA.

Some things an ISA must specify:
- A way to reference registers and memory
- The computational operations available
- How to control the sequence of instructions
- A binary representation for all of the above

ISA must satisfy the needs of the software:
- assembler, compiler, OS, VM
IBM 360: A General-Purpose Register (GPR) Machine

• Processor State
  – 16 General-Purpose 32-bit Registers
    • *may be used as index and base register*
    • *Register 0 has some special properties*
  – 4 Floating Point 64-bit Registers
  – A Program Status Word (PSW)
    • *PC, Condition codes, Control flags*

• Data Formats
  – 8-bit bytes, 16-bit half-words, 32-bit words, 64-bit double-words
  – 24-bit addresses

• A 32-bit machine with 24-bit addresses
  – *No instruction contains a 24-bit address!*

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IBM 360: Some Addressing Modes

R \leftarrow (R) \text{ op } M[(X) + (B) + D]

a 24-bit address is formed by adding the
12-bit displacement (D) to a base register (B)
and an Index register (X), if desired

The most common formats for arithmetic & logic
instructions, as well as Load and Store instructions
# IBM 360: Character String Operations

<table>
<thead>
<tr>
<th>opcode</th>
<th>length</th>
<th>B1</th>
<th>D1</th>
<th>B2</th>
<th>D2</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>4</td>
<td>12</td>
<td>8</td>
<td>4</td>
<td>12</td>
</tr>
</tbody>
</table>

**SS format:** store to store instructions  
\[ M[(B1) + D1] \leftarrow M[(B1) + D1] \text{ op } M[(B2) + D2] \]

*iterate “length” times*

*Most operations on decimal and character strings use this format*

- MVC move characters
- MP multiply two packed decimal strings
- CLC compare two character strings

*Multiple memory operations per instruction complicates exception & interrupt handling*
IBM 360: Branches & Condition Codes

- Arithmetic and logic instructions set *condition codes*
  - equal to zero
  - greater than zero
  - overflow
  - carry...

- I/O instructions also set condition codes
  - channel busy

- Conditional branch instructions are based on testing condition code registers (CC’s)
  - RX and RR formats
    - BC__ branch conditionally
    - BAL__ branch and link, i.e., R15 ← (PC)+1
      *for subroutine calls*
      ⇒ CC’s must be part of the PSW
IBM 360: Precise Interrupts

- IBM 360 ISA (Instruction Set Architecture) preserves sequential execution model
- Programmers view of machine was that each instruction either completed or signaled a fault before the next instruction began execution
- Exception/interrupt behavior identical across family of implementations
# IBM 360: Initial Implementations (1964)

<table>
<thead>
<tr>
<th></th>
<th>Model 30</th>
<th>...</th>
<th>Model 70</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Memory Capacity</strong></td>
<td>8K - 64 KB</td>
<td></td>
<td>256K - 512 KB</td>
</tr>
<tr>
<td><strong>Memory Cycle</strong></td>
<td>2.0µs</td>
<td>...</td>
<td>1.0µs</td>
</tr>
<tr>
<td><strong>Datapath</strong></td>
<td>8-bit</td>
<td></td>
<td>64-bit</td>
</tr>
<tr>
<td><strong>Circuit Delay</strong></td>
<td>30 nsec/level</td>
<td></td>
<td>5 nsec/level</td>
</tr>
<tr>
<td><strong>Registers</strong></td>
<td>in Main Store</td>
<td></td>
<td>in Transistor</td>
</tr>
<tr>
<td><strong>Control Store</strong></td>
<td>Read only 1µsec</td>
<td></td>
<td>Dedicated circuits</td>
</tr>
</tbody>
</table>

- Six implementations (Models, 30, 40, 50, 60, 62, 70)
- 50X performance difference cross models
- *ISA completely hid the underlying technological differences between various models.*

With minor modifications, IBM 360 ISA is still in use
IBM 360: Forty-Six years later…
zEnterprise196 Microprocessor

- 1.4 billion transistors, Quad core design
- Up to 96 cores (80 visible to OS) in one multichip module
- 5.2 GHz, IBM 45nm SOI CMOS technology
- 64-bit virtual addressing
  - original 360 was 24-bit; 370 was a 31-bit extension
- Superscalar, out-of-order
  - Up to 72 instructions in flight
- Variable length instruction pipeline: 15-17 stages
- Each core has 2 integer units, 2 load-store units and 2 floating point units
- 8K-entry Branch Target Buffer
  - Very large buffer to support commercial workload
- Four Levels of caches:
  - 64KB L1 I-cache, 128KB L1 D-cache
  - 1.5MB L2 cache per core
  - 24MB shared on-chip L3 cache
  - 192MB shared off-chip L4 cache

[ September 2010 ]
Instruction Set Architecture (ISA) versus Implementation

• ISA is the hardware/software interface
  - Defines set of programmer visible state
  - Defines data types
  - Defines instruction semantics (operations, sequencing)
  - Defines instruction format (bit encoding)
  - Examples: MIPS, Alpha, x86, IBM 360, VAX, ARM, JVM

• Many possible implementations of one ISA
  - 360 implementations: model 30 (c. 1964), zEnterprise196 (c. 2010)
  - x86 implementations: 8086 (c. 1978), 80186, 286, 386, 486, Pentium, Pentium Pro, Pentium-4, Core i7, AMD Athlon, AMD Opteron, Transmeta Crusoe, SoftPC
  - MIPS implementations: R2000, R4000, R10000, ...
  - JVM: HotSpot, PicoJava, ARM Jazelle, ...
Next lecture:
Implementing an ISA