Influence of Technology and Software on Instruction Sets: Up to the dawn of IBM 360

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Computer Science and Artificial Intelligence Laboratory
M.I.T.

Administrivia

- We've moved!
  - Lectures in 2-105
  - Recitations and quizzes in 37-212
- Second TA: Mark Seifter
- Self-assessment test due today
- Lab 0 due Wed

And then there was IBM 701

IBM 701 -- 30 machines were sold in 1953-54

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Why was IBM late getting into computers?

IBM was making too much money!
Even without computers, IBM revenues were
doubling every 4 to 5 years in 40's and 50's.

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- The *ability to design complex control circuits* to execute an instruction was the central design concern as opposed to *the speed* of decoding or an ALU operation
- Programmer's view of the machine was inseparable from the actual hardware implementation

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Registers expensive

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Burks, Goldstein & von Neumann ~1946

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LOAD	x	$AC \leftarrow M[x]$
STORE	x	$M[x] \leftarrow (AC)$
ADD	x	$AC \leftarrow (AC) + M[x]$
SUB	x	
MUL	x	Involved a quotient register
DIV	x	
SHIFT LEFT		$AC \leftarrow 2 \times (AC)$
SHIFT RIGHT		

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Typically less than 2 dozen instructions!

Programming: Single Accumulator Machine

$C_i \leftarrow A_i + B_i, \quad 1 \le i \le n$

A	
B	
C	
N	-n
ONE	1
code	

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F1      LOAD     A
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DONE    HLT
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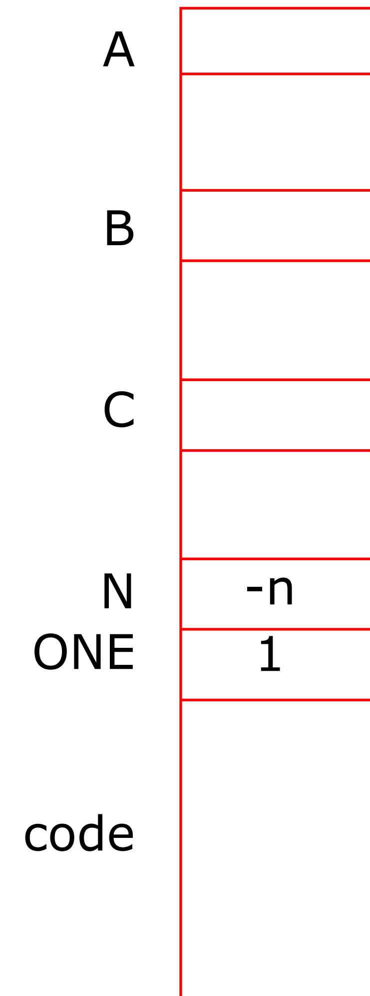

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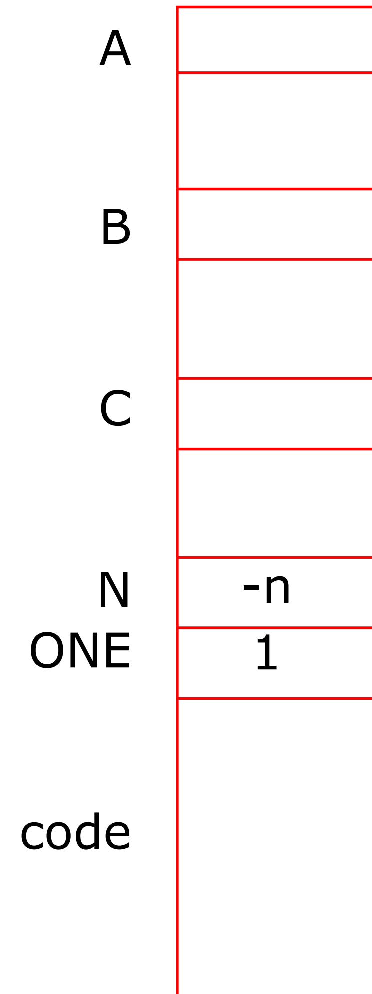

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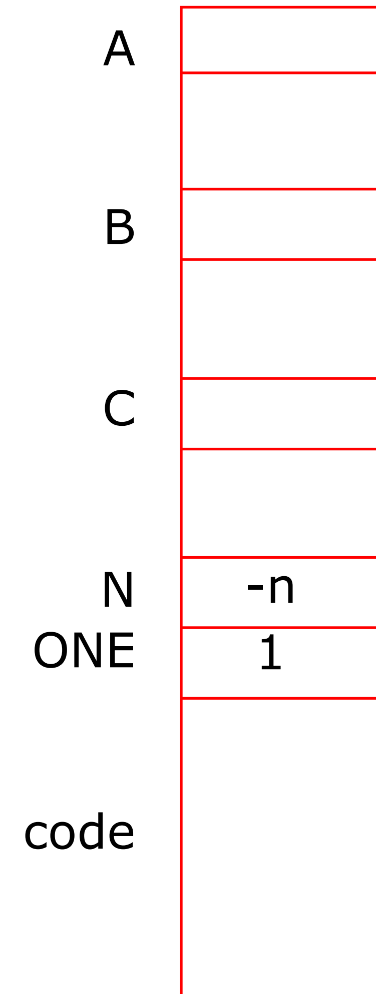

Problem?

How to modify the addresses A, B and C ?

Self-Modifying Code

$C_i \leftarrow A_i + B_i, \quad 1 \le i \le n$

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modify the program for the next iteration

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        LOAD ADR    F1
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        STORE ADR   F1
        LOAD ADR    F2
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Each iteration involves	*total*	*book-keeping*
instruction fetches		
operand fetches		
stores		

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modify the program for the next iteration

Each iteration involves

	total	*book-keeping*
instruction fetches	*17*	
operand fetches		
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modify the program for the next iteration

Each iteration involves

	total	*book-keeping*
instruction fetches	*17*	
operand fetches	*10*	
stores	*5*	

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Each iteration involves

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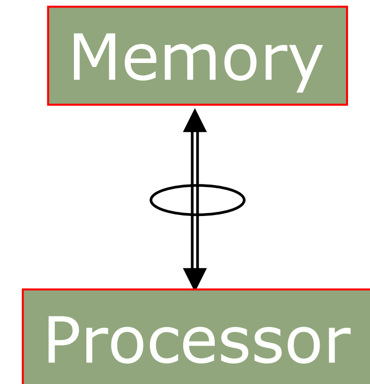
Most of the executed instructions are for book keeping!

Processor-Memory Bottleneck: Early Solutions

- Indexing capability
- Fast local storage in the processor
  - 8-16 registers as opposed to one accumulator
- Complex instructions
- Compact instructions
  - implicit address bits for operands



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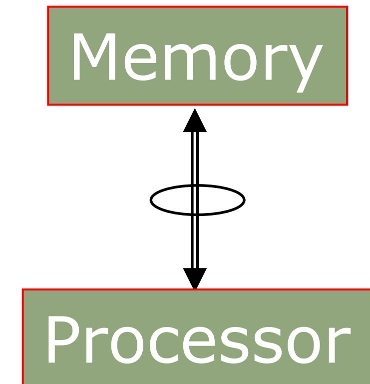

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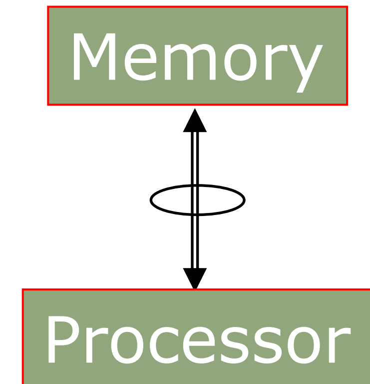

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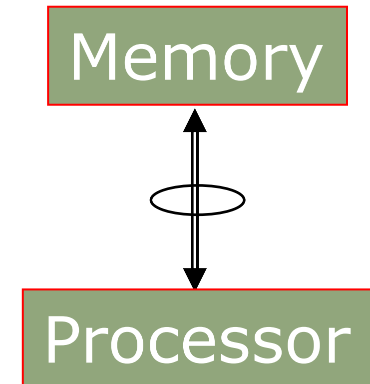

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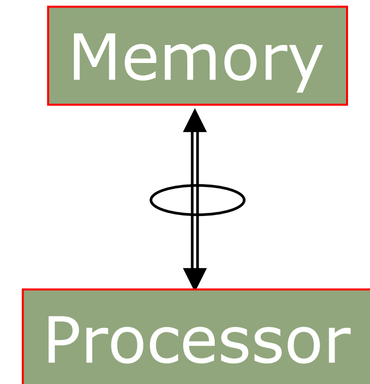
  - to reduce instruction fetch cost



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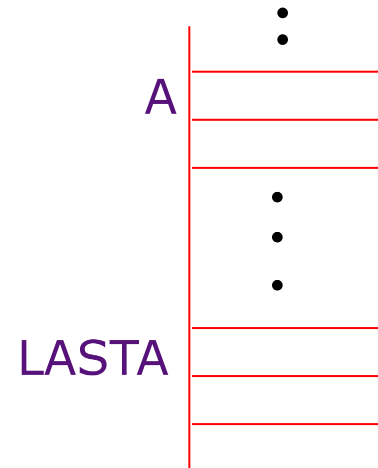
Index registers have accumulator-like characteristics

Using Index Registers

$$C_i \leftarrow A_i + B_i, \quad 1 \leq i \leq n$$

```
        LOADi   N, IX
LOOP    JZi     DONE, IX
        LOAD    LASTA, IX
        ADD     LASTB, IX
        STORE   LASTC, IX
        JUMP    LOOP
DONE    HALT
```

N starts with -n



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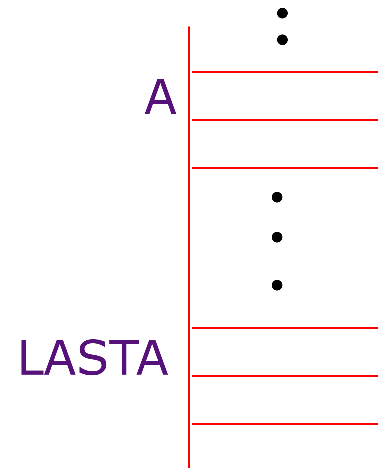

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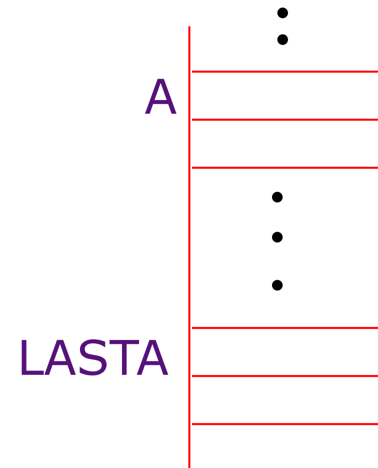

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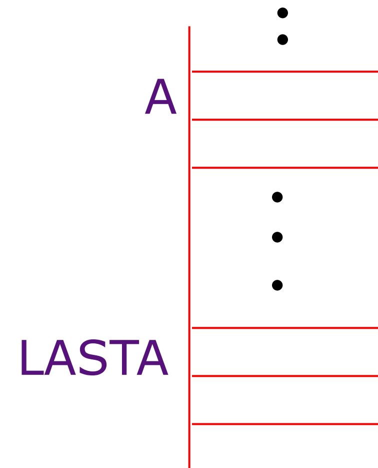

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	with index regs	without index regs
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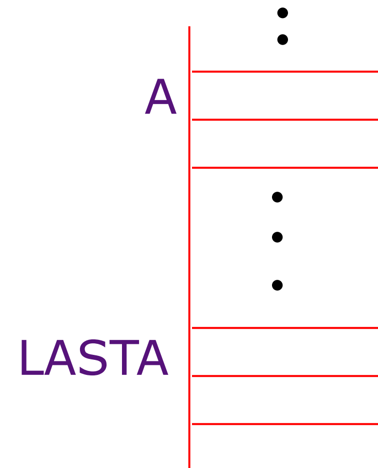

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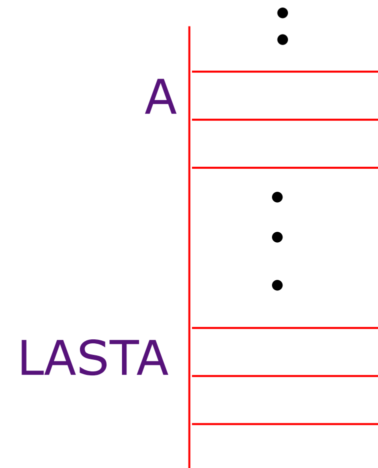

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	with index regs	without index regs
instruction fetch	5(2)	17 (14)
operand fetch	2	10 (8)
store		5 (4)

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```
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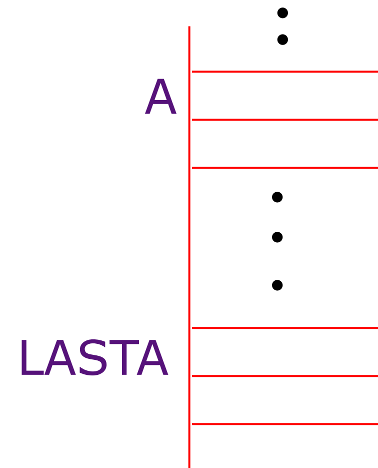

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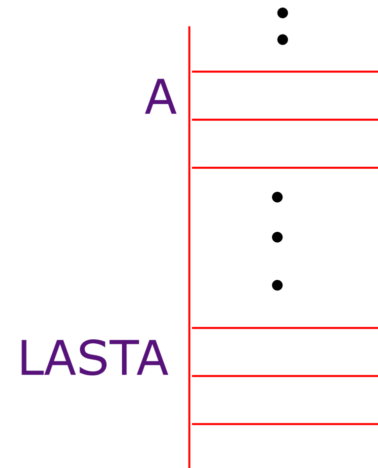

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- *Costs?*

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        LOAD    LASTA, IX
        ADD     LASTB, IX
        STORE   LASTC, IX
        JUMP    LOOP
DONE    HALT
```
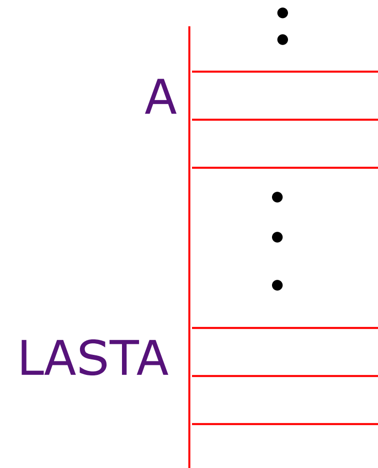

N starts with -n



- *Program does not modify itself*
- *Efficiency has improved dramatically (ops / iter)*

	with index regs	without index regs
instruction fetch	5(2)	17 (14)
operand fetch	2	10 (8)
store	1	5 (4)

- *Costs?*
  - *Complex control*
  - Index register computations (ALU-like circuitry)
  - 1 to 2 bits longer Instructions

Operations on Index Registers

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To increment index register by k

AC ← (IX)	*new instruction*
AC ← (AC) + k	
IX ← (AC)	*new instruction*

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More instructions to manipulate index register

STOREi	x, IX	M[x] ← (IX) (extended to fit a word)
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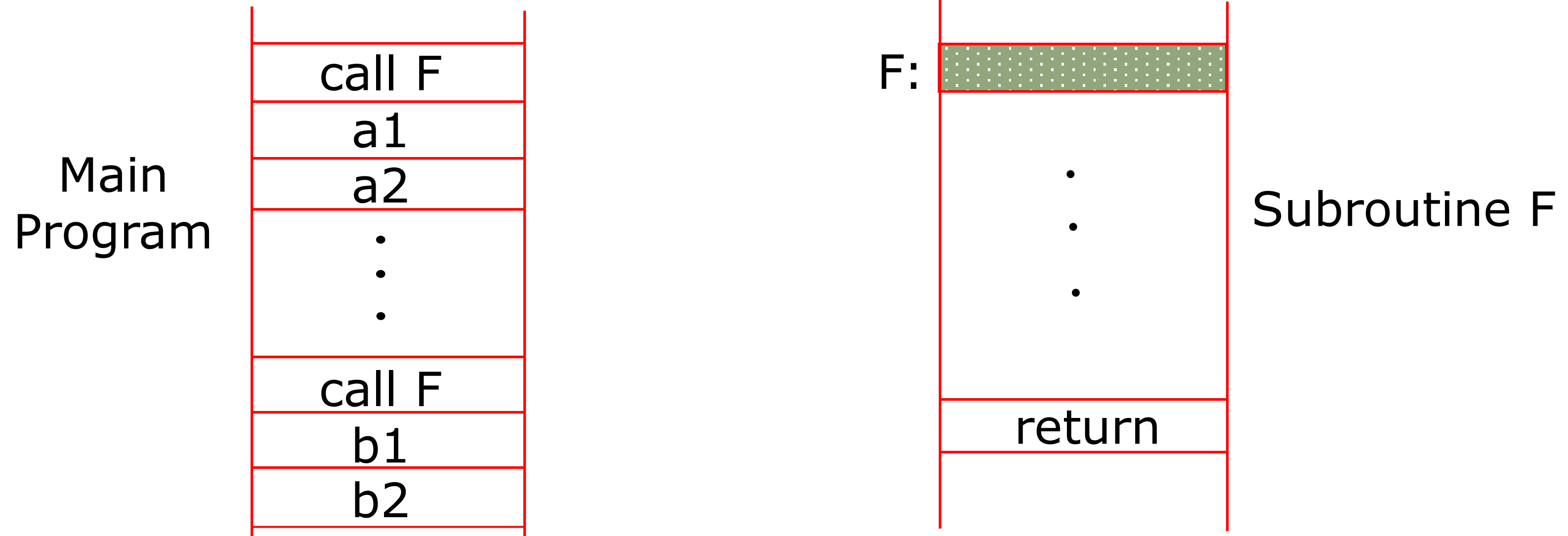
STOREi x, IX M[x] ← (IX) (extended to fit a word)
...

IX begins to look like an accumulator

⇒ several index registers
several accumulators
⇒ *General Purpose Registers*

Support for Subroutine Calls



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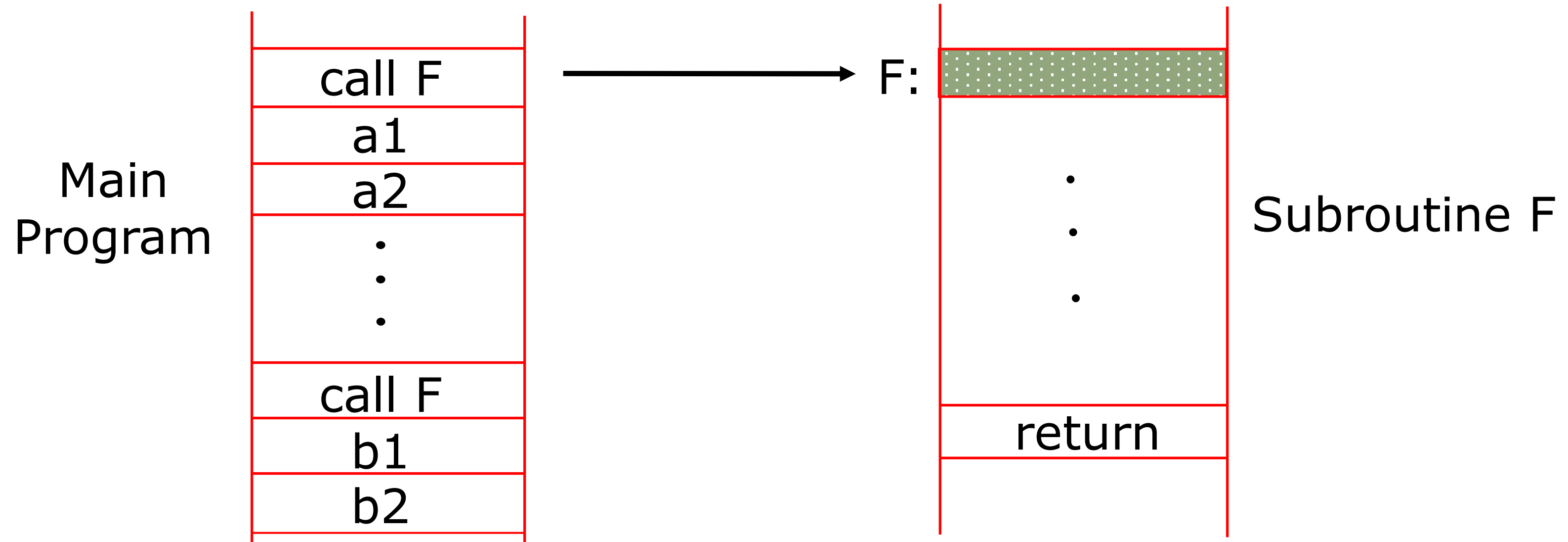

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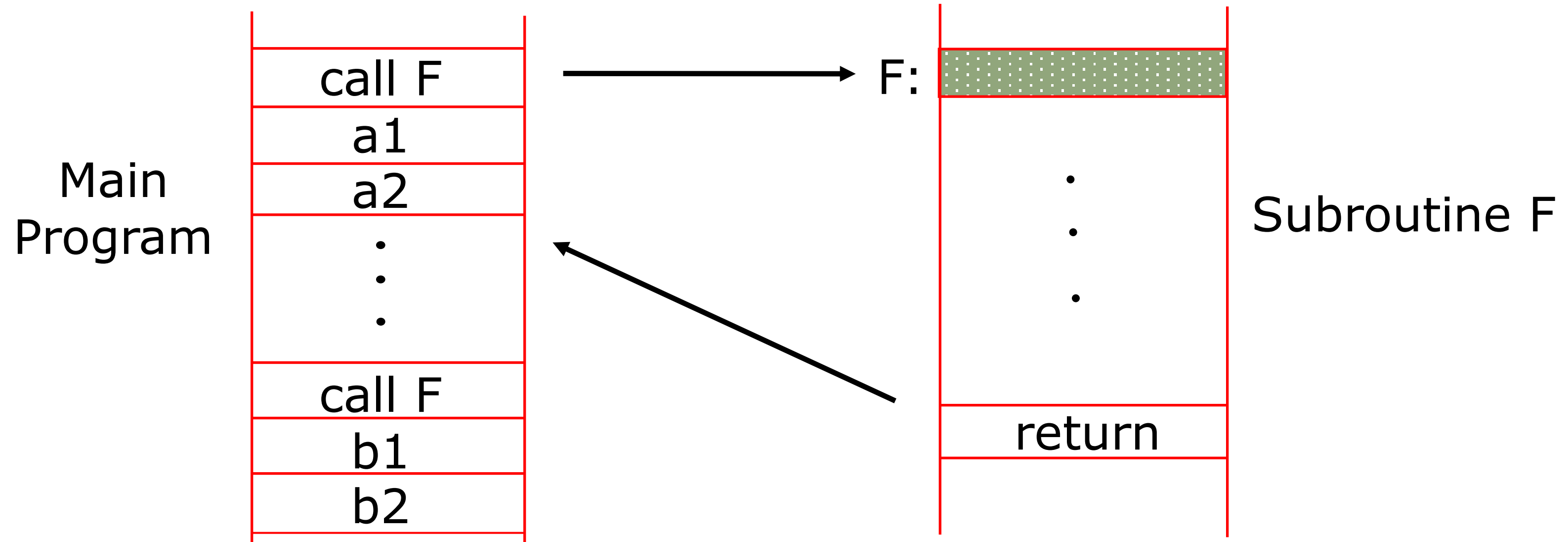

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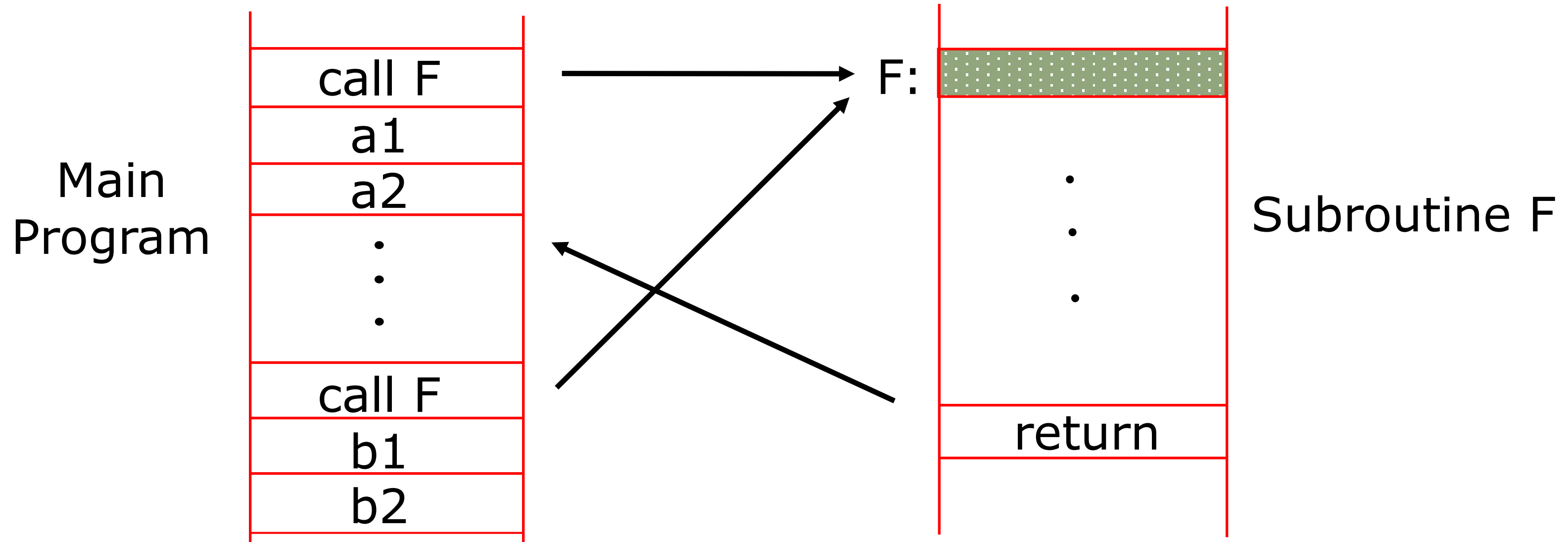

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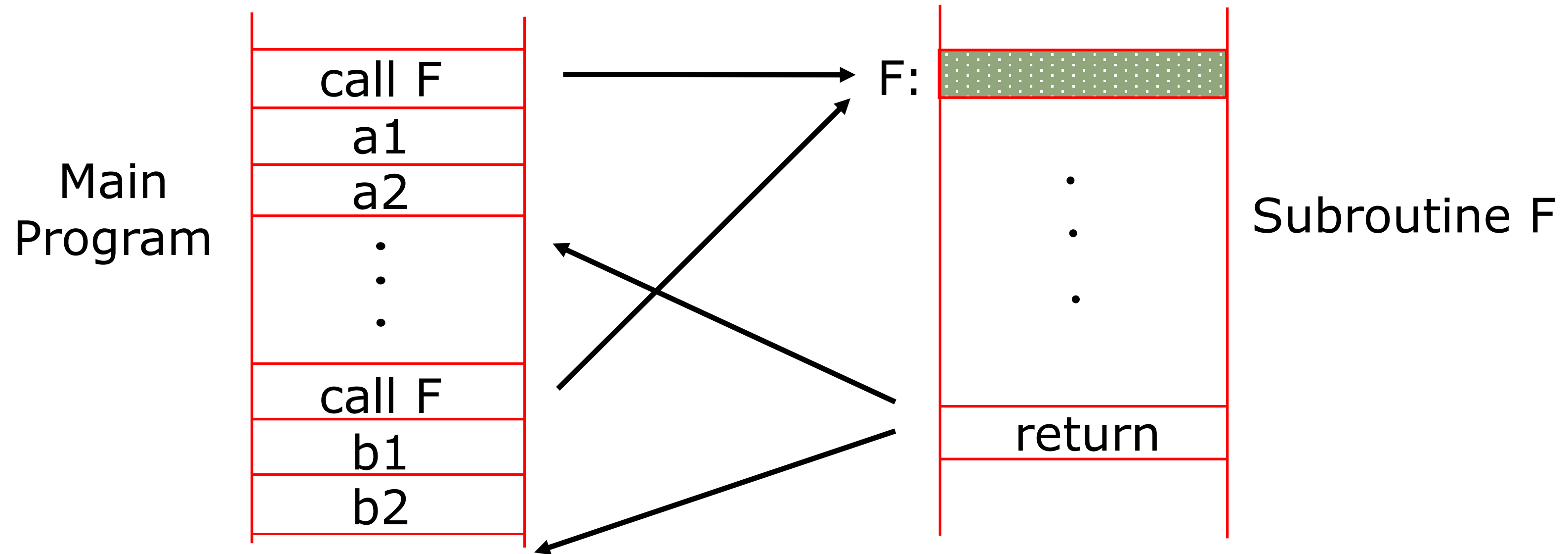

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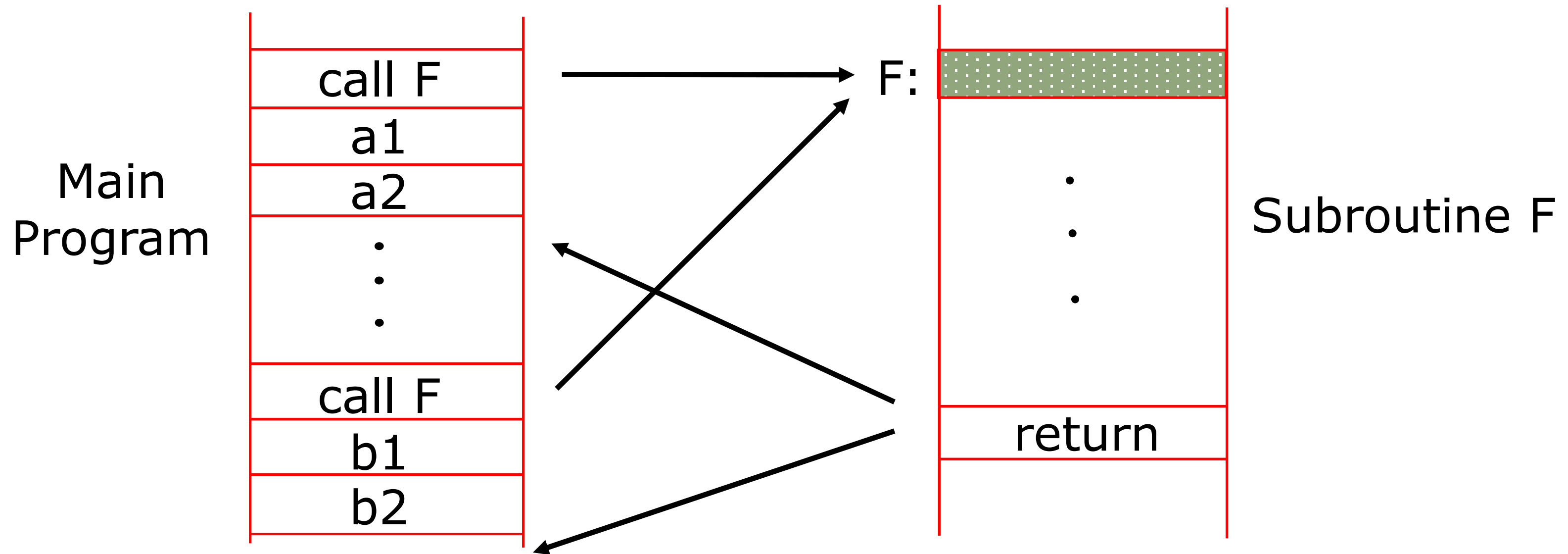

A special *subroutine jump instruction*

A: JSR F

$M[F] \leftarrow A + 1$ and jump to $F + 1$

Indirect Addressing and Subroutine Calls

Indirect addressing

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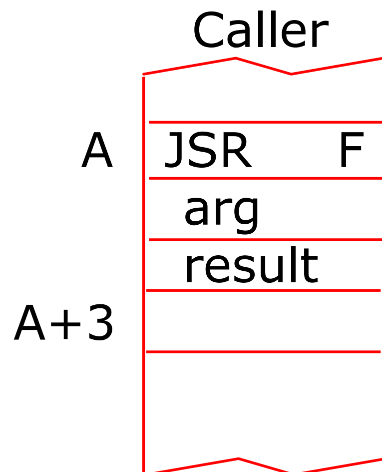
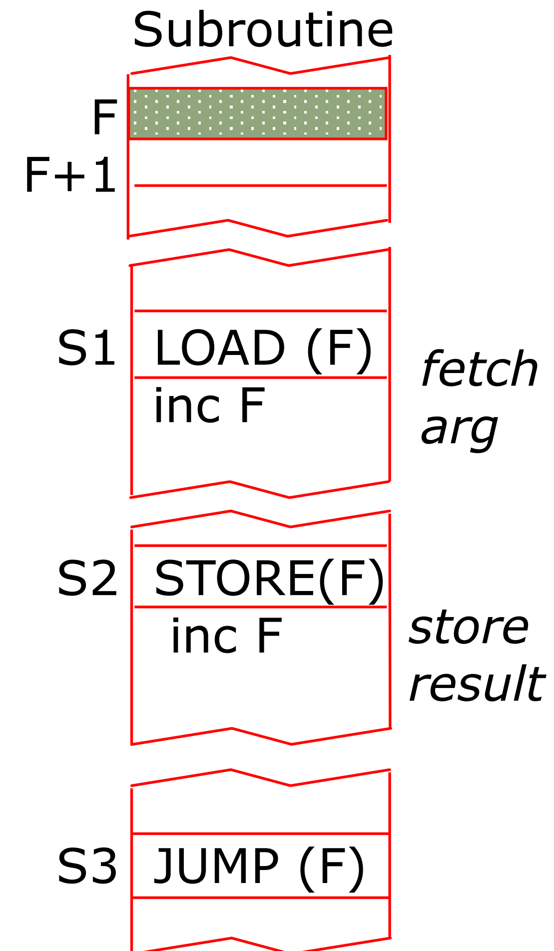
...





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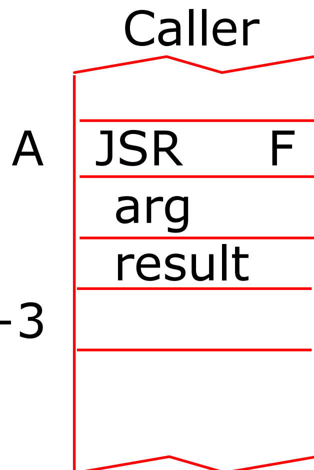

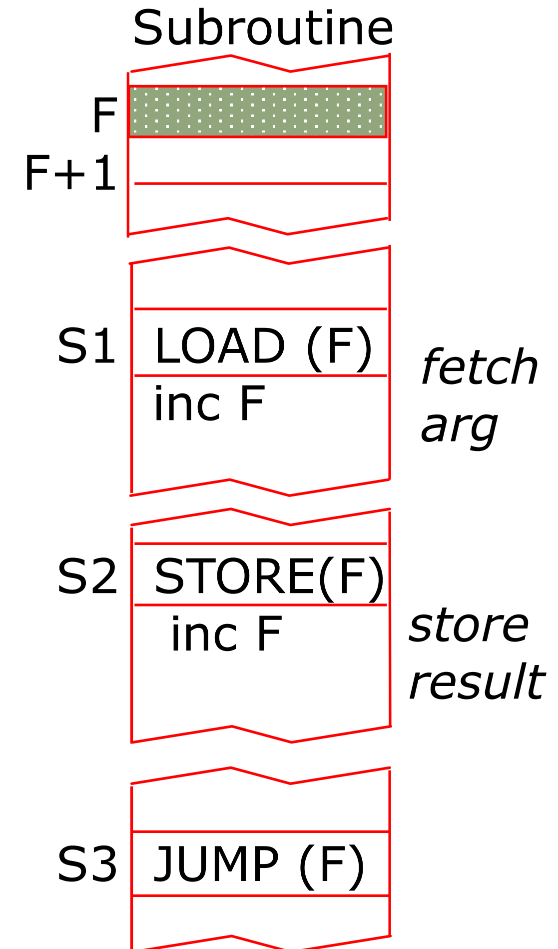

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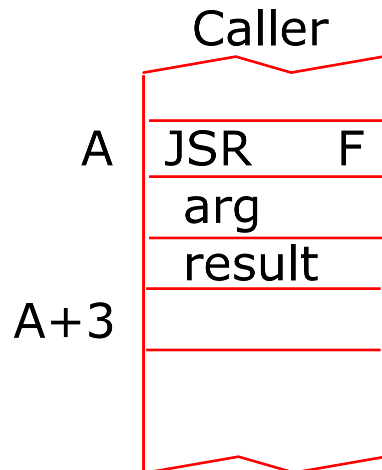

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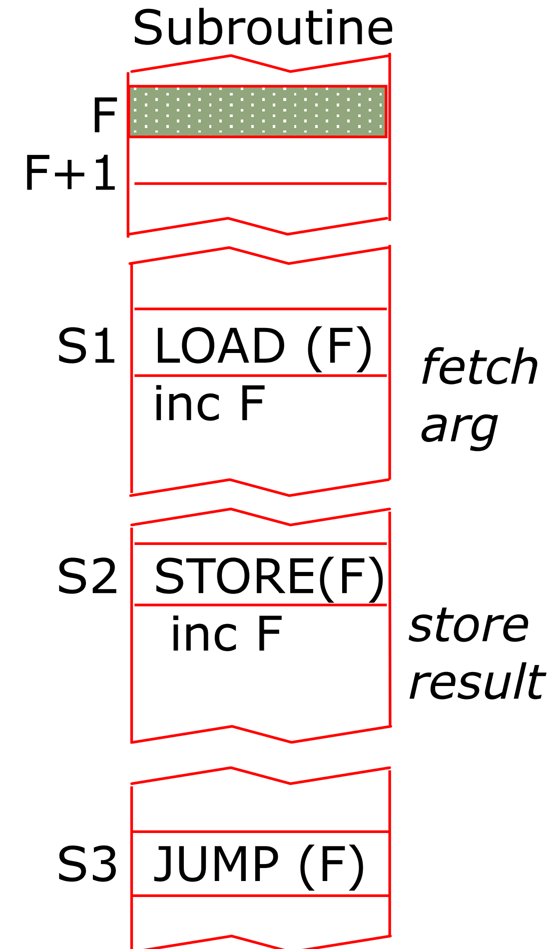

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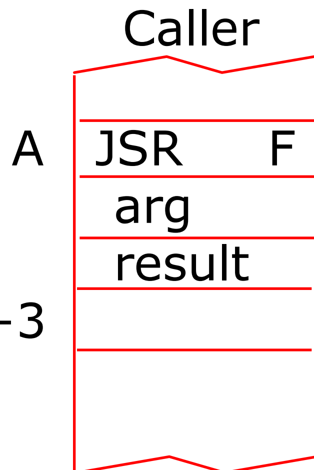

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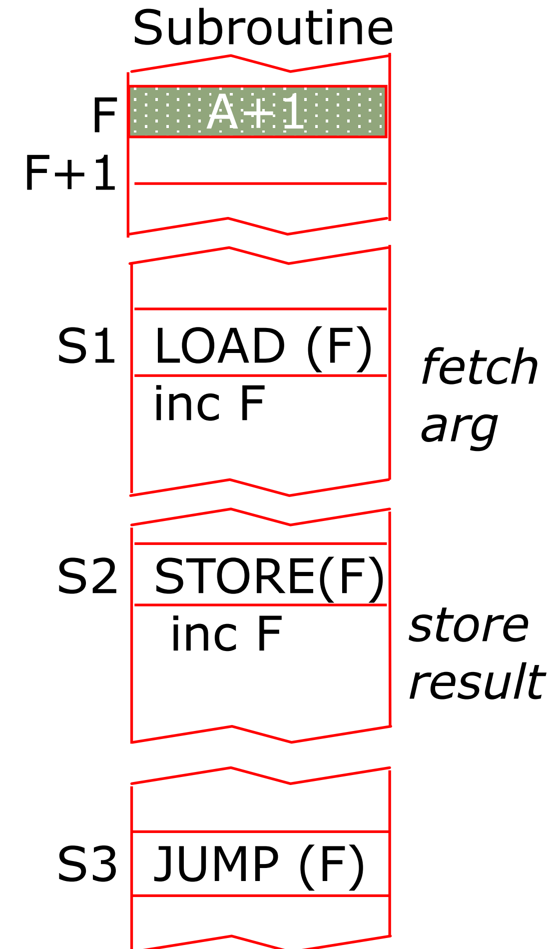

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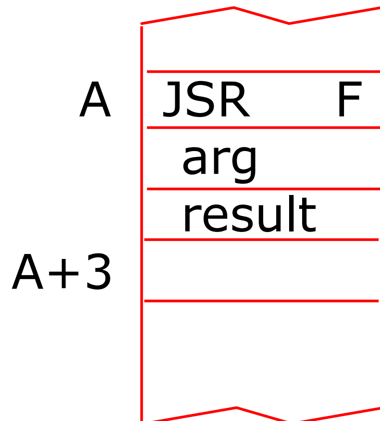

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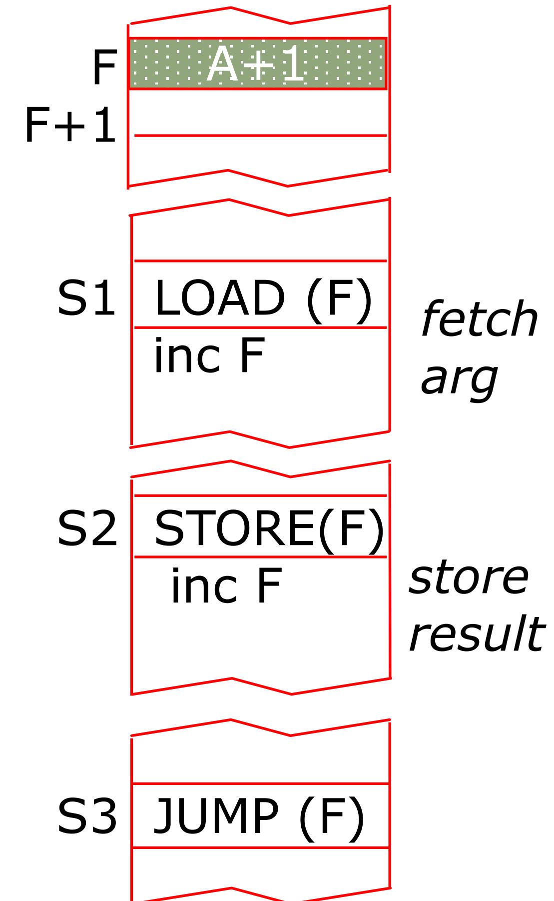
Execute S1



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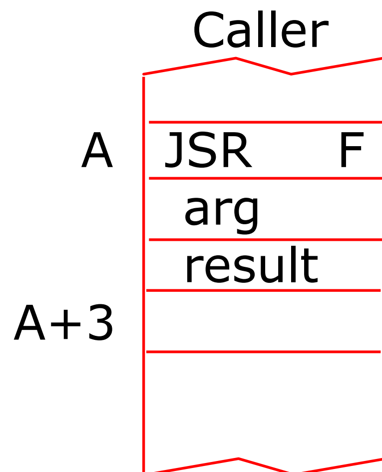

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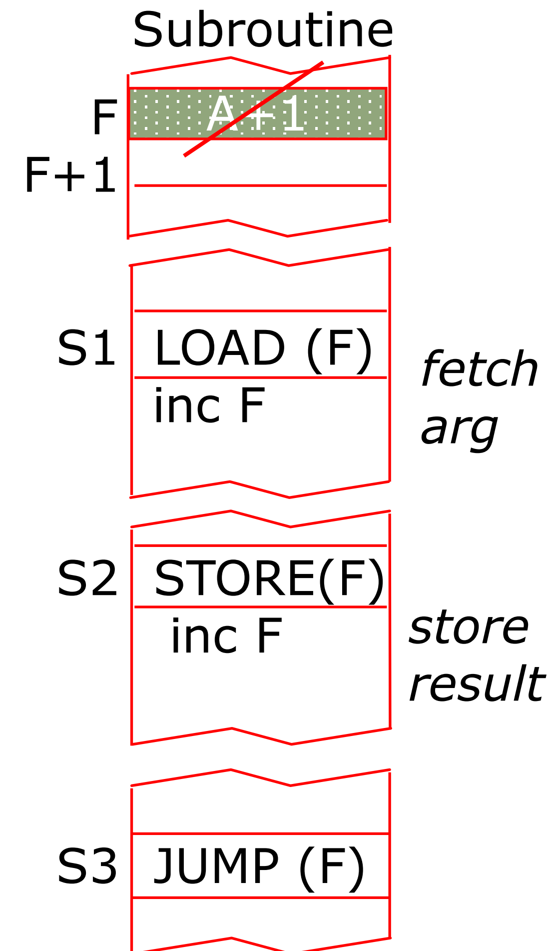

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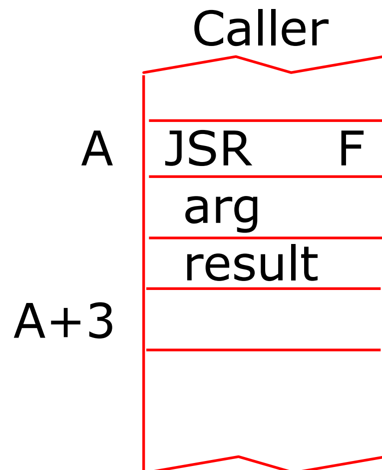

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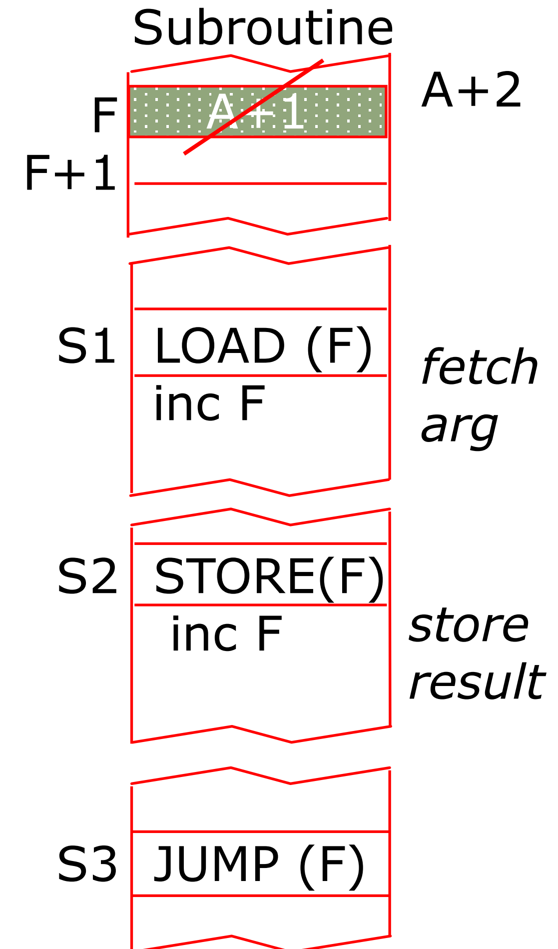

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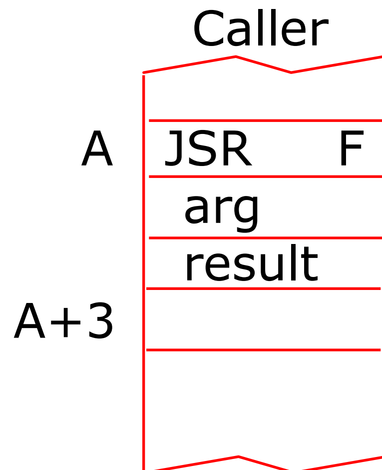

Events:

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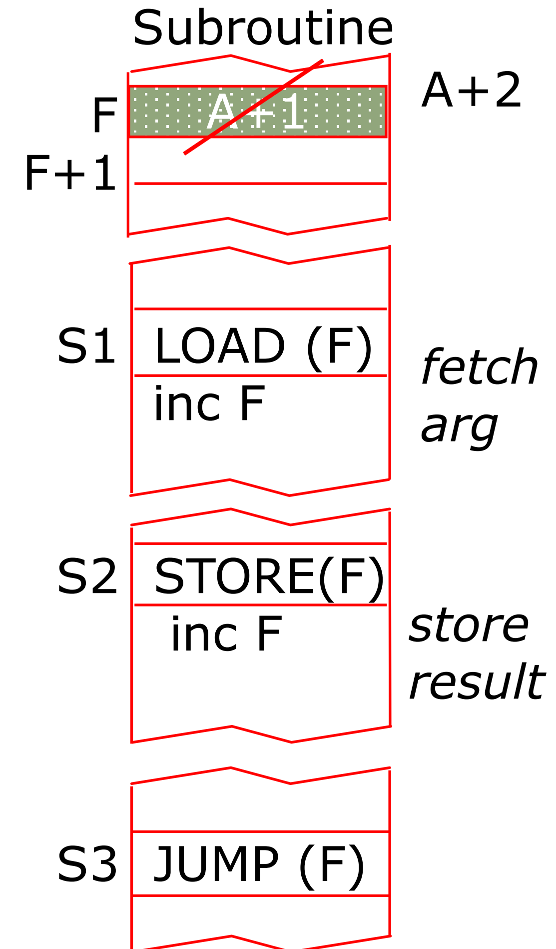
Execute S2



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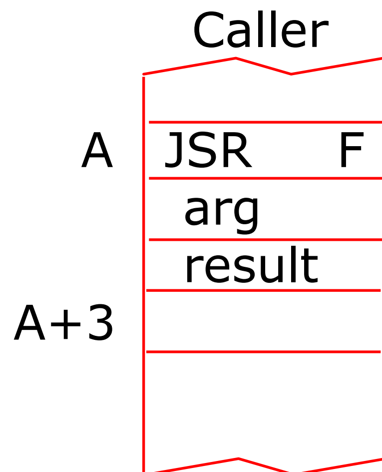

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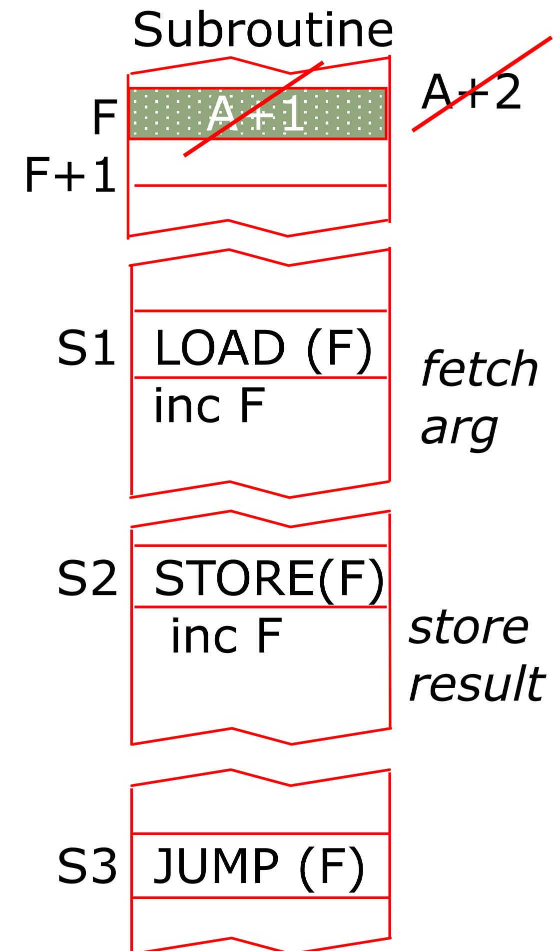

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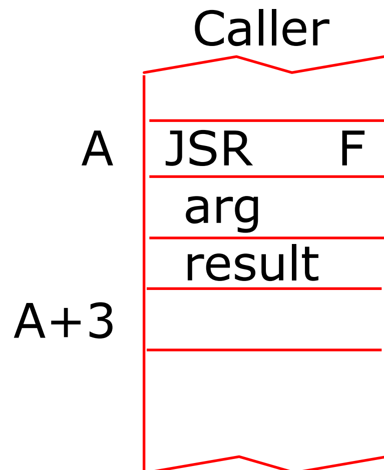

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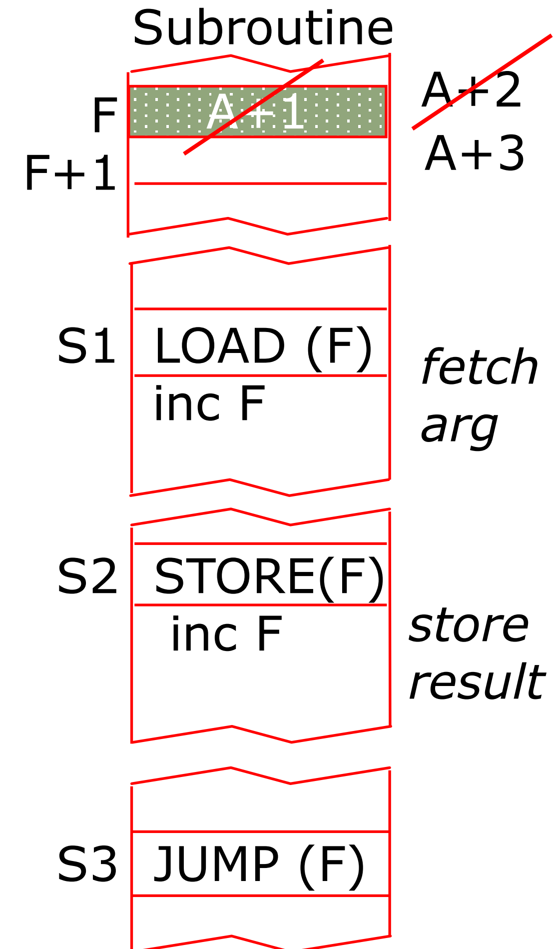

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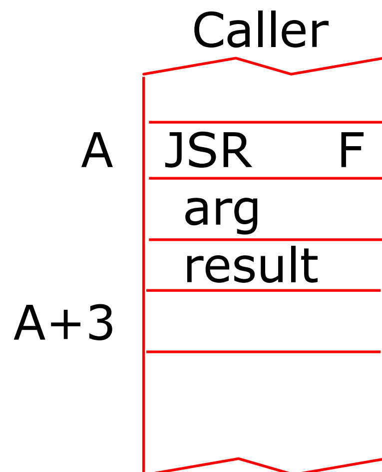
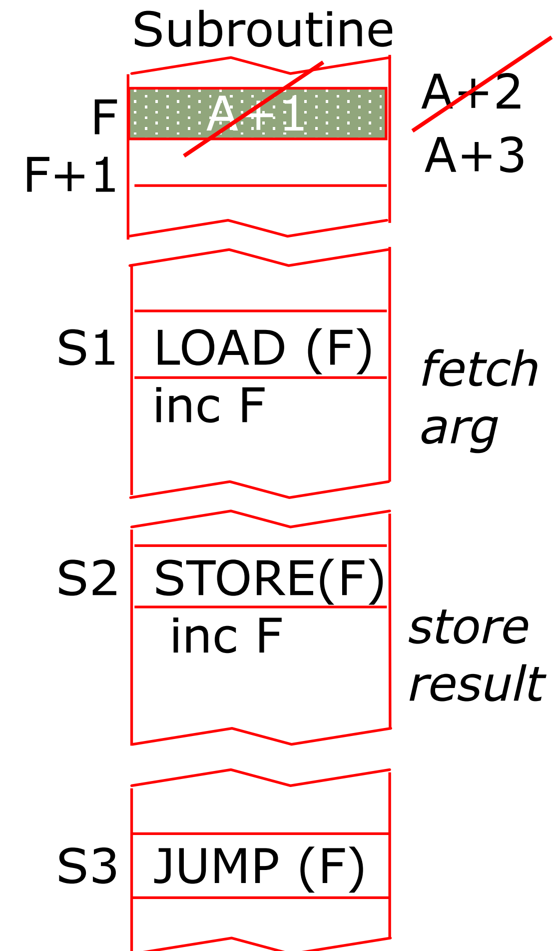


Events:

Execute A
Execute S1
Execute S2
Execute S3



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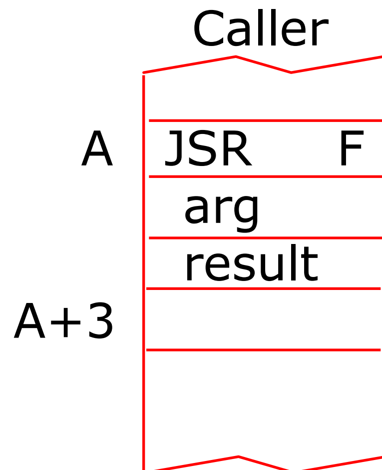
Caller



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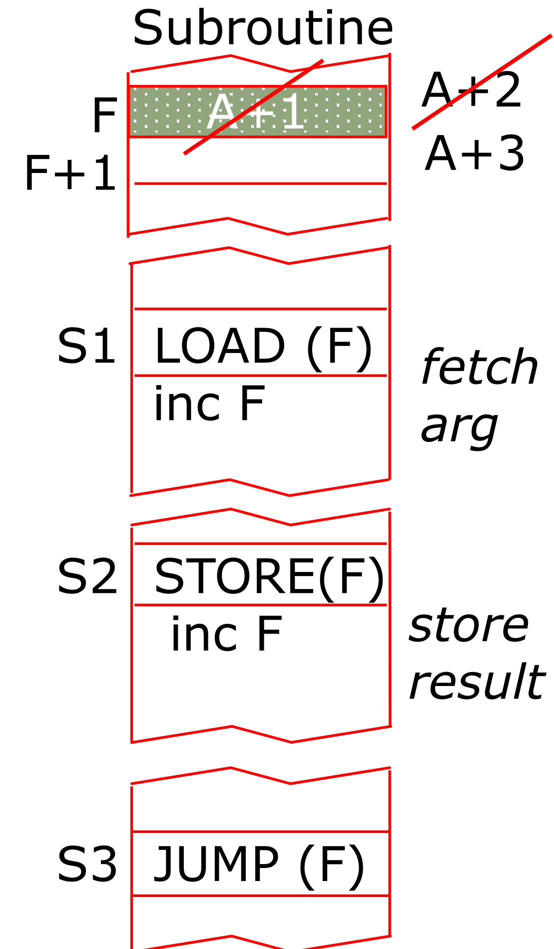
Subroutine



Indirect addressing almost eliminates the need to write self-modifying code (location F still needs to be modified)

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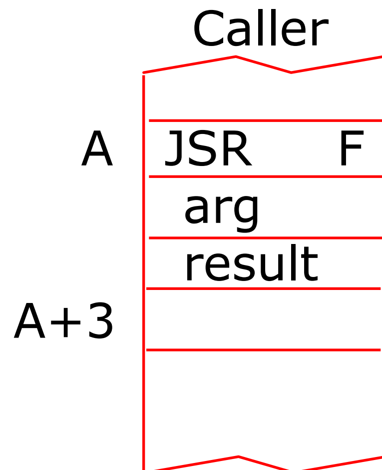

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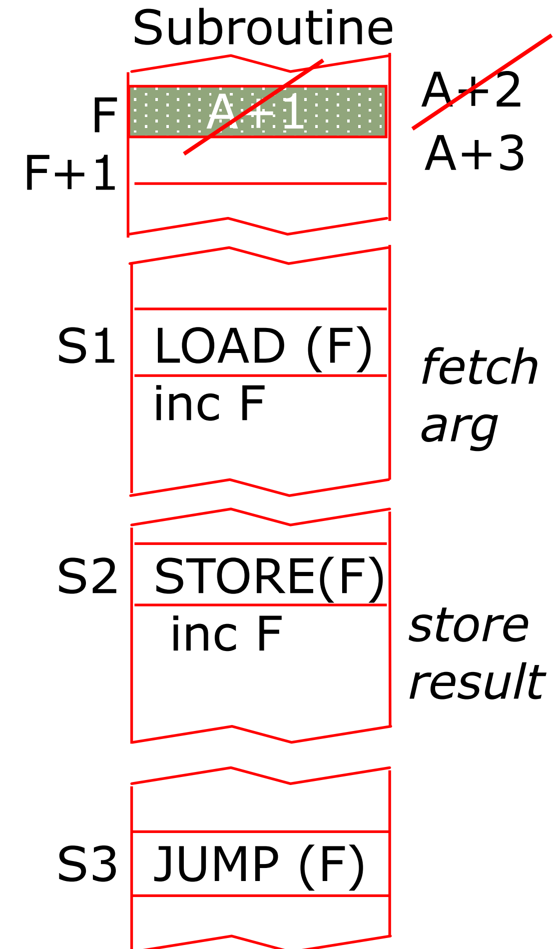

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Problems? ⇒

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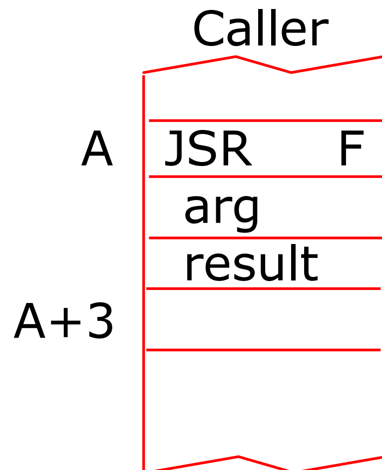

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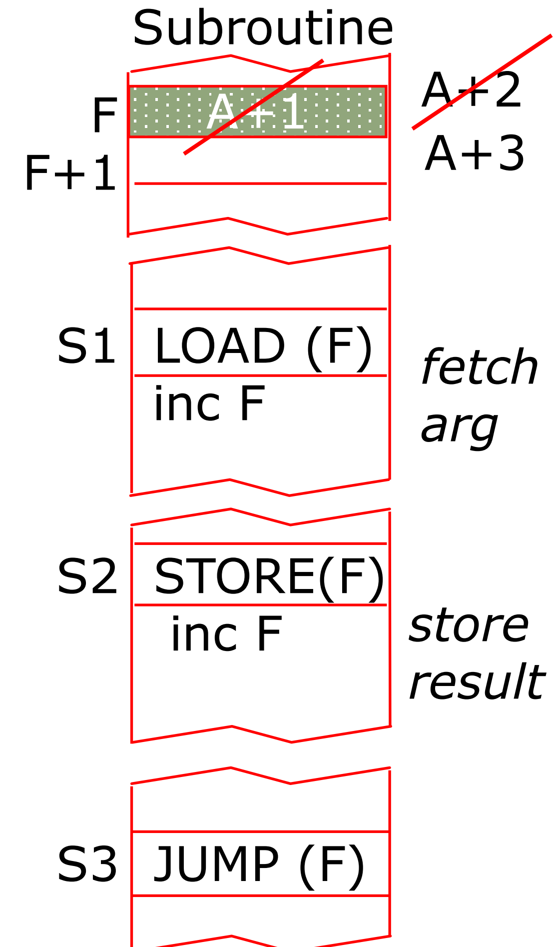

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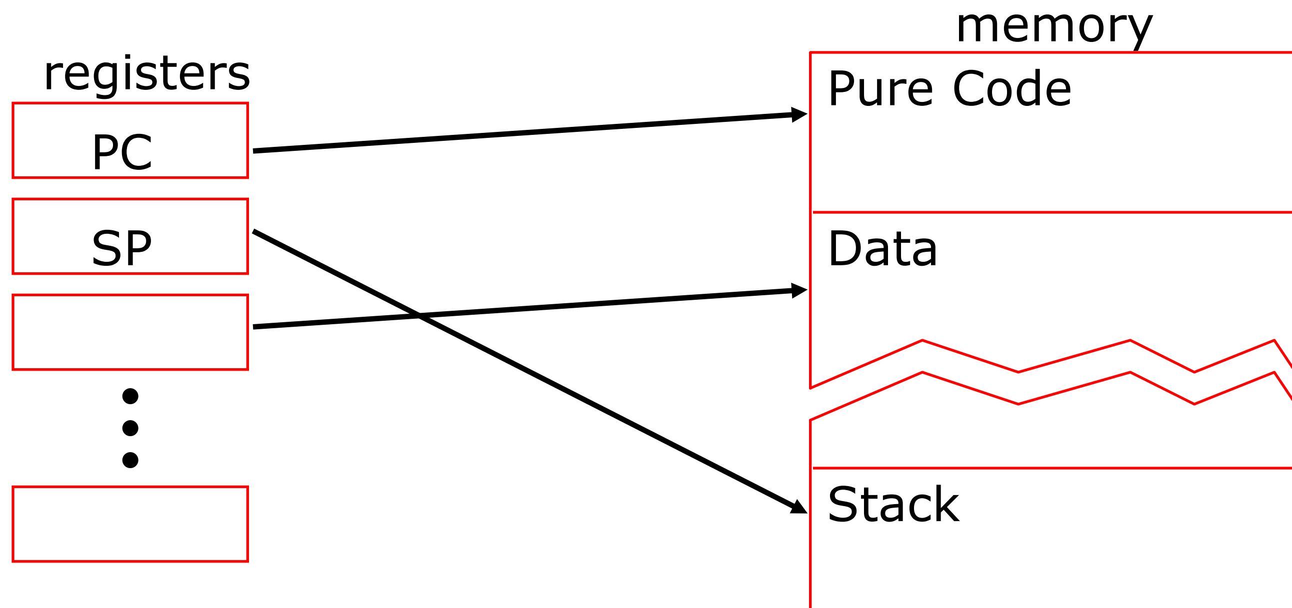
Problems? ⇒ *recursive procedure calls*

Recursive Procedure Calls and Reentrant Codes

Indirect Addressing through a register

LOAD R_1, (R_2)

Load register R_1 with the contents of the word whose address is contained in register R_2



Evolution of Addressing Modes

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4. Multiple accumulators, index registers, indirection

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   or LOAD R, IX, (x)

the meaning?

$R \leftarrow M[M[x] + (IX)]$

or $R \leftarrow M[M[x + (IX)]]$

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6. The works

   LOAD R_I, R_J, (R_K)

   R_J = index, R_K = base addr

Variety of Instruction Formats

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- *Three address formats:* One destination and up to two operand sources per instruction

(Reg op Reg) to Reg	$R_I \leftarrow (R_J)$ op (R_K)
(Reg op Mem) to Reg	$R_I \leftarrow (R_J)$ op M[x]

  – x can be specified directly or via a register
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- *Two address formats:* the destination is same as one of the operand sources

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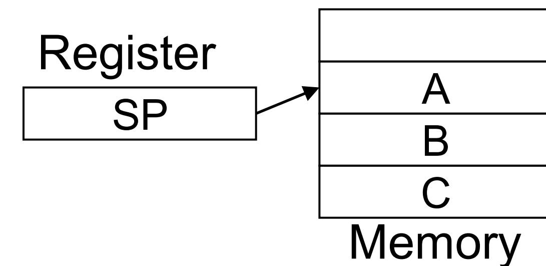

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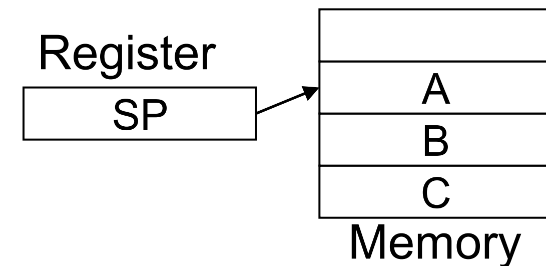

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Many different formats are possible!

Data Formats and Memory Addresses

Data formats:

Bytes, Half words, words and double words

Some issues

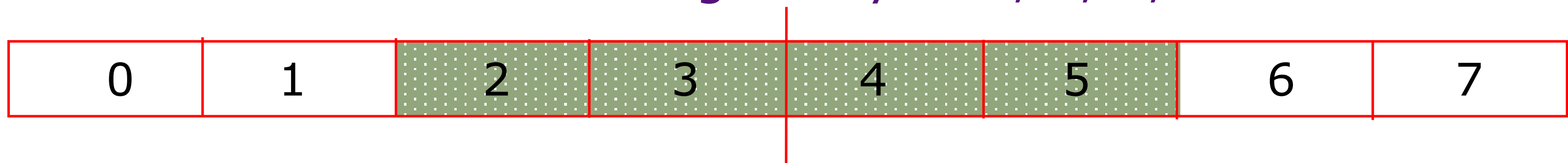
- *Byte addressing*

Big Endian	0	1	2	3
vs. Little Endian	3	2	1	0

- *Word alignment*

Suppose the memory is organized in 32-bit words.

Can a word address begin only at 0, 4, 8, ... ?



Some Tradeoffs

- Should all addressing modes be provided for every operand?

  ⇒ *regular vs. irregular instruction formats*

- Separate instructions to manipulate Accumulators, Index registers, Base registers

  ⇒ *large number of instructions*

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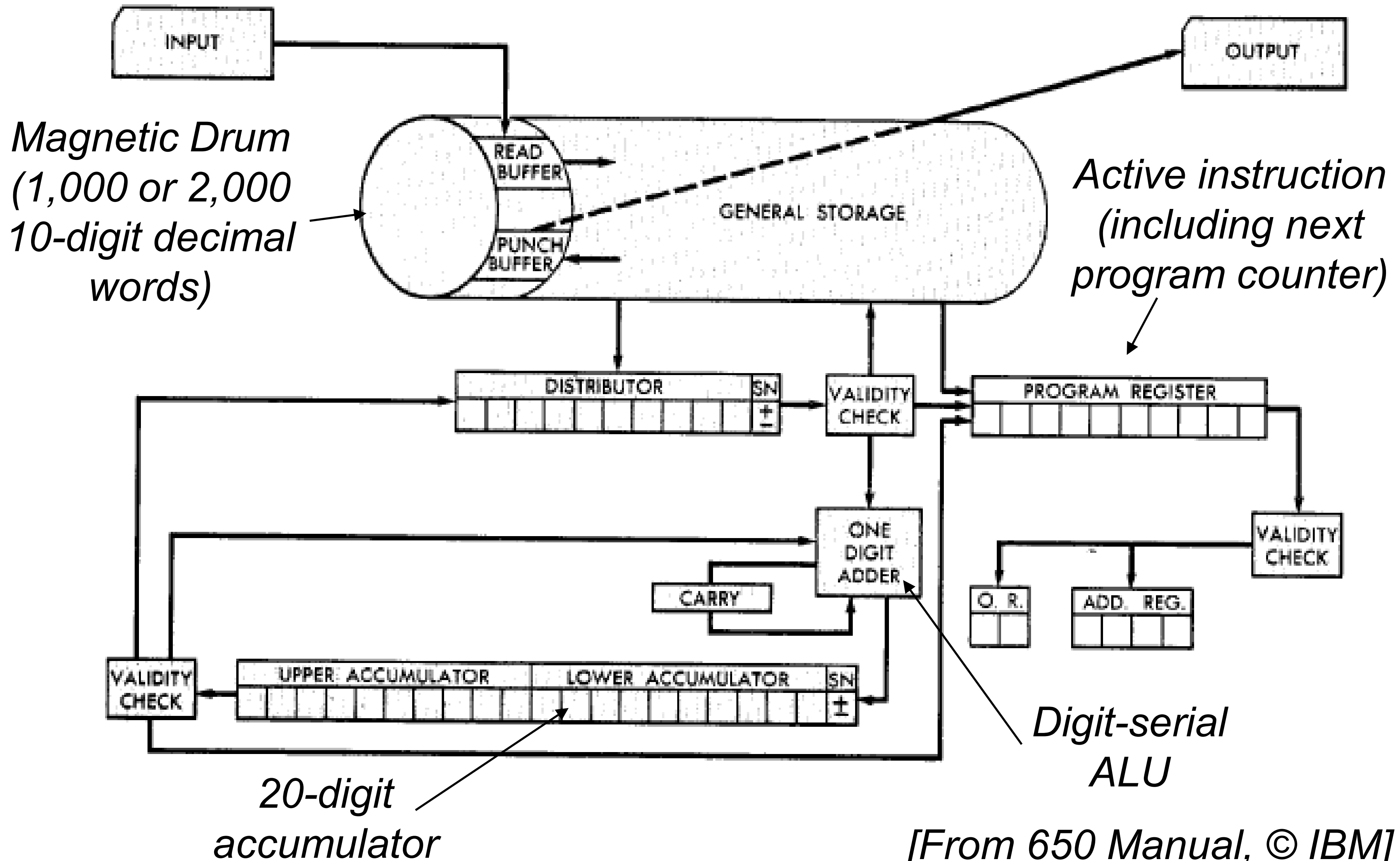
Great variety of instruction sets

The first definition of the Instruction Set Abstraction: IBM 360

The IBM 650 (1953-4)



[From 650 Manual, © IBM]

Programmer's view of a machine: IBM 650

A drum machine with 44 instructions

Instruction: 60 1234 1009

- "Load the contents of location 1234 into the *distribution*; put it also into the *upper accumulator*; set *lower accumulator* to zero; and then go to location 1009 for the next instruction."

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- Programmer's view of the machine was inseparable from the actual hardware implementation
- Good programmers optimized the placement of instructions on the drum to reduce latency!

Compatibility Problem at IBM

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701	→	7094
650	→	7074
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- Instruction set
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- assemblers, compilers, libraries,...
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⇒ *IBM 360*

IBM 360 : Design Premises
Amdahl, Blaauw and Brooks, 1964

The design must lend itself to *growth and successor machines*

- General method for connecting I/O devices
- Total performance - answers per month rather than bits per microsecond $\Rightarrow$ *programming aids*
- Machine must be capable of *supervising itself* without manual intervention
- Built-in *hardware fault checking* and locating aids to reduce down time
- Simple to assemble systems with redundant I/O devices, memories etc. for *fault tolerance*
- Some problems required floating point words larger than 36 bits

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Programmer's machine model is a contract between the hardware and software

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ISA must satisfy the needs of the software:
- assembler, compiler, OS, VM

IBM 360: *A General-Purpose Register (GPR) Machine*

- Processor State
  - 16 General-Purpose 32-bit Registers
    - *may be used as index and base register*
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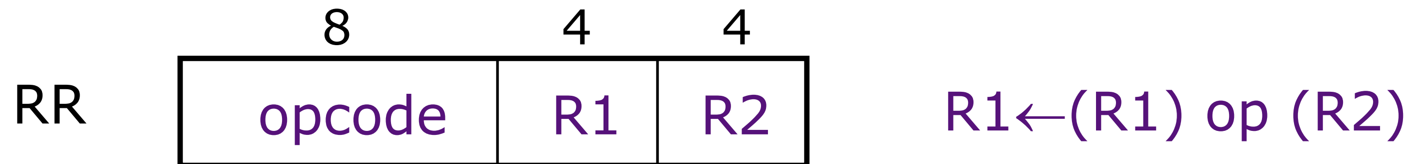
- A 32-bit machine with 24-bit addresses
  - *No instruction contains a 24-bit address !*

IBM 360: Some Addressing Modes



R1←(R1) op (R2)

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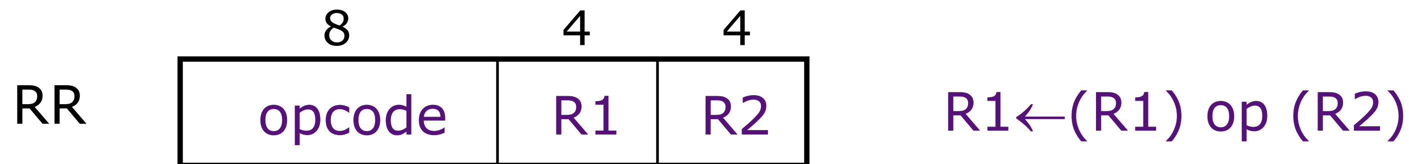
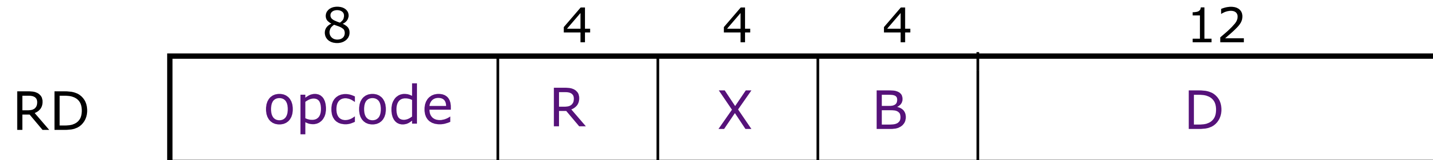
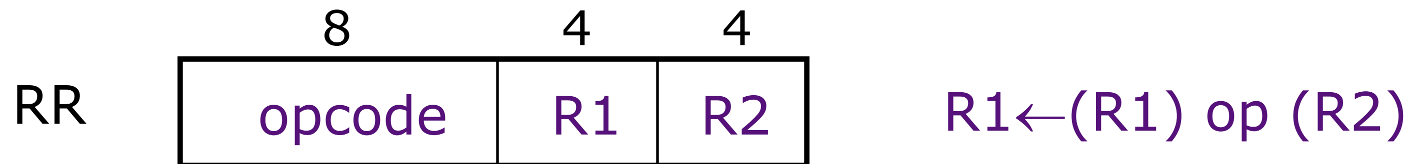




IBM 360: Some Addressing Modes

RR



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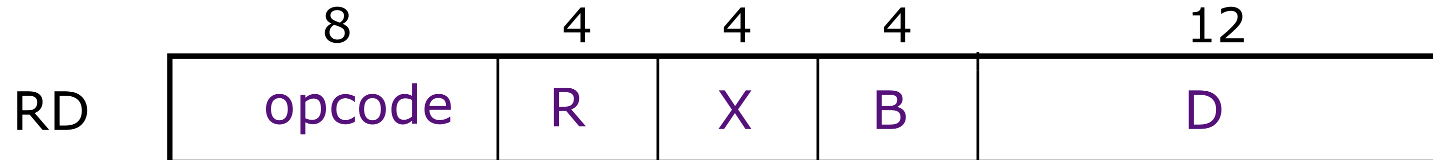

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a 24-bit address is formed by adding the 12-bit displacement (D) to a base register (B) and an Index register (X), if desired

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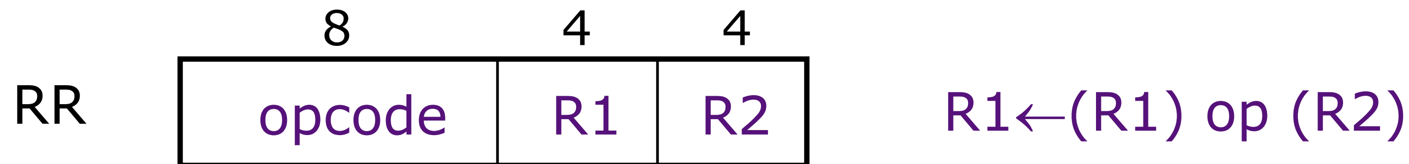

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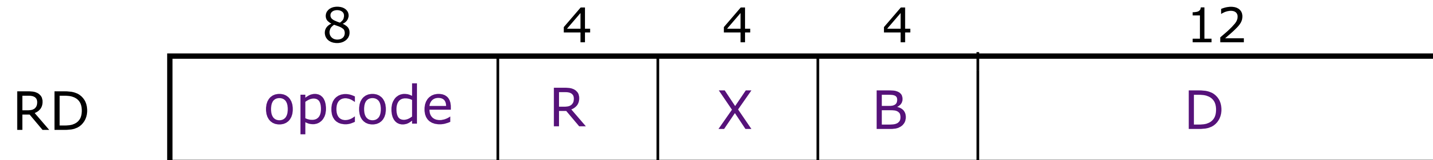

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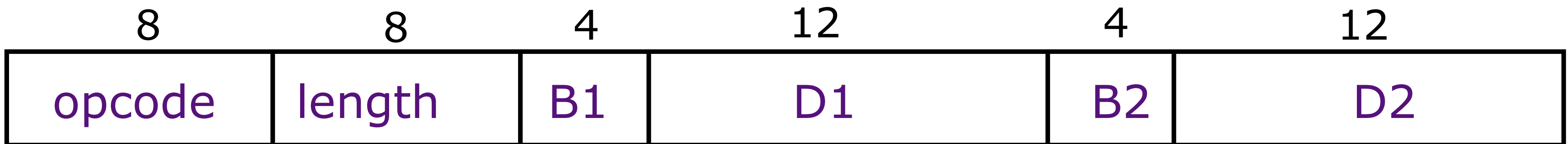
The most common formats for arithmetic & logic instructions, as well as Load and Store instructions

IBM 360: Character String Operations



SS format: store to store instructions

M[(B1) + D1] ← M[(B1) + D1] op M[(B2) + D2]

iterate "length" times

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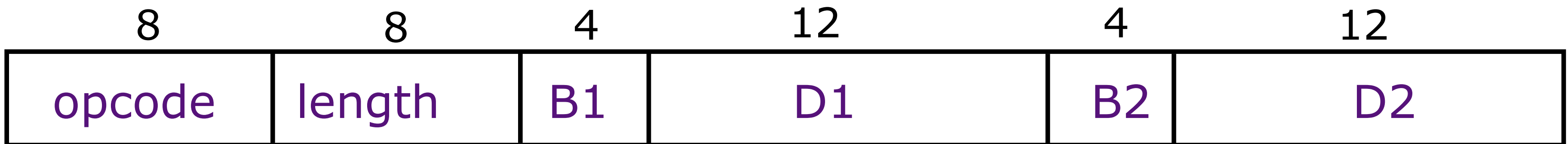

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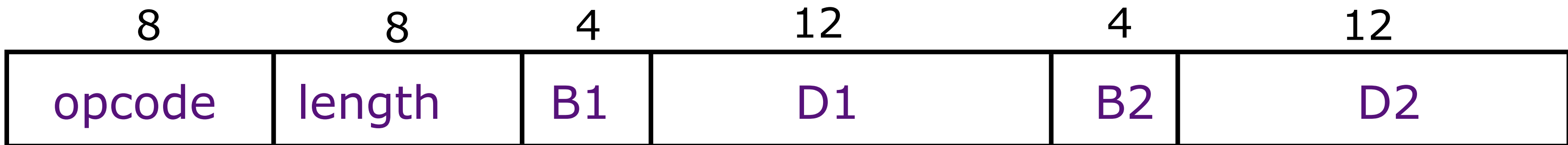

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Multiple memory operations per instruction complicates exception & interrupt handling

IBM 360: Branches & Condition Codes

- Arithmetic and logic instructions set *condition codes*
  - equal to zero
  - greater than zero
  - overflow
  - carry...
- I/O instructions also set condition codes
  - channel busy
- Conditional branch instructions are based on testing condition code registers (CC's)
  - RX and RR formats
    - BC_ branch conditionally
    - BAL_ branch and link, i.e., R15 $\leftarrow$ (PC)+1 *for subroutine calls*

      $\Rightarrow$ CC's must be part of the PSW

IBM 360: Precise Interrupts

- IBM 360 ISA (Instruction Set Architecture) preserves sequential execution model

- Programmers view of machine was that each instruction either completed or signaled a fault before the next instruction began execution

- Exception/interrupt behavior identical across family of implementations

IBM 360: Initial Implementations (1964)

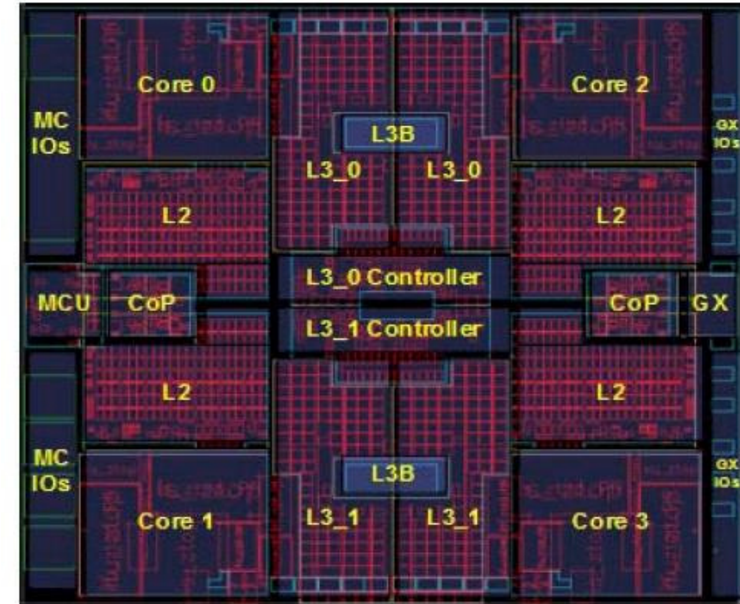
	Model 30	*. . .*	*Model 70*
Memory Capacity	8K - 64 KB		256K - 512 KB
Memory Cycle	2.0μs	...	1.0μs
Datapath	8-bit		64-bit
Circuit Delay	30 nsec/level		5 nsec/level
Registers	in Main Store		in Transistor
Control Store	Read only 1μsec		Dedicated circuits

- Six implementations (Models, 30, 40, 50, 60, 62, 70)
- 50X performance difference cross models
- *ISA completely hid the underlying technological differences between various models.*

With minor modifications, IBM 360 ISA is still in use

IBM 360: Forty-Six years later… zEnterprise196 Microprocessor

- 1.4 billion transistors, Quad core design
- Up to 96 cores (80 visible to OS) in one multichip module
- 5.2 GHz, IBM 45nm SOI CMOS technology
- 64-bit virtual addressing
  - original 360 was 24-bit; 370 was a 31-bit extension
- Superscalar, out-of-order
  - Up to 72 instructions in flight
- Variable length instruction pipeline: 15-17 stages
- Each core has 2 integer units, 2 load-store units and 2 floating point units
- 8K-entry Branch Target Buffer
  - Very large buffer to support commercial workload
- Four Levels of caches:
  - 64KB L1 I-cache, 128KB L1 D-cache
  - 1.5MB L2 cache per core
  - 24MB shared on-chip L3 cache
  - 192MB shared off-chip L4 cache



[September 2010]

Instruction Set Architecture (ISA) versus Implementation

- ISA is the hardware/software interface
  - Defines set of programmer visible state
  - Defines data types
  - Defines instruction semantics (operations, sequencing)
  - Defines instruction format (bit encoding)
  - Examples: *MIPS, Alpha, x86, IBM 360, VAX, ARM, JVM*

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- Many possible implementations of one ISA
  - 360 implementations: model 30 (c. 1964), zEnterprise196 (c. 2010)
  - x86 implementations: *8086 (c. 1978), 80186, 286, 386, 486, Pentium, Pentium Pro, Pentium-4, Core i7, AMD Athlon, AMD Opteron, Transmeta Crusoe, SoftPC*
  - MIPS implementations: *R2000, R4000, R10000, ...*
  - JVM: *HotSpot, PicoJava, ARM Jazelle, ...*

Next lecture:

Implementing an ISA