Instruction Pipelining and Hazards

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Princeton Microarchitecture

Datapath & Control for 2-cycles-per-instruction
Princeton Microarchitecture (redrawn)

Only one of the phases is active in any cycle
⇒ a lot of datapath is not in use at any given time
Princeton Microarchitecture
Overlapped execution

Can we overlap instruction fetch and execute?
Yes, unless IR contains a Load or Store

Which action should be prioritized? Execute

What do we do with Fetch? Stall it

How?
Stalling the instruction fetch

Princeton Microarchitecture

When stall condition is indicated
- *don’t fetch a new instruction and don’t change the PC*
- *insert a nop in the IR*
- *set the Memory Address mux to ALU (not shown)*

What if IR contains a jump or branch instruction?
Need to stall on branches
Princeton Microarchitecture

When IR contains a jump or branch-taken
- *no “structural conflict” for the memory*
- *but we do not have the correct PC value in the PC*
- *memory cannot be used – Address Mux setting is irrelevant*
- *insert a nop in the IR*
- *insert the nextPC (branch-target) address in the PC*
Pipelined Princeton Microarchitecture

- **PCen**
  - PCSrc2
  - PCSrc
  - RegWrite

**IR**
- IRSrc
- 0x4
- Add

**PC**
- clk
- nop
- PC

**ExtSel**
- OpCode
- Add
- Ext
- addr
- wdata
- rdata
- Data
- Memory

**ALU**
- Add
- ALU
- CLA
- Control
- z

**MemWrite**
- clk
- MemWrite
- WBSrc

**WBSrc**
- clk
- stall?
- stall
## Pipelined Princeton: Control Table

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Stall</th>
<th>Ext Sel</th>
<th>B Src</th>
<th>Op Sel</th>
<th>Mem W</th>
<th>Reg W</th>
<th>WB Src</th>
<th>Reg Dst</th>
<th>PC Src1</th>
<th>PC Src2</th>
<th>IR Src</th>
<th>MAAddr Src</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALU</td>
<td>no</td>
<td>*</td>
<td>Reg</td>
<td>Func</td>
<td>no</td>
<td>yes</td>
<td>ALU</td>
<td>rd</td>
<td>pc+4</td>
<td>npc</td>
<td>mem</td>
<td>pc</td>
</tr>
<tr>
<td>ALUi</td>
<td>no</td>
<td>sE_{16}</td>
<td>Imm</td>
<td>Op</td>
<td>no</td>
<td>yes</td>
<td>ALU</td>
<td>rt</td>
<td>pc+4</td>
<td>npc</td>
<td>mem</td>
<td>pc</td>
</tr>
<tr>
<td>ALUiu</td>
<td>no</td>
<td>uE_{16}</td>
<td>Imm</td>
<td>Op</td>
<td>no</td>
<td>yes</td>
<td>ALU</td>
<td>rt</td>
<td>pc+4</td>
<td>npc</td>
<td>mem</td>
<td>pc</td>
</tr>
<tr>
<td>LW</td>
<td>yes</td>
<td>sE_{16}</td>
<td>Imm</td>
<td>+</td>
<td>no</td>
<td>yes</td>
<td>Mem</td>
<td>rt</td>
<td>pc+4</td>
<td>pc</td>
<td>nop</td>
<td>ALU</td>
</tr>
<tr>
<td>SW</td>
<td>yes</td>
<td>sE_{16}</td>
<td>Imm</td>
<td>+</td>
<td>yes</td>
<td>no</td>
<td>*</td>
<td>*</td>
<td>pc+4</td>
<td>pc</td>
<td>nop</td>
<td>ALU</td>
</tr>
<tr>
<td>BEQZ_{z=0}</td>
<td>yes</td>
<td>sE_{16}</td>
<td>*</td>
<td>0?</td>
<td>no</td>
<td>no</td>
<td>*</td>
<td>*</td>
<td>br</td>
<td>npc</td>
<td>nop</td>
<td>*</td>
</tr>
<tr>
<td>BEQZ_{z=1}</td>
<td>no</td>
<td>sE_{16}</td>
<td>*</td>
<td>0?</td>
<td>no</td>
<td>no</td>
<td>*</td>
<td>*</td>
<td>pc+4</td>
<td>npc</td>
<td>mem</td>
<td>pc</td>
</tr>
<tr>
<td>J</td>
<td>yes</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>no</td>
<td>no</td>
<td>*</td>
<td>*</td>
<td>jabs</td>
<td>npc</td>
<td>nop</td>
<td>*</td>
</tr>
<tr>
<td>JAL</td>
<td>yes</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>no</td>
<td>yes</td>
<td>PC</td>
<td>R31</td>
<td>jabs</td>
<td>npc</td>
<td>nop</td>
<td>*</td>
</tr>
<tr>
<td>JR</td>
<td>yes</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>no</td>
<td>no</td>
<td>*</td>
<td>*</td>
<td>rind</td>
<td>npc</td>
<td>nop</td>
<td>*</td>
</tr>
<tr>
<td>JALR</td>
<td>yes</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>no</td>
<td>yes</td>
<td>PC</td>
<td>R31</td>
<td>rind</td>
<td>npc</td>
<td>nop</td>
<td>*</td>
</tr>
<tr>
<td>NOP</td>
<td>no</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>no</td>
<td>no</td>
<td>*</td>
<td>*</td>
<td>pc+4</td>
<td>npc</td>
<td>mem</td>
<td>pc</td>
</tr>
</tbody>
</table>

BSrc = Reg / Imm ; WBSrc = ALU / Mem / PC; IRSrc = nop/mem; MAAddr Src = pc/ALU
RegDst = rt / rd / R31; PCSrc1 = pc+4 / br / rind / jabs; PCSrc2 = pc/nPC

stall & IRSrc columns are identical
Pipelined Princeton Architecture

Clock: \( t_{\text{C-Princeton}} > t_{\text{RF}} + t_{\text{ALU}} + t_{\text{M}} + t_{\text{WB}} \)

CPI: \((1 - f) + 2f\) cycles per instruction where \( f \) is the fraction of instructions that cause a stall

What is a likely value of \( f \)?
An Ideal Pipeline

- All objects go through the same stages
- No sharing of resources between any two stages
- Propagation delay through all pipeline stages is equal
- The scheduling of an object entering the pipeline is not affected by the objects in other stages

These conditions generally hold for industrial assembly lines.
But what about an instruction pipeline?
Pipelined Datapath

Clock period can be reduced by dividing the execution of an instruction into multiple cycles

\[ t_C > \max \{ t_{IM}, t_{RF}, t_{ALU}, t_{DM}, t_{RW} \} \quad (= t_{DM} \text{ probably}) \]

However, CPI will increase unless instructions are pipelined
How to divide the datapath into stages

Suppose memory is significantly slower than other stages. In particular, suppose

\[
\begin{align*}
    t_{IM} &= 10 \text{ units} \\
    t_{DM} &= 10 \text{ units} \\
    t_{ALU} &= 5 \text{ units} \\
    t_{RF} &= 1 \text{ unit} \\
    t_{RW} &= 1 \text{ unit}
\end{align*}
\]

Since the slowest stage determines the clock, it may be possible to combine some stages without any loss of performance.
Alternative Pipelining

\[ t_C > \max \{ t_{IM}, t_{RF}+t_{ALU}, t_{DM}+t_{RW} \} = t_{DM} + t_{RW} \]

⇒ *increase the critical path by 10%*

Write-back stage takes much less time than other stages. Suppose we combined it with the memory phase.
## Maximum Speedup by Pipelining

<table>
<thead>
<tr>
<th>Assumptions</th>
<th>Unpipelined $t_C$</th>
<th>Pipelined $t_C$</th>
<th>Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. $t_{IM} = t_{DM} = 10$, $t_{ALU} = 5$, $t_{RF} = t_{RW} = 1$ 4-stage pipeline</td>
<td>27</td>
<td>10</td>
<td>2.7</td>
</tr>
<tr>
<td>2. $t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5$ 4-stage pipeline</td>
<td>25</td>
<td>10</td>
<td>2.5</td>
</tr>
<tr>
<td>3. $t_{IM} = t_{DM} = t_{ALU} = t_{RF} = t_{RW} = 5$ 5-stage pipeline</td>
<td>25</td>
<td>5</td>
<td>5.0</td>
</tr>
</tbody>
</table>

What seems to be the message here?

*One can achieve higher speedup with more pipeline stages.*
5-Stage Pipelined Execution

Instruction Flow Diagram

**I-Fetch (IF)**
- **time**
  - instruction1
  - instruction2
  - instruction3
  - instruction4
  - instruction5

**Decode, Reg. Fetch (ID)**
- t0
  - IF
- t1
  - ID
- t2
  - EX
- t3
  - MA
- t4
  - WB

**Execute (EX)**
- t4
  - MA
- t5
  - WB

**Memory (MA)**
- t5
  - WB

**Write-Back (WB)**
- t6
- t7
- . . .
5-Stage Pipelined Execution
Resource Usage Diagram
Pipelined Execution: ALU Instructions

Not quite correct!

We need an Instruction Reg (IR) for each stage
Pipelined MIPS Datapath
without jumps

Control Points Need to Be Connected

What else is needed?
How instructions can interact with each other in a pipeline

- An instruction in the pipeline may need a resource being used by another instruction in the pipeline \(\rightarrow\) **structural hazard**

- An instruction may depend on something produced by an earlier instruction
  - Dependence may be for a data calculation \(\rightarrow\) **data hazard**
  - Dependence may be for calculating the next PC \(\rightarrow\) **control hazard** (branches, interrupts)
Data Hazards

\[
r_4 \leftarrow r_1 + 10
\]

\[
r_4 \leftarrow r_1 + 17
\]

\[
r_1 \text{ is stale. Oops!}
\]
Resolving Data Hazards

Strategy 1: Wait for the result to be available by freezing earlier pipeline stages → **interlocks**

Strategy 2: Route data as soon as possible after it is calculated to the earlier pipeline stage → **bypass**

Strategy 3: Speculate on the dependence
Two cases:
- Guessed correctly → do nothing
- Guessed incorrectly → kill and restart
Resolving Data Hazards (1)

Strategy 1:

*Wait for the result to be available by freezing earlier pipeline stages → interlocks*
Feedback to Resolve Hazards

- Later stages provide dependence information to earlier stages which can stall (or kill) instructions.

- Controlling a pipeline in this manner works provided the instruction at stage $i+1$ can complete without any interference from instructions in stages 1 to $i$ (otherwise, deadlocks may occur).
Interlocks to resolve Data Hazards

Stall Condition

... r1 ← r0 + 10
r4 ← r1 + 17
...
Stalled Stages and Pipeline Bubbles

\[
\begin{align*}
\text{time} & \quad t_0 & t_1 & t_2 & t_3 & t_4 & t_5 & t_6 & t_7 & \ldots \ \\
(I_1) & \quad r_1 & \leftarrow (r_0) + 10 & \text{IF}_1 & \text{ID}_1 & \text{EX}_1 & \text{MA}_1 & \text{WB}_1 \\
(I_2) & \quad r_4 & \leftarrow (r_1) + 17 & \text{IF}_2 & \text{ID}_2 & \text{ID}_2 & \text{ID}_2 & \text{IF}_3 \\
(I_3) & \quad \text{IF}_3 & \text{IF}_3 & \text{IF}_3 \\
(I_4) & \quad \text{IF}_4 & \text{ID}_4 & \text{EX}_4 & \text{MA}_4 & \text{WB}_4 \\
(I_5) & \quad \text{IF}_5 & \text{ID}_5 & \text{EX}_5 & \text{MA}_5 & \text{WB}_5 \\
\end{align*}
\]

\text{Resource Usage}

\[
\begin{align*}
\text{IF} & \quad I_1 & I_2 & I_3 & I_3 & I_3 & I_4 & I_5 & \ldots \\
\text{ID} & \quad I_1 & I_2 & I_2 & I_2 & I_3 & I_4 & I_5 & \ldots \\
\text{EX} & \quad I_1 & \text{nop} & \text{nop} & \text{nop} & \text{nop} & I_2 & I_3 & I_4 & I_5 \\
\text{MA} & \quad I_1 & \text{nop} & \text{nop} & \text{nop} & \text{nop} & \text{nop} & I_2 & I_3 & I_4 & I_5 \\
\text{WB} & \quad I_1 & \text{nop} & \text{nop} & \text{nop} & \text{nop} & \text{nop} & \text{nop} & I_2 & I_3 & I_4 & I_5 \\
\end{align*}
\]

\[
\begin{align*}
\text{nop} & \Rightarrow \quad \text{pipeline bubble}
\end{align*}
\]
Interlock Control Logic

Compare the source registers of the instruction in the decode stage with the destination register of the uncommitted instructions.