Instruction Pipelining: Hazard Resolution, Timing Constraints

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Resolving Data Hazards

Strategy 1: *Wait for the result to be available by freezing earlier pipeline stages → interlocks*

Strategy 2: *Route data as soon as possible after it is calculated to the earlier pipeline stage → bypass*

Strategy 3: *Speculate on the dependence*
*Two cases:*

- *Guessed correctly → no special action required*
- *Guessed incorrectly → kill and restart*
Resolving Data Hazards (1)

**Strategy 1:**

*Wait for the result to be available by freezing earlier pipeline stages* → *interlocks*
Interlocks to resolve Data Hazards

**Stall Condition**

```
... r1 ← r0 + 10
r4 ← r1 + 17
...
```

How do we know when to stall?
Interlock Control Logic

Compare the source registers of the instruction in the decode stage with the destination register of the uncommitted instructions.
Interlocks Control Logic

ignoring jumps & branches

Should we always stall if the rs field matches some rd?

not every instruction writes a register ⇒ we
not every instruction reads a register ⇒ re
# Source & Destination Registers

### R-type:

<table>
<thead>
<tr>
<th>op</th>
<th>rs</th>
<th>rt</th>
<th>rd</th>
<th>func</th>
</tr>
</thead>
</table>

### I-type:

<table>
<thead>
<tr>
<th>op</th>
<th>rs</th>
<th>rt</th>
<th>immediate16</th>
</tr>
</thead>
</table>

### J-type:

<table>
<thead>
<tr>
<th>op</th>
<th>immediate26</th>
</tr>
</thead>
</table>

### source(s) destination

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALU</td>
<td>rd ← (rs) func (rt)</td>
</tr>
<tr>
<td>ALUi</td>
<td>rt ← (rs) op imm</td>
</tr>
<tr>
<td>LW</td>
<td>rt ← M [(rs) + imm]</td>
</tr>
<tr>
<td>SW</td>
<td>M [(rs) + imm] ← (rt)</td>
</tr>
<tr>
<td>BZ</td>
<td>cond (rs)</td>
</tr>
<tr>
<td>true:</td>
<td>PC ← (PC) + imm</td>
</tr>
<tr>
<td>false:</td>
<td>PC ← (PC) + 4</td>
</tr>
<tr>
<td>J</td>
<td>PC ← (PC) + imm</td>
</tr>
<tr>
<td>JAL</td>
<td>r31 ← (PC), PC ← (PC) + imm</td>
</tr>
<tr>
<td>JR</td>
<td>PC ← (rs)</td>
</tr>
<tr>
<td>JALR</td>
<td>r31 ← (PC), PC ← (rs)</td>
</tr>
</tbody>
</table>
Deriving the Stall Signal

\[ C_{\text{dest}} \]
\[ \begin{align*}
ws &= \text{Case opcode} \\
\text{ALU} &\Rightarrow rd \\
\text{ALUi, LW} &\Rightarrow rt \\
\text{JAL, JALR} &\Rightarrow R31 \\
\end{align*} \]

\[ we = \text{Case opcode} \\
\text{ALU, ALUi, LW} &\Rightarrow (ws \neq 0) \\
\text{JAL, JALR} &\Rightarrow on \\
... &\Rightarrow off \\
\]

\[ C_{\text{re}} \]
\[ \begin{align*}
\text{re1} &= \text{Case opcode} \\
\text{ALU, ALUi, LW} &\Rightarrow on \\
\text{JR, JALR} &\Rightarrow off \\
\text{J, JAL} &\Rightarrow off \\
\end{align*} \]

\[ \text{re2} = \text{Case opcode} \\
\text{ALU, SW} &\Rightarrow on \\
... &\Rightarrow off \\
\]

\[ C_{\text{stall}} \]
\[ \begin{align*}
stall &= ((rs_D = ws_E) \cdot we_E + \\
(rs_D = ws_M) \cdot we_M + \\
(rs_D = ws_W) \cdot we_W) \cdot re1_D + \\
((rt_D = ws_E) \cdot we_E + \\
(rt_D = ws_M) \cdot we_M + \\
(rt_D = ws_W) \cdot we_W) \cdot re2_D \\
\end{align*} \]

This is not the full story!
Hazards due to Loads & Stores

Stall Condition

What if 
(r1)+7 = (r3)+5 ?

Is there any possible data hazard in this instruction sequence?

M[(r1)+7] ← (r2)
r4 ← M[(r3)+5]

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http://www.csg.csail.mit.edu/6.823
Sanchez & Emer
Load & Store Hazards

However, the hazard is avoided because our memory system completes writes in one cycle!

Load/Store hazards are sometimes resolved in the pipeline and sometimes in the memory system itself.

More on this later in the course.
Resolving Data Hazards (2)

Strategy 2:

Route data as soon as possible after it is calculated to the earlier pipeline stage → bypass
Bypassing

Each *stall or kill* introduces a bubble $\Rightarrow CPI > 1$

When is data actually available? **At Execute**

A new datapath, i.e., *a bypass*, can get the data from the output of the ALU to its input
Adding a Bypass

When does this bypass help?

\( I_1 \)  
\[ r1 \leftarrow r0 + 10 \]  
yes

\( I_2 \)  
\[ r4 \leftarrow r1 + 17 \]  

\( JAL \ 500 \)  
\[ r4 \leftarrow r31 + 17 \]  
no
The Bypass Signal

Deriving it from the Stall Signal

\[\text{stall} = ((\text{rs}_D = \text{ws}_E) \cdot \text{we}_E) + (\text{rs}_D = \text{ws}_M) \cdot \text{we}_M + (\text{rs}_D = \text{ws}_W) \cdot \text{we}_W) \cdot \text{re}^{1_D} \]
\[+ (\text{rt}_D = \text{ws}_E) \cdot \text{we}_E + (\text{rt}_D = \text{ws}_M) \cdot \text{we}_M + (\text{rt}_D = \text{ws}_W) \cdot \text{we}_W) \cdot \text{re}^{2_D} \]

ws = Case opcode
- ALU \implies \text{rd}
- ALUi, LW \implies \text{rt}
- JAL, JALR \implies \text{R31}

we = Case opcode
- ALU, ALUi, LW \implies (ws \neq 0)
- JAL, JALR \implies \text{on}
- ... \implies \text{off}

ASrc = (\text{rs}_D = \text{ws}_E) \cdot \text{we}_E \cdot \text{re}^{1_D}

Is this correct?

No because only ALU and ALUi instructions can benefit from this bypass

How might we address this?

Split we_E into two components: we-bypass, we-stall
Bypass and Stall Signals

Split $we_E$ into two components: $we$-bypass, $we$-stall

$we$-bypass$E = \text{Case opcode}_E$
- ALU, ALUi $\Rightarrow (ws \neq 0)$
- ... $\Rightarrow \text{off}$

$we$-stall$E = \text{Case opcode}_E$
- LW $\Rightarrow (ws \neq 0)$
- JAL, JALR $\Rightarrow \text{on}$
- ... $\Rightarrow \text{off}$

$$\text{ASrc} = (rs_D = ws_E) \cdot we$-bypass$E \cdot re_{1D}$$

$$\text{stall} = ((rs_D = ws_E) \cdot we$-stall$E +
(rs_D = ws_M) \cdot we_M + (rs_D = ws_W) \cdot we_W) \cdot re_{1D} +
((rt_D = ws_E) \cdot we_E + (rt_D = ws_M) \cdot we_M + (rt_D = ws_W) \cdot we_W) \cdot re_{2D}$$
Is there still a need for the stall signal?

\[
\text{stall} = (rs_D = ws_E) \cdot (\text{opcode}_E = \text{LW}_E) \cdot (ws_E \neq 0) \cdot \text{re1}_D + (rt_D = ws_E) \cdot (\text{opcode}_E = \text{LW}_E) \cdot (ws_E \neq 0) \cdot \text{re2}_D
\]
Resolving Data Hazards (3)

**Strategy 3:**

*Speculate on the dependence. Two cases:*

- **Guessed correctly** → no special action required
- **Guessed incorrectly** → kill and restart
Instruction to Instruction Dependence

• What do we need to calculate next PC:
  – For Jumps
    • Opcode, offset and PC
  – For Jump Register
    • Opcode and register value
  – For Conditional Branches
    • Opcode, offset, PC, and register (for condition)
  – For all others
    • Opcode and PC

• In what stage do we know these?
  – PC → Fetch
  – Opcode, offset → Decode (or Fetch?)
  – Register value → Decode
  – Branch condition ((rs)==0) → Execute (or Decode?)
NextPC Calculation Bubbles

\[
(I_1) \quad r_1 \leftarrow (r_0) + 10 \\
(I_2) \quad r_3 \leftarrow (r_2) + 17 \\
(I_3) \\
(I_4)
\]

\[
\begin{array}{cccccccc}
& \text{time} & t0 & t1 & t2 & t3 & t4 & t5 & t6 & t7 & \ldots \\
& \text{IF}_1 & \text{ID}_1 & \text{EX}_1 & \text{MA}_1 & \text{WB}_1 \\
& \text{IF}_2 & \text{IF}_2 & \text{ID}_2 & \text{EX}_2 & \text{MA}_2 & \text{WB}_2 \\
& \text{IF}_3 & \text{IF}_3 & \text{ID}_3 & \text{EX}_3 & \text{MA}_3 & \text{WB}_3 \\
& \text{IF}_4 & \text{IF}_4 & \text{ID}_4 & \text{EX}_4 & \text{MA}_4 & \text{WB}_4 \\
\end{array}
\]

Resource Usage

\[
\begin{array}{cccccccc}
\text{IF} & I_1 & \text{nop} & I_2 & \text{nop} & I_3 & \text{nop} & I_4 \\
\text{ID} & I_1 & \text{nop} & I_2 & \text{nop} & I_3 & \text{nop} & I_4 \\
\text{EX} & I_1 & \text{nop} & I_2 & \text{nop} & I_3 & \text{nop} & I_4 \\
\text{MA} & I_1 & \text{nop} & I_2 & \text{nop} & I_3 & \text{nop} & I_4 \\
\text{WB} & I_1 & \text{nop} & I_2 & \text{nop} & I_3 & \text{nop} & I_4 \\
\end{array}
\]

\[\text{nop} \Rightarrow \text{pipeline bubble}\]

What’s a good guess for next PC? PC+4
Speculate NextPC is PC+4

What happens on mis-speculation, i.e., when next instruction is not PC+4?

How?
Pipelining Jumps

To kill a fetched instruction -- Insert a nop in IR

Any interaction between stall and jump?

\[ \text{IRSrc}_D = \text{Case opcode}_D \]
- \( J, \text{JAL} \) \( \Rightarrow \text{nop} \)
- \( \ldots \) \( \Rightarrow \text{IM} \)

I_1 096 ADD
I_2 100 J 200
I_3 104 ADD
I_4 304 ADD

I_2 \text{ stall}
Jump Pipeline Diagrams

\[ \text{time} \]
\[ t_0 \ t_1 \ t_2 \ t_3 \ t_4 \ t_5 \ t_6 \ t_7 \ldots \]

(I_1) 096: ADD
(I_2) 100: J 200
(I_3) 104: ADD
(I_4) 304: ADD

Resource Usage

\[ \text{Resource Usage} \]

IF \ \ I_1 \ \ I_2 \ \ I_3 \ \ I_4 \ \ I_5
ID \ \ I_1 \ \ I_2 \ \ I_3 \ \ I_4 \ \ I_5
EX \ \ I_1 \ \ I_2 \ \ I_3 \ \ I_4 \ \ I_5
MA \ \ I_1 \ \ I_2 \ \ I_3 \ \ I_4 \ \ I_5
WB \ \ I_1 \ \ I_2 \ \ I_3 \ \ I_4 \ \ I_5

nop \ \Rightarrow \ \ pipeline \ bubble
Pipelining Conditional Branches

Branch condition is not known until the execute stage

what action should be taken in the decode stage?
Pipelining Conditional Branches

If the branch is taken
- kill the two following instructions
- the instruction at the decode stage is not valid

⇒ stall signal is not valid
Pipelining Conditional Branches

If the branch is taken
- kill the two following instructions
- the instruction at the decode stage is not valid

⇒ stall signal is not valid
New Stall Signal

\[
stall = ( ((rs_D = ws_E) \cdot we_E + (rs_D = ws_M) \cdot we_M + (rs_D = ws_W) \cdot we_W) \cdot re1_D
+ ((rt_D = ws_E) \cdot we_E + (rt_D = ws_M) \cdot we_M + (rt_D = ws_W) \cdot we_W) \cdot re2_D
) \cdot !((\text{opcode}_E = \text{BEQZ}) \cdot z + (\text{opcode}_E = \text{BNEZ}) \cdot !z)
\]

Don’t stall if the branch is taken. Why?

Instruction at the decode stage is invalid
Control Equations for PC and IR Muxes

IRS\textsubscript{D} = \text{Case opcode\textsubscript{E}}
\begin{align*}
\text{BEQZ} \cdot z, \text{BNEZ} \cdot !z & \Rightarrow \text{nop} \\
\ldots & \Rightarrow \\
\text{Case opcode}\textsubscript{D} & \\
\text{J, JAL, JR, JALR} & \Rightarrow \text{nop} \\
\ldots & \Rightarrow \text{IM}
\end{align*}

IRS\textsubscript{E} = \text{Case opcode\textsubscript{E}}
\begin{align*}
\text{BEQZ} \cdot z, \text{BNEZ} \cdot !z & \Rightarrow \text{nop} \\
\ldots & \Rightarrow \\
\text{stall} \cdot \text{nop} + !\text{stall} \cdot \text{IR}\textsubscript{D}
\end{align*}

PC\textsubscript{src} = \text{Case opcode\textsubscript{E}}
\begin{align*}
\text{BEQZ} \cdot z, \text{BNEZ} \cdot !z & \Rightarrow \text{br} \\
\ldots & \Rightarrow \\
\text{Case opcode}\textsubscript{D} & \\
\text{J, JAL} & \Rightarrow \text{jabs} \\
\text{JR, JALR} & \Rightarrow \text{rind} \\
\ldots & \Rightarrow \text{pc+4}
\end{align*}

\textit{Give priority to the older instruction, i.e., execute stage instruction over decode stage instruction}.

\textit{pc+4 is a speculative guess}.

\text{nop} \Rightarrow \text{Kill}
\text{br/jabs/rind} \Rightarrow \text{Restart}
\text{pc+4} \Rightarrow \text{Speculate}
Branch Pipeline Diagrams
(resolved in execute stage)

<table>
<thead>
<tr>
<th>time</th>
<th>t0</th>
<th>t1</th>
<th>t2</th>
<th>t3</th>
<th>t4</th>
<th>t5</th>
<th>t6</th>
<th>t7</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_1) 096: ADD</td>
<td>IF_1</td>
<td>ID_1</td>
<td>EX_1</td>
<td>MA_1</td>
<td>WB_1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_2) 100: BEQZ 200</td>
<td>IF_2</td>
<td>ID_2</td>
<td>EX_2</td>
<td>MA_2</td>
<td>WB_2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_3) 104: ADD</td>
<td>IF_3</td>
<td>nop</td>
<td>nop</td>
<td>nop</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_4) 108:</td>
<td>nop</td>
<td>nop</td>
<td>nop</td>
<td>nop</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_5) 304: ADD</td>
<td>IF_5</td>
<td>ID_5</td>
<td>EX_5</td>
<td>MA_5</td>
<td>WB_5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Resource Usage

<table>
<thead>
<tr>
<th>IF</th>
<th>I_1</th>
<th>I_2</th>
<th>I_3</th>
<th>I_4</th>
<th>I_5</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID</td>
<td>I_1</td>
<td>I_2</td>
<td>I_3</td>
<td>nop</td>
<td>I_5</td>
</tr>
<tr>
<td>EX</td>
<td>I_1</td>
<td>I_2</td>
<td>nop</td>
<td>nop</td>
<td>I_5</td>
</tr>
<tr>
<td>MA</td>
<td>I_1</td>
<td>I_2</td>
<td>nop</td>
<td>nop</td>
<td>I_5</td>
</tr>
<tr>
<td>WB</td>
<td>I_1</td>
<td>I_2</td>
<td>nop</td>
<td>nop</td>
<td>I_5</td>
</tr>
</tbody>
</table>

nop ⇒ pipeline bubble
Reducing Branch Penalty (resolve in decode stage)

- One pipeline bubble can be removed if an extra comparator is used in the Decode stage.

`PCSsrc` (pc+4 / jabs / rind/ br)

Pipeline diagram now same as for jumps
Branch Delay Slots (expose control hazard to software)

- Change the ISA semantics so that the instruction that follows a jump or branch is always executed
  - gives compiler the flexibility to put in a useful instruction where normally a pipeline bubble would have resulted.

\[\begin{array}{l|c|l}
I_1 & 096 & ADD \\
I_2 & 100 & BEQZ r1 200 \\
I_3 & 104 & ADD \\
I_4 & 304 & ADD \\
\end{array}\]

Delay slot instruction executed regardless of branch outcome

- Other techniques include branch prediction, which can dramatically reduce the branch penalty... to come later
Why an Instruction may not be dispatched every cycle (CPI>1)

- Full bypassing may be too expensive to implement
  - typically all frequently used paths are provided
  - some infrequently used bypass paths may increase cycle time and counteract the benefit of reducing CPI

- Loads have two cycle latency
  - Instruction after load cannot use load result
  - MIPS-I ISA defined load delay slots, a software-visible pipeline hazard (compiler schedules independent instruction or inserts NOP to avoid hazard). Removed in MIPS-II.

- Conditional branches may cause bubbles
  - kill following instruction(s) if no delay slots

Machines with software-visible delay slots may execute significant number of NOP instructions inserted by the compiler.