6.823 Computer System Architecture
Virtual-channel Router

http://csg.csail.mit.edu/6.823/

This handout introduces an input-buffered, on-chip network router with virtual-channel flow control. It is based on material from Chapter 16 of the book "Principles and Practices of interconnection Networks" by Dally & Towles.

Figure H10-A shows the router's main components. These components can be partitioned broadly into two groups: *datapath* and *control plane*. The router's datapath handles the storage and movement of packet flits. It consists of a set of input units (which buffer arriving flits until they can be forwarded to their desired outputs), a switch, and a set of output units. The remaining blocks implement the control plane, which performs route computation, virtual-channel allocation, and switch allocation.

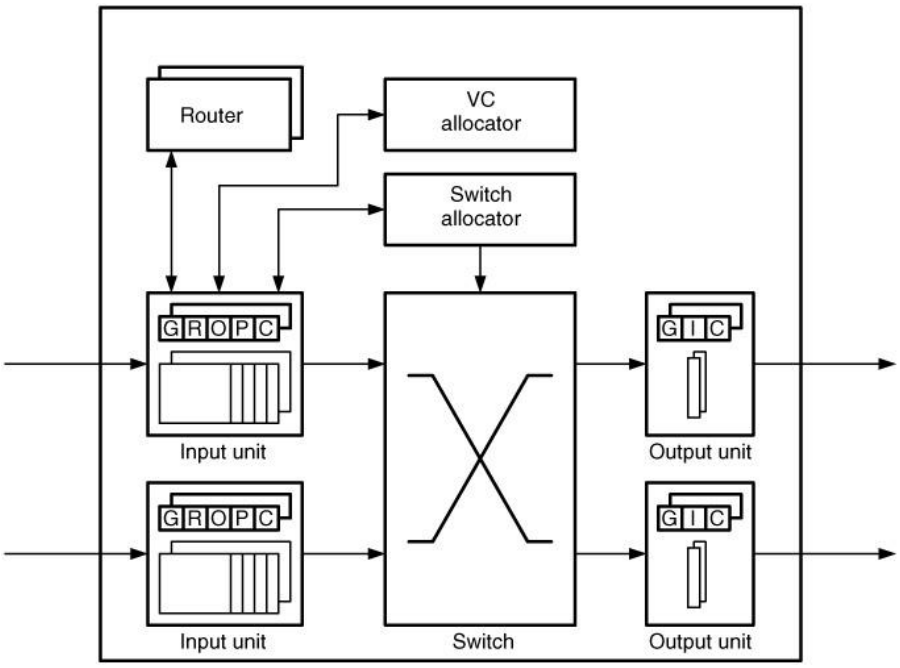

Figure H10-A Virtual-channel router block diagram

Pipeline stages: The router uses a 5-stage pipeline, consisting of route computation (RC), virtual-channel allocation (VA), switch allocation (SA), switch traversal (ST), and link traversal (LT). Only head flits go through RC and VA; all flits traverse SA, ST, and LT. Pipeline stalls may occur in the VA and SA stages if an output virtual channel or time slot on the switch cannot be allocated.

Credit-based flow control: Each time flit leaves the input unit (at the beginning of the ST stage), a credit is sent to the output unit of the upstream router to grant access to the buffer slot. In routers with limited buffer space, the latency of credit handling can limit performance.

Input unit: The input unit maintains the state of each virtual channel associated with that input link. Each input virtual channel uses five fields, described in Table H10-B

Field	***Name***	***Description***
G	Global state	Either idle (I), routing (R), waiting for an output VC (V), active (A), or waiting for credits (C).
R	Route	After routing is completed for a packet, this field holds the output port selected for the packet.
O	Output VC	After virtual-channel allocation is completed for a packet, this field holds the output virtual channel of port R assigned to the packet.
P	Pointers	Flit head and tail pointers into the input buffer. From these pointers, we can also get an implicit count on the number of flits in the buffer for this virtual channel.
C	Credit count	The number of credits (available downstream flit buffers) for output virtual channel O on output port R.

Table H10-B Input virtual channel state fields

Output unit: The output unit forwards the flit to the output channel. Similar to the input unit, each output virtual channel, described in Table H10-C.

Field	***Name***	***Description***
G	Global state	Either idle (I), active (A), or waiting for credits (C).
I	Input VC	Input port and virtual channel that are forwarding flits to this output virtual channel.
C	Credit count	Number of free buffers available to hold flits from this virtual channel at the downstream node

Table H10-C Output virtual channel state fields

Example: The two tables below show a snapshot of the state of a 2-link router with 2 virtual channels per physical channel, shown in Figure H10-D. Suppose all three (red, blue, green) packets need to traverse output 2. The head flits of the red and blue packets have finished RC and VA, while the head flit of the green packet is stalled at the VA stage waiting for an output virtual channel to become available.

	G	R	O	P	C
Input 1 VC1	I				
Input 1 VC2	A (red)	Output 2	VC1	Head: 0 Tail: 1	4
Input 2 VC1	V (green)	Output 2		Head: 0 Tail: 2	
Input 2 VC2	A (blue)	Output 2	VC2	Head: 0 Tail: 3	2

Input virtual channel state table snapshot

	G	I	C
Output 1 VC1	I		
Output 1 VC2	I		
Output 2 VC1	A (red)	Input 1 VC2	4 (not shown)
Output 2 VC2	A (blue)	Input 2 VC2	4 (not shown)

Output virtual channel state table snapshot

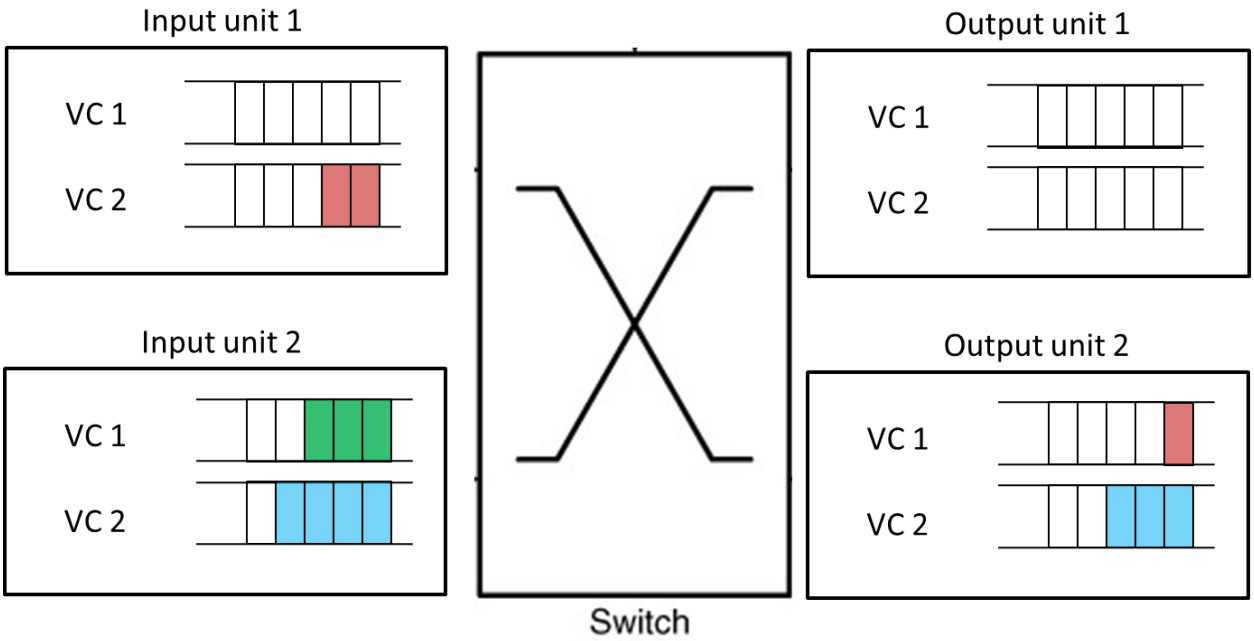

Table H10-D A snapshot of a 2-input-unit, 2-output-unit router with 2 virtual channels

The two tables below show how state fields change over time, assuming a 4-flit packet is routed from input unit 2, virtual channel 2 to output unit 2, virtual channel 2, as shown in Figure H10-E. For simplicity, the credit fields in those two tables are not shown. Assume that, at cycle 0, the full packet is stored in the buffer of input unit 2, virtual channel 2.

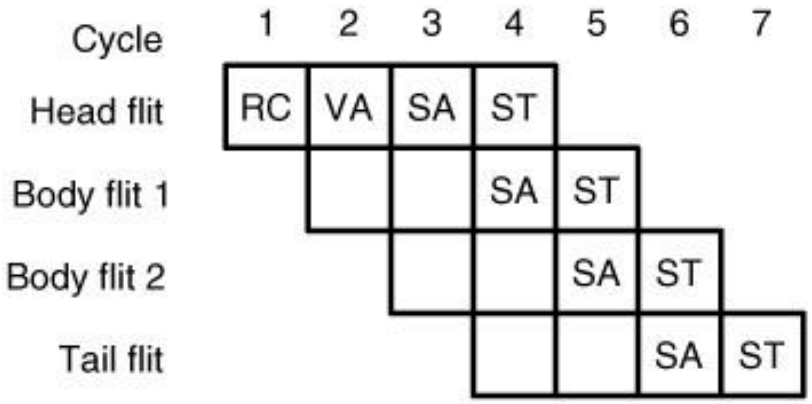

Figure H10-E Pipelined routing of a 4-flit packet

Cycle	**G**	**R**	**O**	**P**
1	R	-	-	Head: 0 Tail: 3
2	V	Output 2	-	Head: 0 Tail: 3
3	A	Output 2	VC2	Head: 0 Tail: 3
4	A	Output 2	VC2	Head: 1 Tail: 3
5	A	Output 2	VC2	Head: 2 Tail: 3
6	A	Output 2	VC2	Head: 3 Tail: 3
7	I	-	-	-

State fields table for input unit 1, virtual channel 2

Cycle	**G**	**I**
1	I	-
2	I	-
3	A	Input 1 VC2
4	A	Input 1 VC2
5	A	Input 1 VC2
6	A	Input 1 VC2
7	A	Input 1 VC2

State fields table for output unit 2, virtual channel 2