Quiz 1 Review

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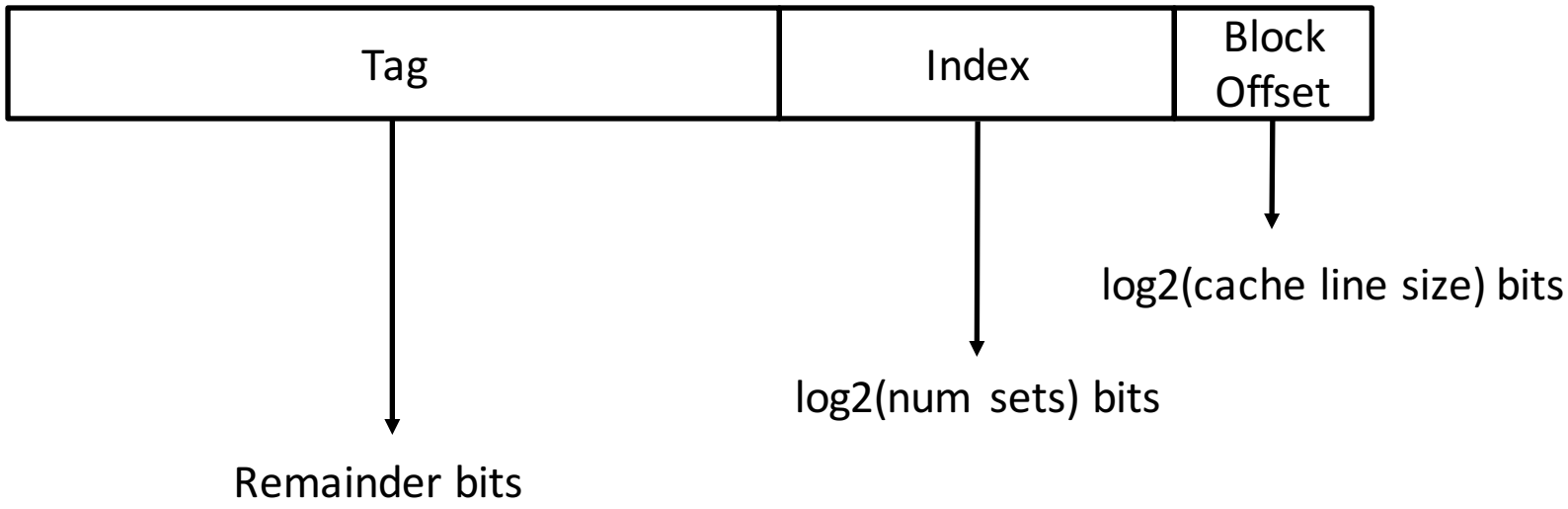
Adapted from: Suvinay Subramanian, 2016

EDSAC

- Accumulator based
- No concept Index Registers, PC
- Use self-modifying code for indirect accesses, subroutine calls etc.

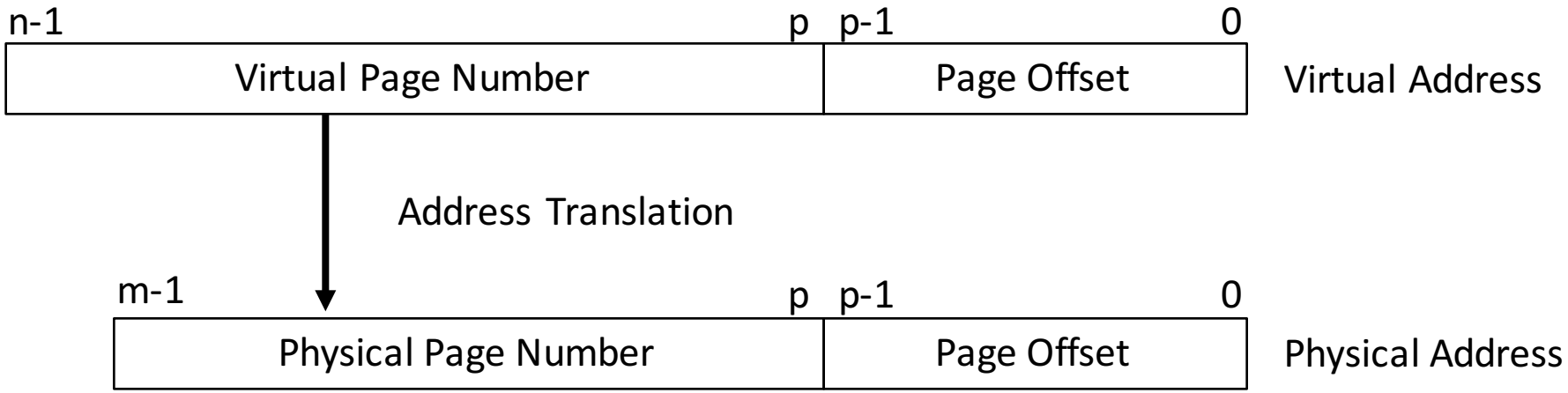
Caches


Tag
Index
Block Offset
log2(cache line size) bits
log2(num sets) bits
Remainder bits

Address Translation

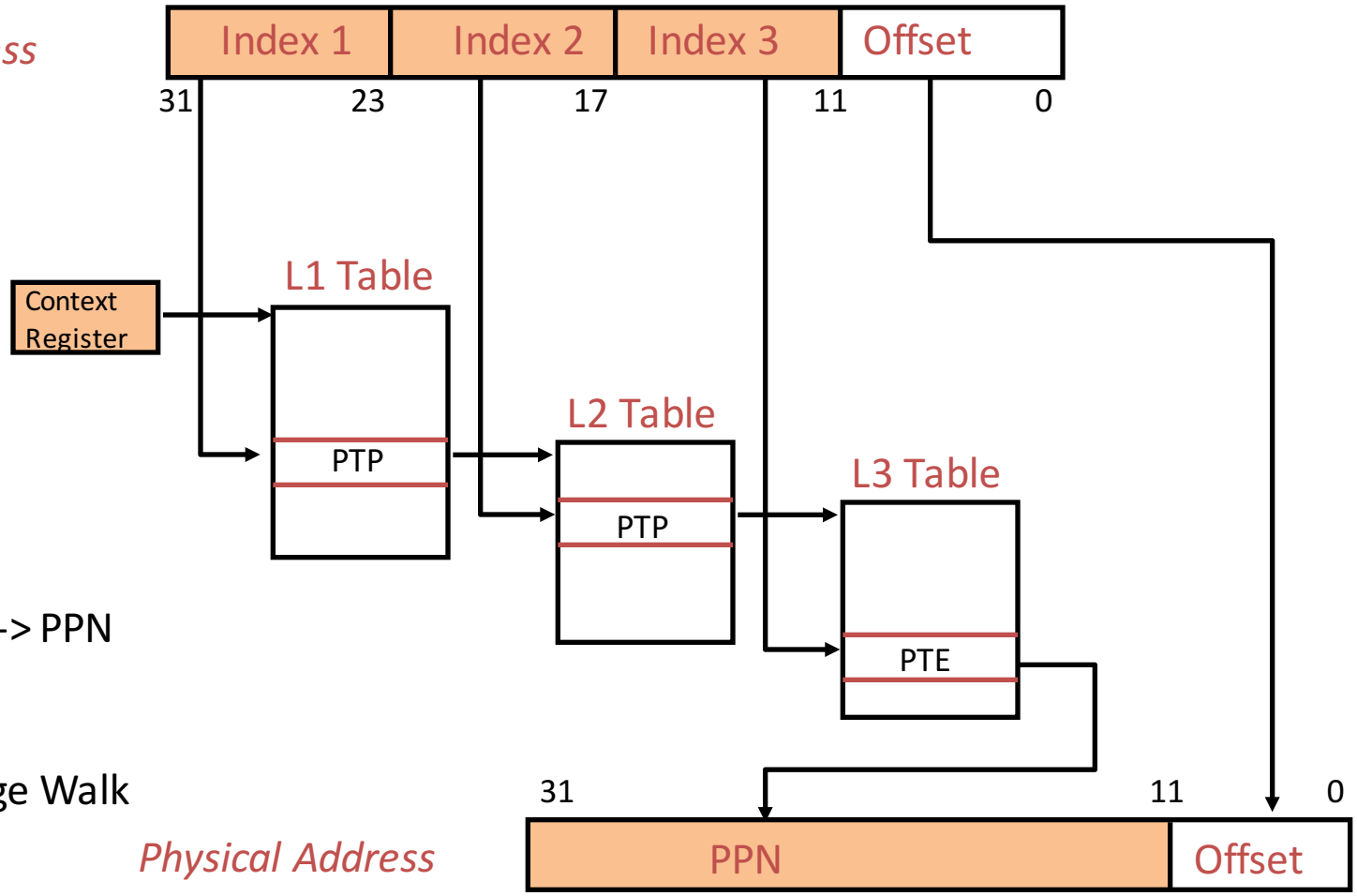
Parameters

- $P = 2^p$ = page size (bytes).
- $N = 2^n$ = Virtual-address limit
- $M = 2^m$ = Physical-address limit



Page offset bits do not change with translation

Hierarchical Page Tables

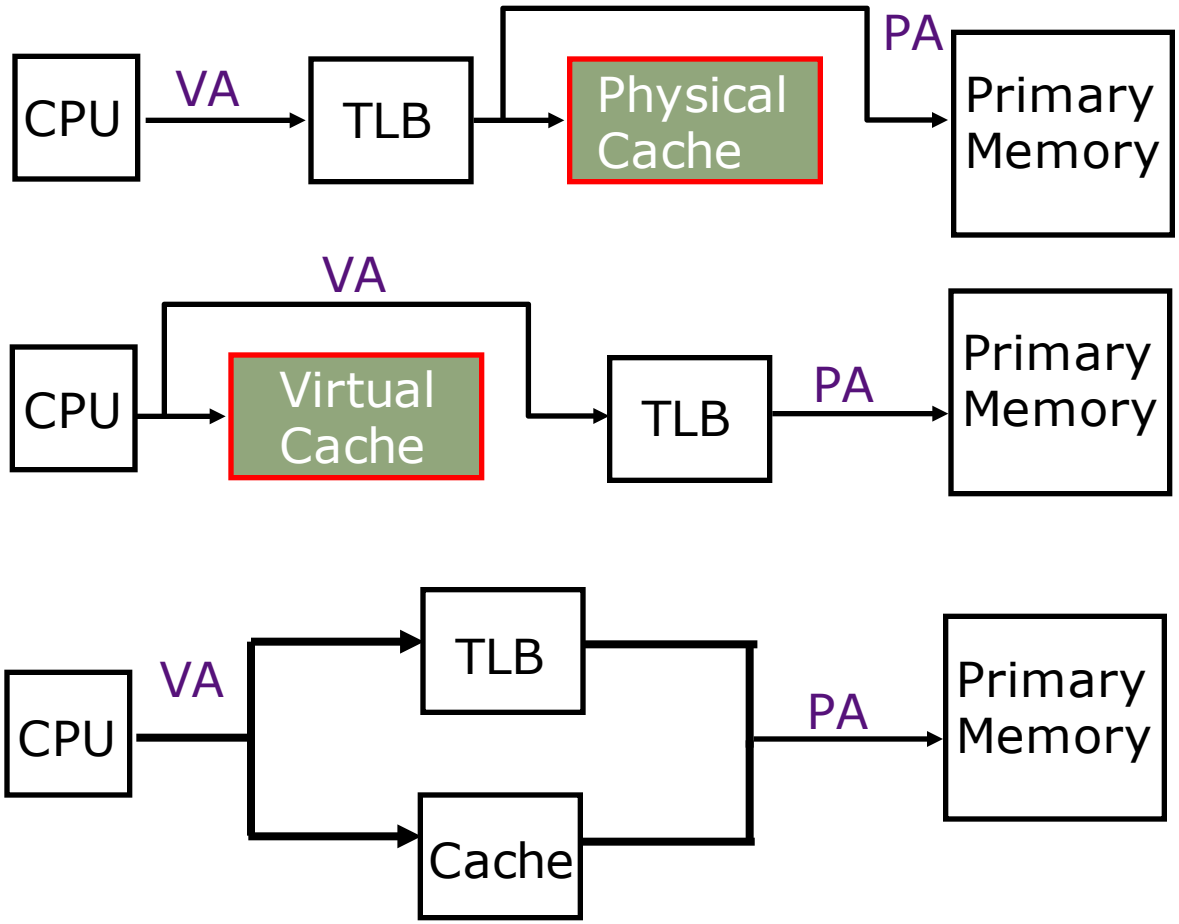


TLB:

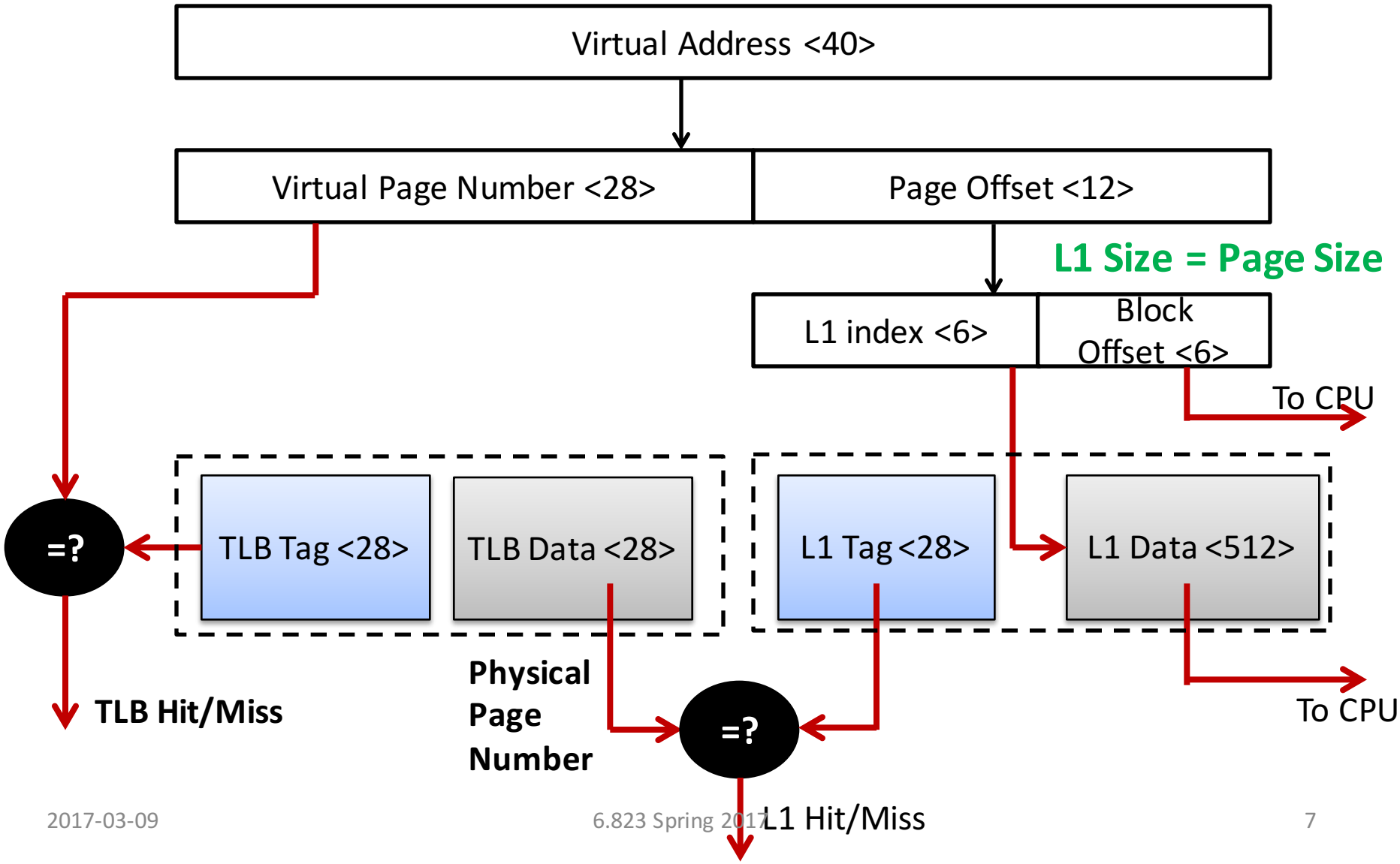
- Holds VPN --> PPN mapping

TLB miss → Page Walk

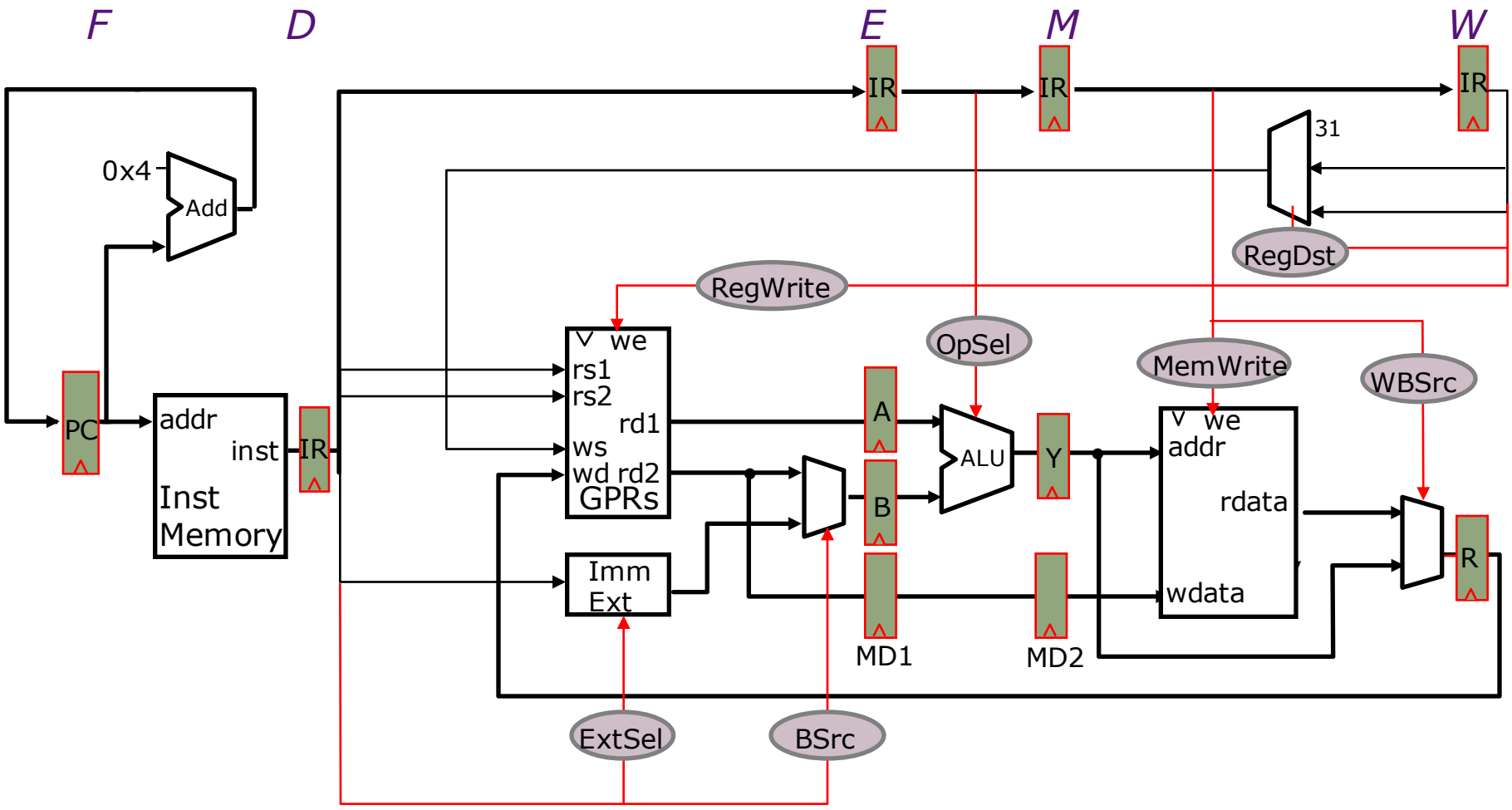
Physical vs Virtual Address Caches?



Concurrent Accesses to TLB and Cache



Pipelining


F
D
E
M
W
IR
IR
IR
0x4
Add
31
RegDst
RegWrite
we
rs1
rs2
rd1
ws
wd rd2
GPRs
OpSel
MemWrite
WBSrc
A
B
ALU
Y
we
addr
rdata
wdata
PC
addr
inst
Inst
Memory
IR
Imm
Ext
MD1
MD2
R
ExtSel
BSrc

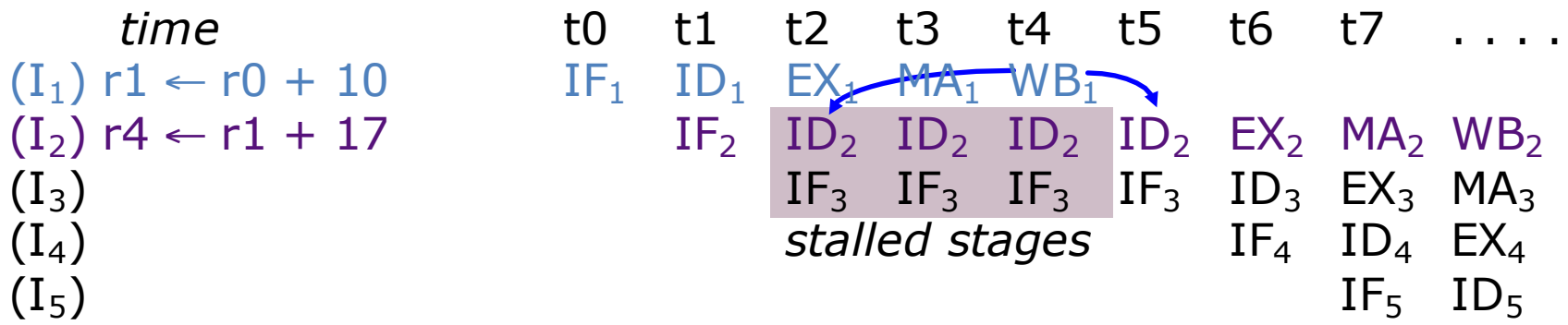
Pipeline Hazards

1. Structural
2. Data
3. Control

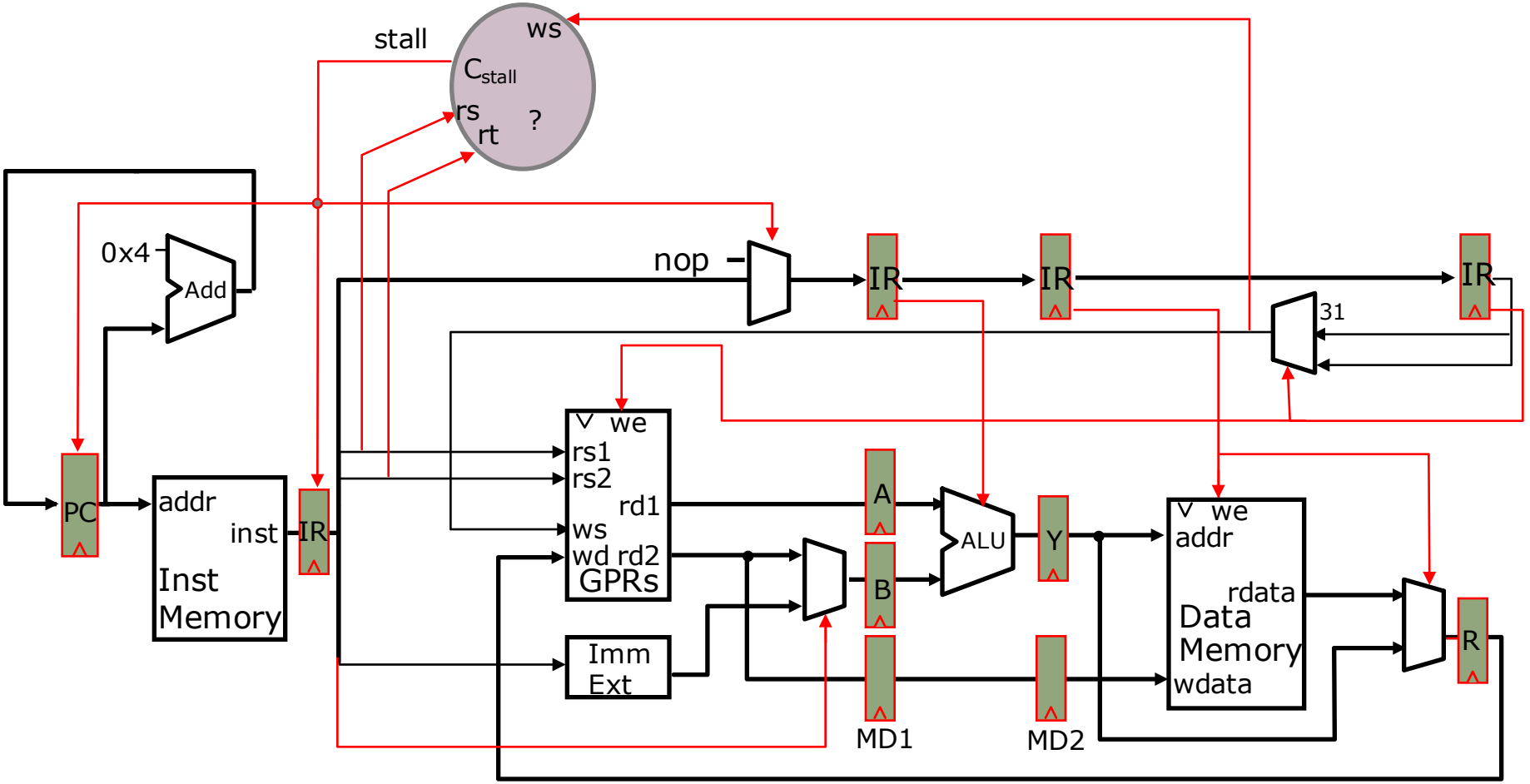
Handling Pipeline Hazards: Recipe

1. Stall
2. Bypass
3. Speculate

Instruction Flow Diagram



Pipelining



Compare the *source registers* of the instruction in the decode stage with the *destination register* of the *uncommitted in*structions.

Mechanics of Processor Design

- Analyze ISA
  - Determine data path requirements
- Select components of data path
  - ALU, Register file etc.
- Analyze implementation of instruction
  - Do we need to bypass, stall, speculate?
  - Assemble control signals

That's All!

I wish you all the best ☺