Memory Management: *From Absolute Addresses to Demand Paging*

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Based on slides from Daniel Sanchez

Recap: Cache Organization

- Caches are small and fast memories that transparently retain recently accessed data

- Cache organizations
  - Direct-mapped
  - Set-associative
  - Fully associative

- Cache performance
  - AMAT = HitLatency + MissRate * MissLatency
  - Minimizing AMAT requires balancing competing tradeoffs

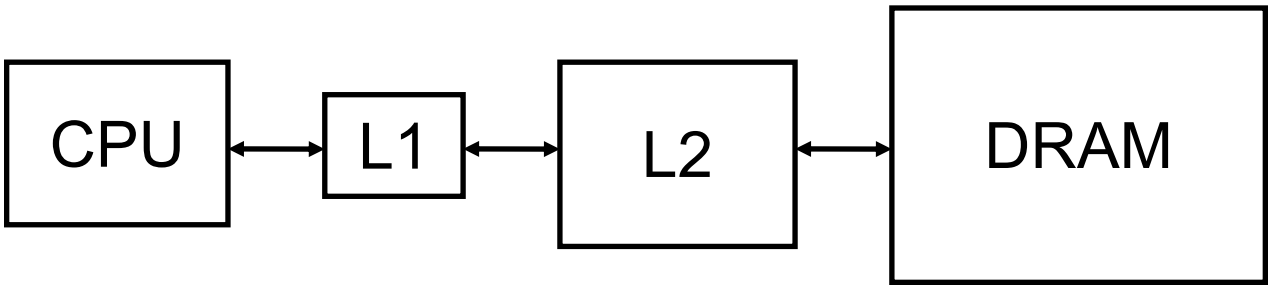
Replacement Policy

Which block from a set should be evicted?

- Random
- Least Recently Used (LRU)
  - LRU cache state must be updated on every access
  - true implementation only feasible for small sets (2-way)
  - pseudo-LRU binary tree was often used for 4-8 way
- First In, First Out (FIFO) a.k.a. Round-Robin
  - used in highly associative caches
- Not Least Recently Used (NLRU)
  - FIFO with exception for most recently used block or blocks
- One-bit LRU
  - Each way represented by a bit. Set on use, replace first unused.

Multilevel Caches

- A memory cannot be large and fast
- Add level of cache to reduce miss penalty
  - Each level can have longer latency than level above
  - So, increase sizes of cache at each level



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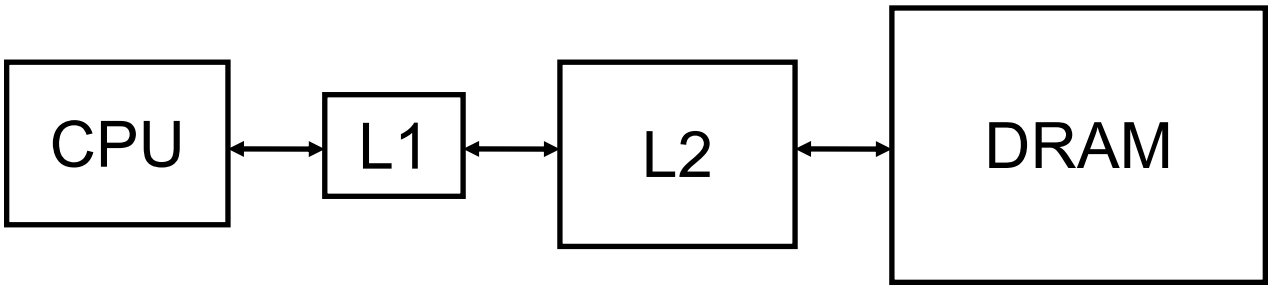

Metrics:

Local miss rate = misses in cache / accesses to cache

Global miss rate = misses in cache / CPU memory accesses

Misses per instruction = misses in cache / number of instructions

Inclusion Policy

- Inclusive multilevel cache:
  - Inner cache holds copies of data in outer cache
  - External access need only check outer cache
  - Most common case
- *Exclusive* multilevel caches:
  - Inner cache holds data not in outer cache
  - Swap lines between inner/outer caches on miss
  - Used in AMD Athlon with 64KB primary and 256KB secondary cache
- *Non-inclusive multilevel caches:*
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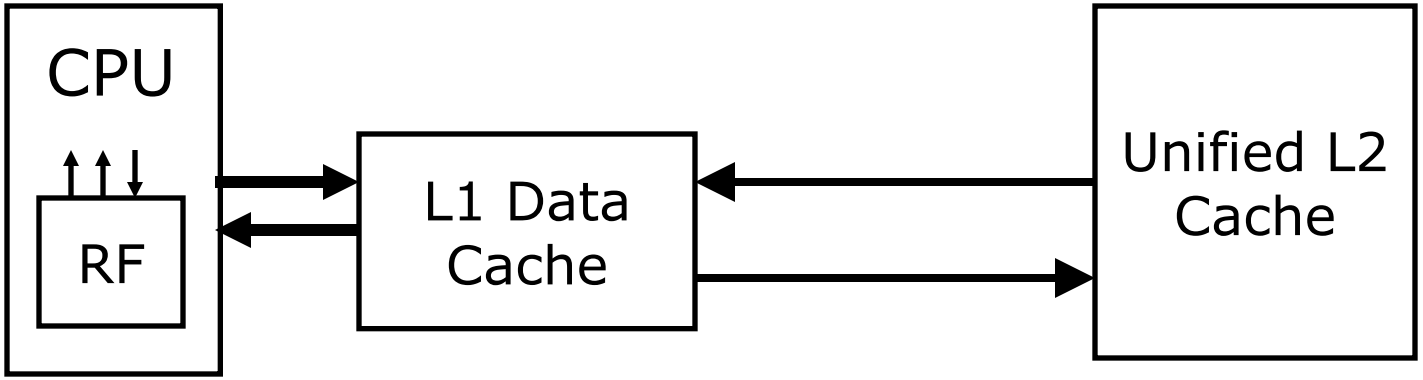
Exclusive: Outer cache retains more data
Inclusive: Less traffic, easier coherence

Victim Caches (HP 7200)



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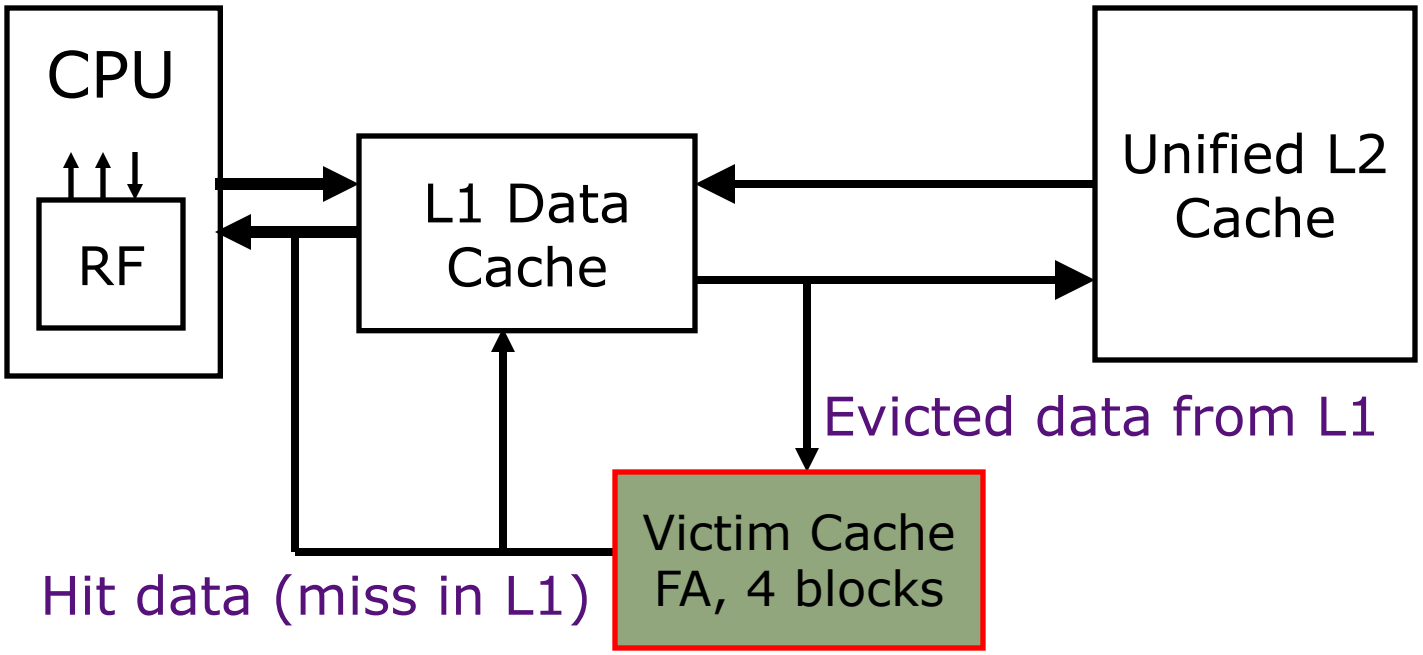

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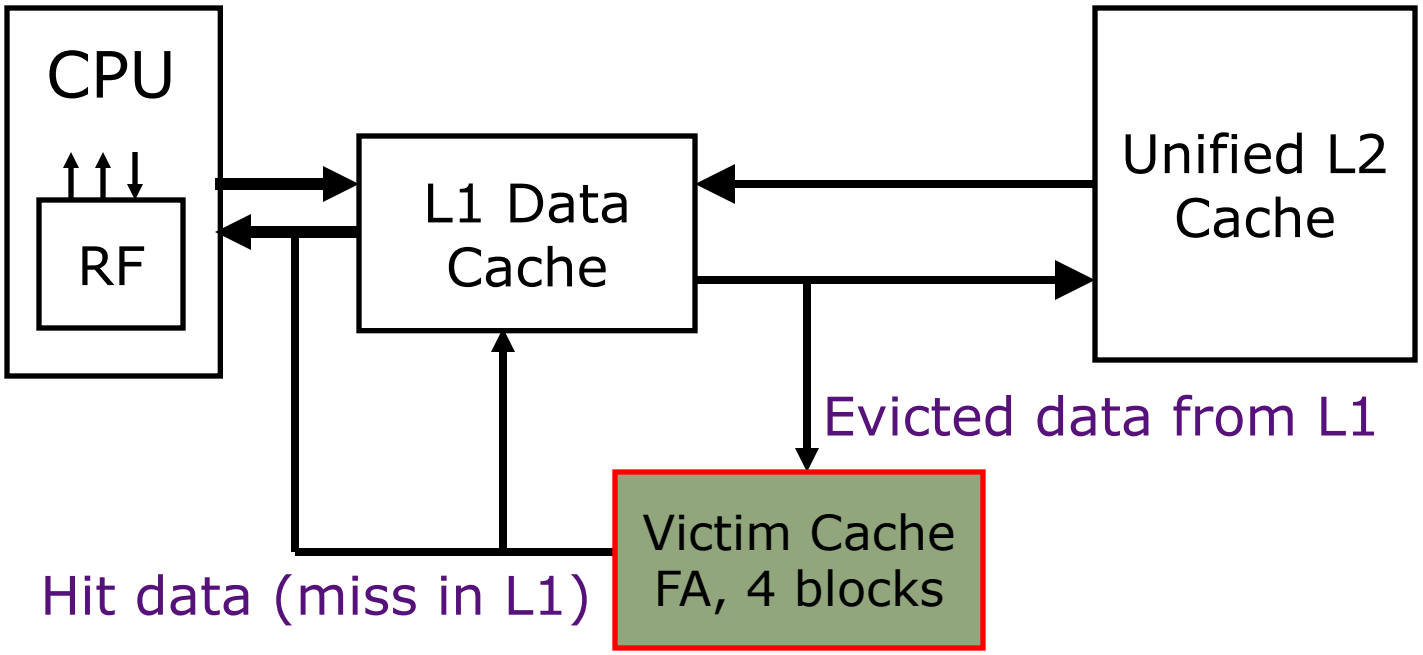

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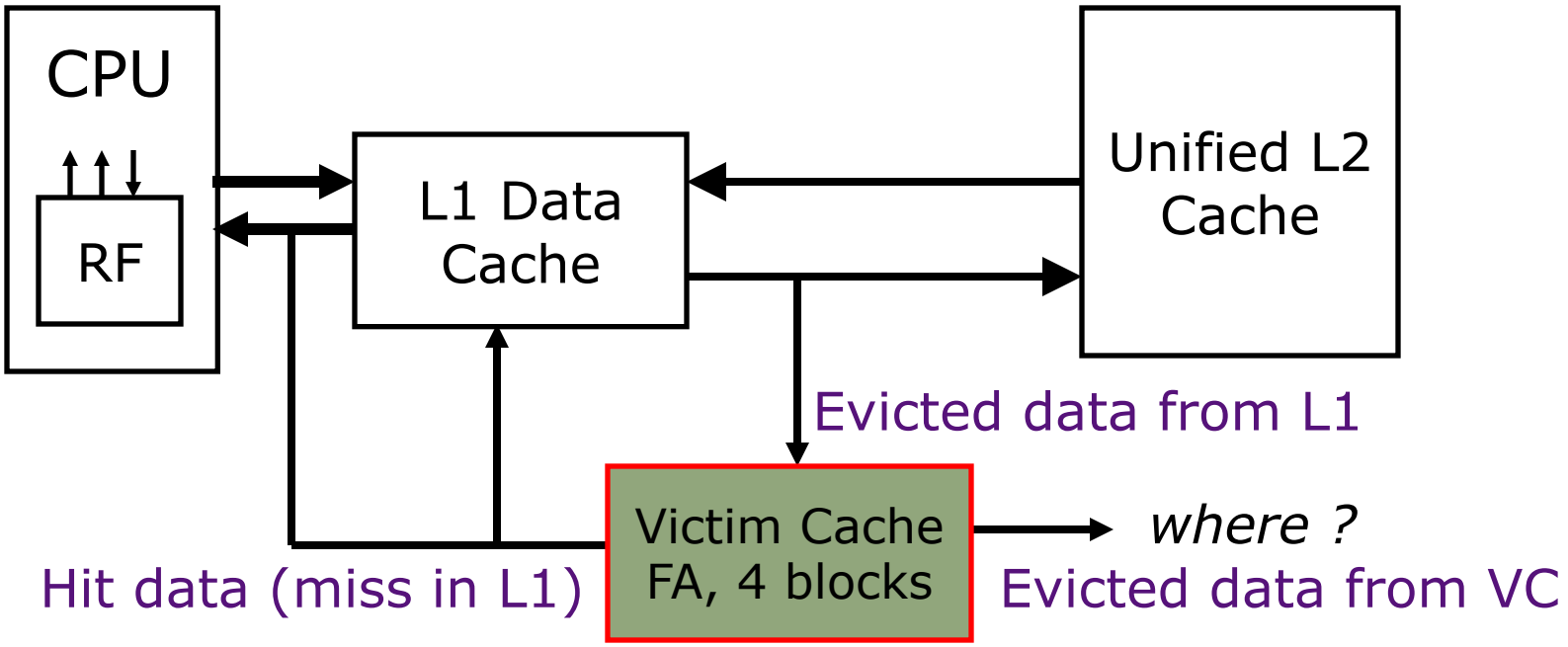

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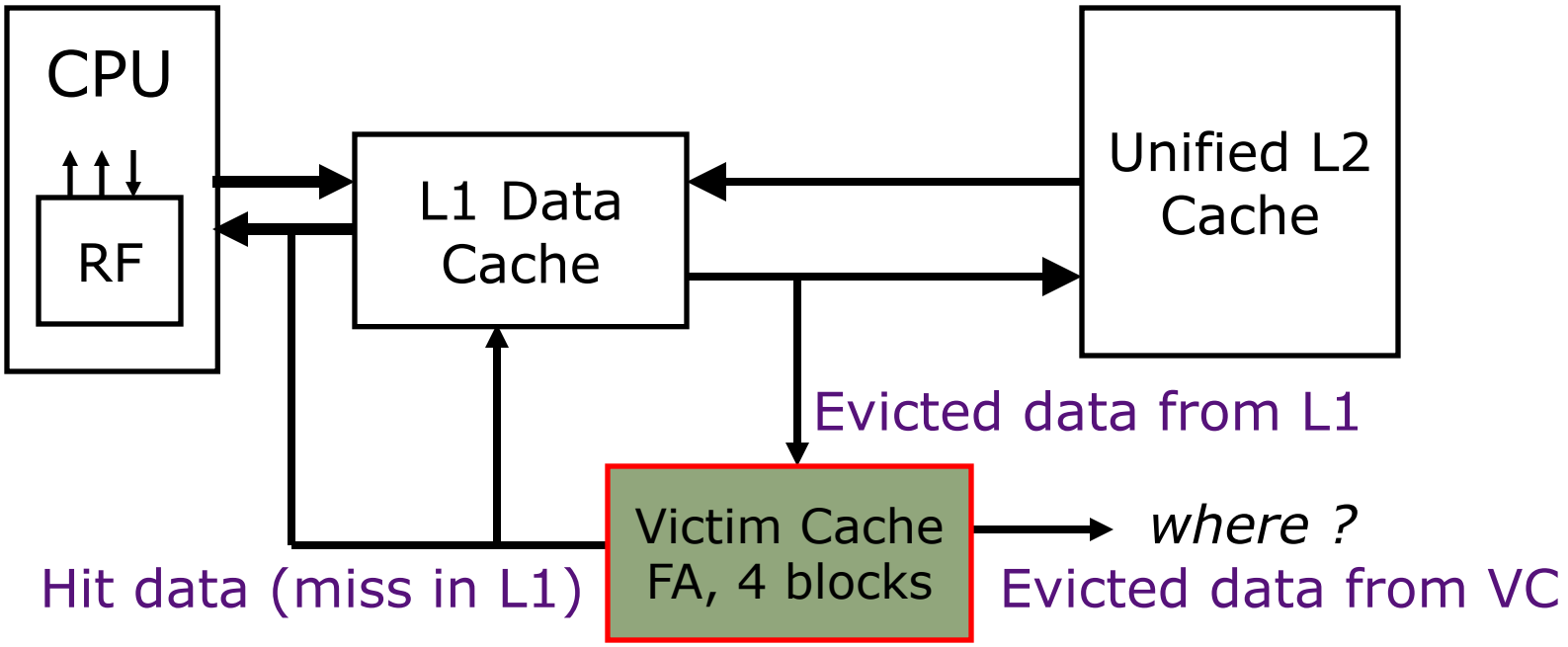

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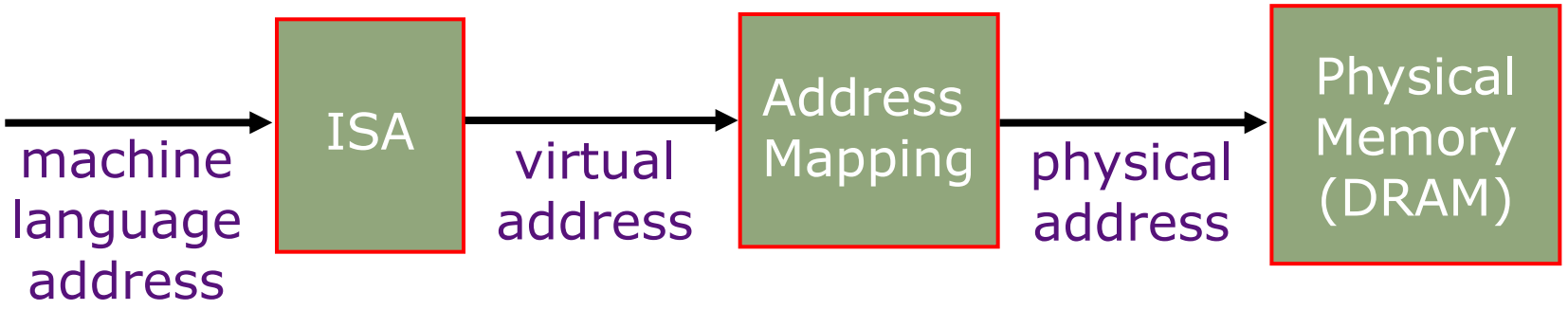
+ Fast hit time of direct-mapped but with reduced conflict misses

Memory Management

- The Fifties
  - Absolute Addresses
  - Dynamic address translation
- The Sixties
  - Atlas and Demand Paging
  - Paged memory systems and TLBs
- Modern Virtual Memory Systems

Names for Memory Locations



- Machine language address
  - as specified in machine code
- Virtual address *(sometimes called **effective address**)*
  - ISA specifies translation of machine code address into virtual address of program variable
- Physical address

  ⇒ operating system specifies mapping of virtual address into name for a physical memory location

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EDSAC, early 50's

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How could location independence be achieved?

Linker and/or loader modify addresses of subroutines and callers when building a program memory image

Multiprogramming

Motivation

- In the early machines, I/O operations were slow and each word transferred involved the CPU
- Higher throughput if CPU and I/O of 2 or more programs were overlapped. *How?*

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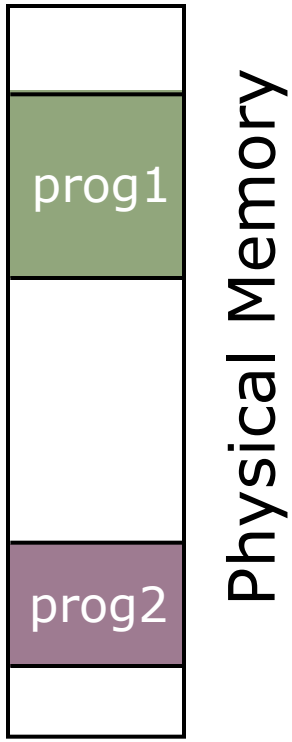

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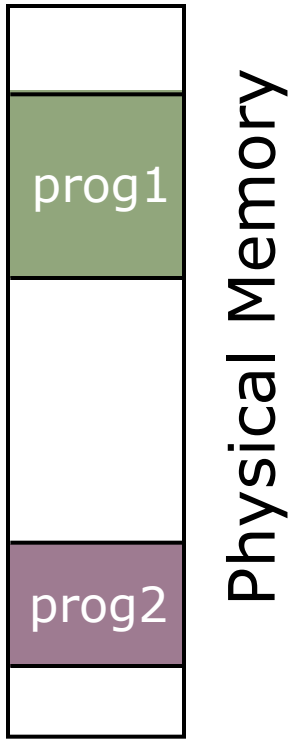

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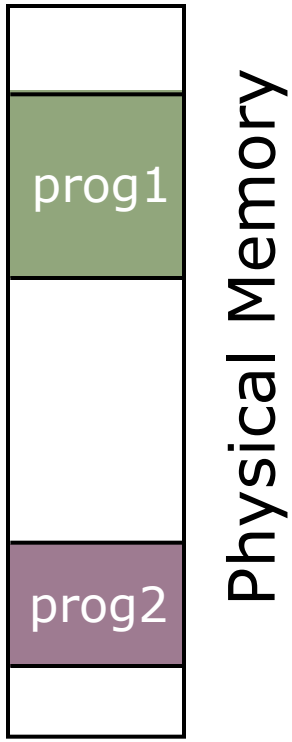

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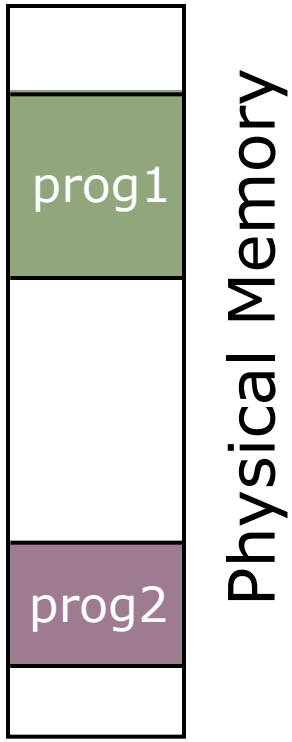

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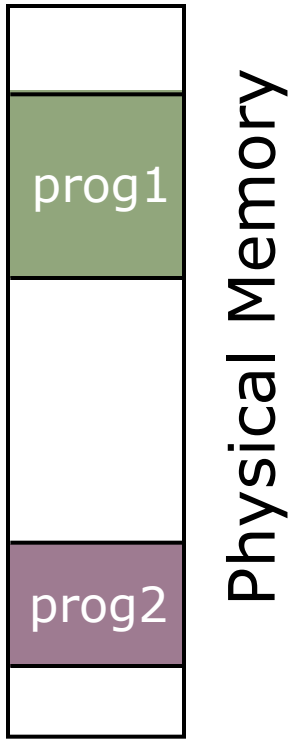
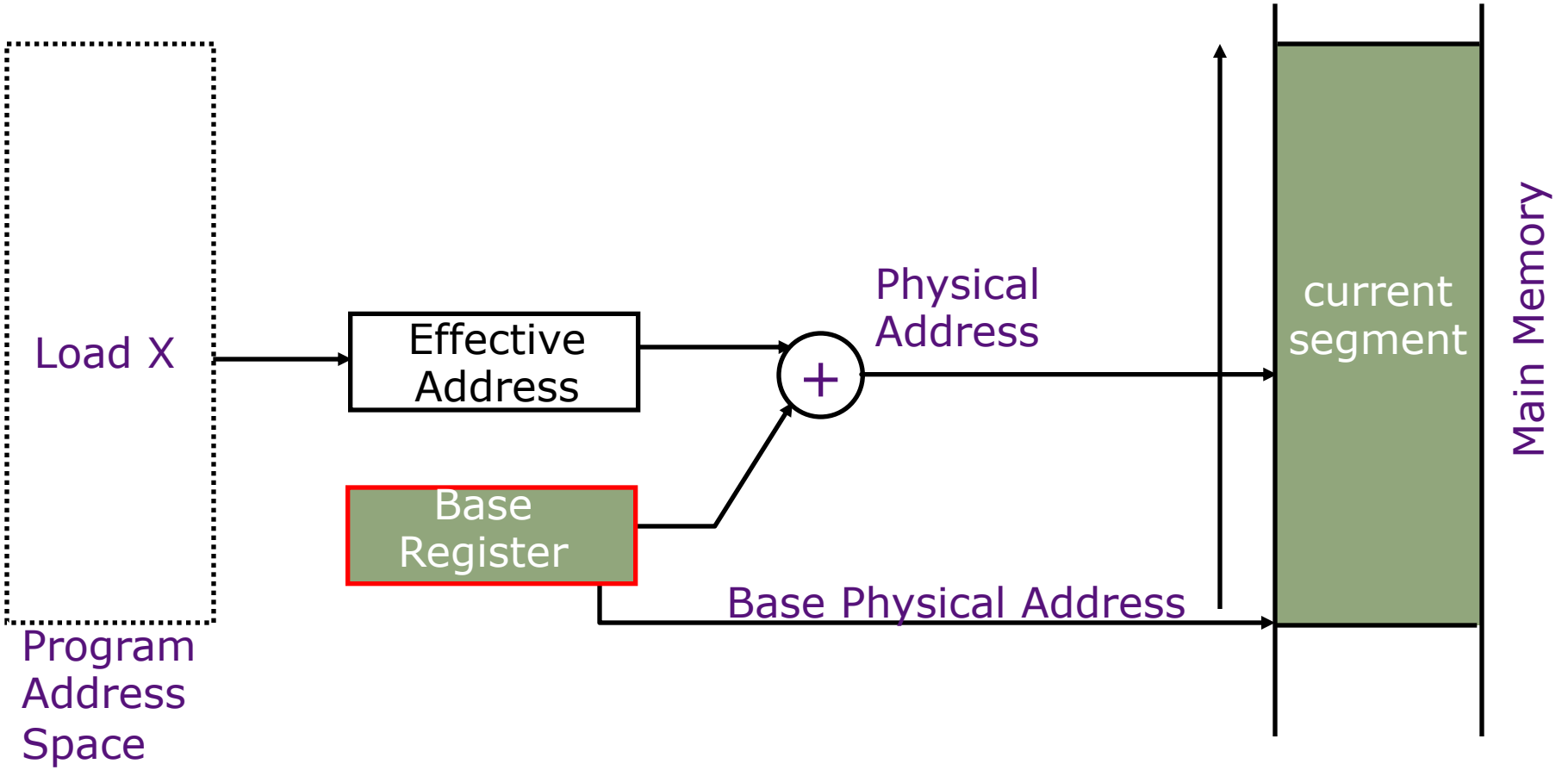


Simple Base and Bound Translation



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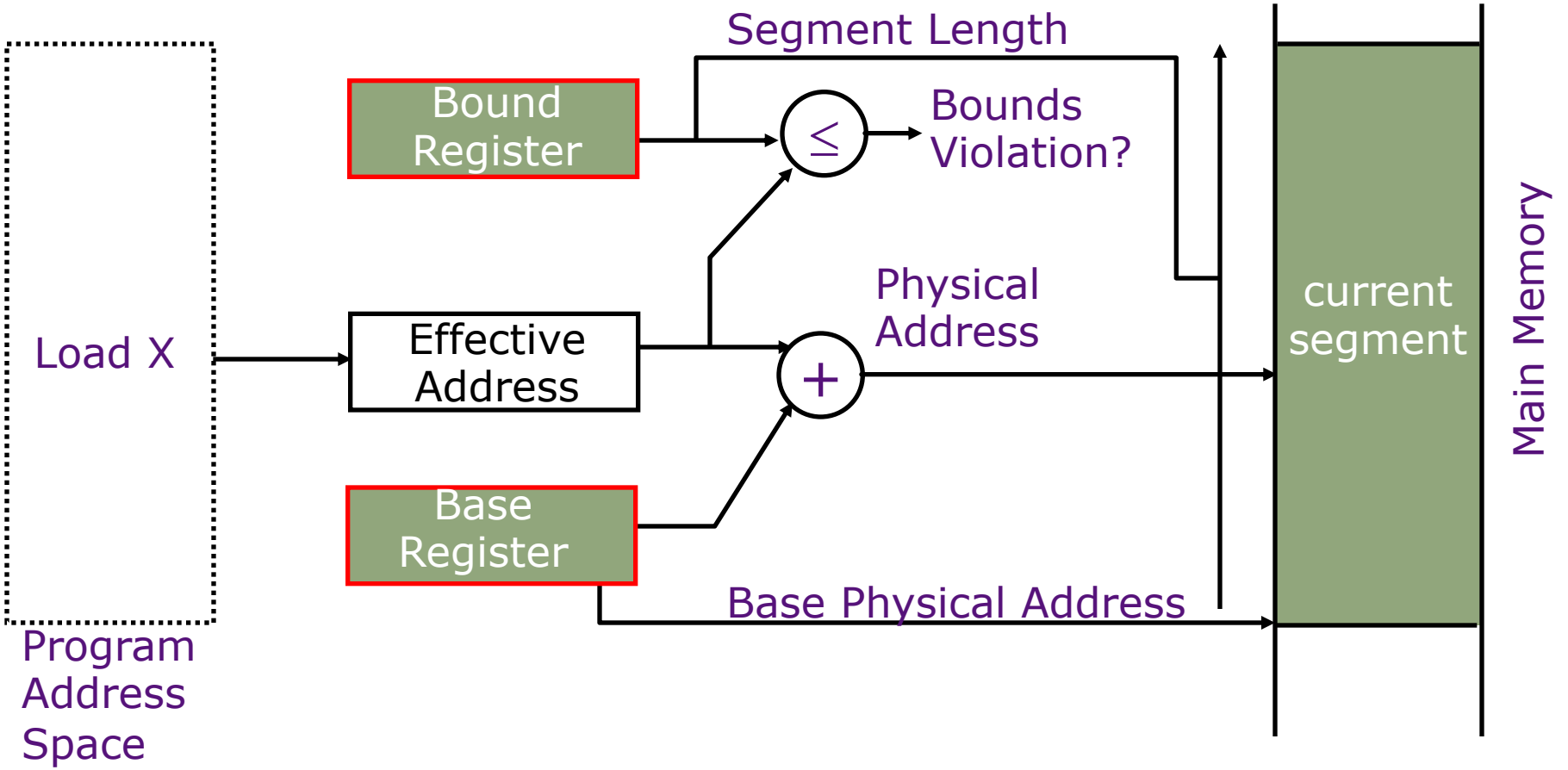

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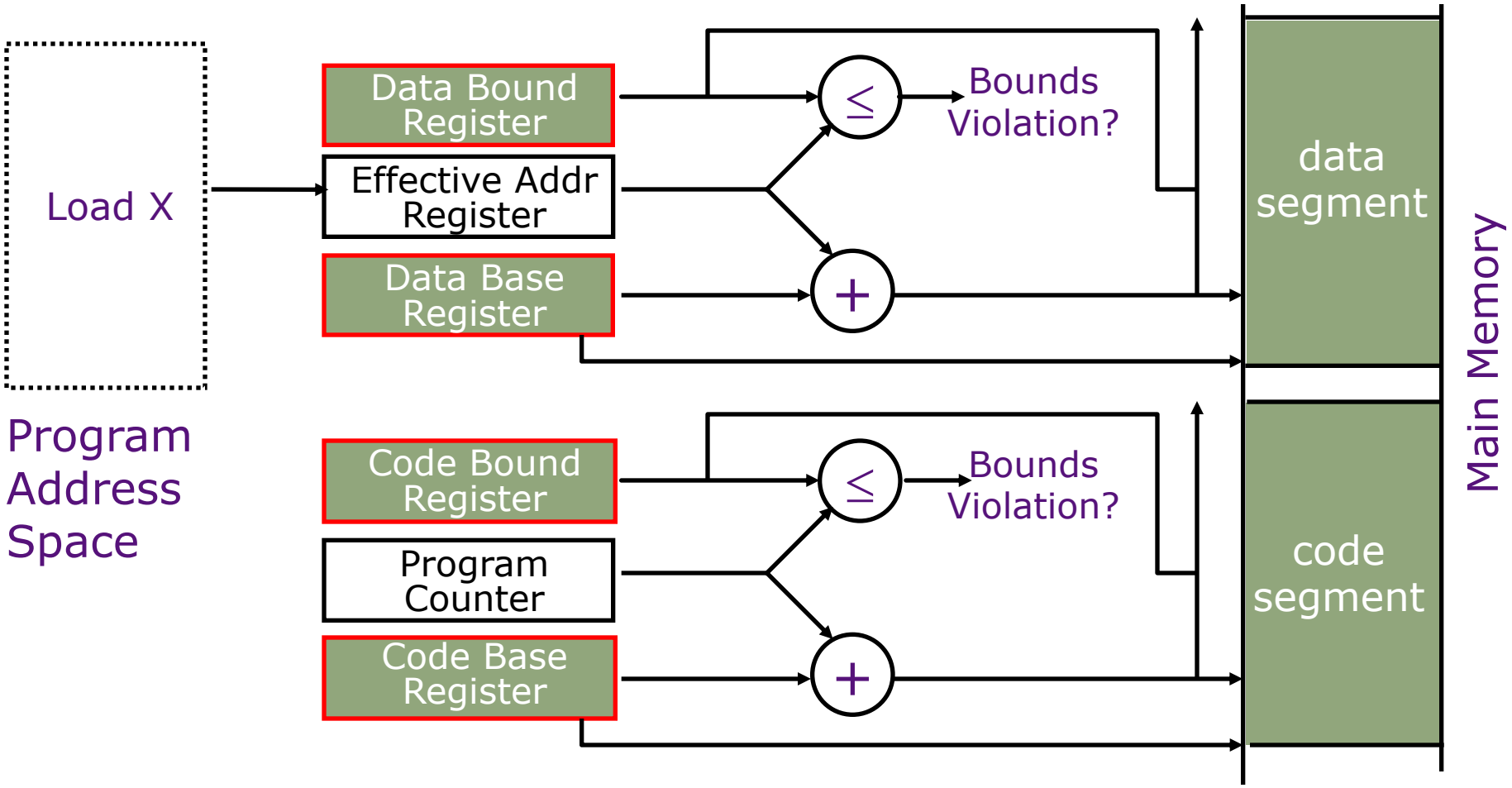
Separate Areas for Code and Data



What is an advantage of this separation?

(Scheme used on all Cray vector supercomputers prior to X1, 2002)

Memory Fragmentation

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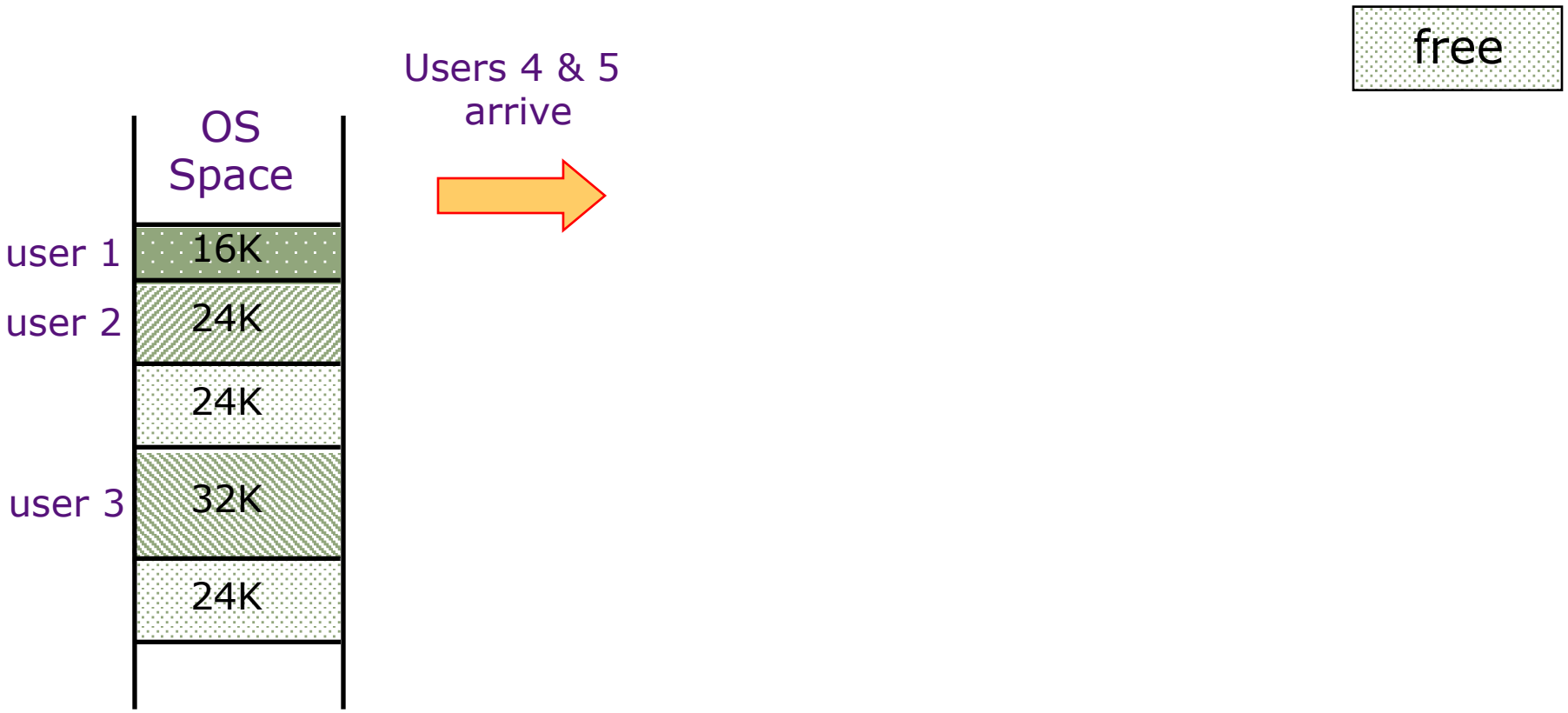

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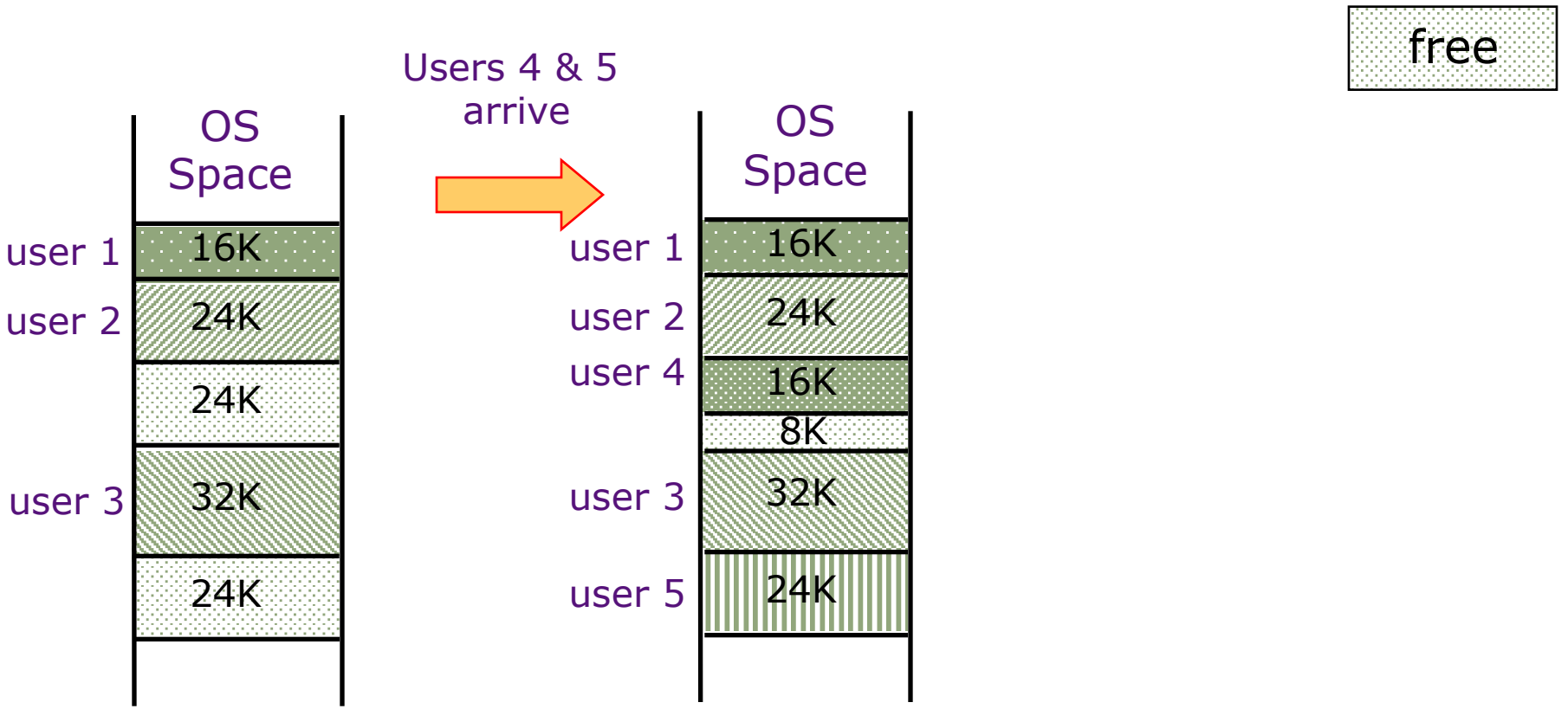

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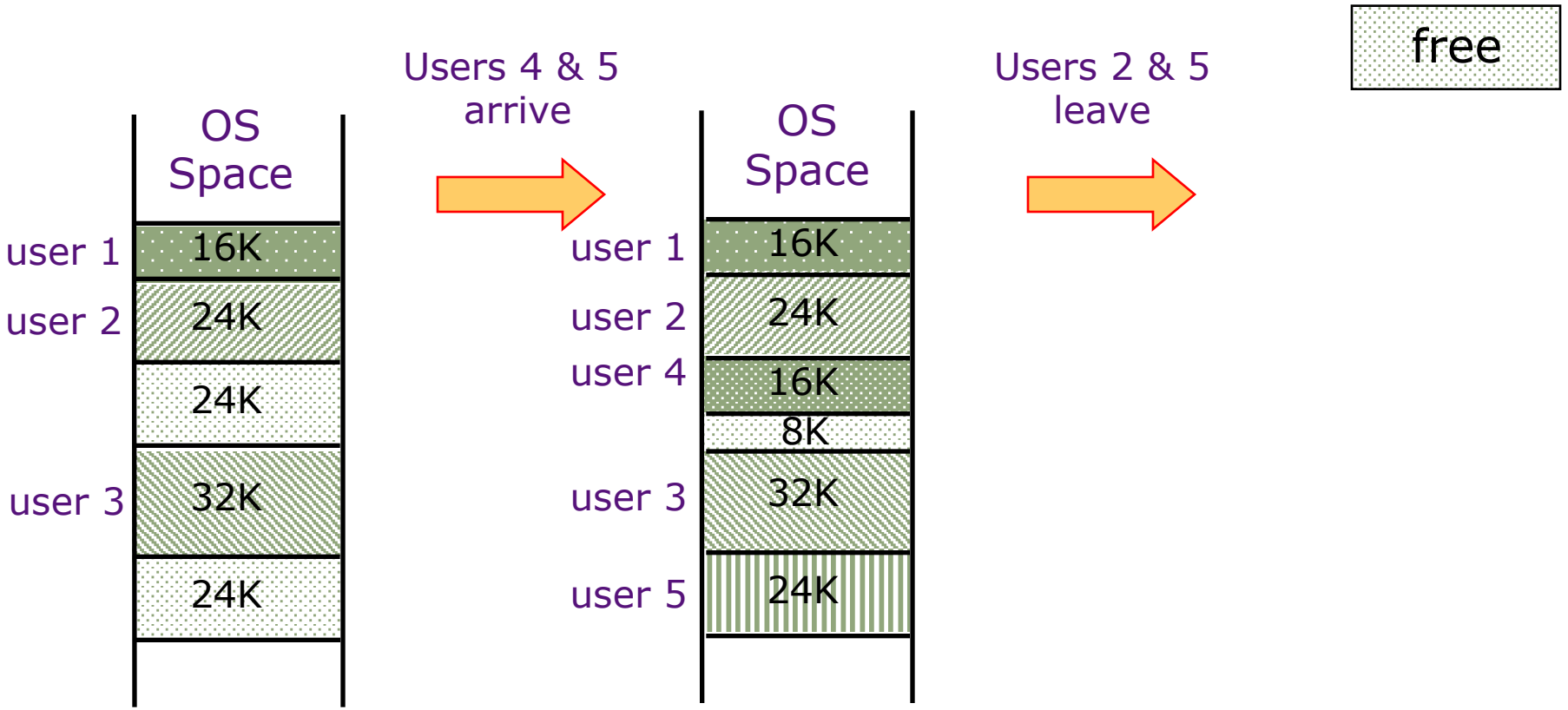

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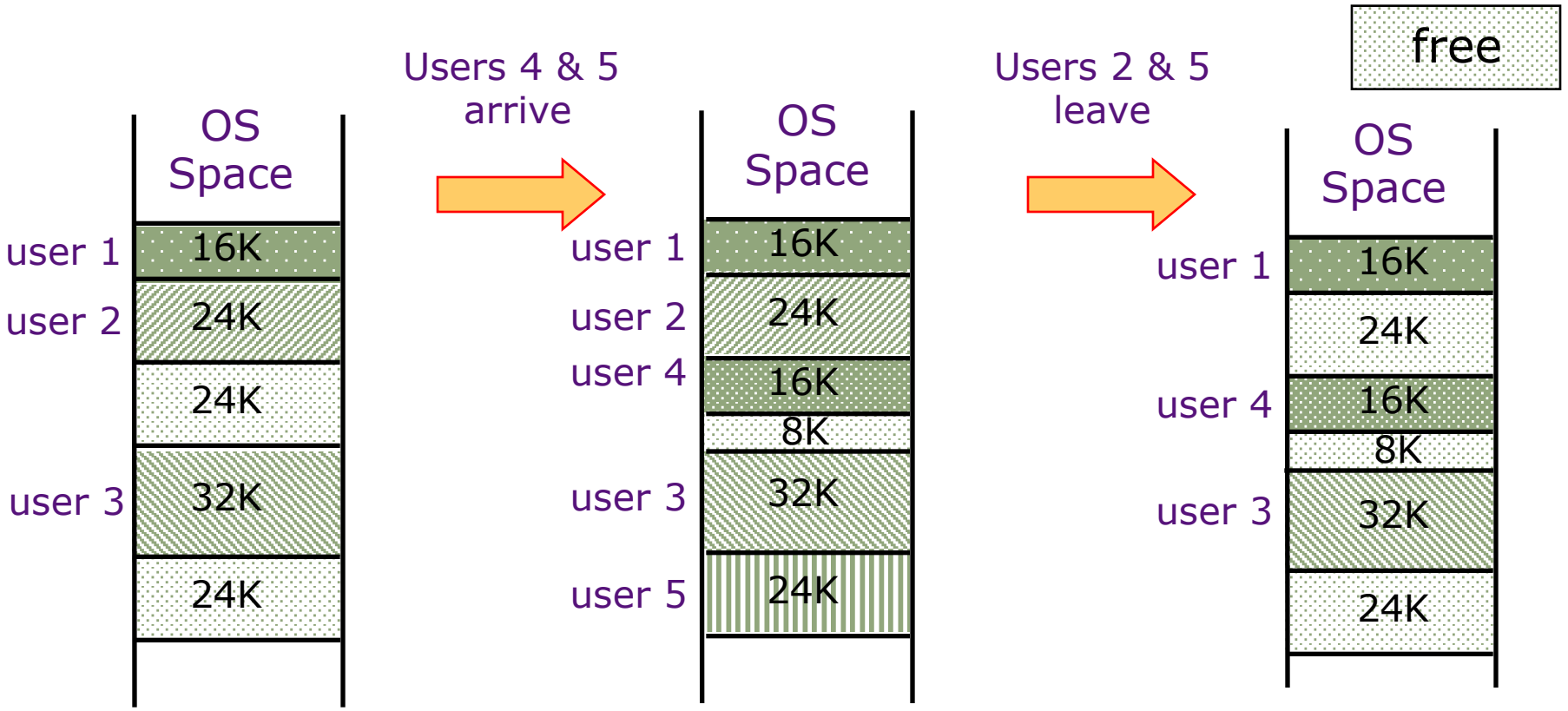

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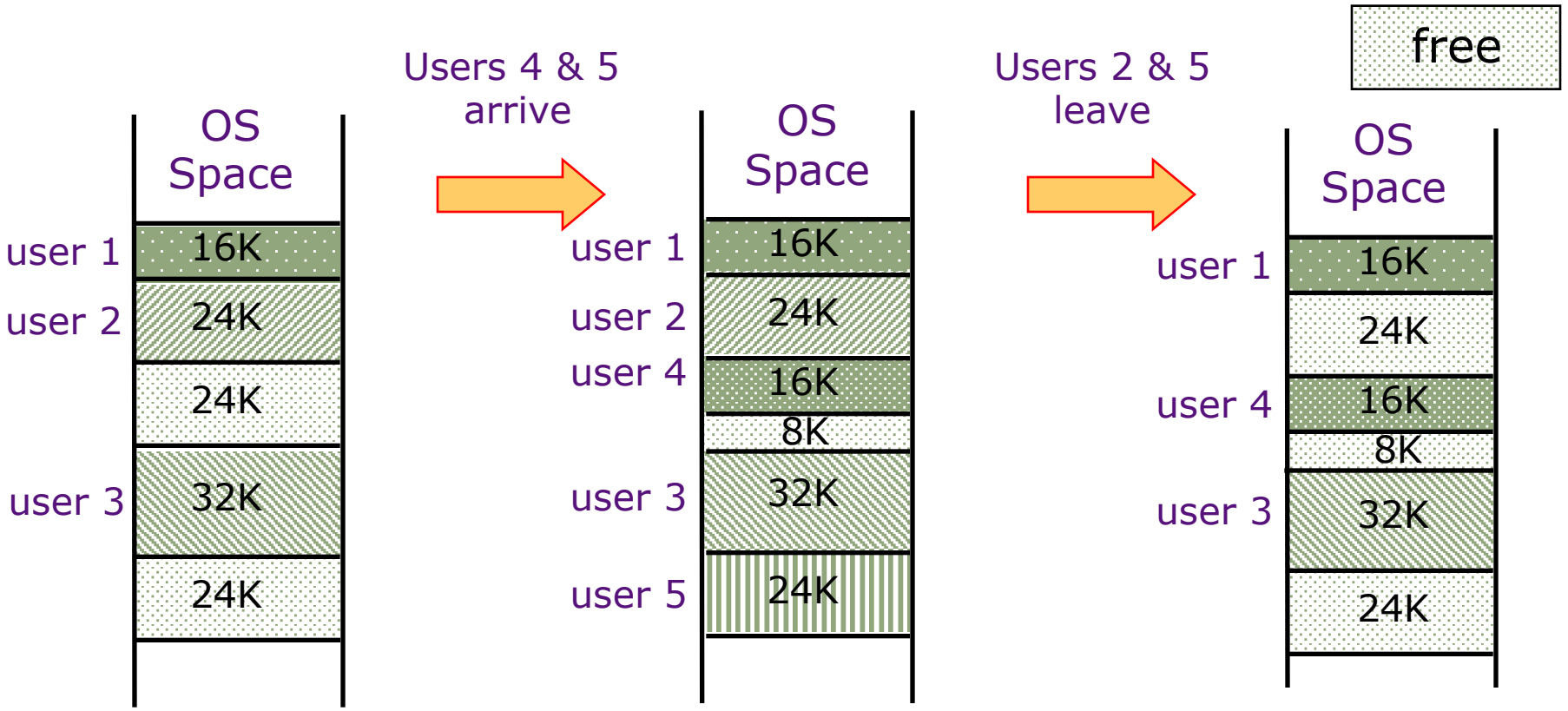

As users come and go, the storage is "fragmented". Therefore, at some stage programs have to be moved around to compact the storage.

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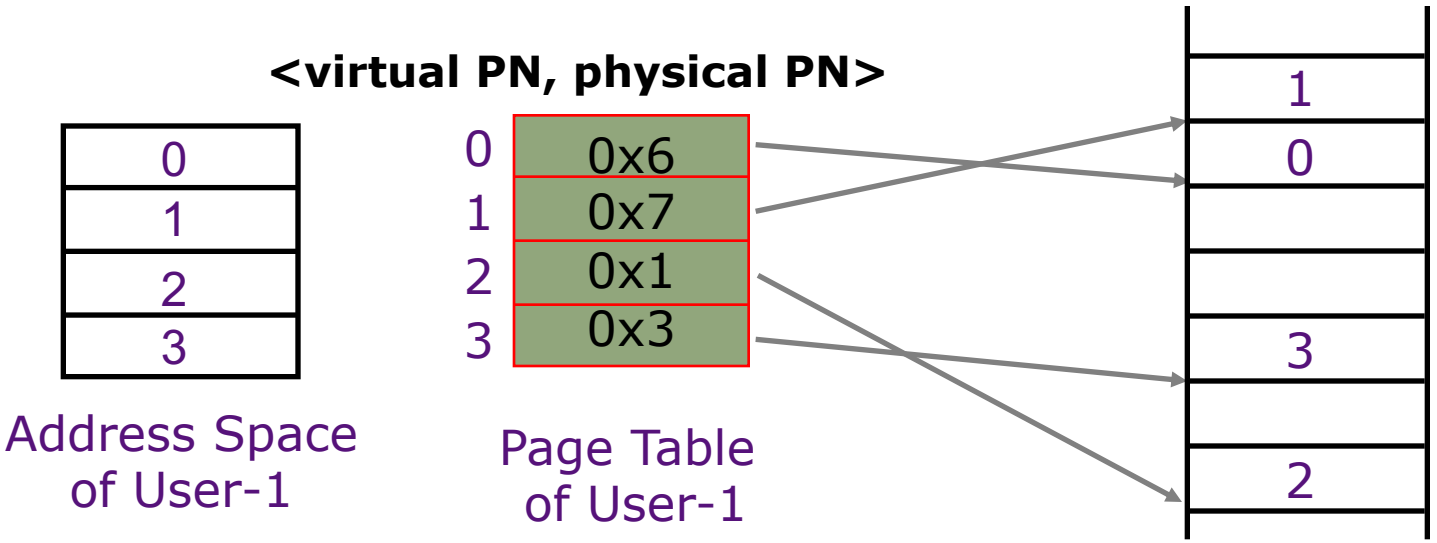

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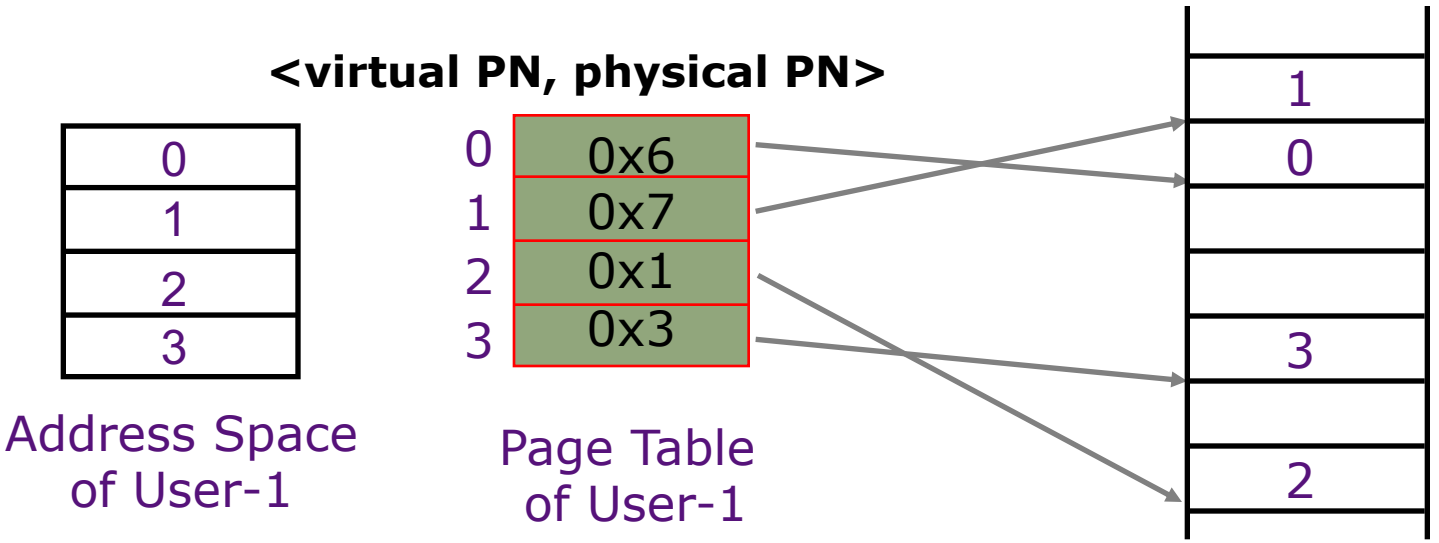
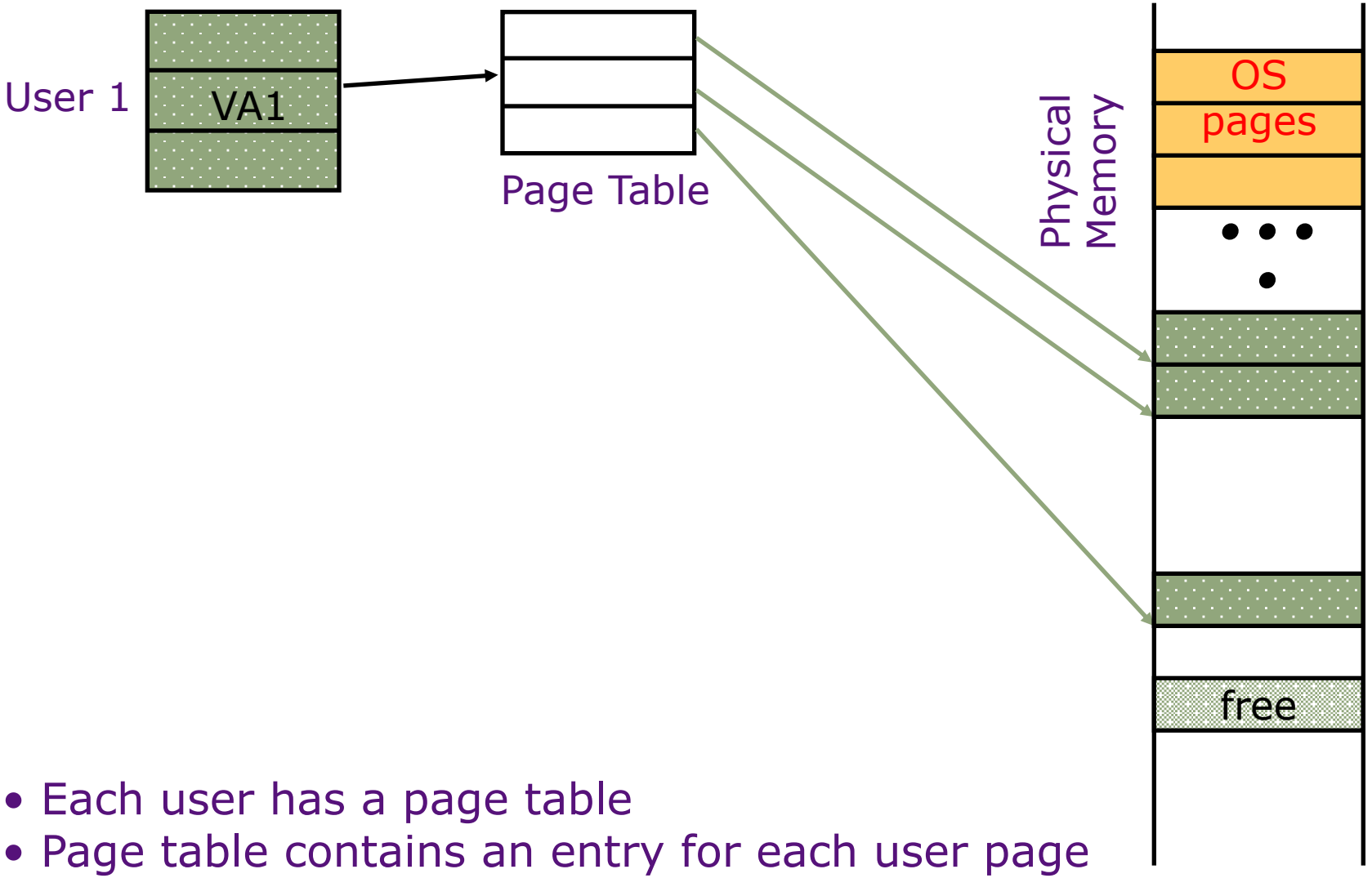


Page tables make it possible to store the pages of a program non-contiguously.

Private Address Space per User



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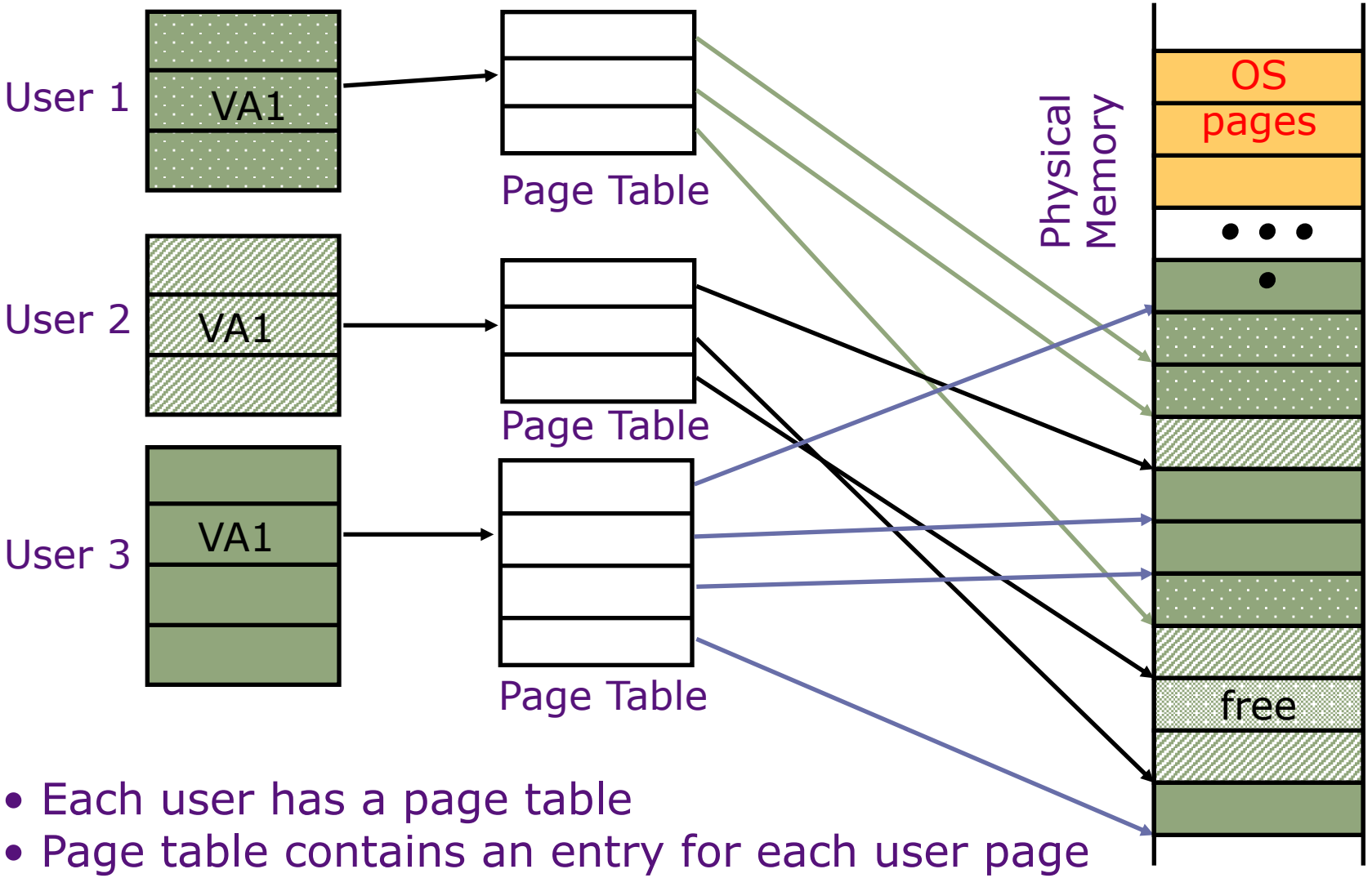

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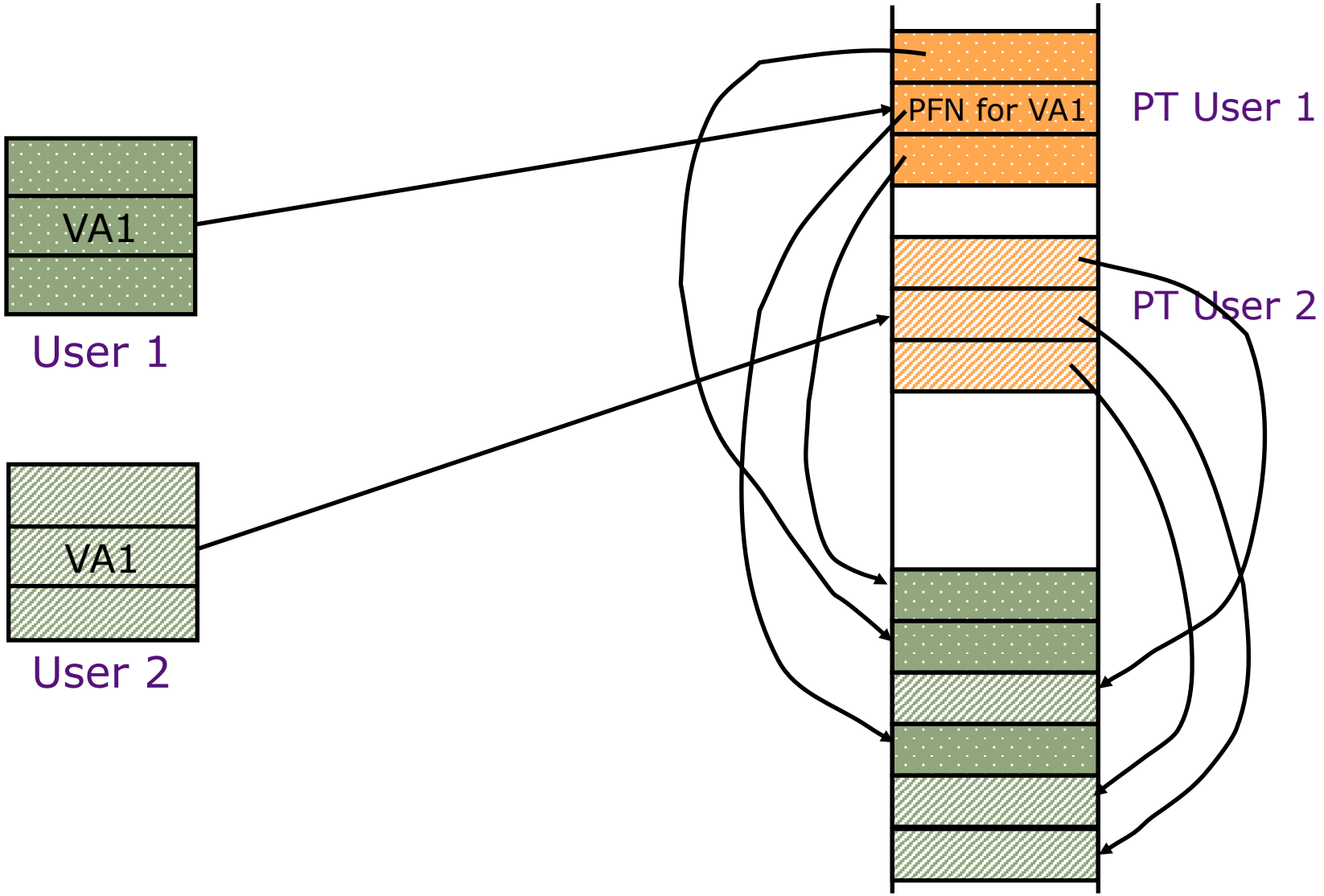
  - needs one reference to retrieve the page base address and another to access the data word
    - ⇒ *doubles the number of memory references!*

Page Tables in Physical Memory



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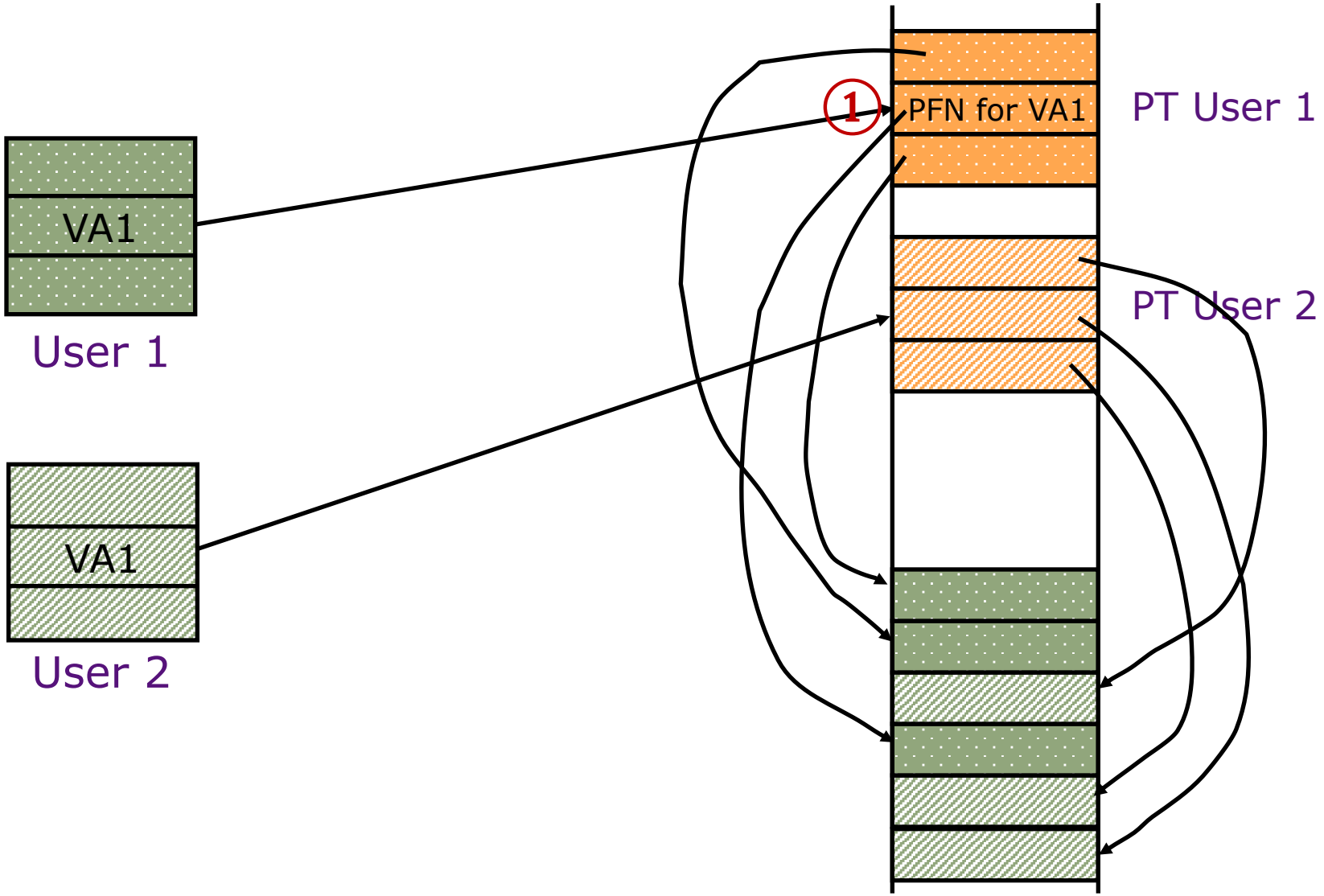

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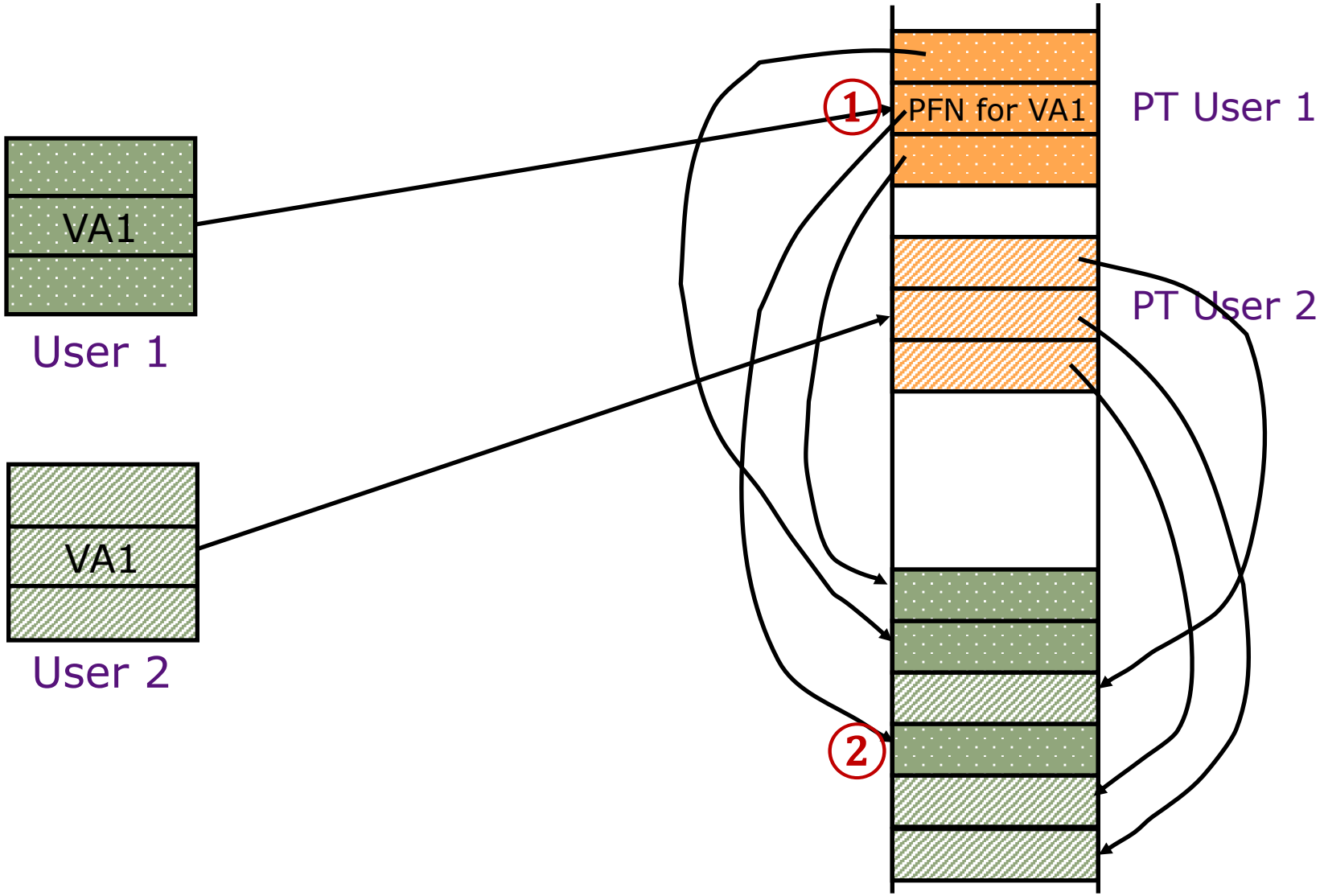

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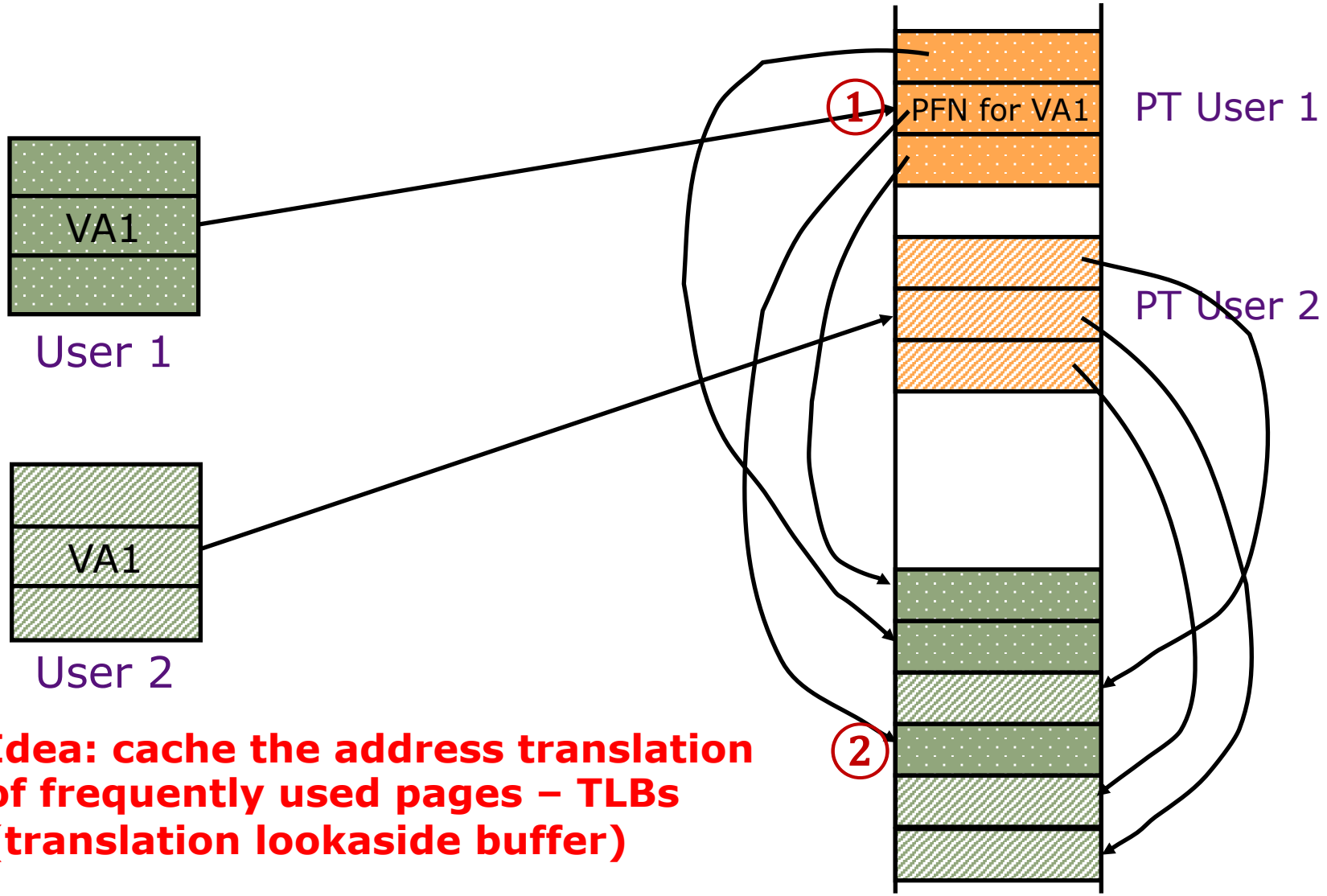

Idea: cache the address translation of frequently used pages – TLBs (translation lookaside buffer)

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- Programmers moved the data back and forth from the secondary store by *overlaying* it repeatedly on the primary store

tricky programming!

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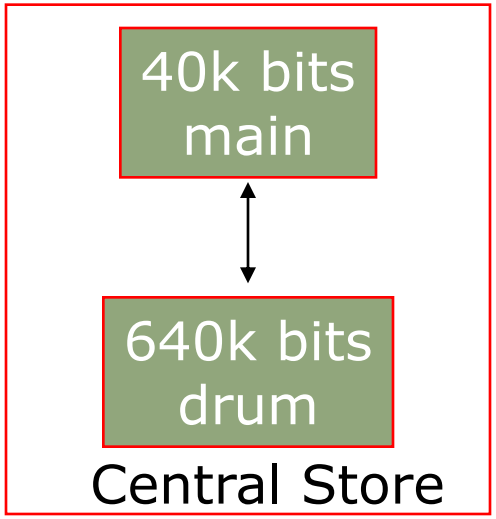

Ferranti Mercury
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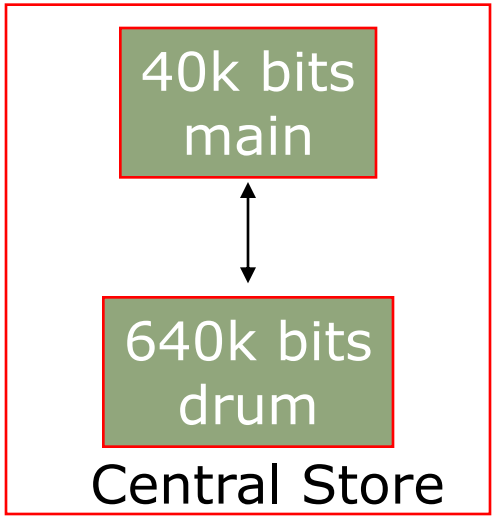

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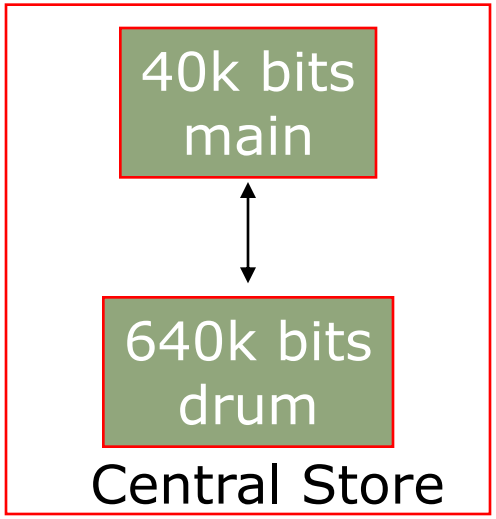

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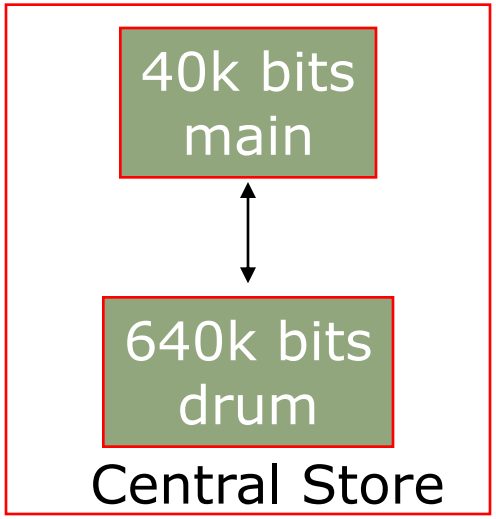

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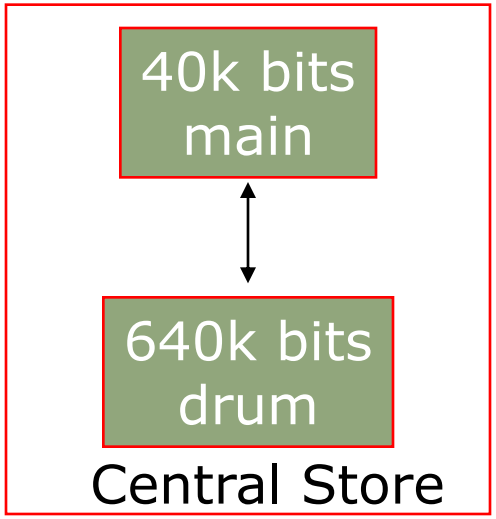
  - *Inefficient*



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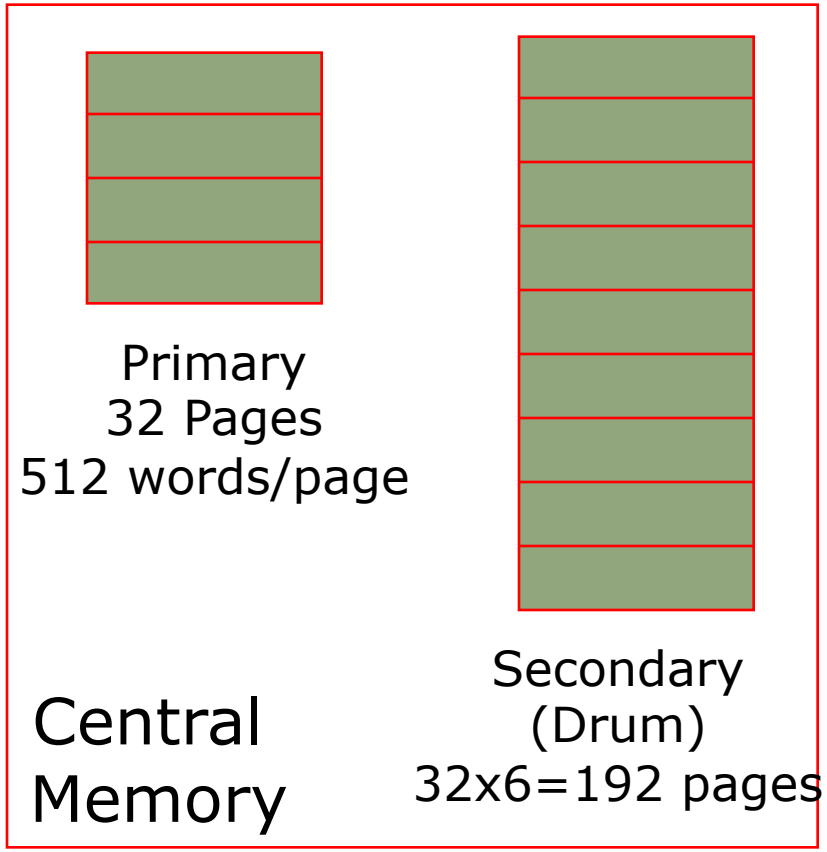
Demand Paging in Atlas (1962)

"A page from secondary storage is brought into the primary storage whenever it is (implicitly) demanded by the processor."

Tom Kilburn



Demand Paging in Atlas (1962)

"A page from secondary storage is brought into the primary storage whenever it is (implicitly) demanded by the processor."

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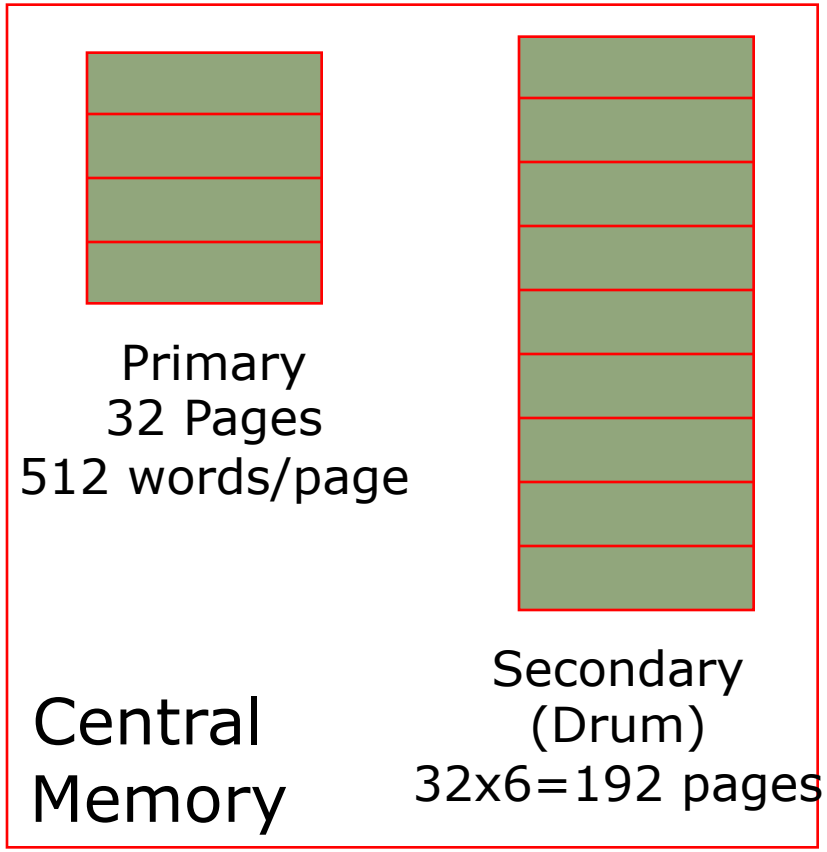
Primary memory as a *cache* for secondary memory



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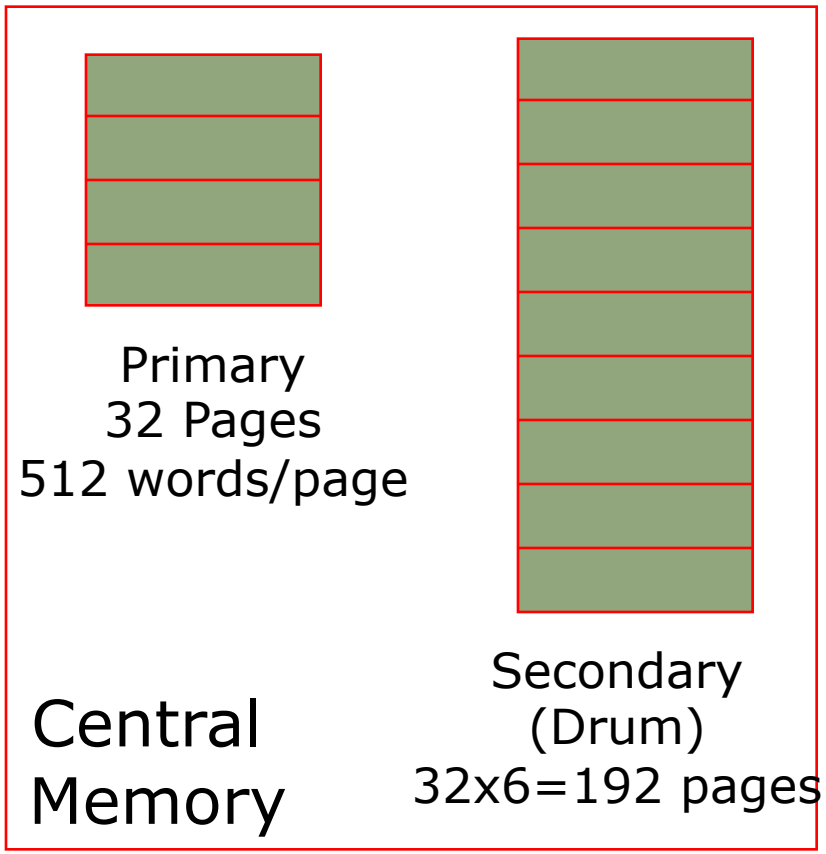
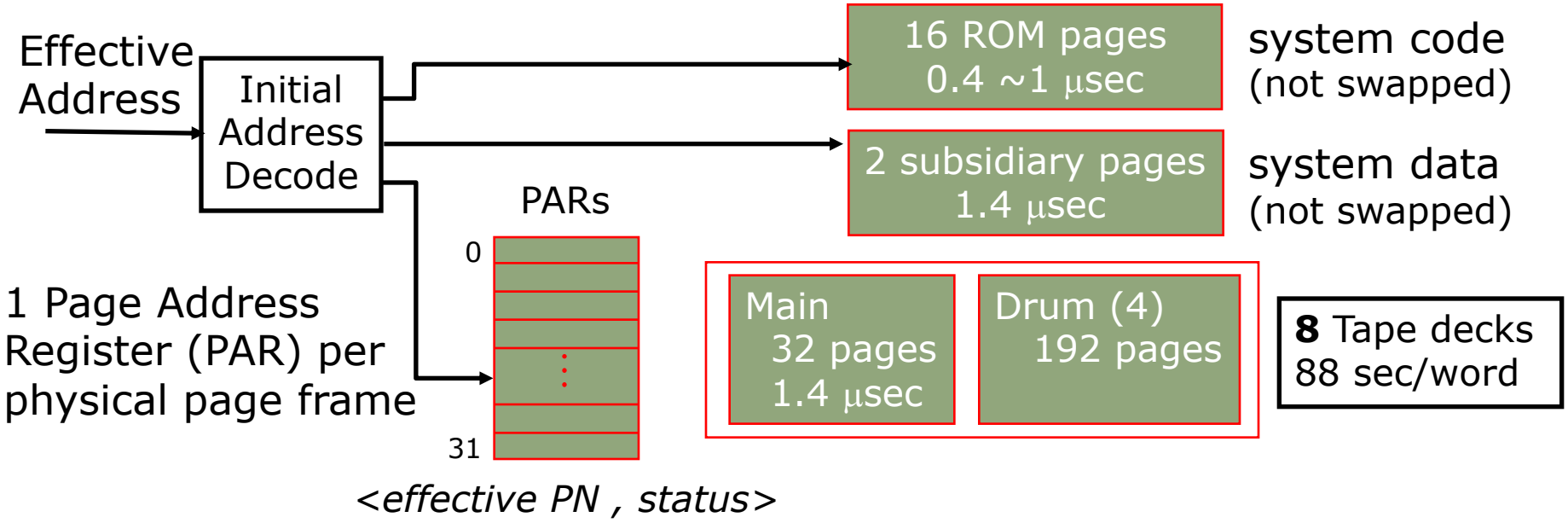
User sees 32 x 6 x 512 words of storage



Hardware Organization of Atlas



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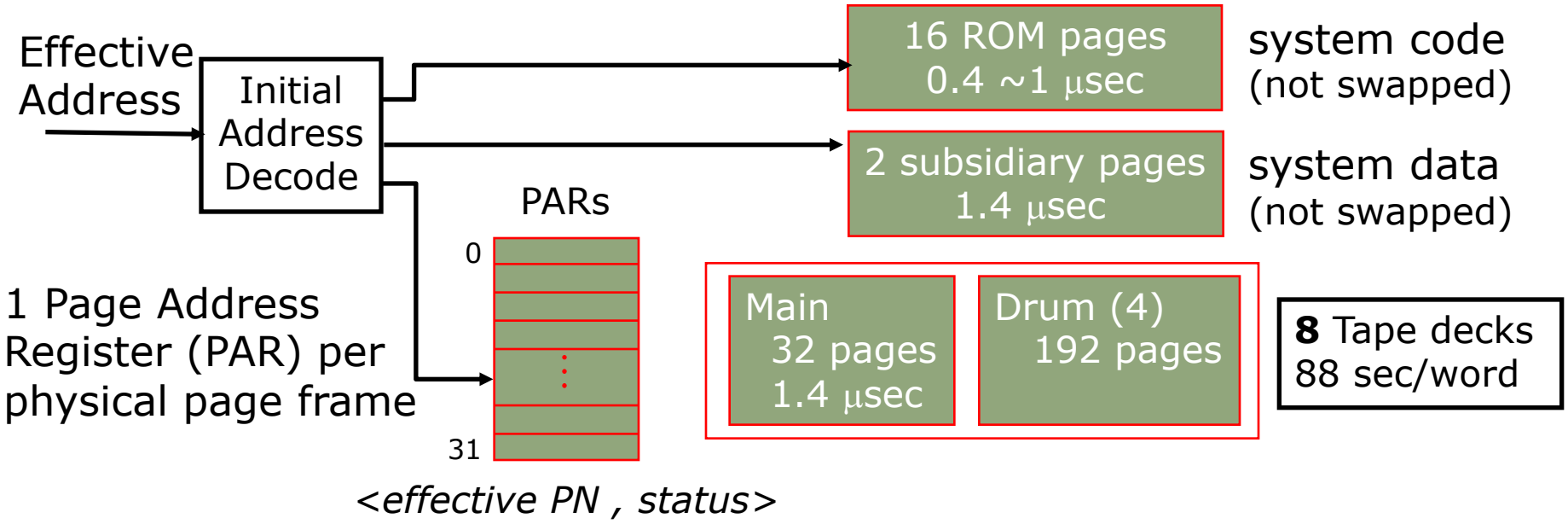


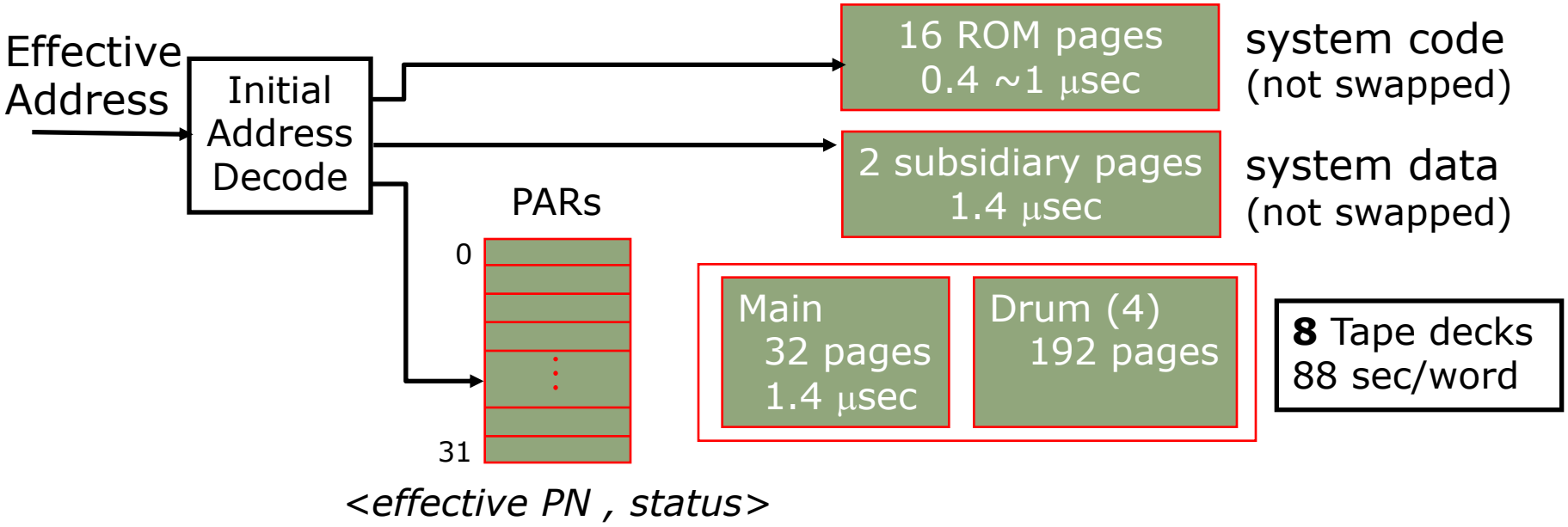
Compare the effective page address against all 32 PARs

match ⇒ normal access

no match ⇒ *page fault*

save the state of the partially executed instruction

Atlas Demand Paging Scheme



On a page fault:

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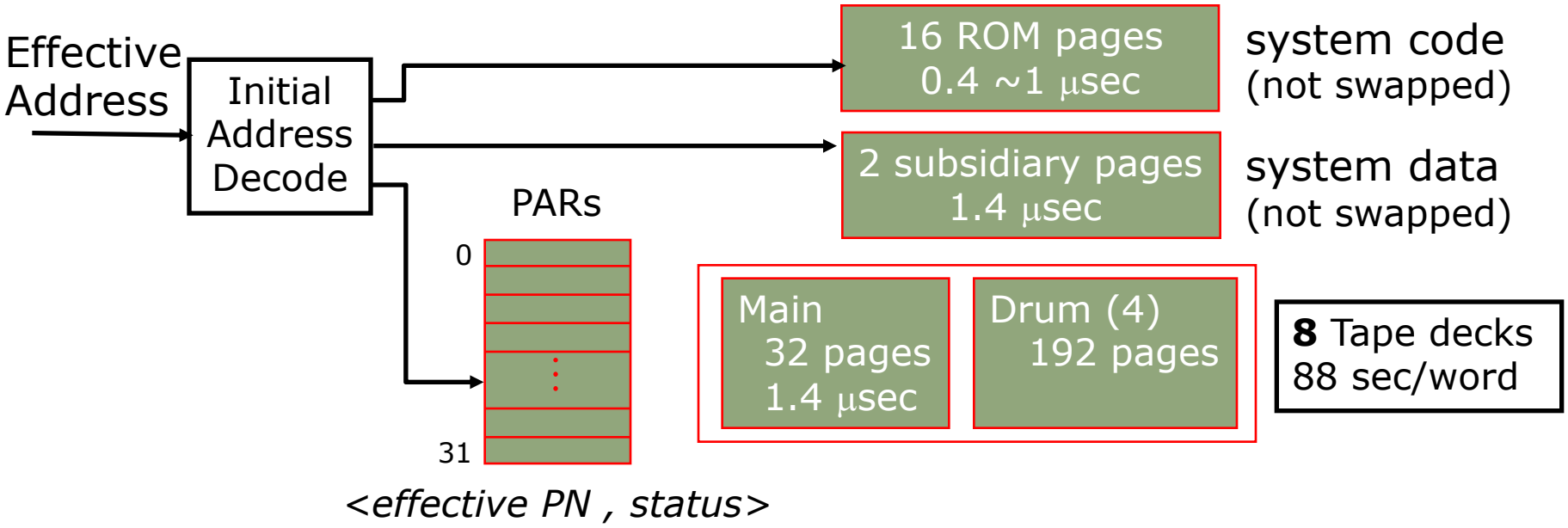
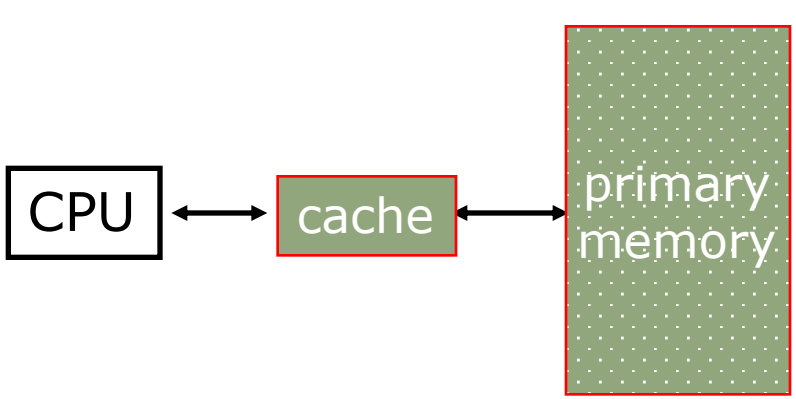
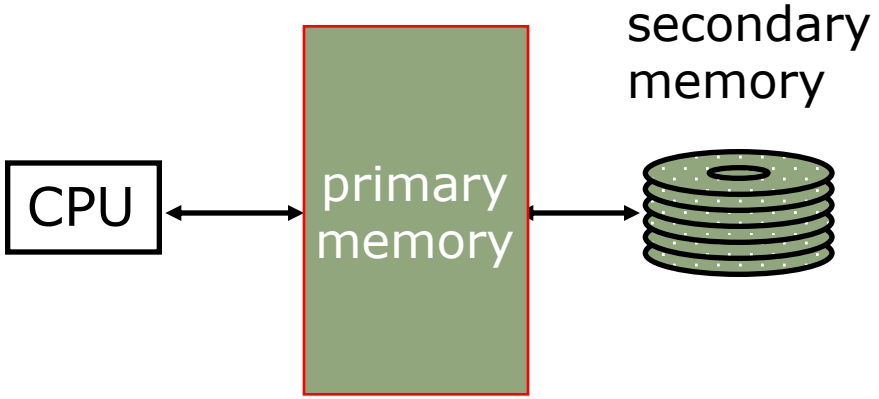


On a page fault:

- Input transfer into a free page is initiated
- The Page Address Register (PAR) is updated
- If no free page is left, a page is selected to be replaced (based on usage)
- The replaced page is written on the drum (to minimize the drum latency effect, the first empty page on the drum was selected)
- The page table is updated to point to the new location of the page on the drum

Caching vs. Demand Paging





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- cache entry
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Demand paging
- page frame
- page (~4K bytes)

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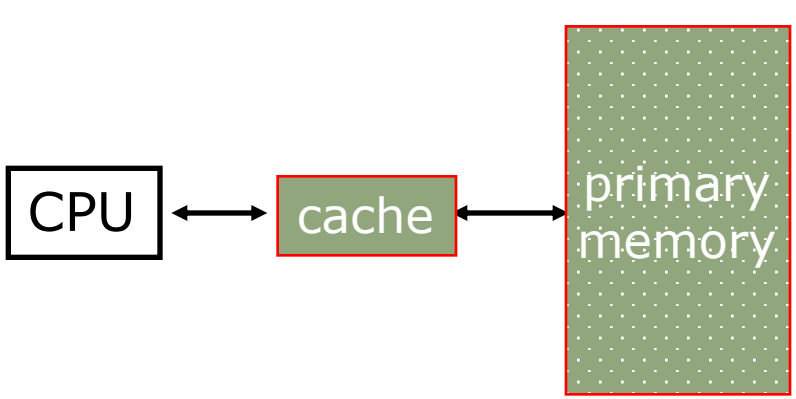

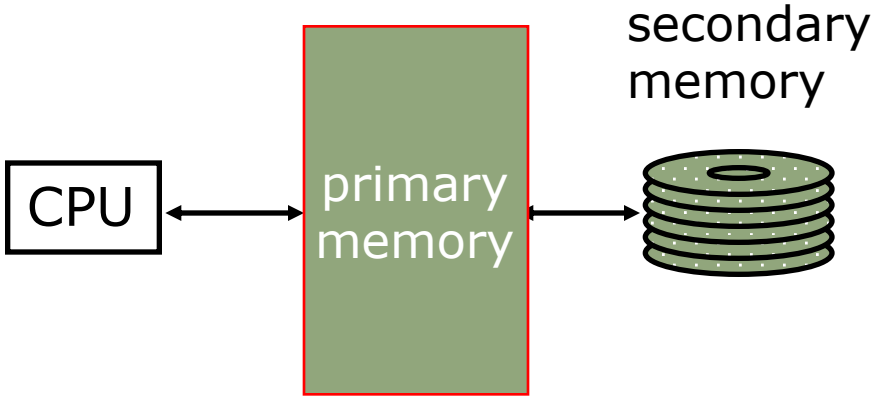

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- cache miss rate (1% to 20%)
- cache hit (~1 cycle)
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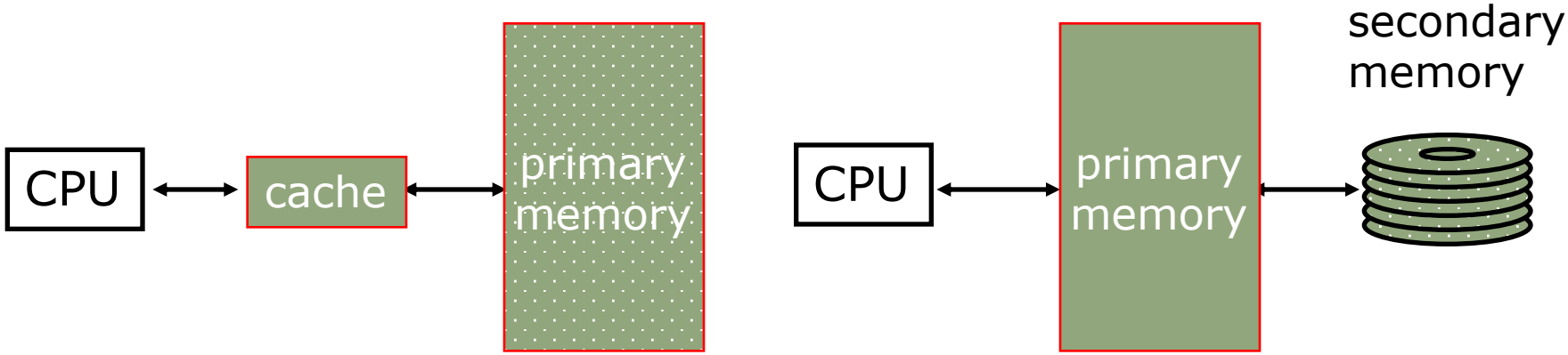

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Modern Virtual Memory Systems

Illusion of a large, private, uniform store

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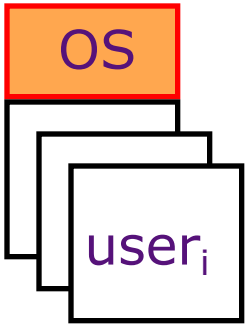
Illusion of a large, private, uniform store

Protection & Privacy

- several users, each with their private address space and one or more shared address spaces
  - page table ≡ name space



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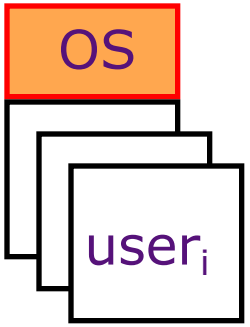
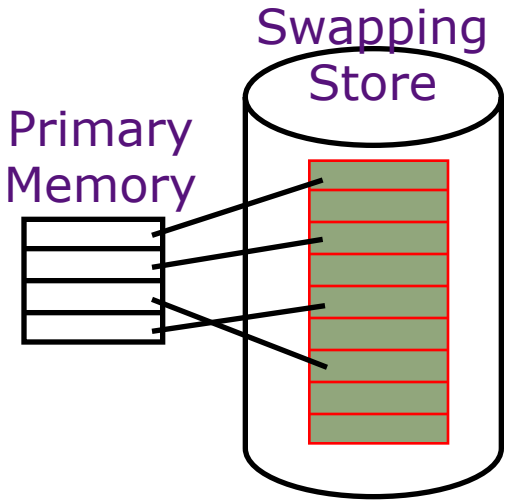


Demand Paging

- Provides the ability to run programs larger than the primary memory
- Hides differences in machine configurations



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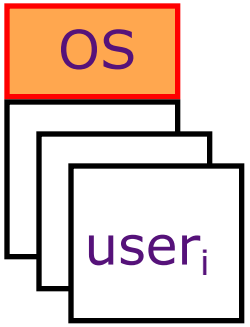

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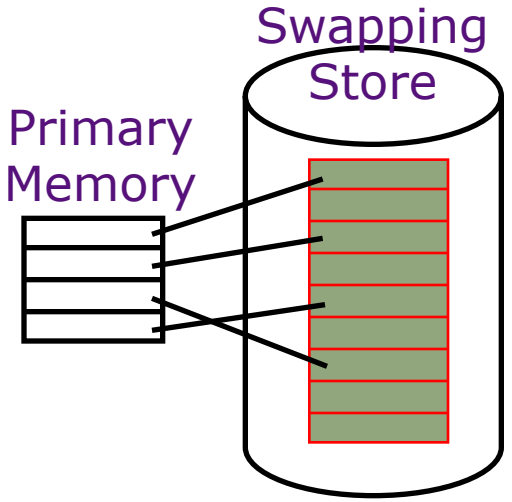

The price is address translation on each memory reference

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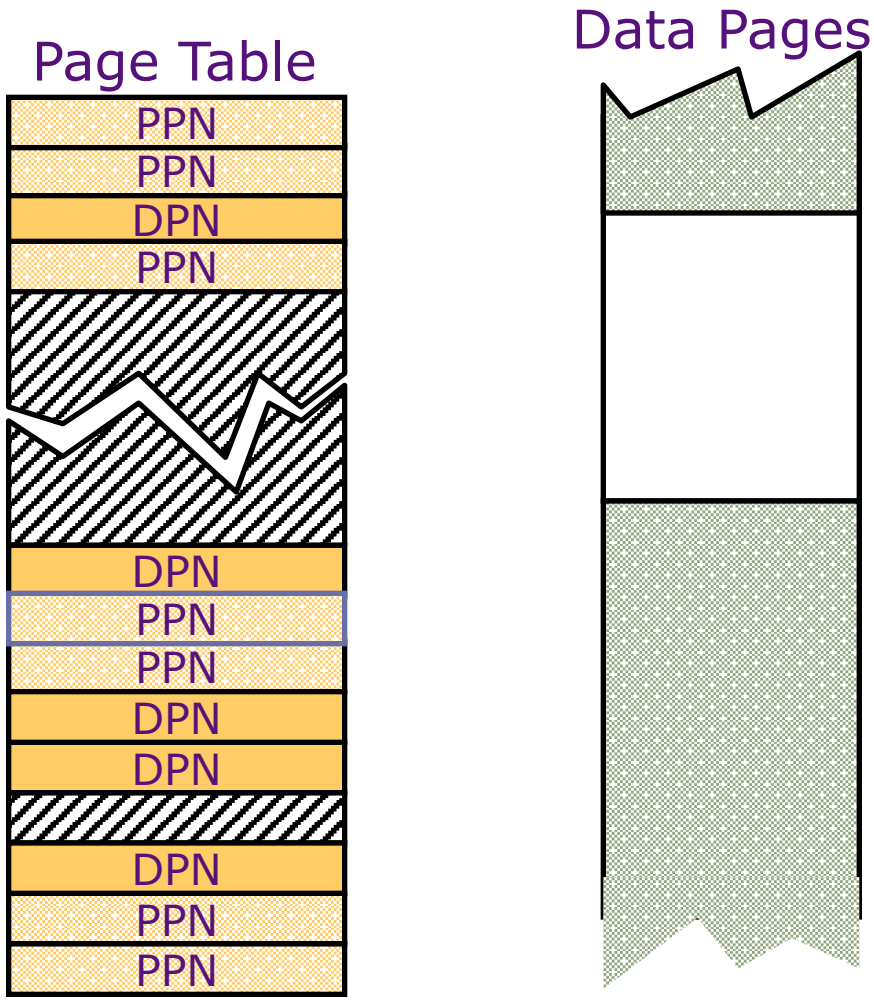

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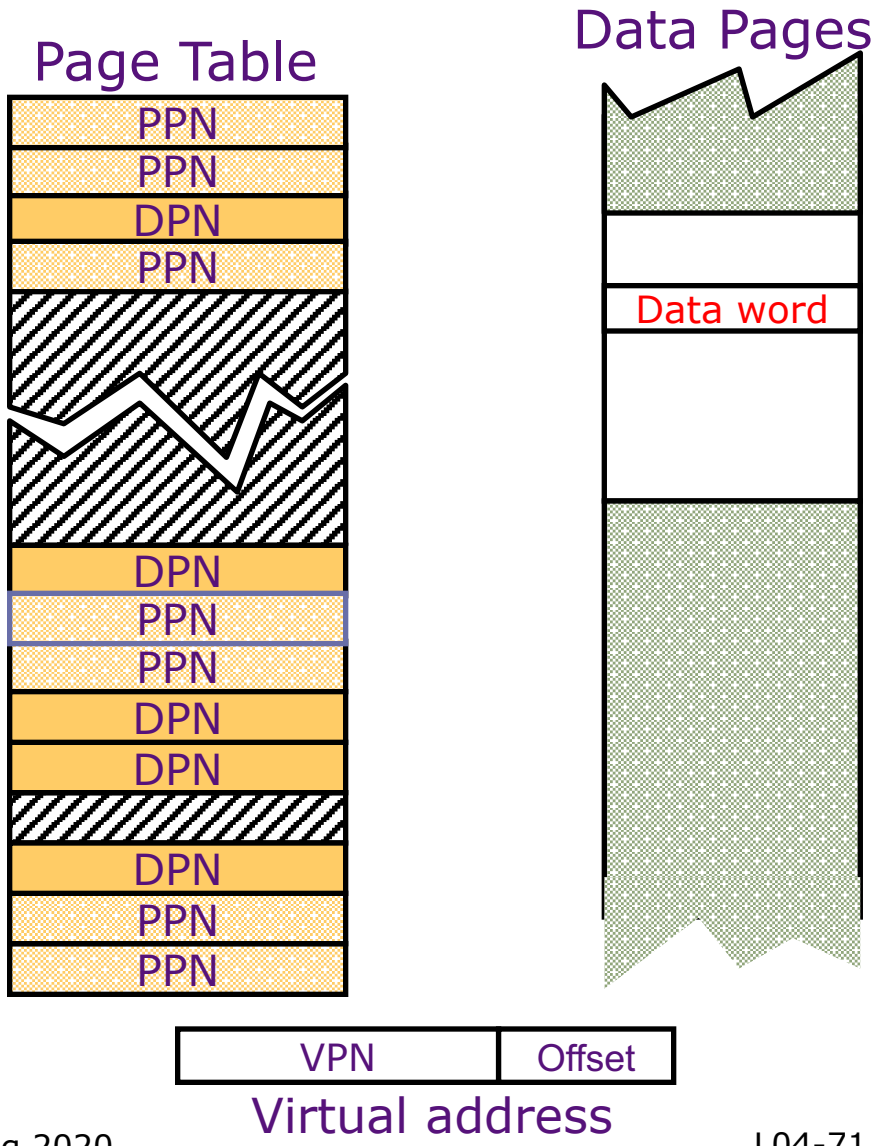

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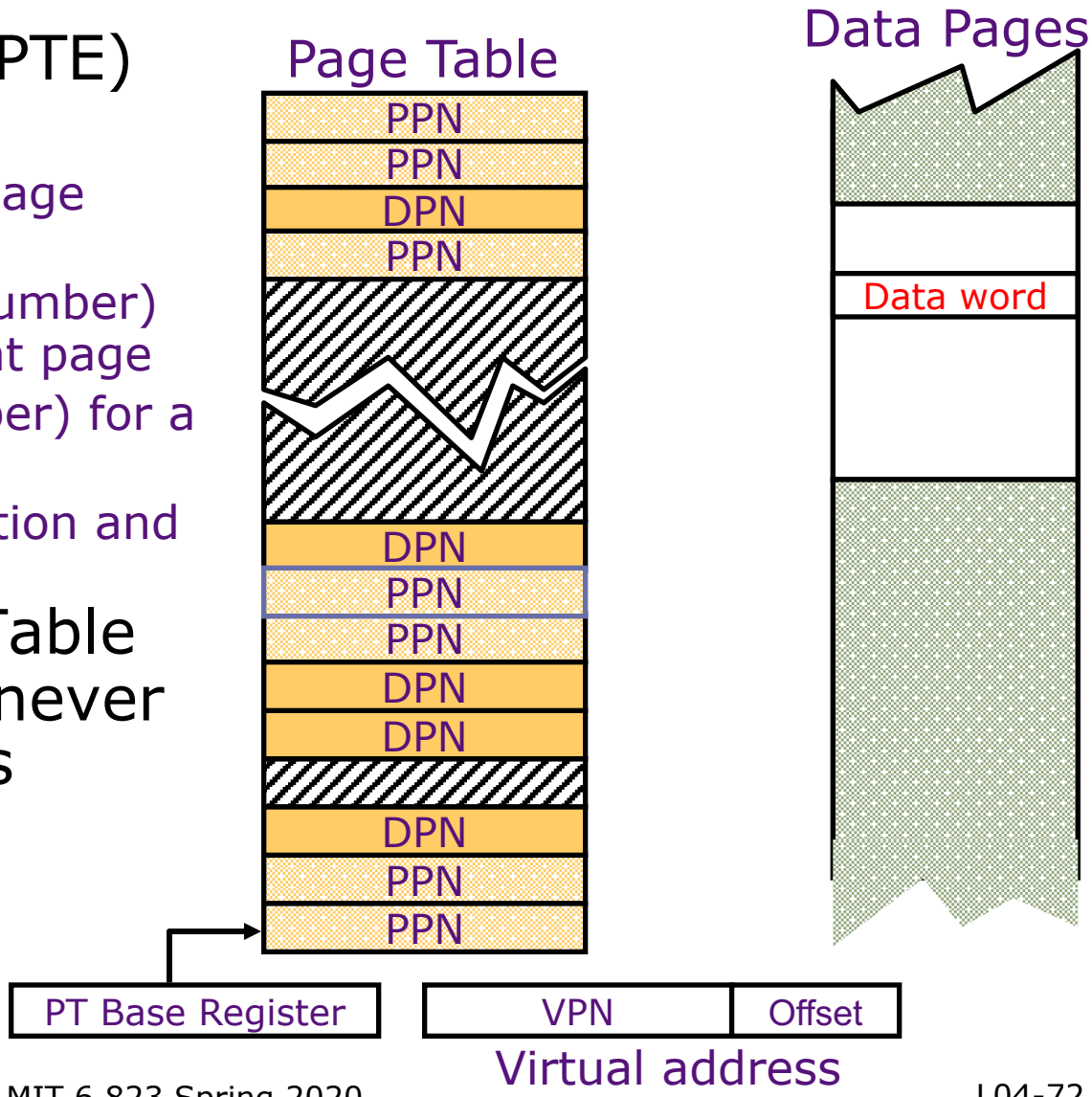

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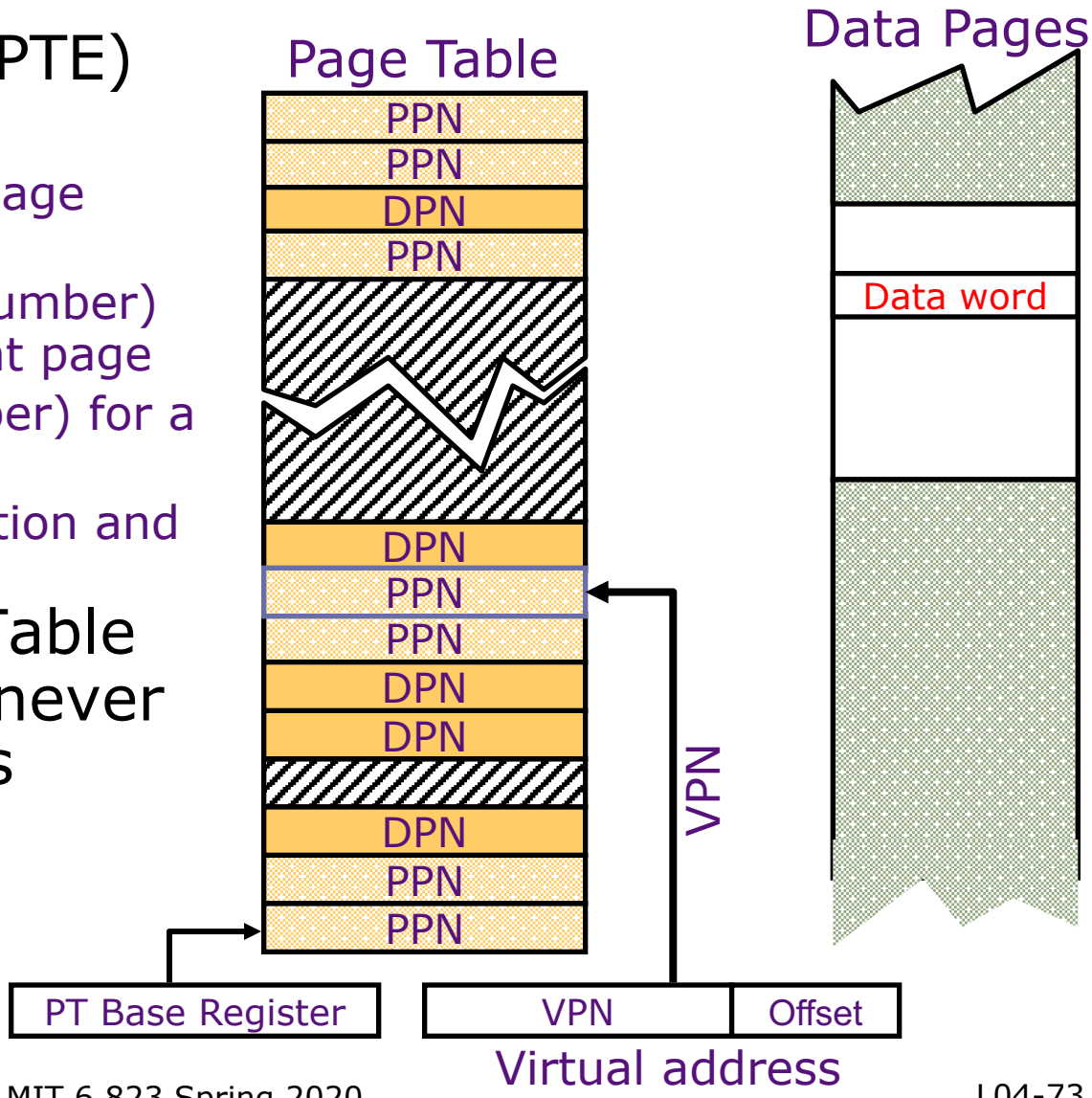

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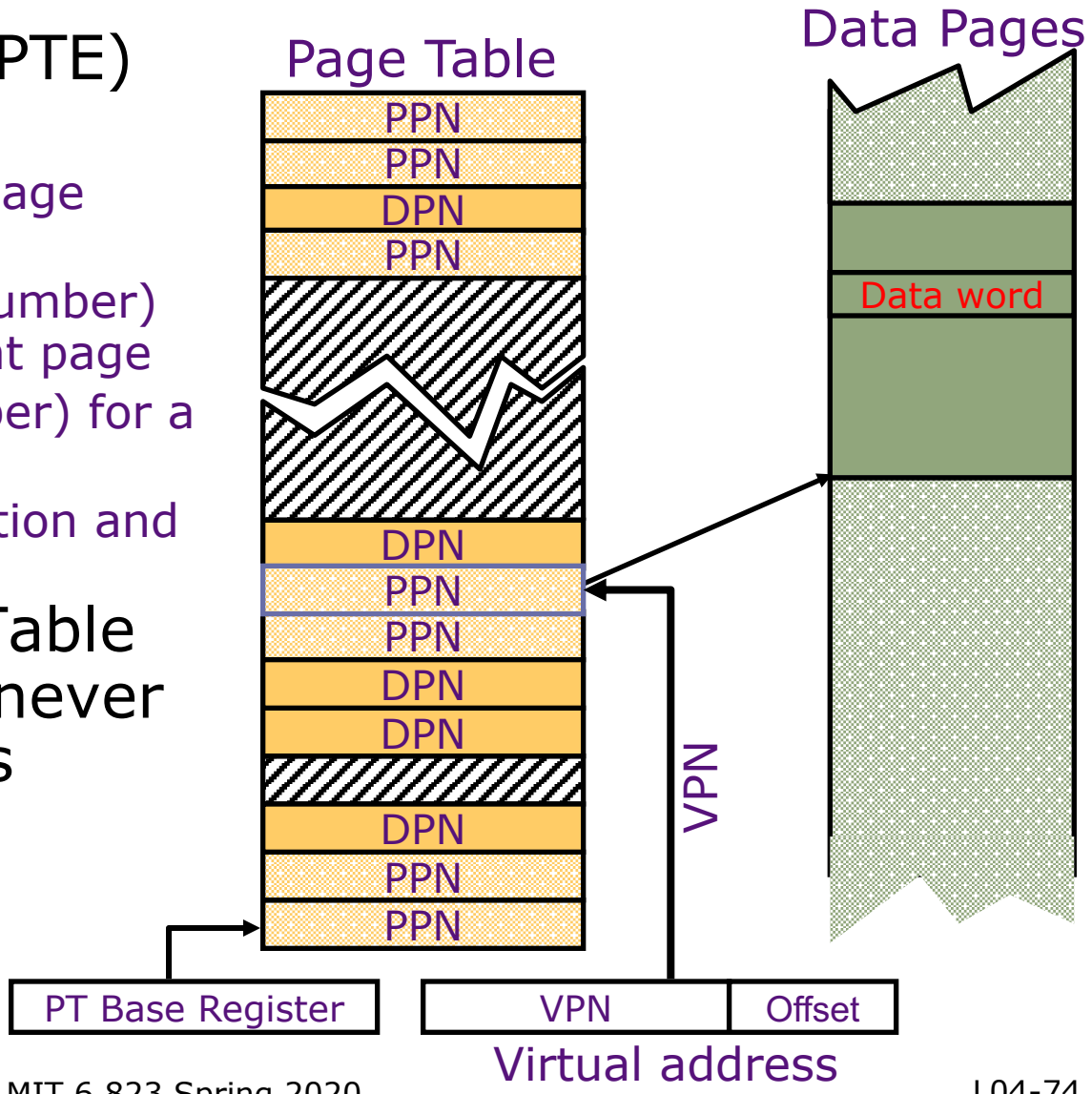

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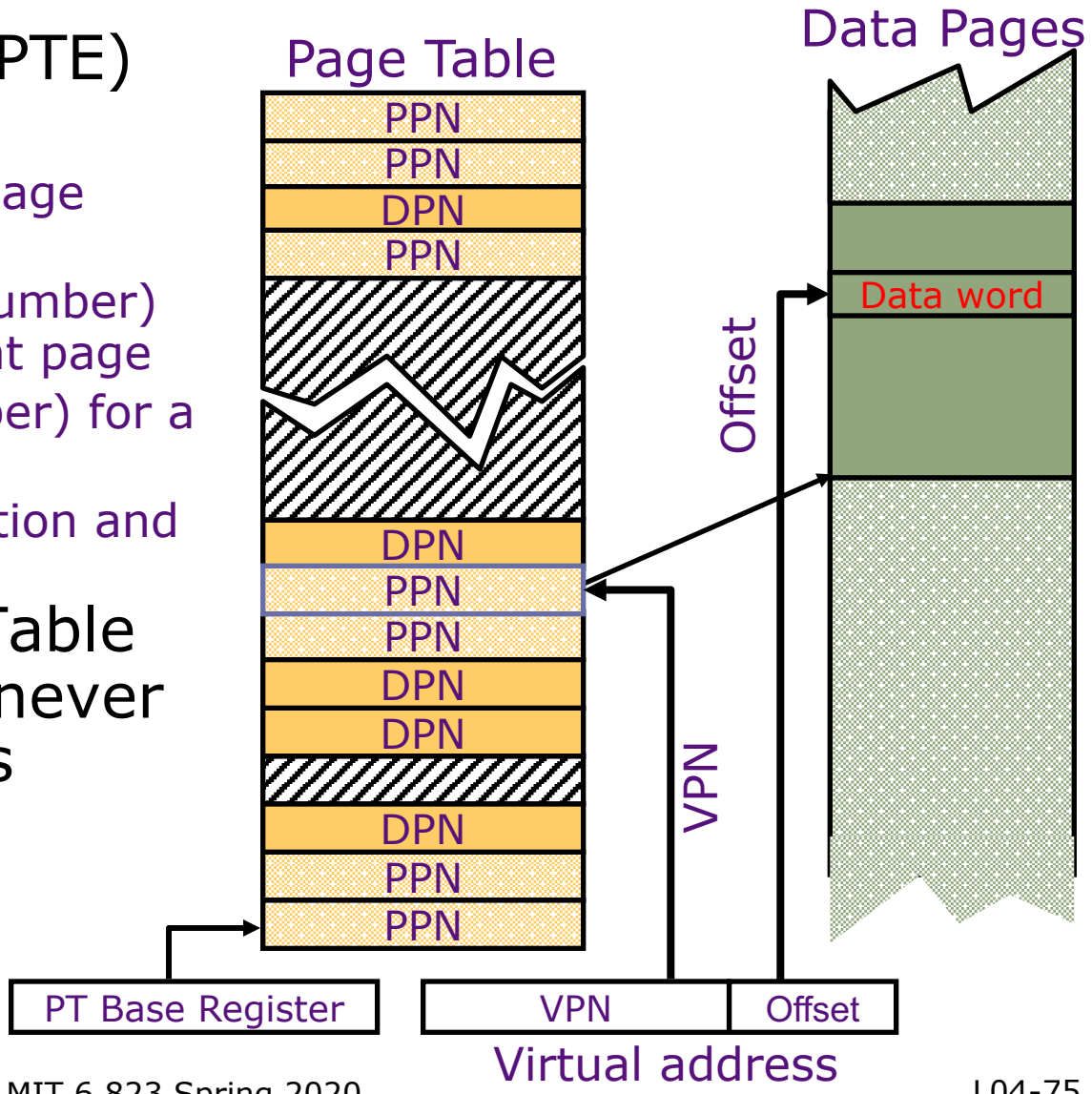

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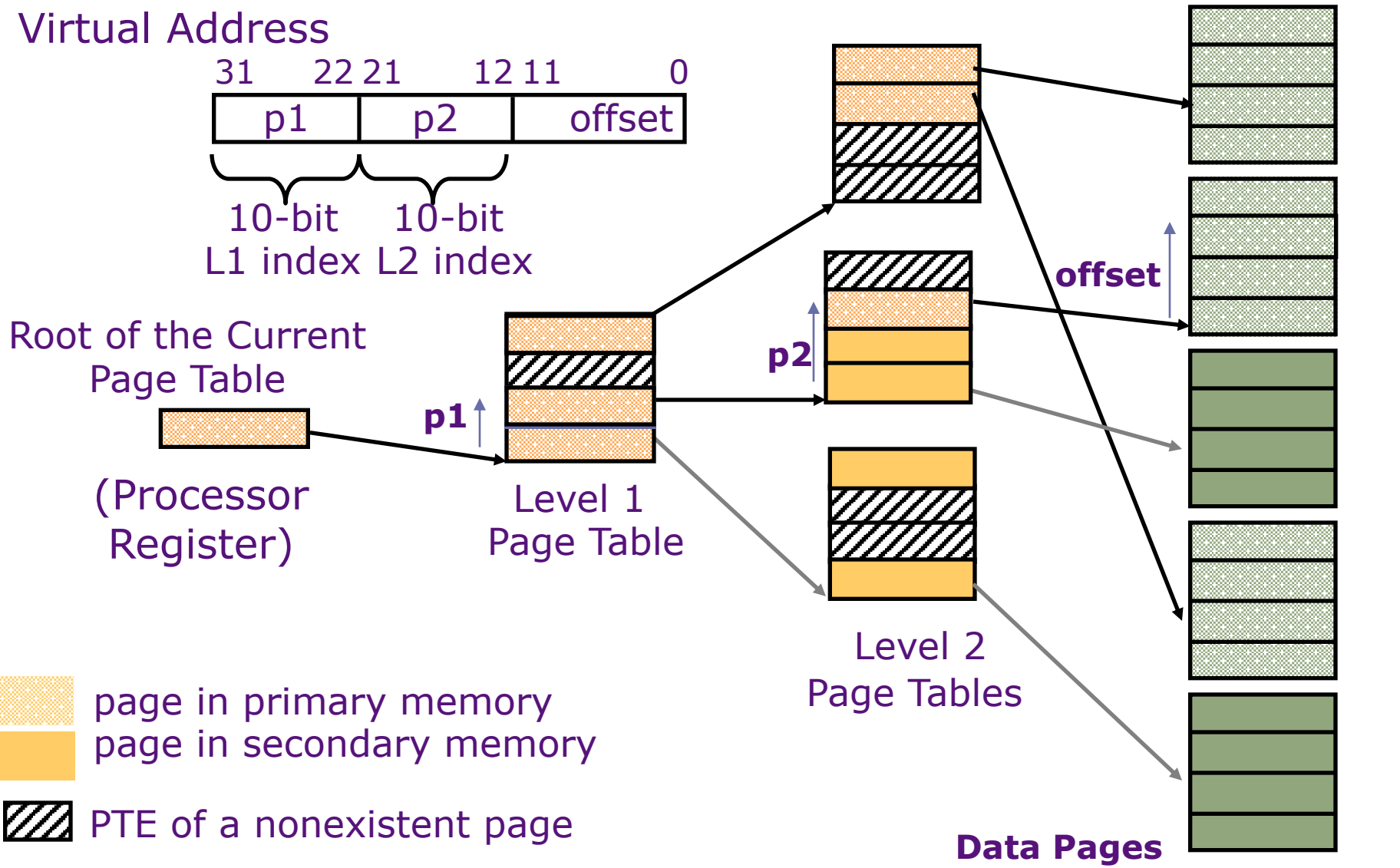
What is the "saving grace"?

Hierarchical Page Table



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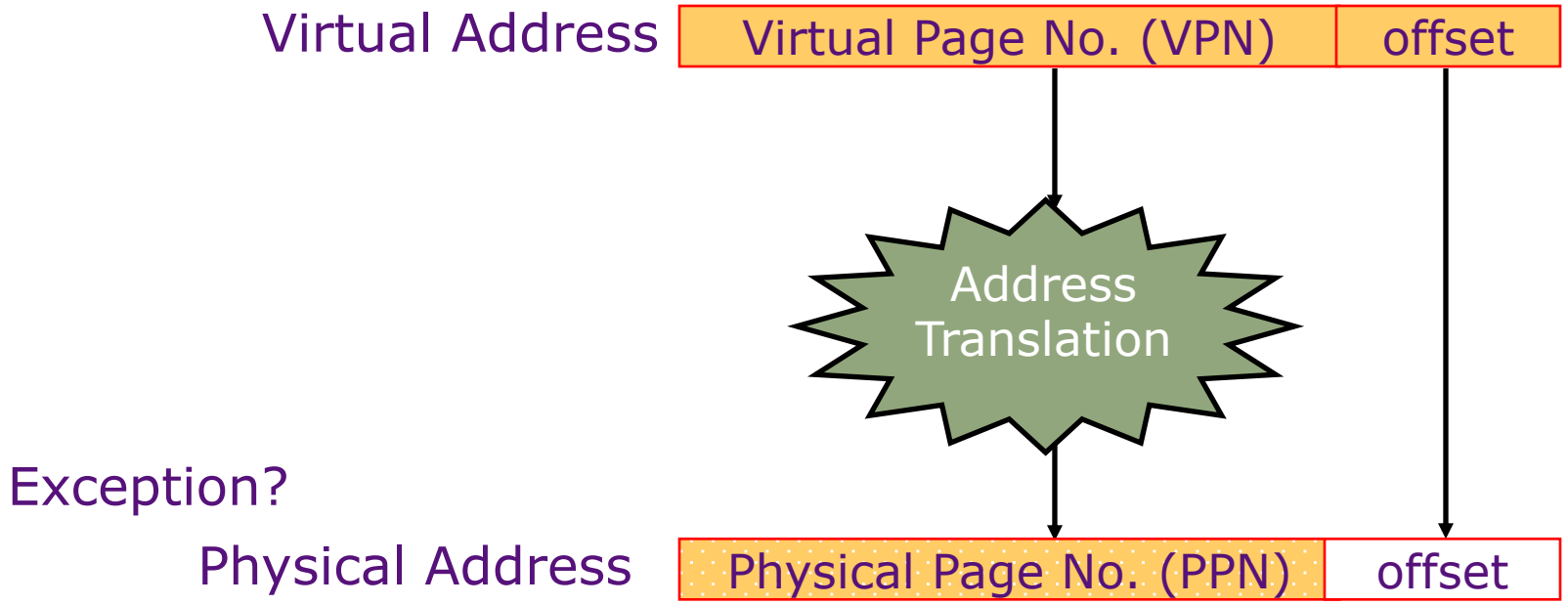

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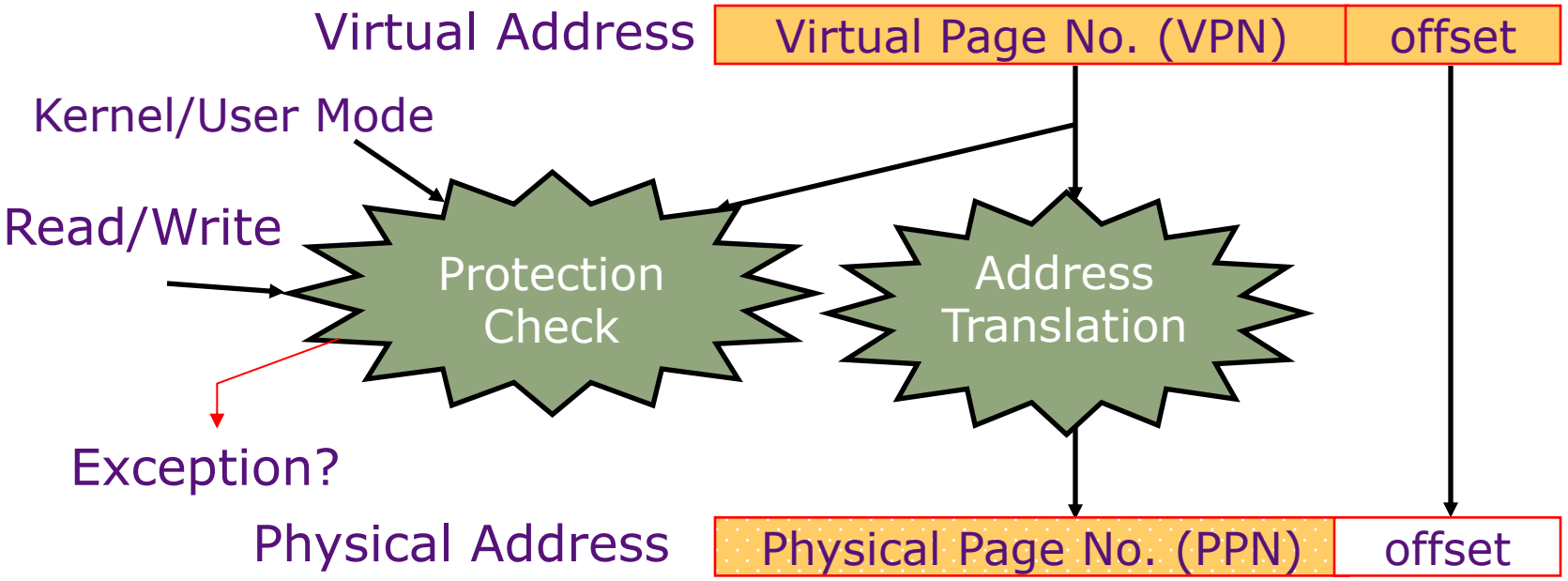

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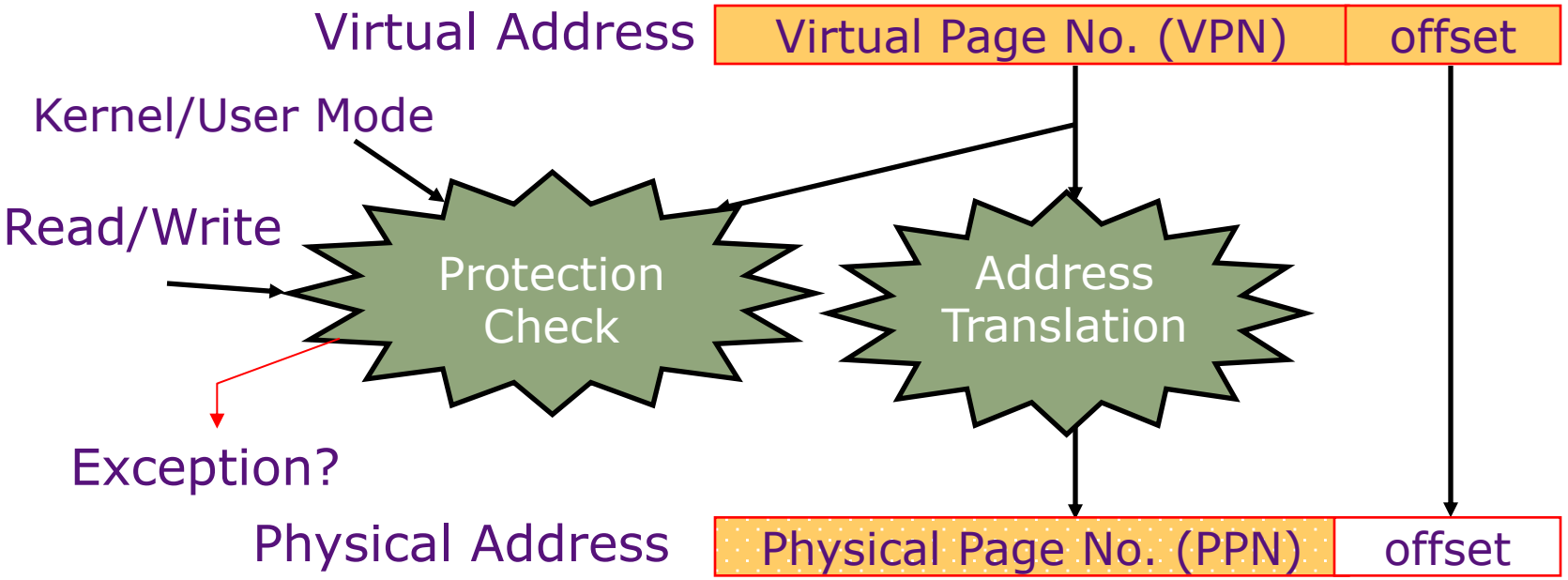


- Every instruction and data access needs address translation and protection checks

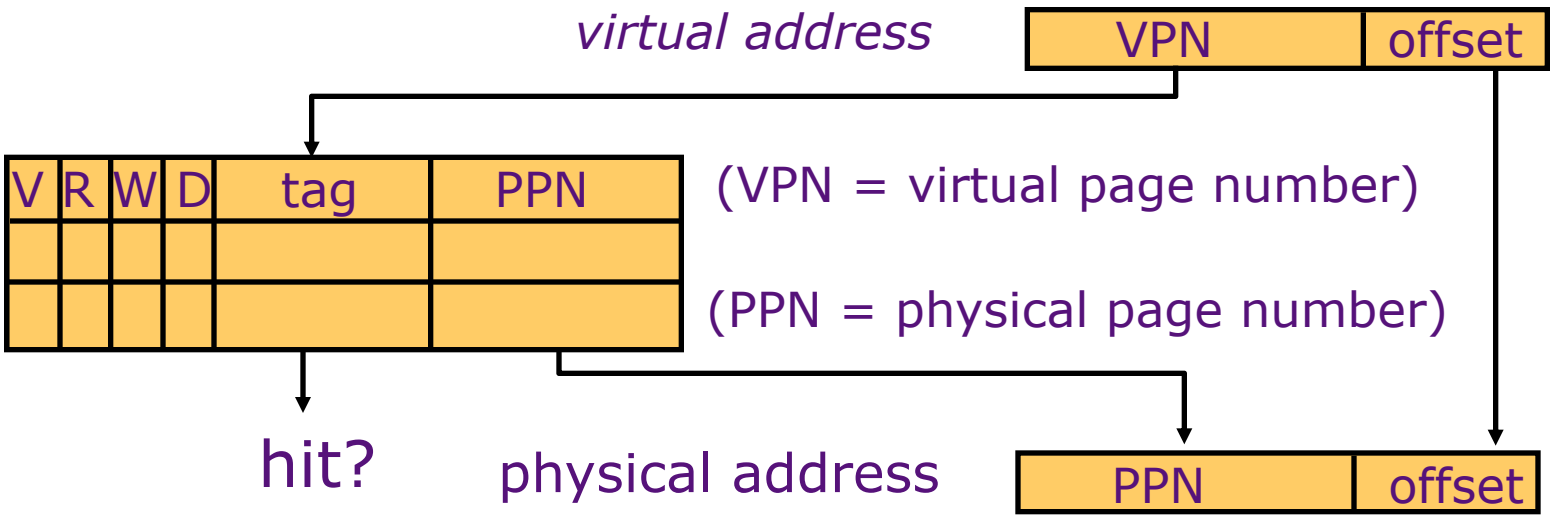
A good VM design needs to be fast (~ one cycle) and space-efficient

Translation Lookaside Buffers

Address translation is very expensive!

- In a two-level page table, each reference becomes several memory accesses

Solution: *Cache translations in TLB*



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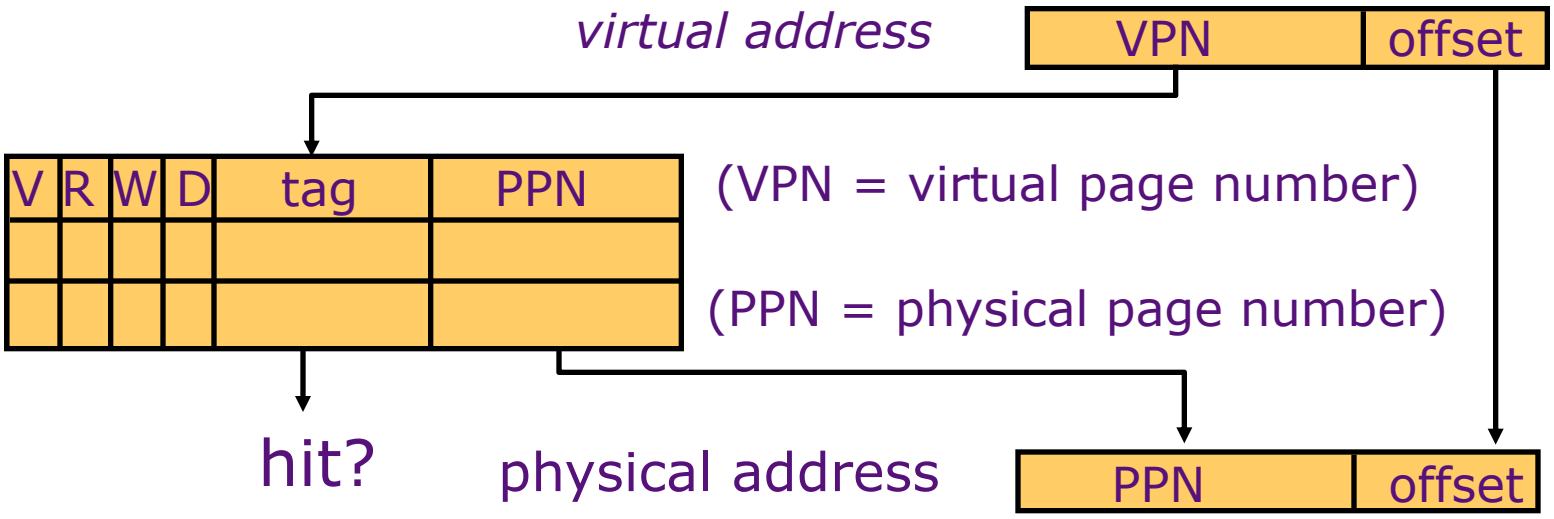
TLB hit ⇒ *Single-cycle Translation*

TLB miss ⇒ *Page Table Walk to refill*



TLB Designs

- Typically 32-128 entries, usually fully associative
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TLB Reach = _____*?*

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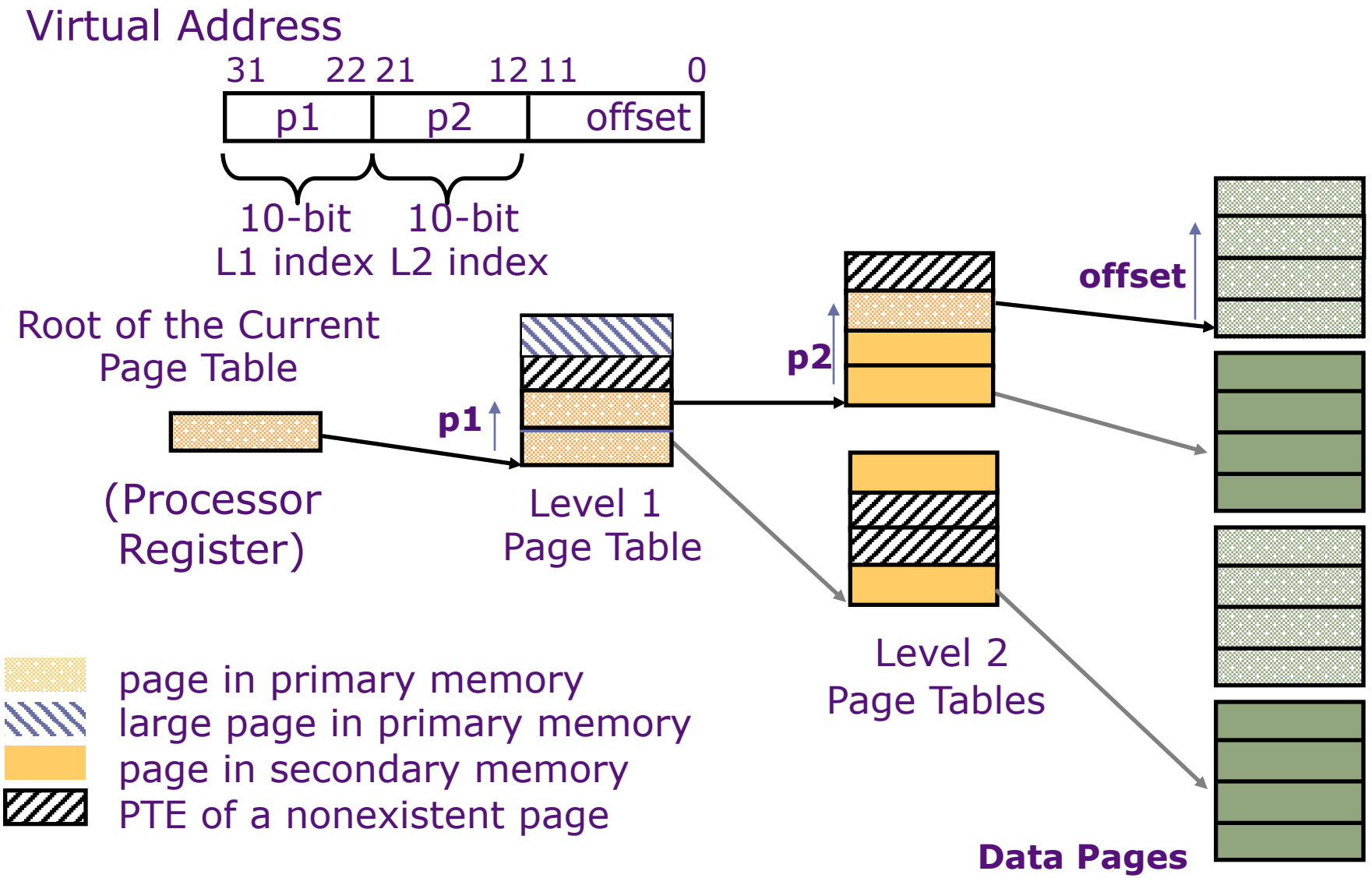
TLB Reach = *64 entries * 4 KB = 256 KB (if contiguous) ?*

Variable-Sized Page Support



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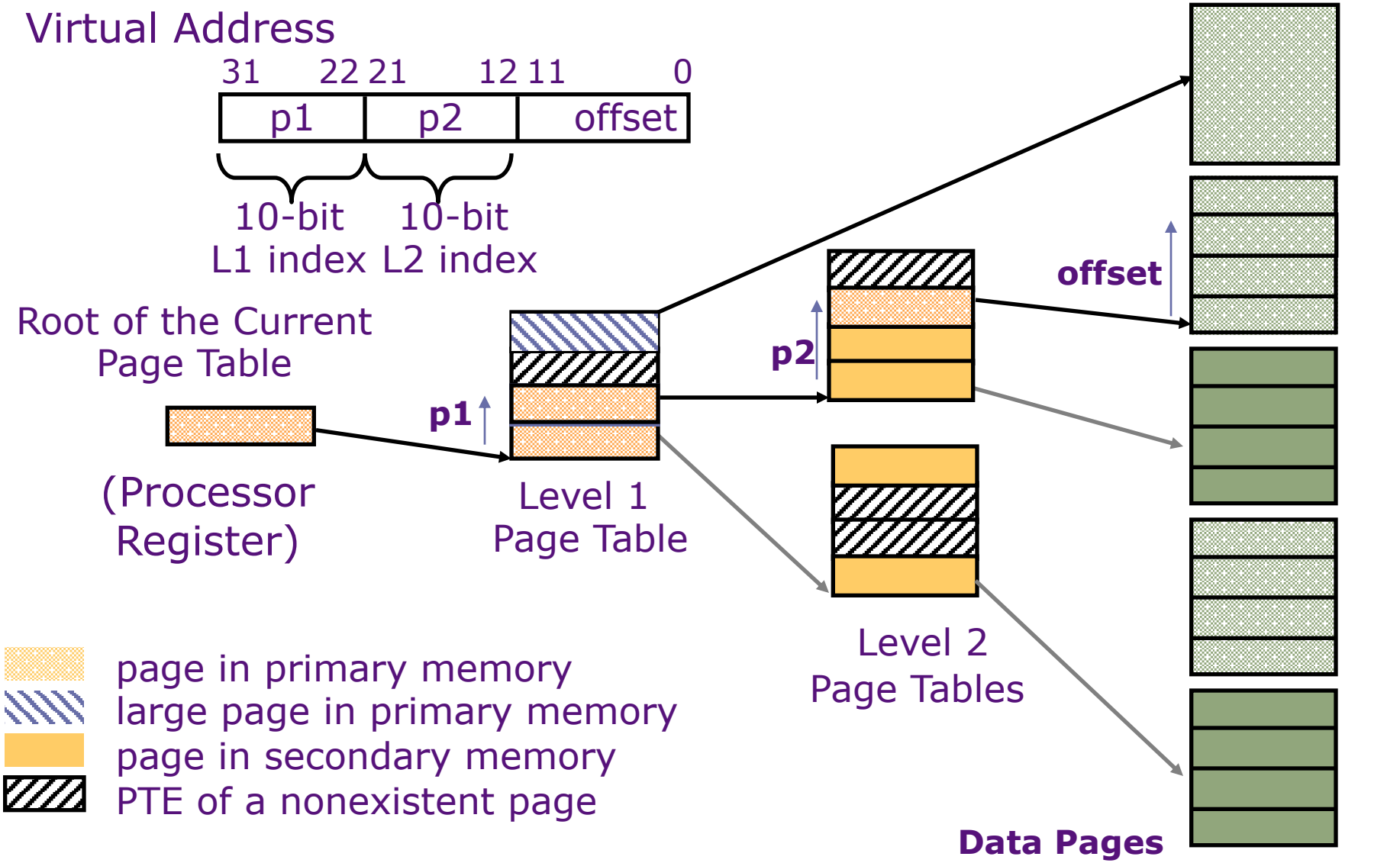
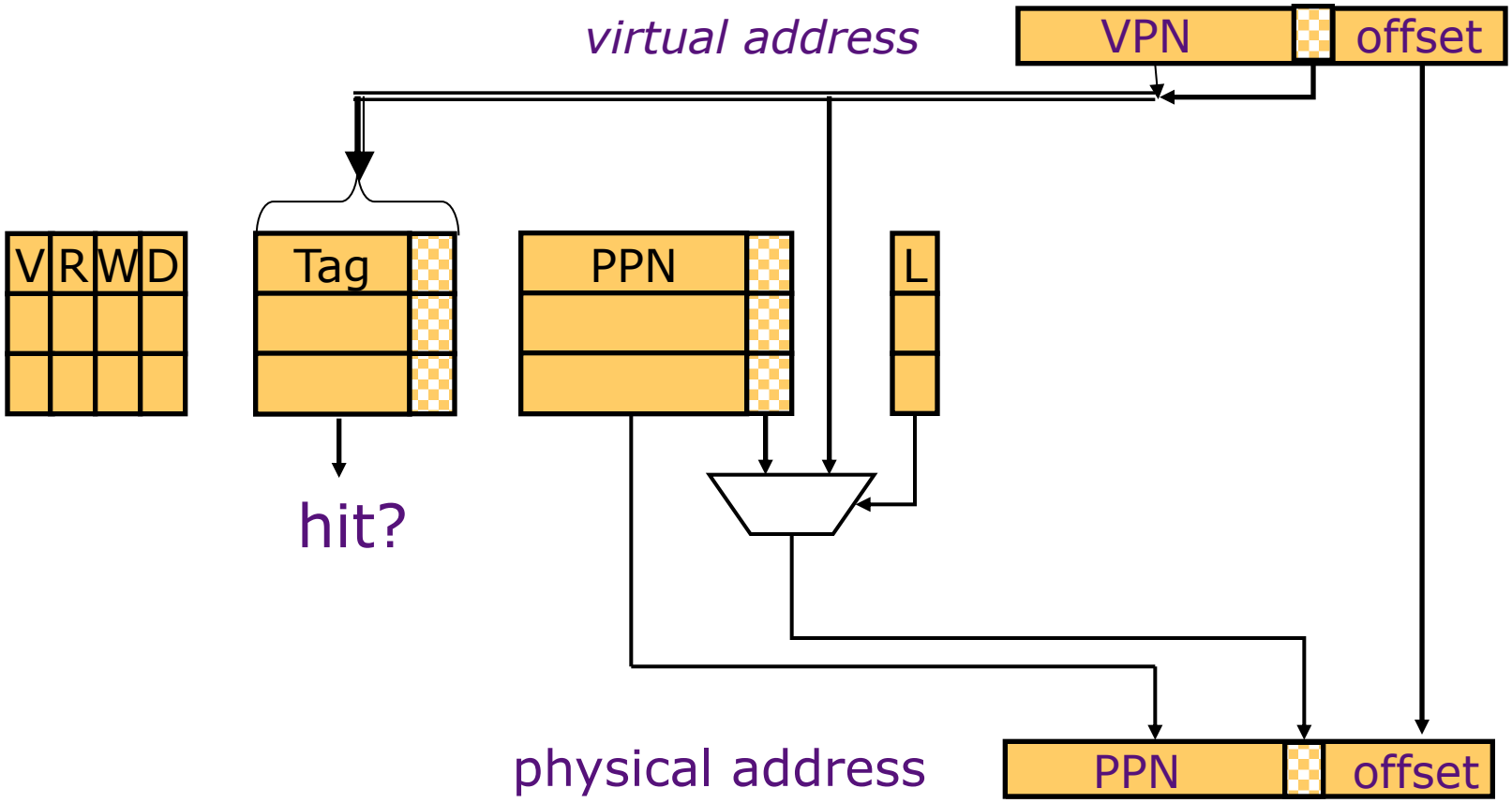


Variable-Size Page TLB

Some systems support multiple page sizes.



Handling a TLB Miss

Software (MIPS, Alpha)

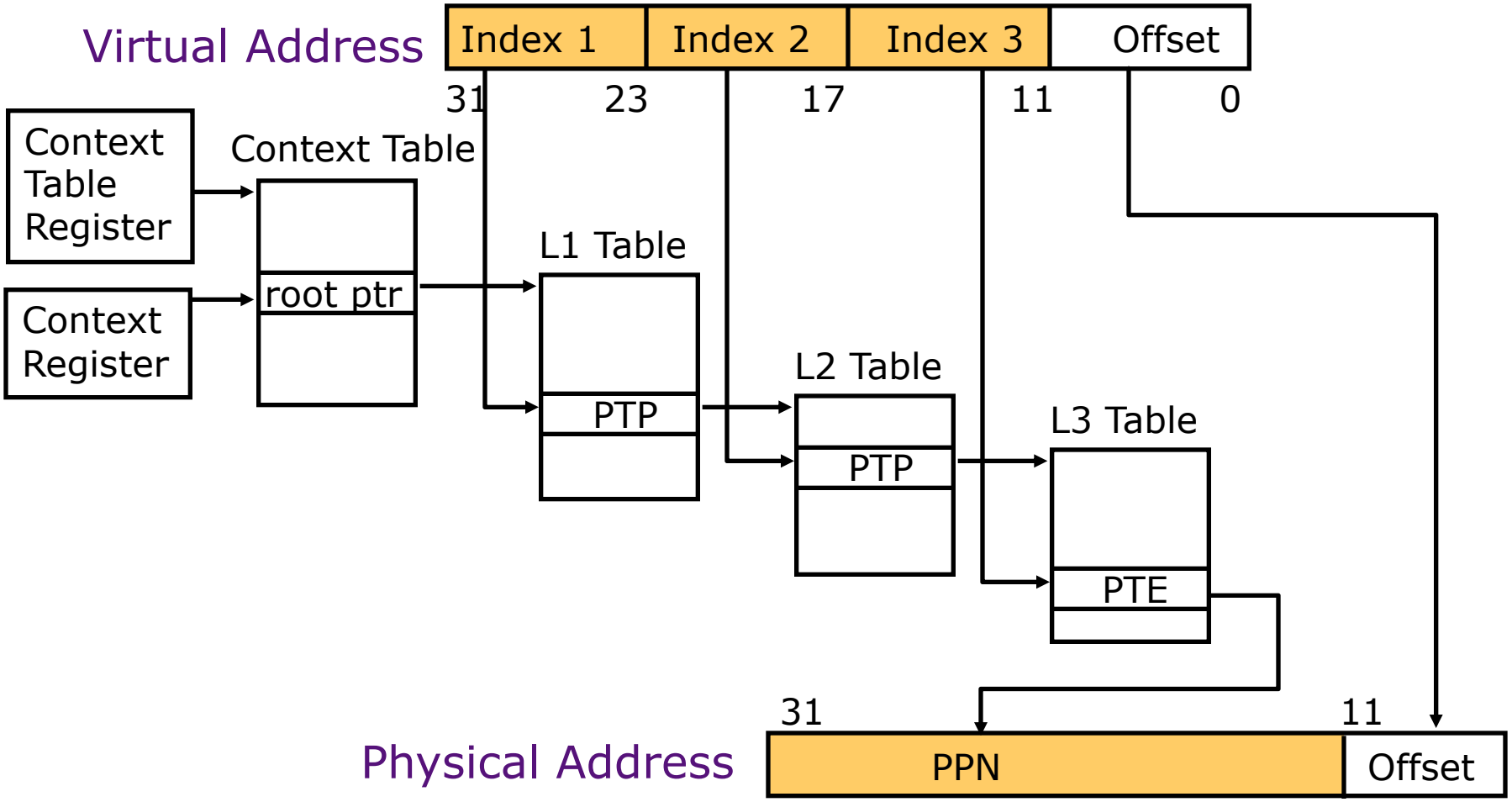
TLB miss causes an exception and the operating system walks the page tables and reloads TLB. *A privileged "untranslated" addressing mode used for walk*

Hardware (SPARC v8, x86, PowerPC)

A memory management unit (MMU) walks the page tables and reloads the TLB

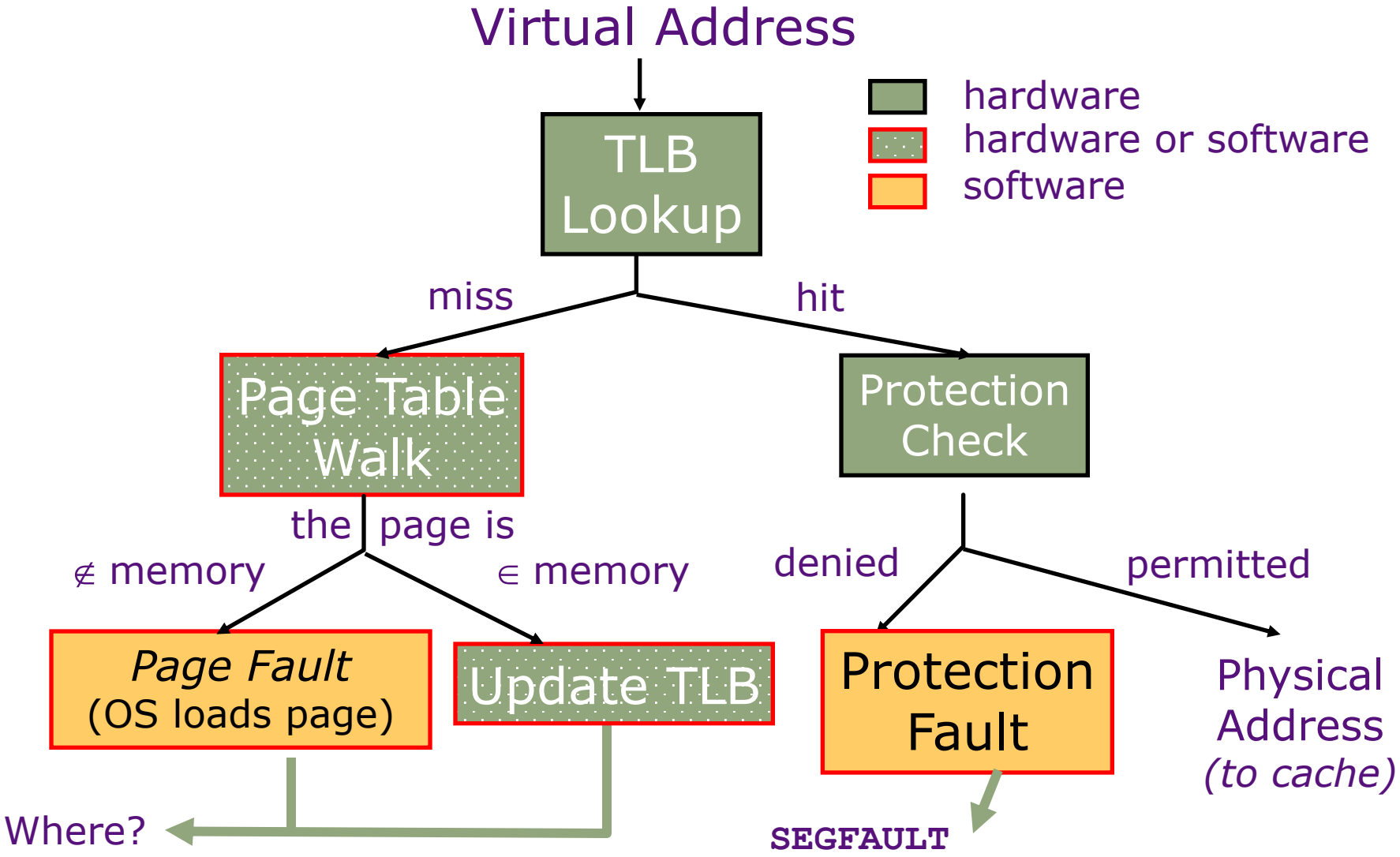
If a missing (data or PT) page is encountered during the TLB reloading, MMU gives up and signals a Page-Fault exception for the original instruction

Hierarchical Page Table Walk: SPARC v8



MMU does this table walk in hardware on a TLB miss

Address Translation:
putting it all together



Next lecture:

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