Advanced Memory Operations

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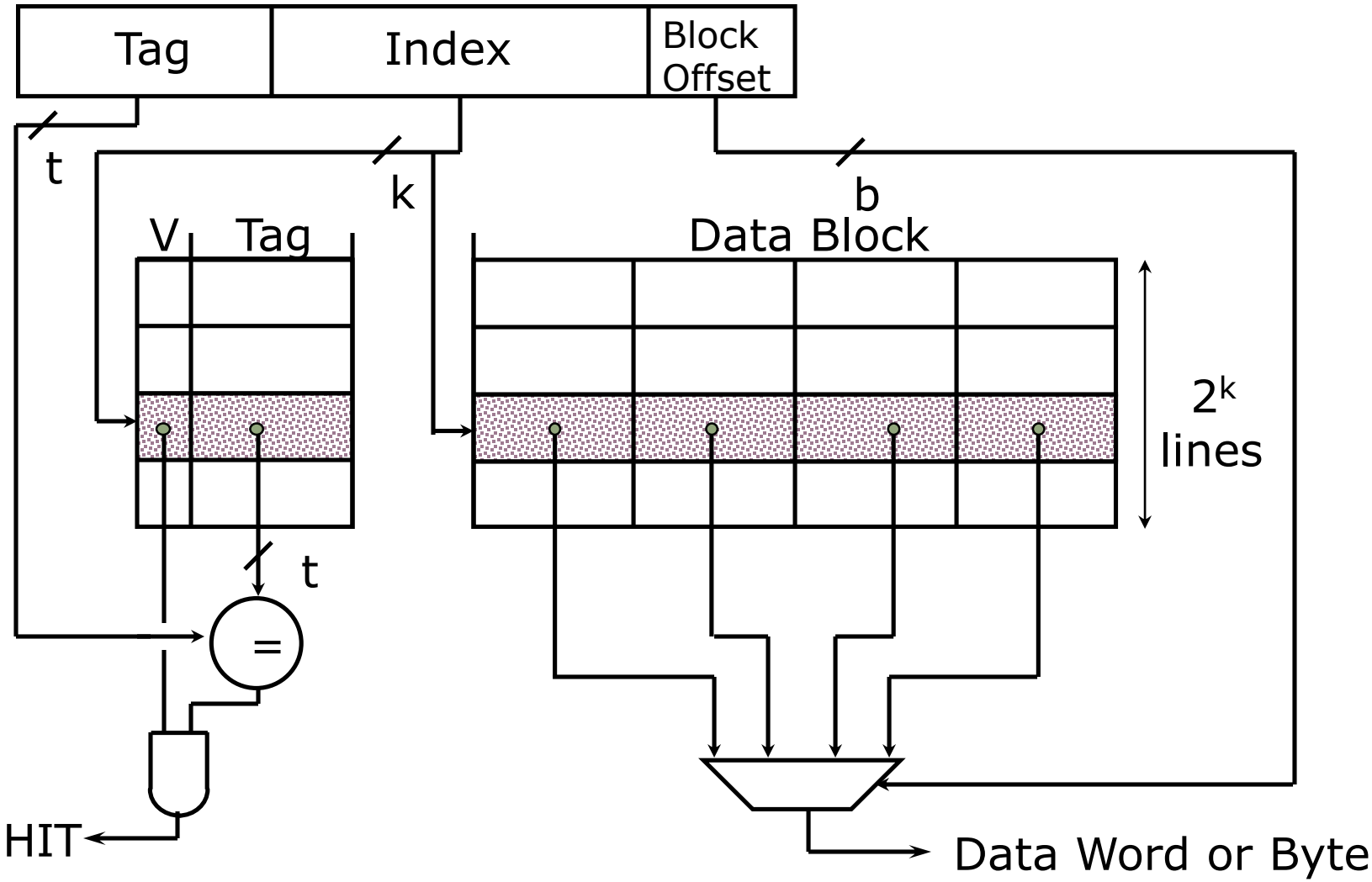
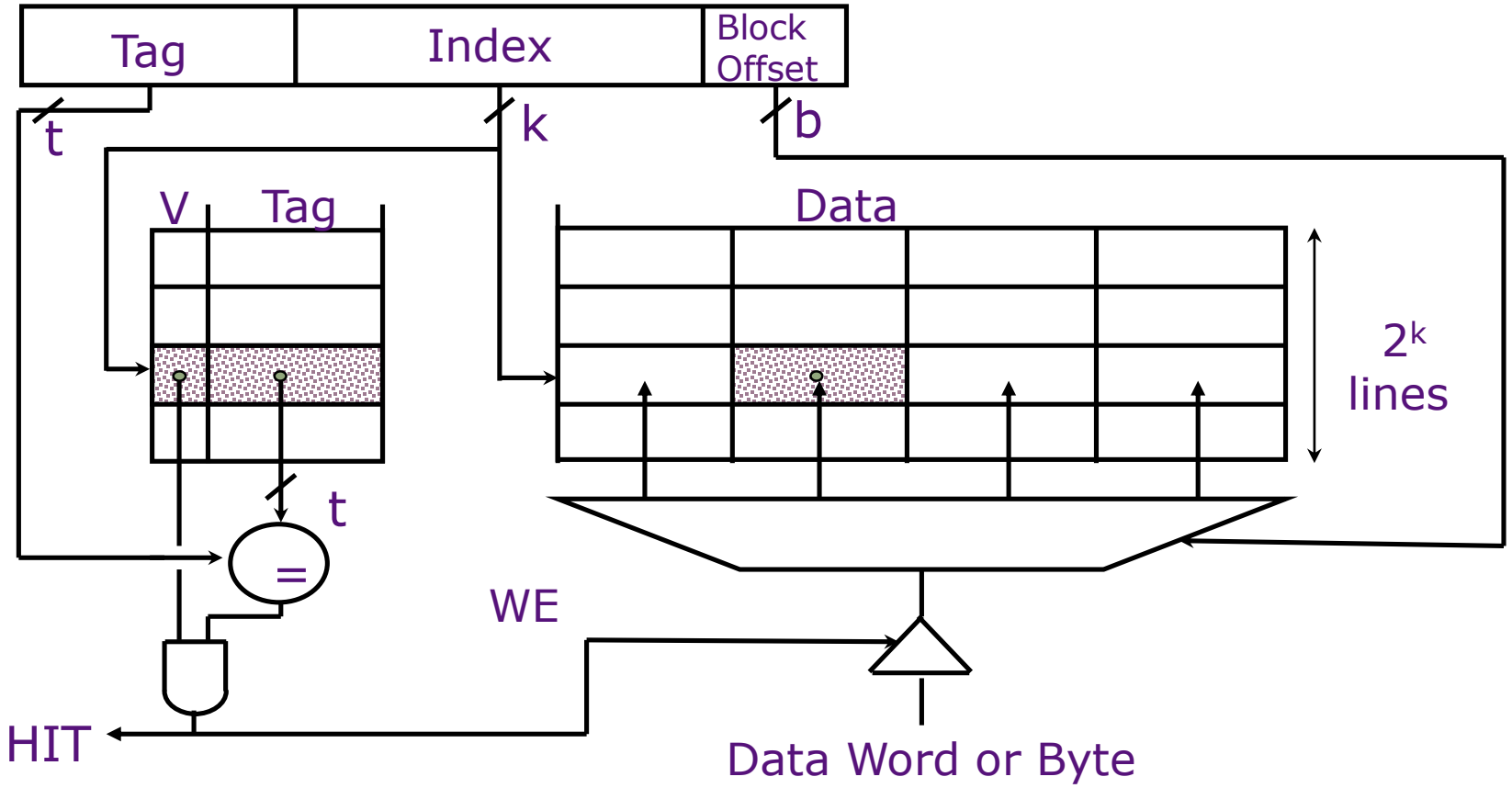
Computer Science and Artificial Intelligence Laboratory
M.I.T.

Reminder: Direct-Mapped Cache



Write Performance



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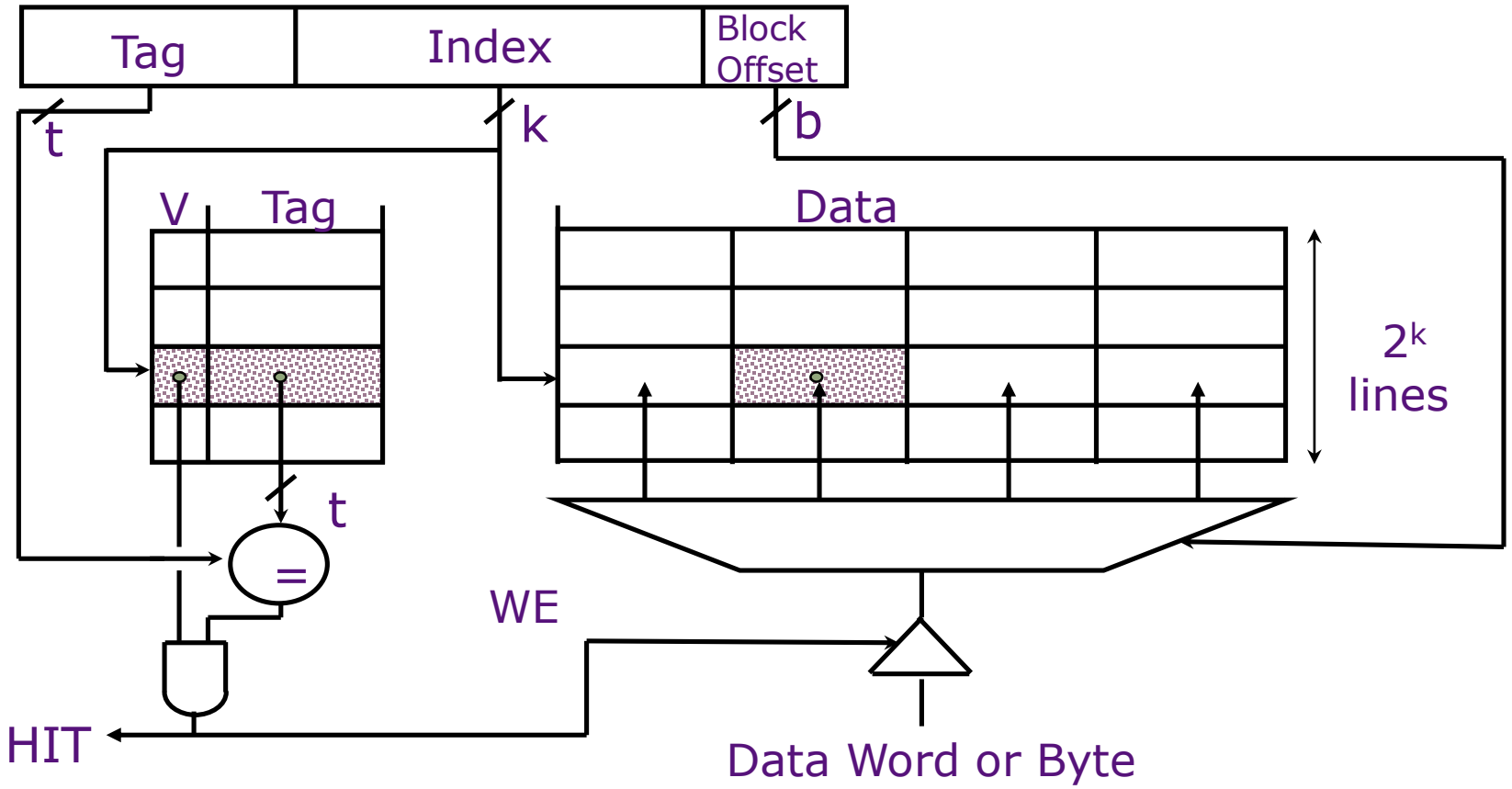

How does write timing compare to read timing?

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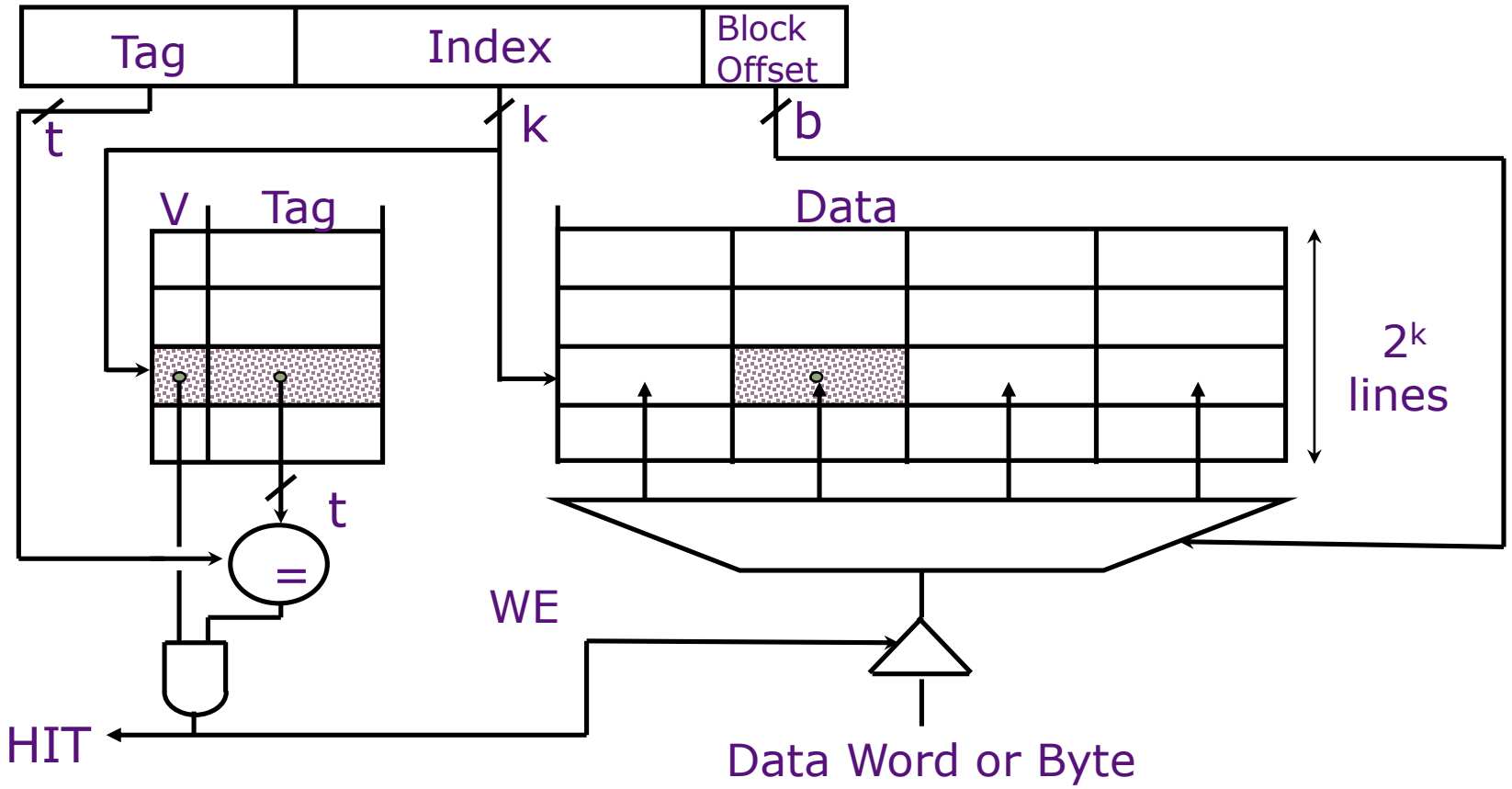

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Completely serial!

Reducing Write Hit Time

Problem: Writes take two cycles in memory stage, one cycle for tag check plus one cycle for data write if hit

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- Speculate predicting miss with lazy data update:
  - Hold write data for store in single buffer ahead of cache
  - Write cache data during next idle data access cycle (commit)

Pipelined/Delayed Write Timing

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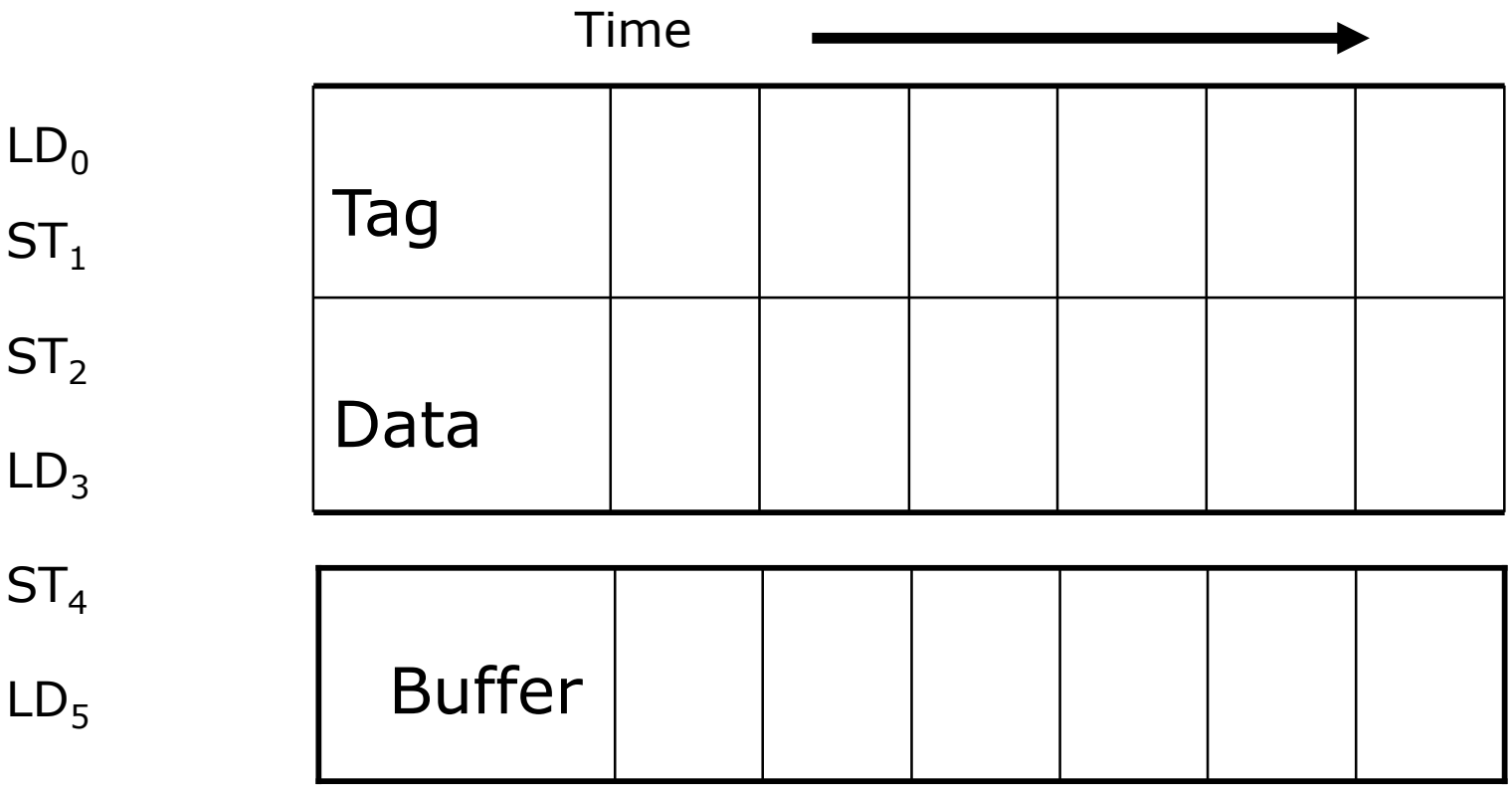

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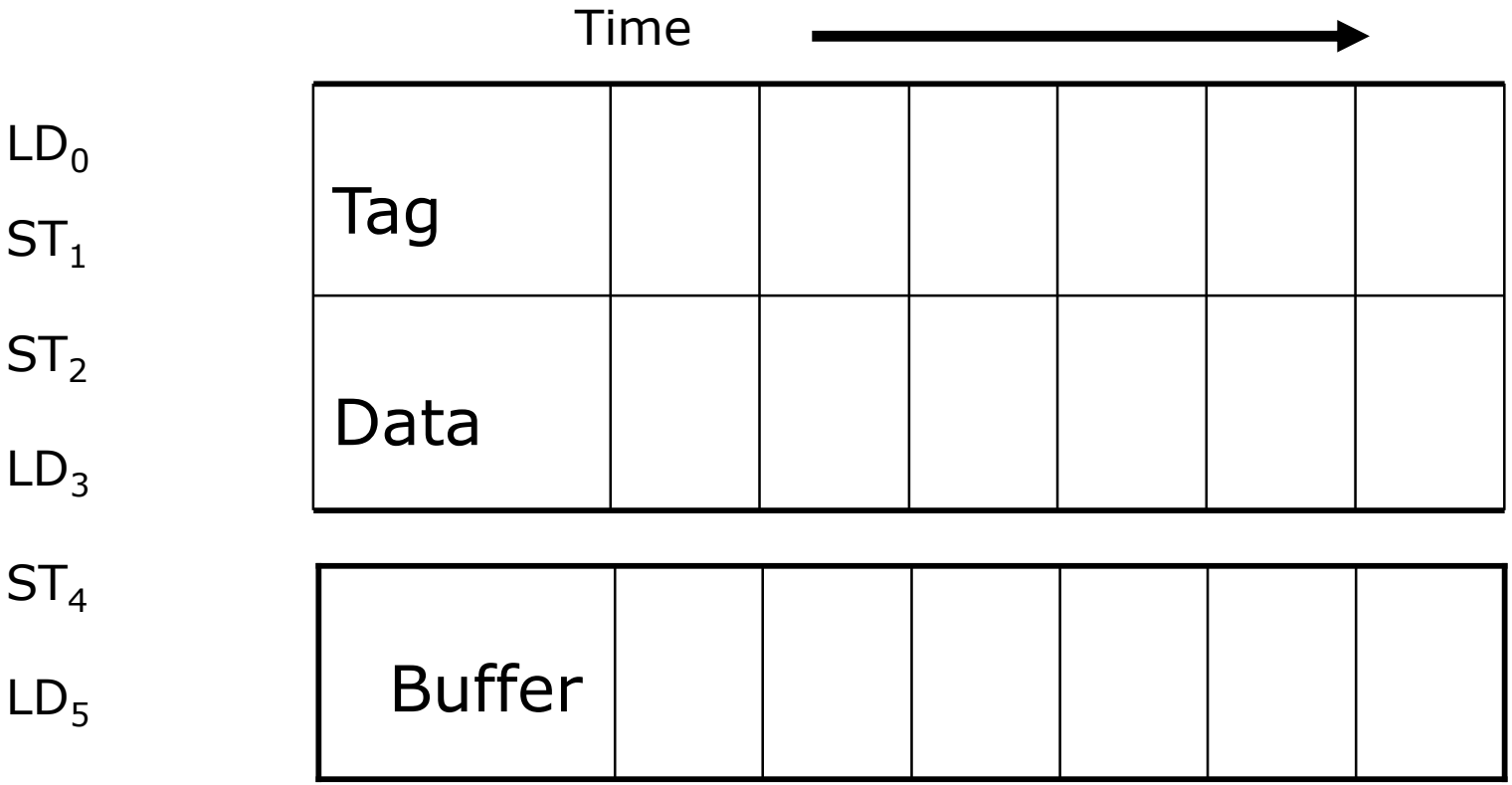

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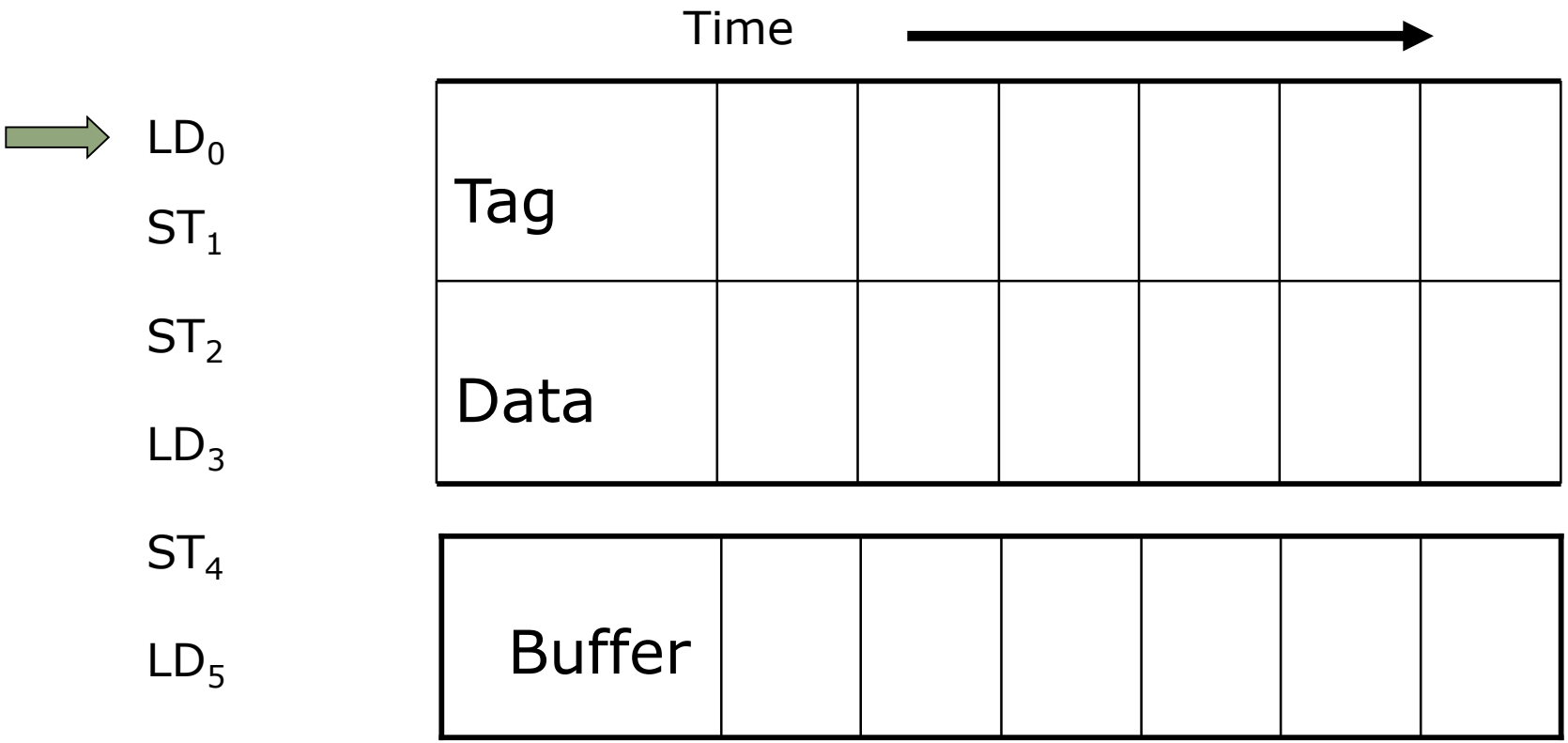

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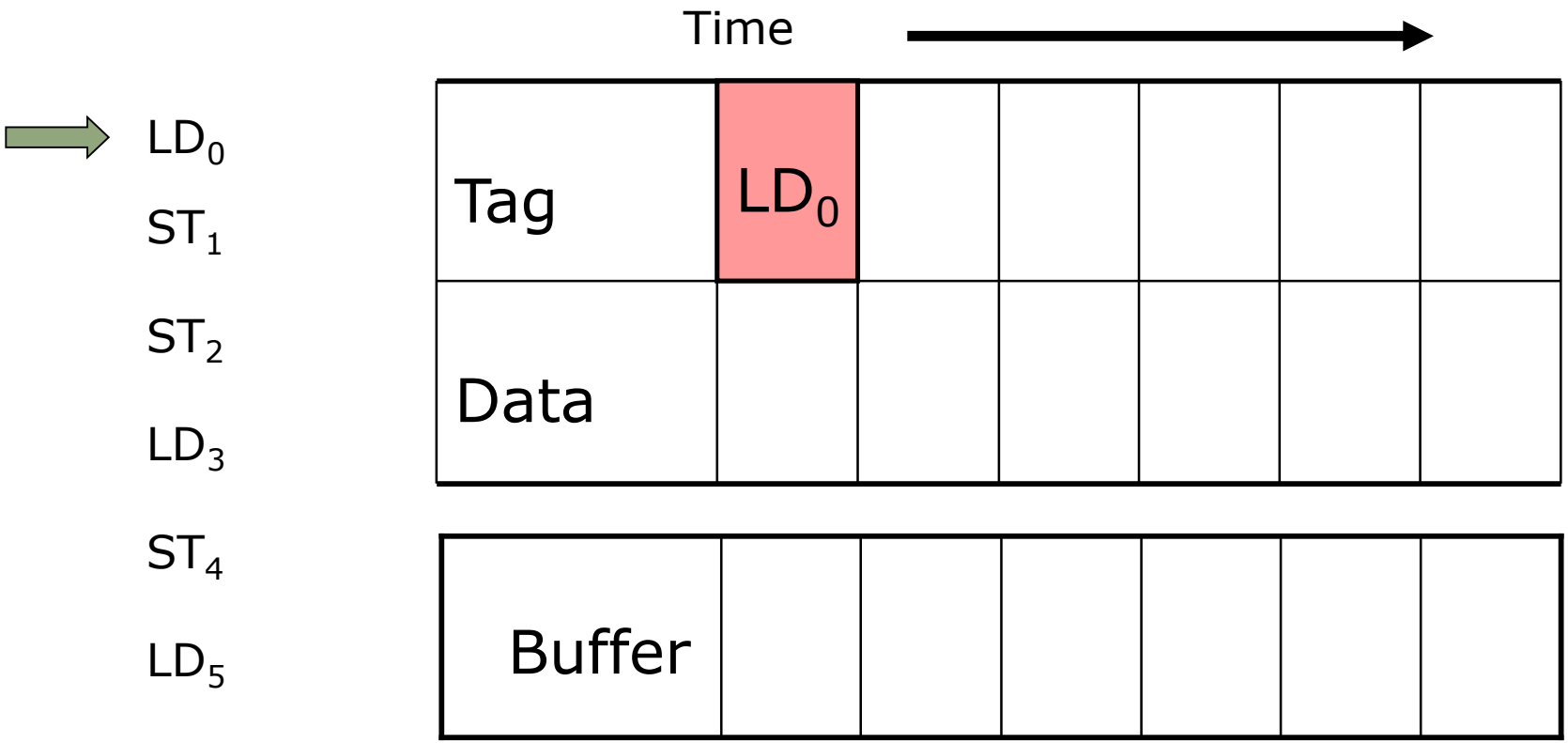

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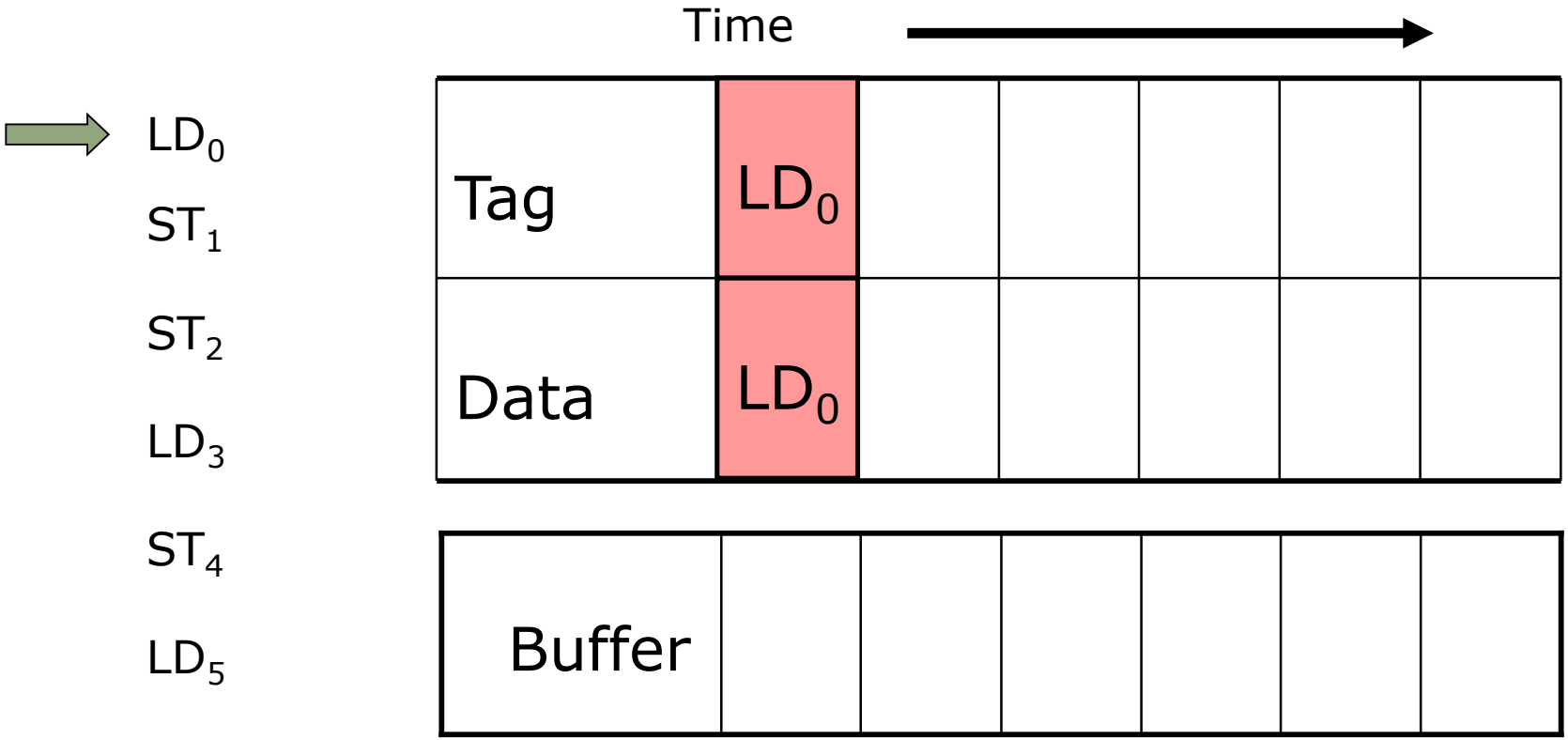

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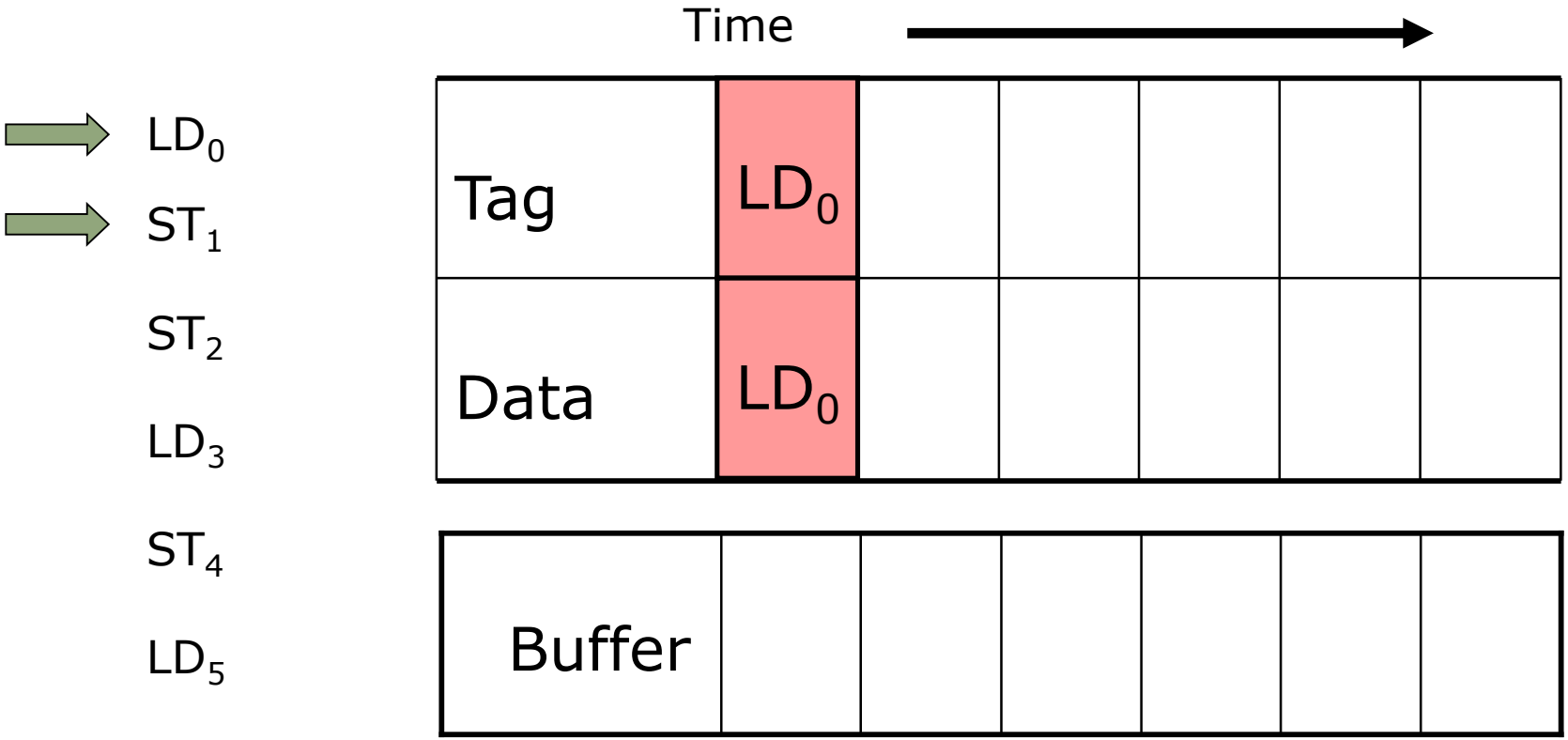

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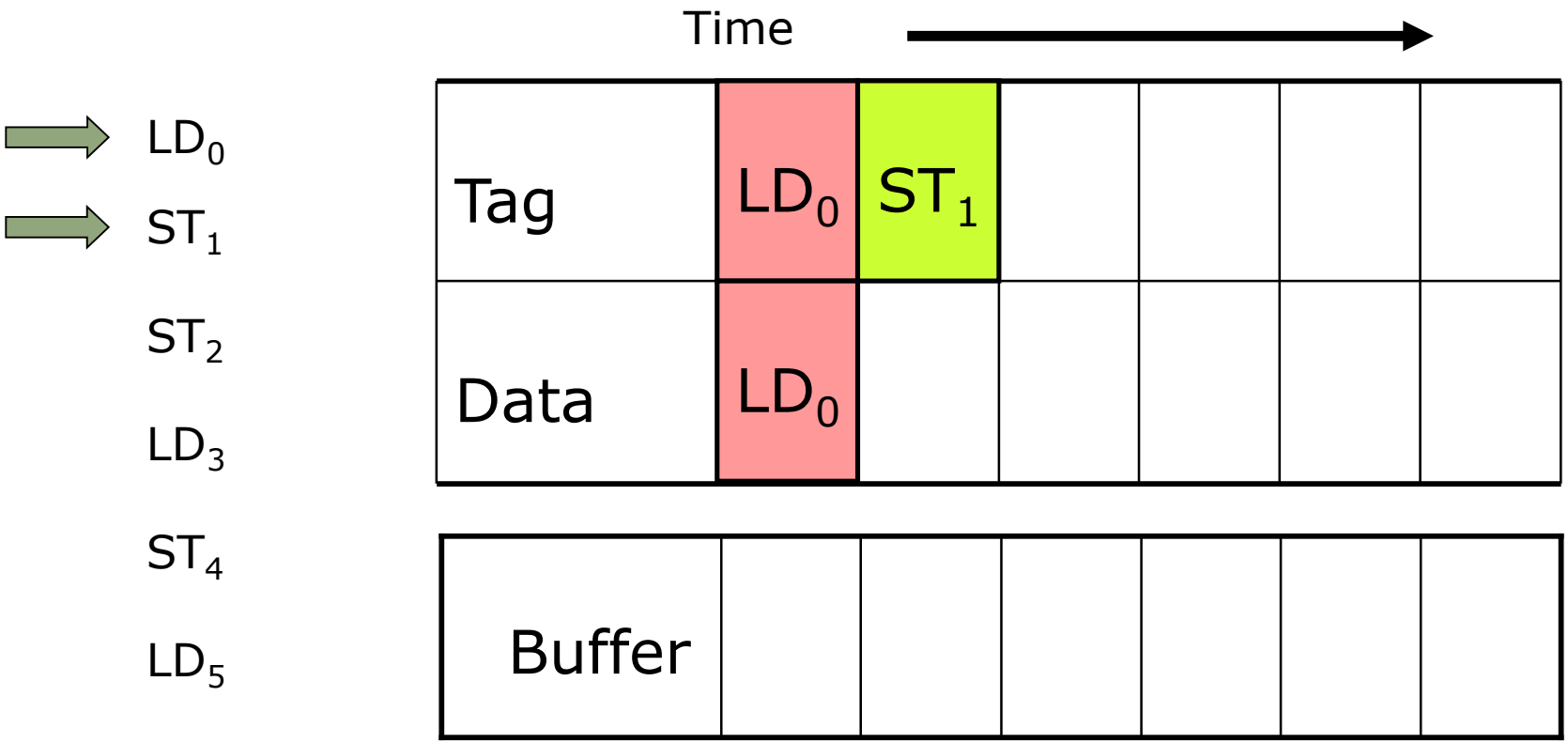

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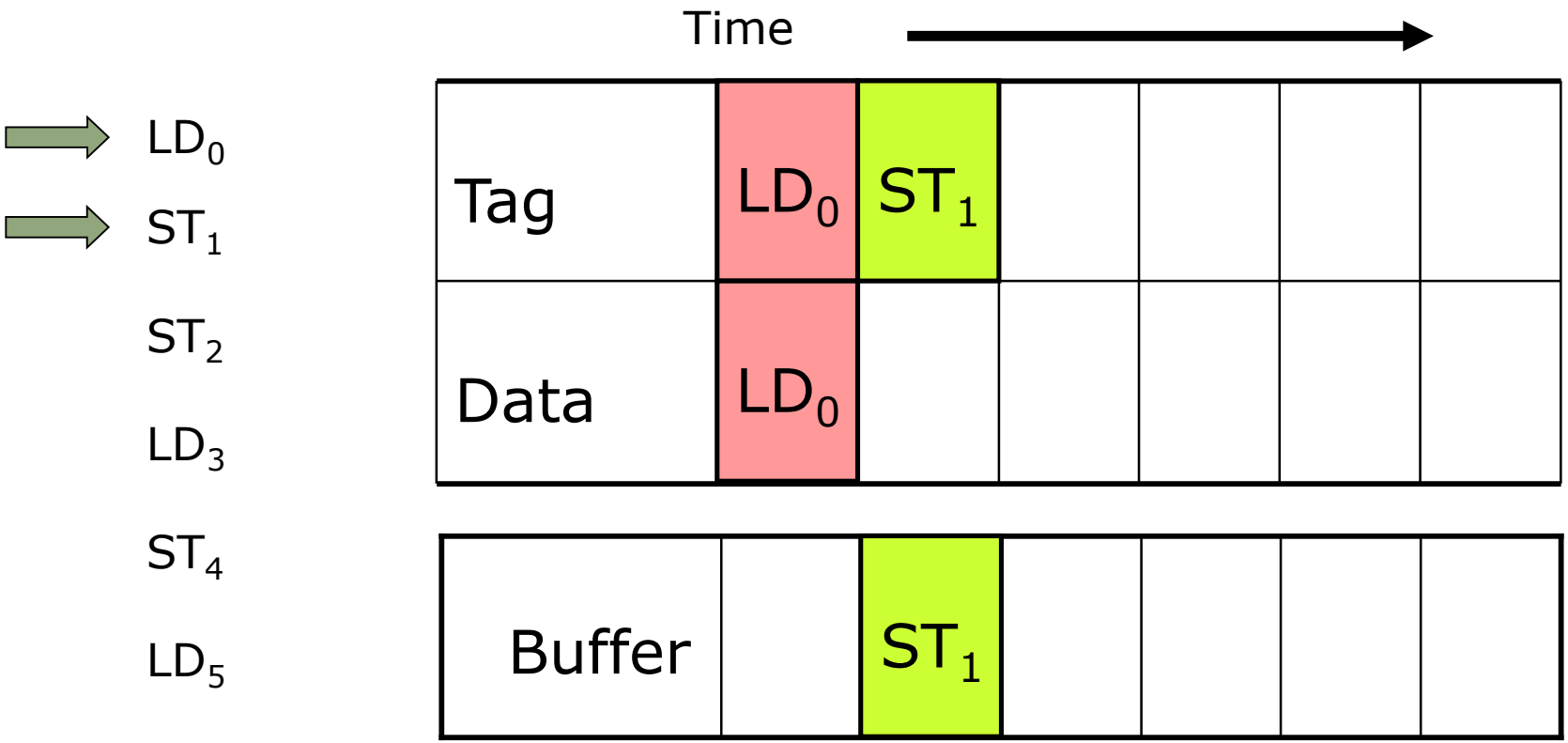

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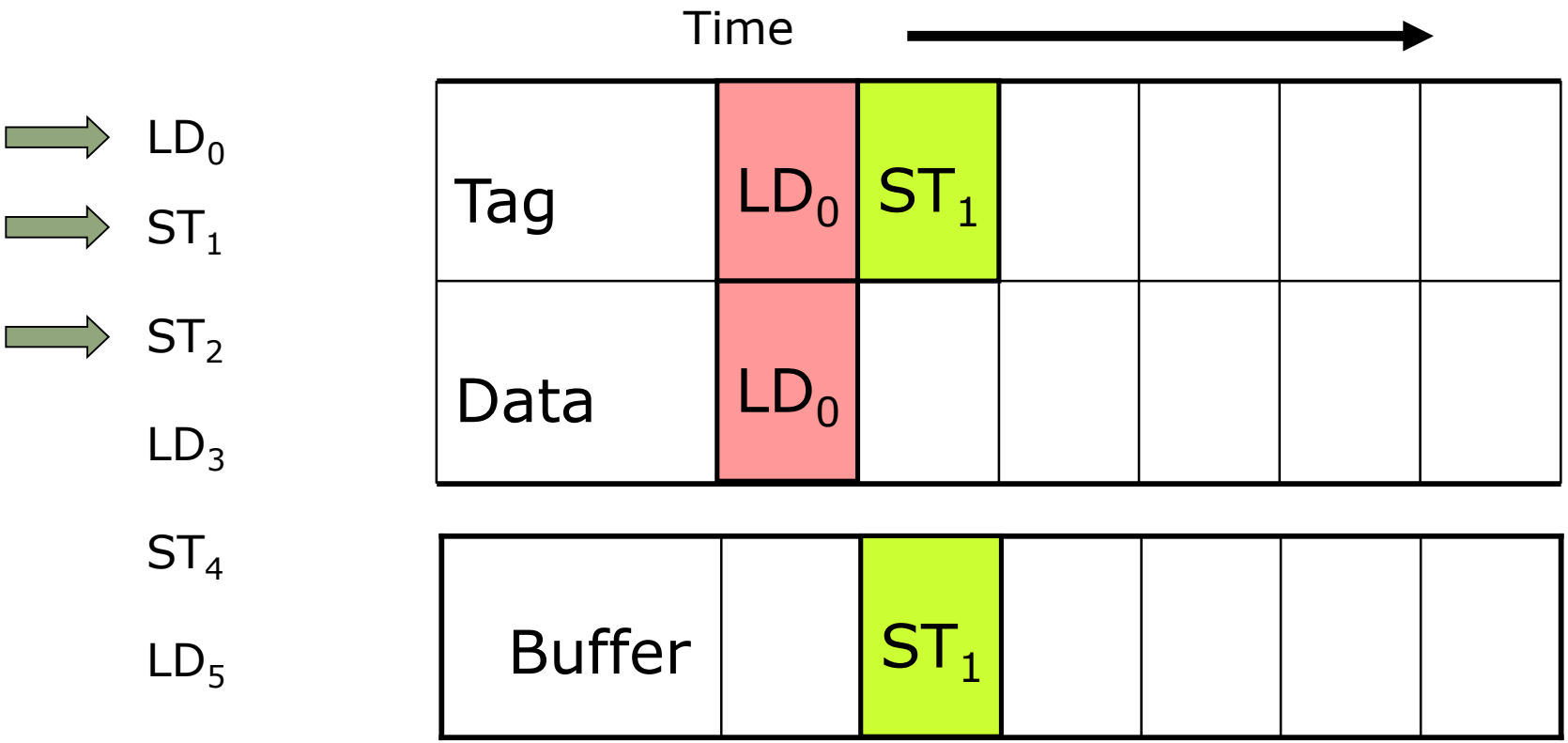

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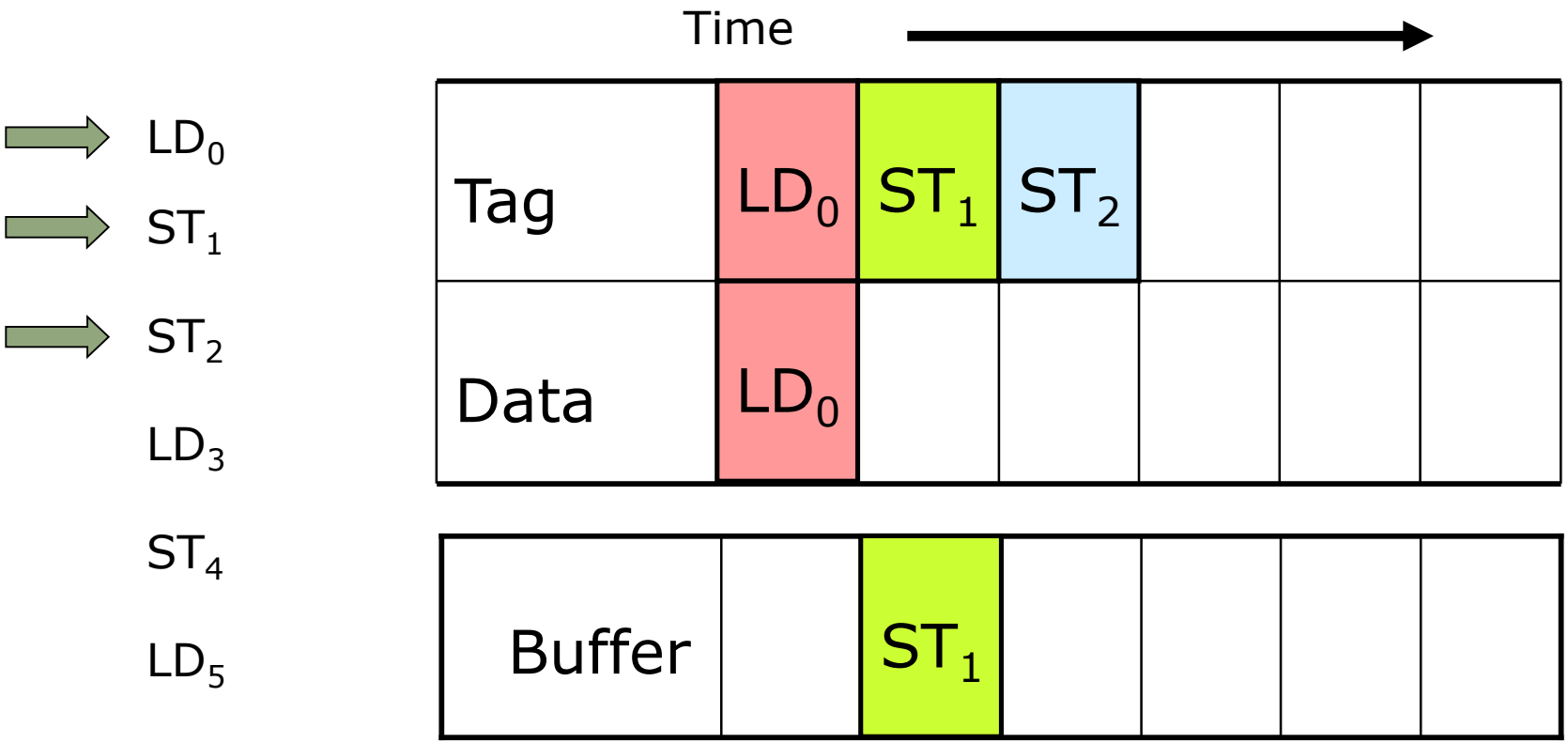

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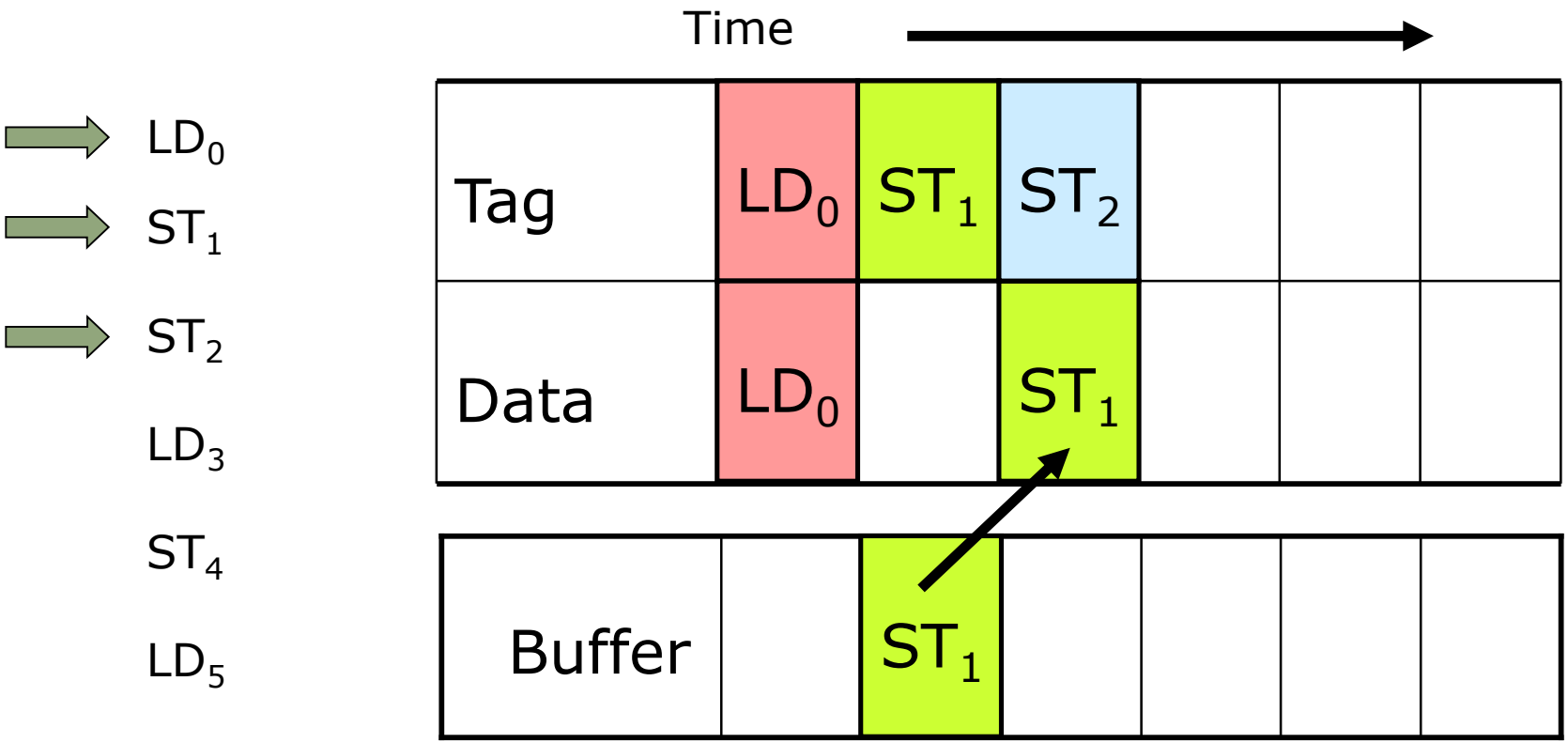

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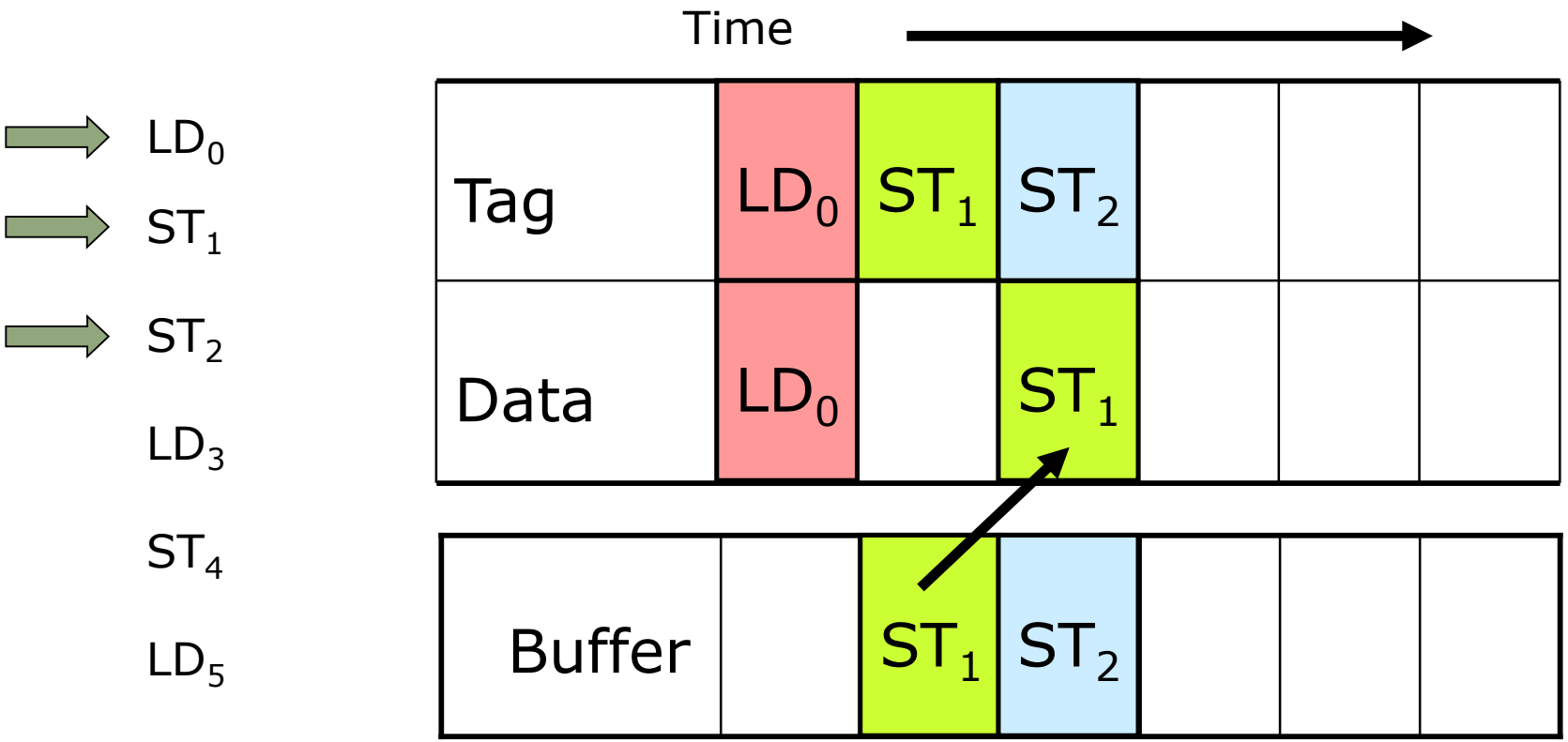

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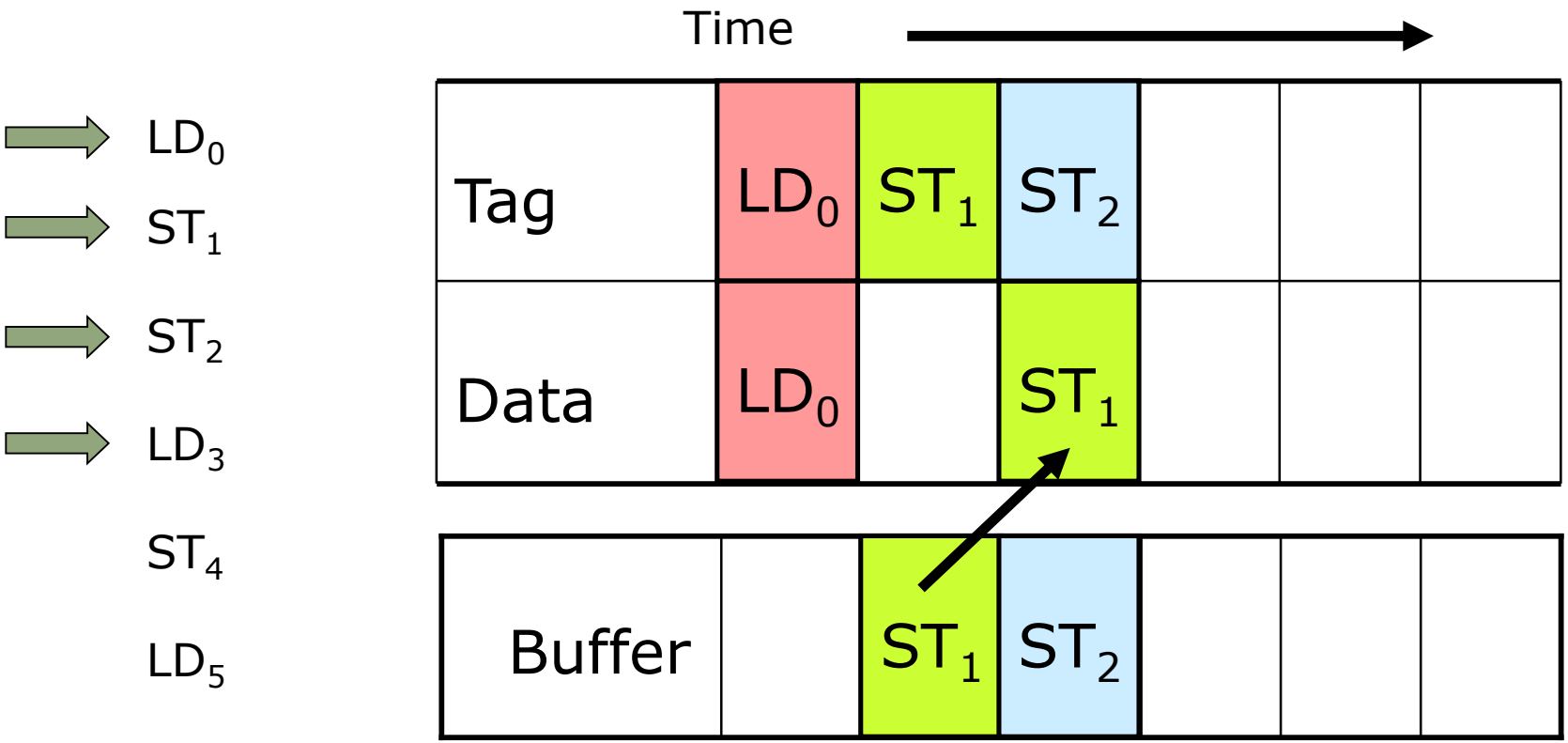

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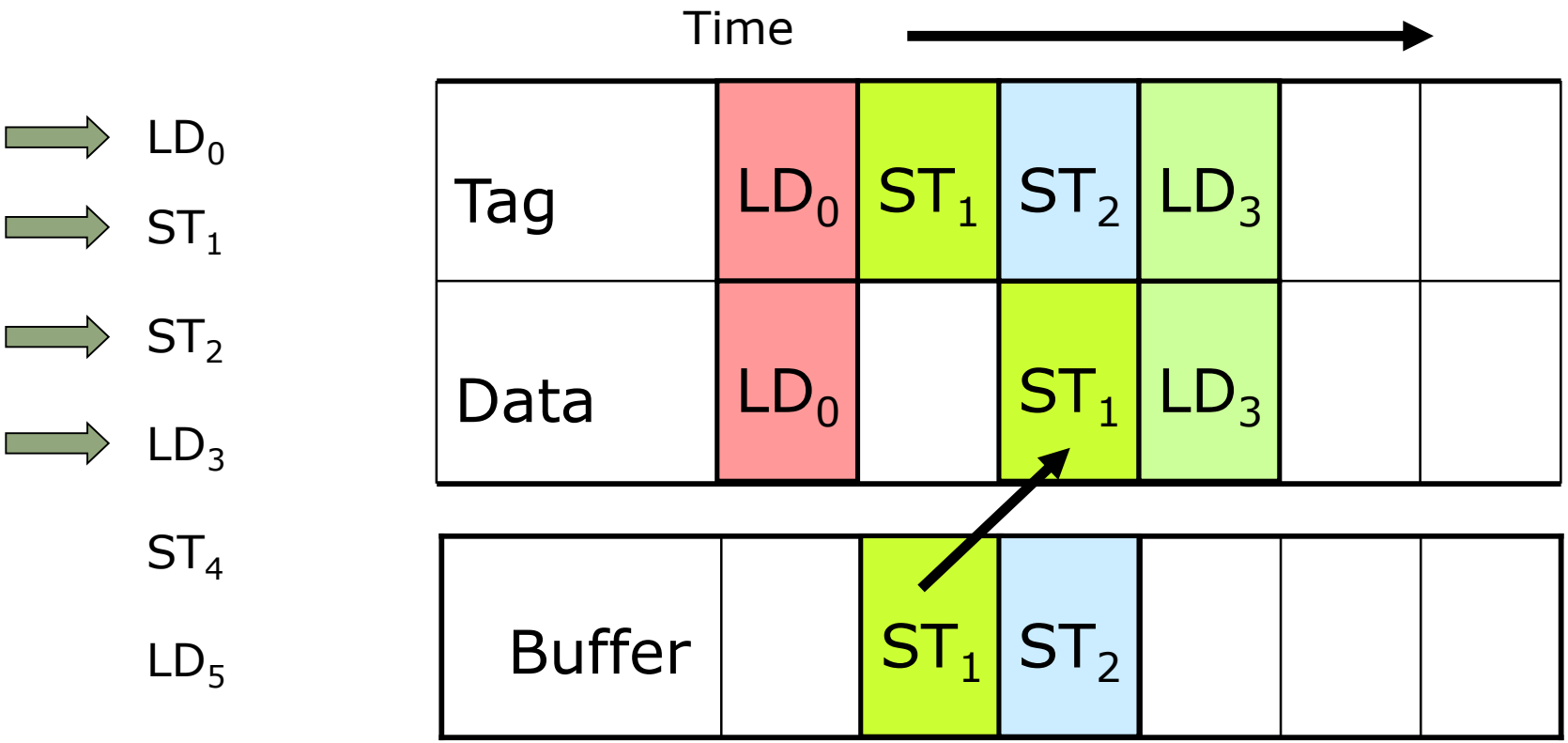

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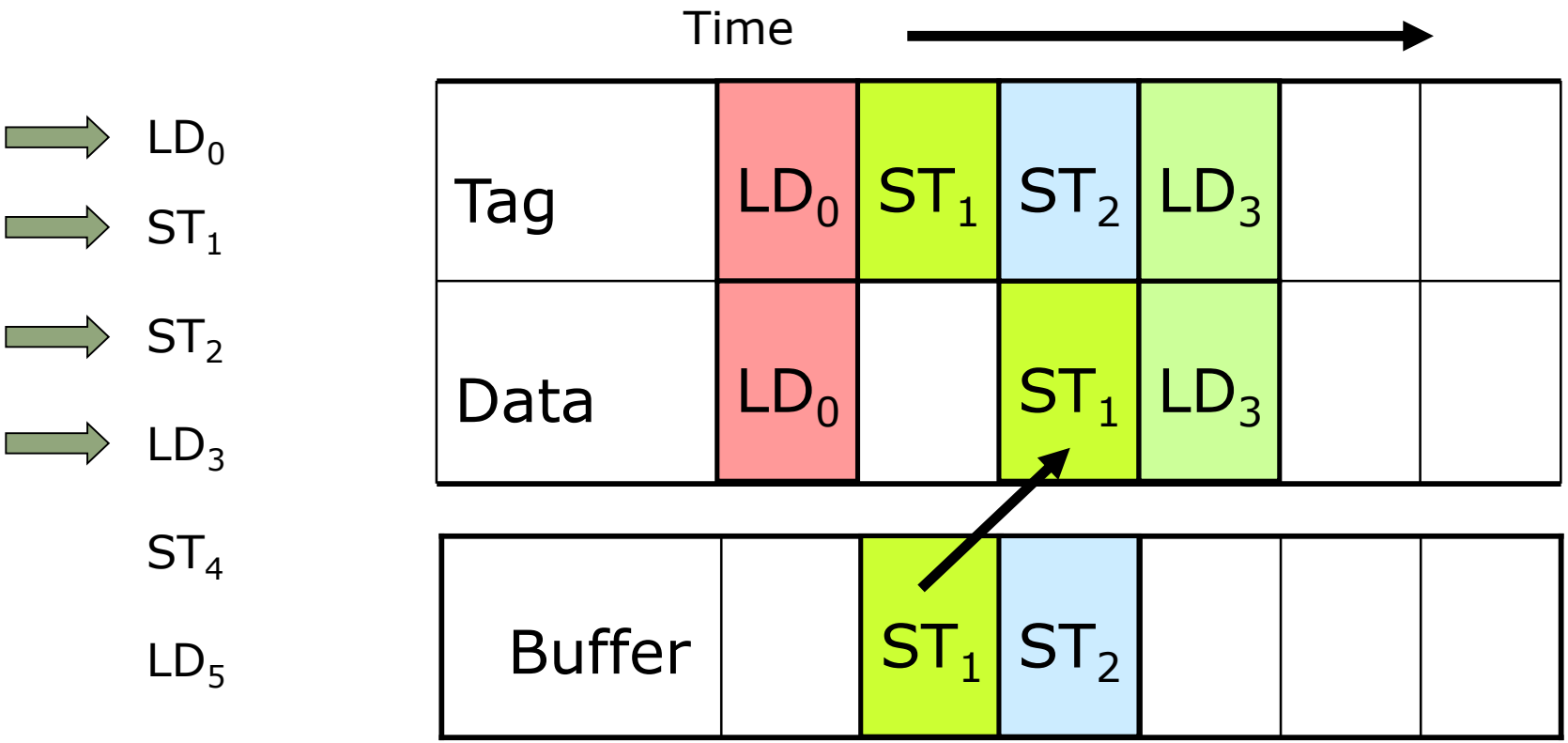

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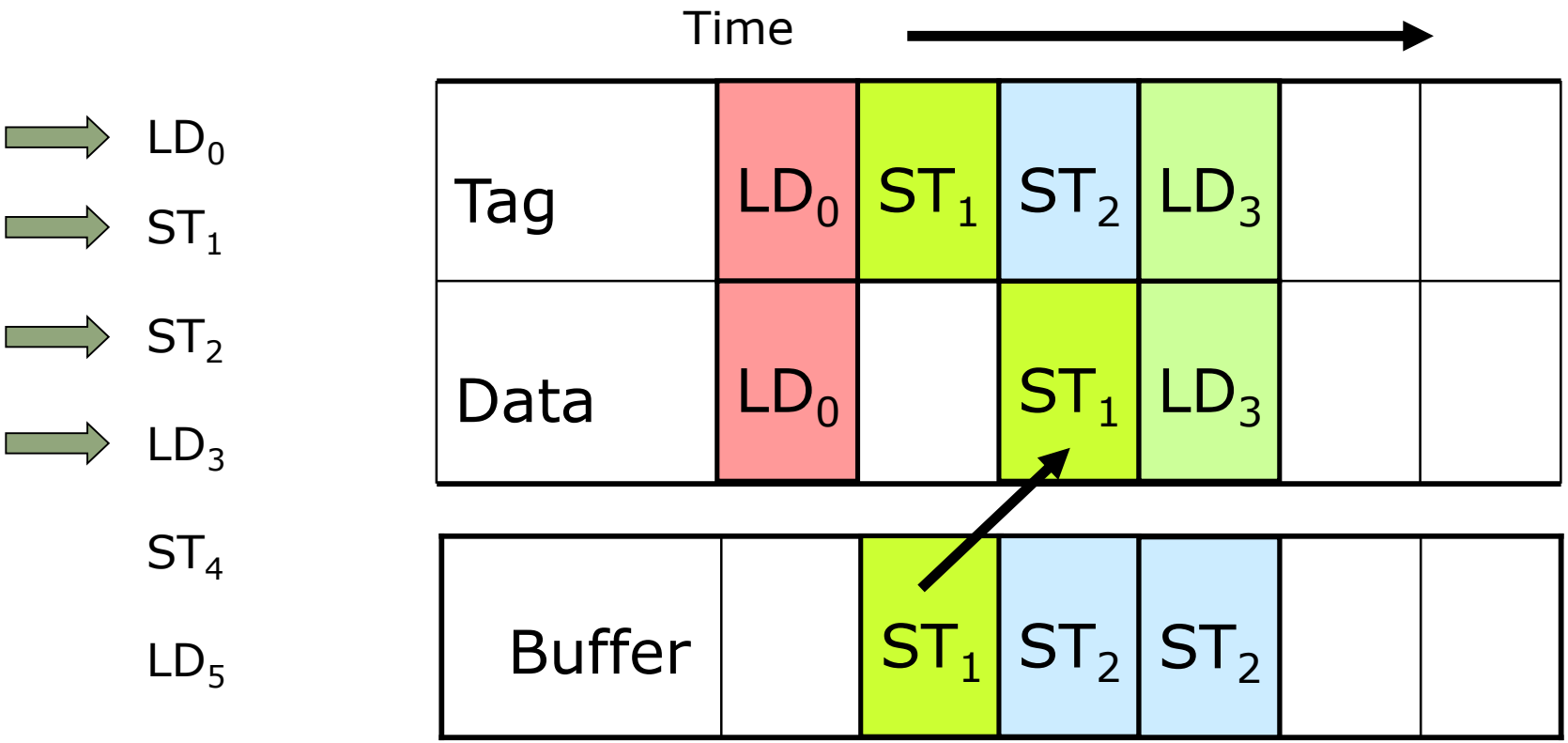

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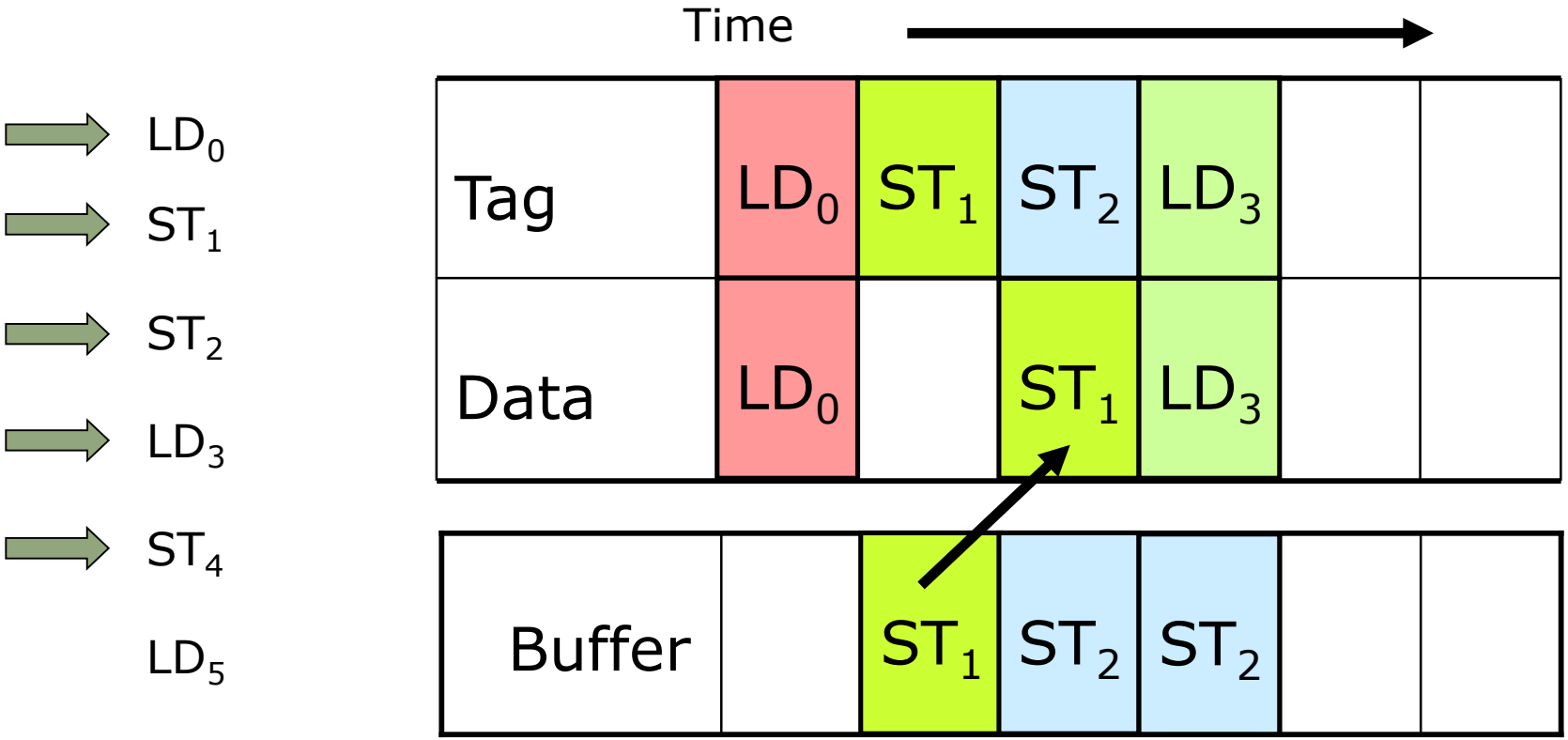

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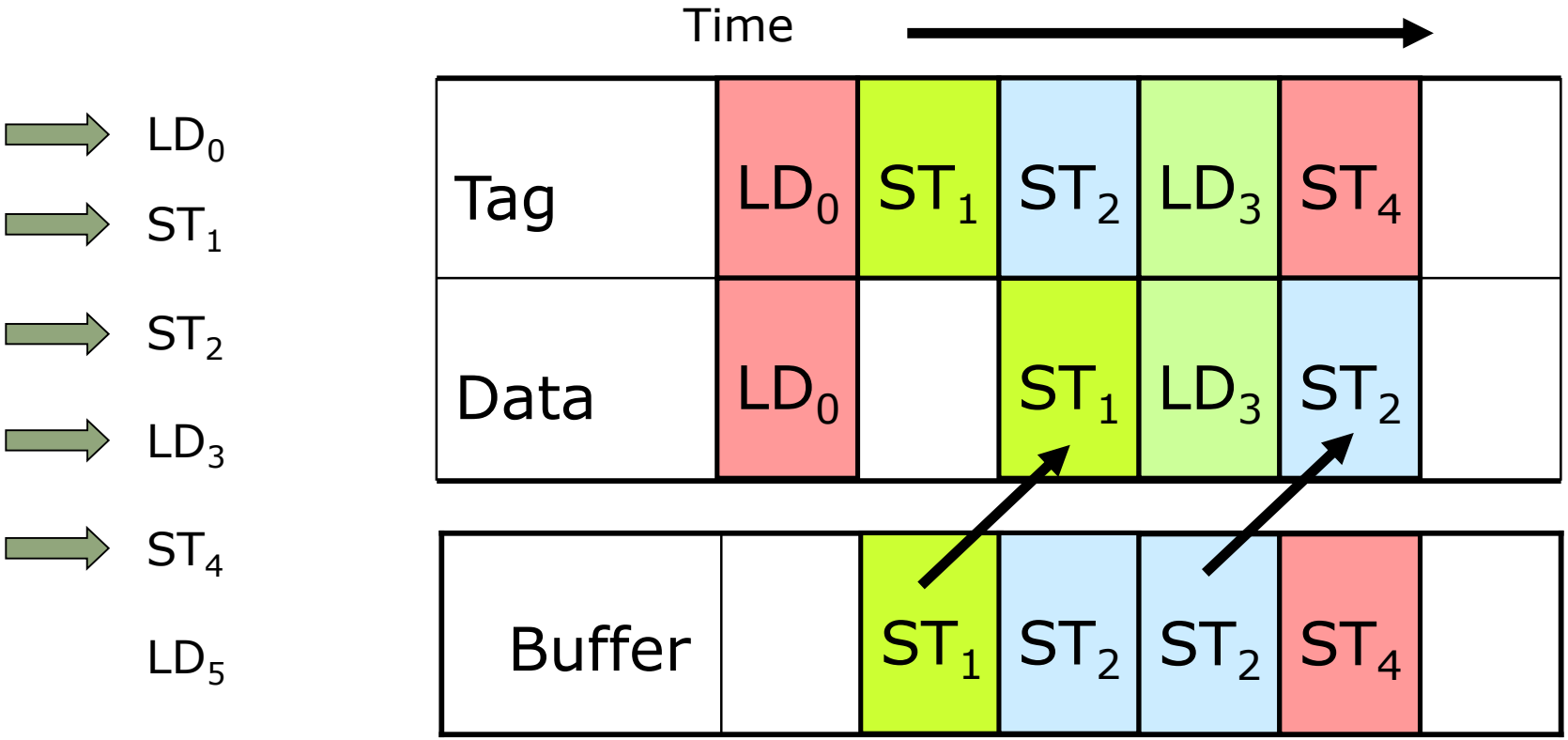

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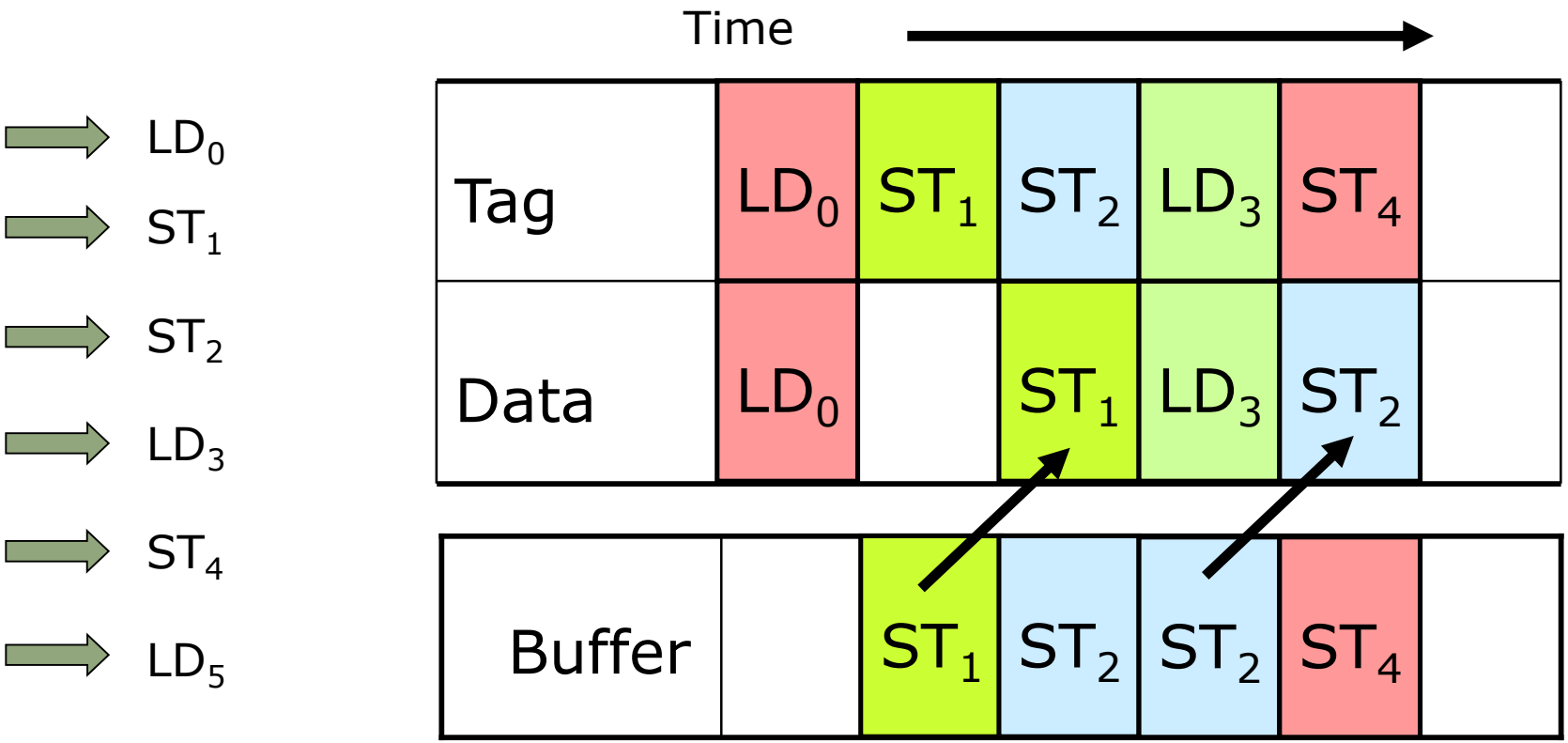

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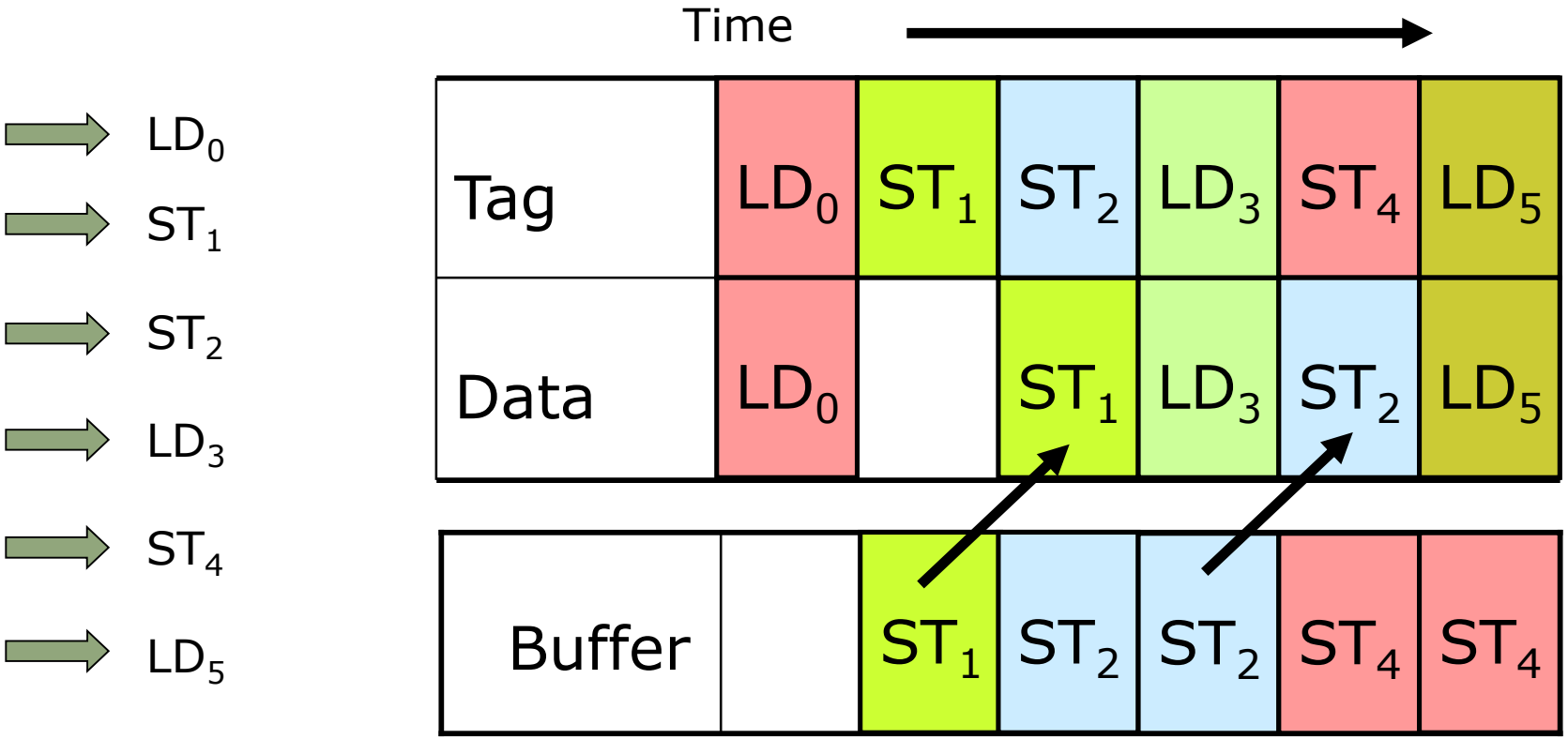

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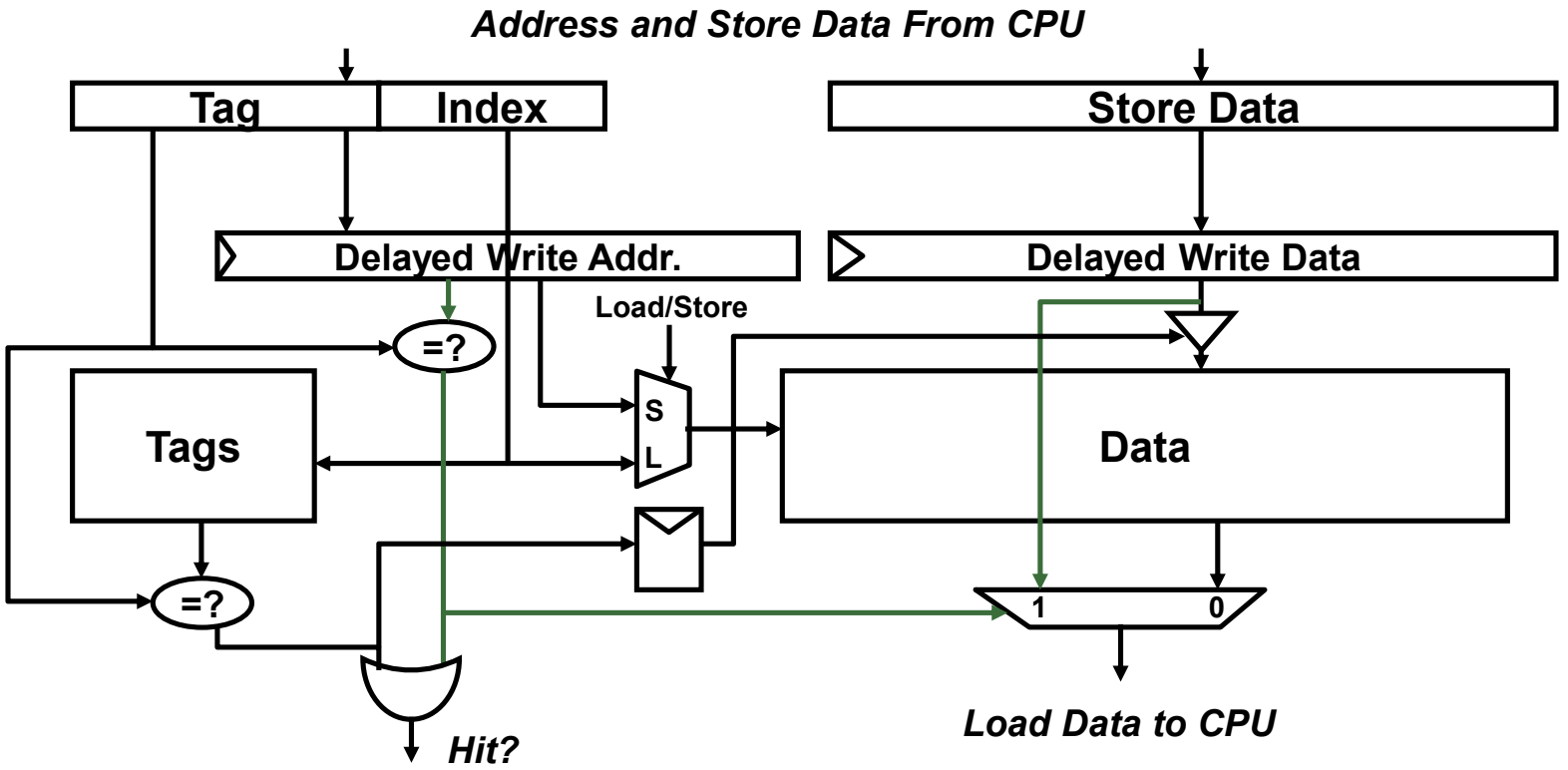

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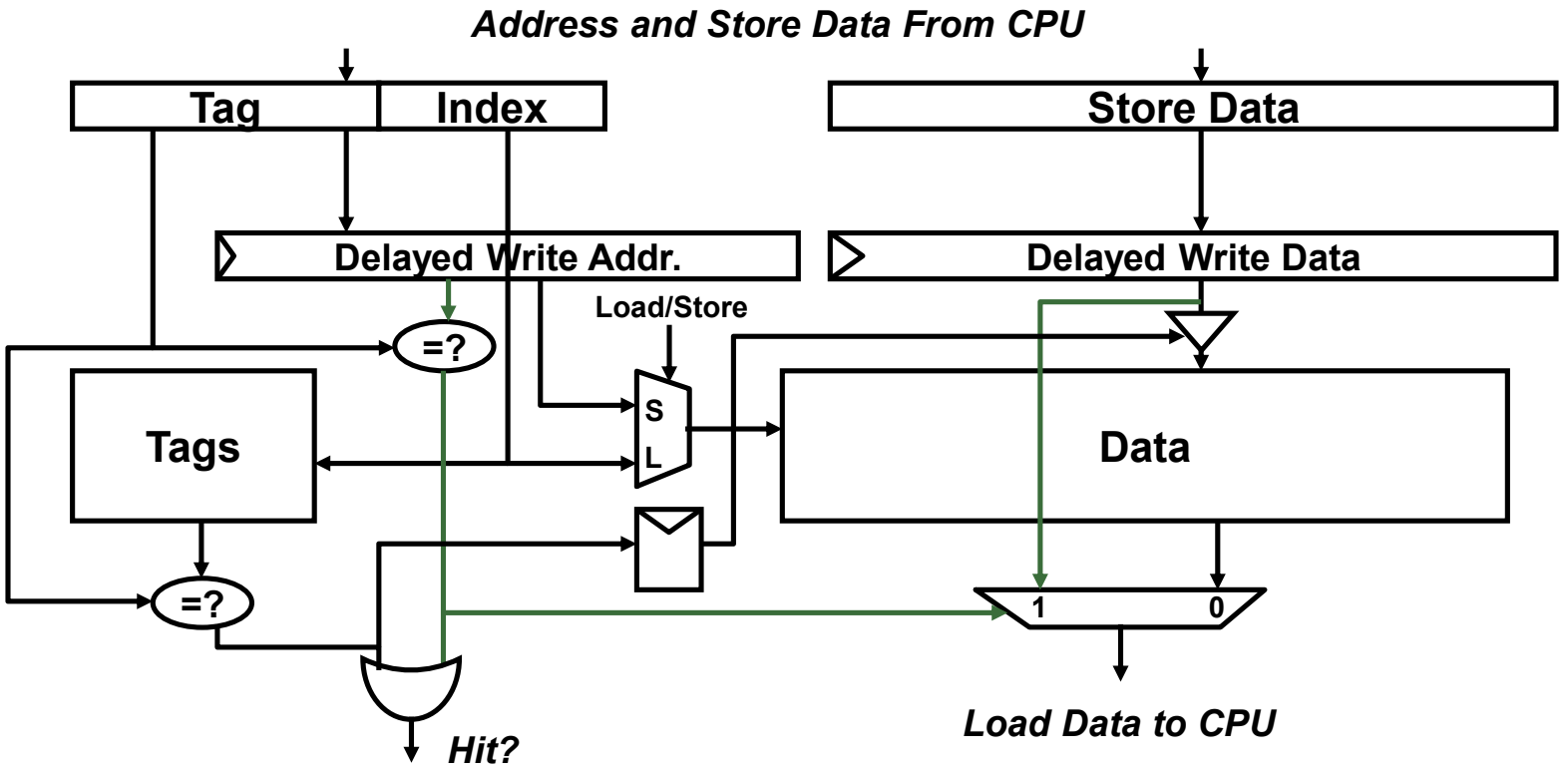
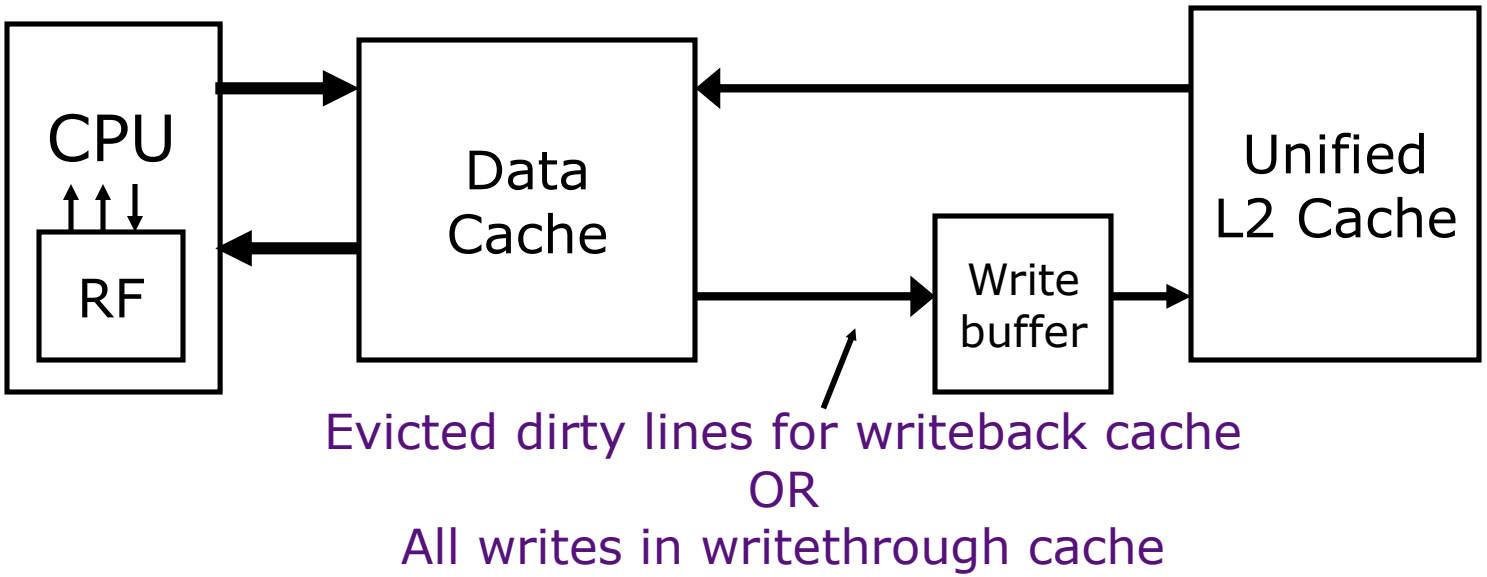


Write Policy Choices

- Cache hit:
  - ***Write-through:*** write both cache & memory
    - generally higher traffic but simplifies multi-processor design
  - ***Write-back:*** write cache only
    (memory is written only when the entry is evicted)
    - a dirty bit per block can further reduce the traffic
- Cache miss:
  - ***No-write-allocate:*** only write to main memory
  - ***Write-allocate*** *(aka fetch on write):* fetch into cache
- Common combinations:
  - write-through and no-write-allocate
  - write-back with write-allocate

Reducing Read Miss Penalty



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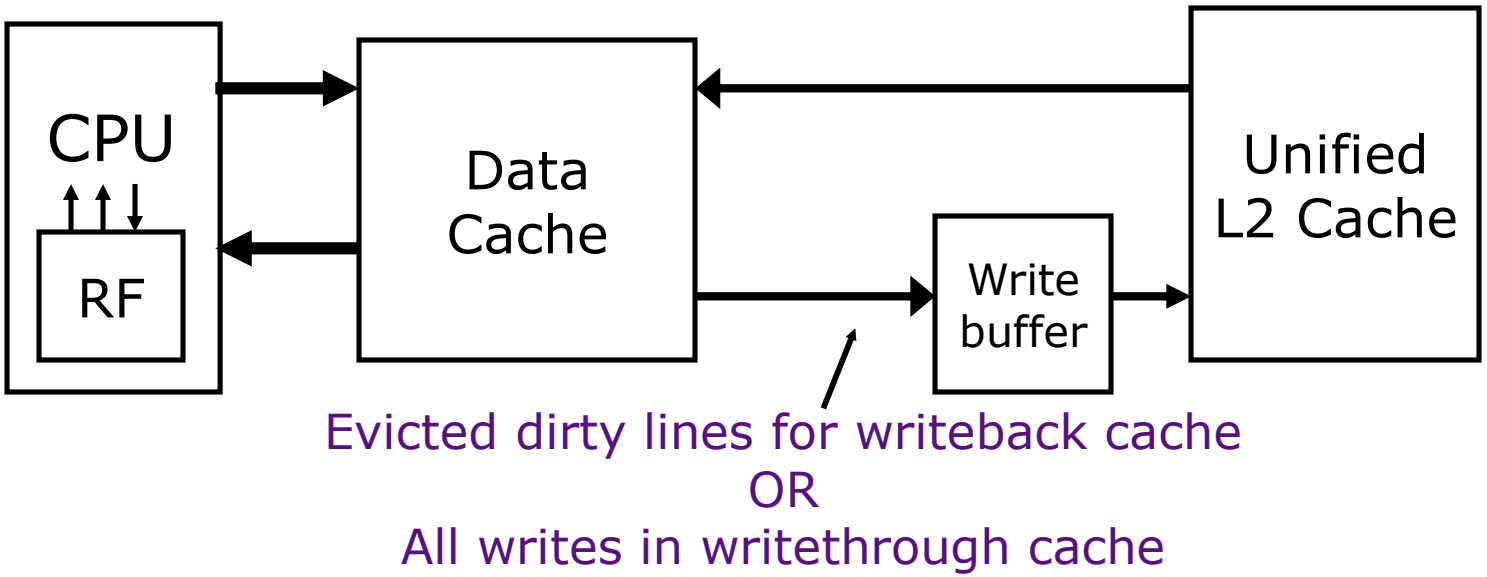

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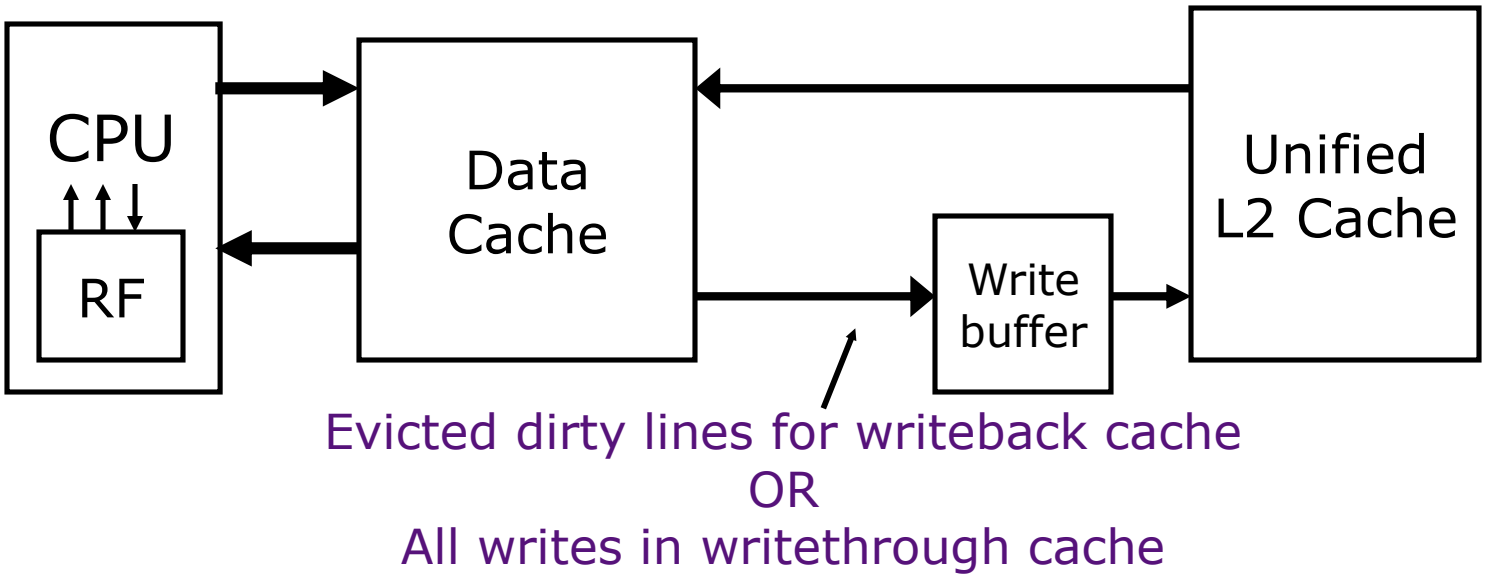

Problem: Write buffer may hold updated value of location needed by a read miss – RAW data hazard

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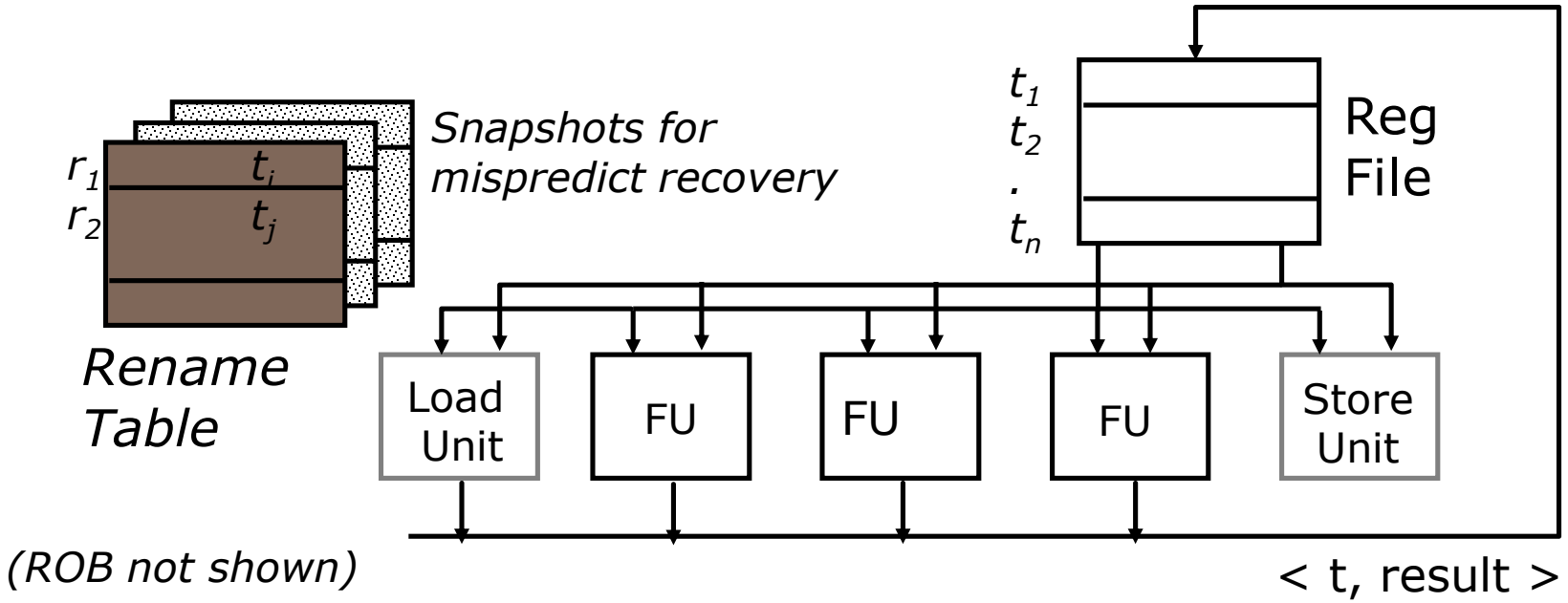
Bypass: Check write buffer addresses against read miss addresses, if no match, allow read miss to go ahead of writes, else, return value in write buffer

O-o-O With Physical Register File

(MIPS R10K, Alpha 21264, Pentium 4)



We've handled the register dependencies, but what about memory operations?

Speculative Loads / Stores

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- Choice: Data update policy: greedy or lazy?

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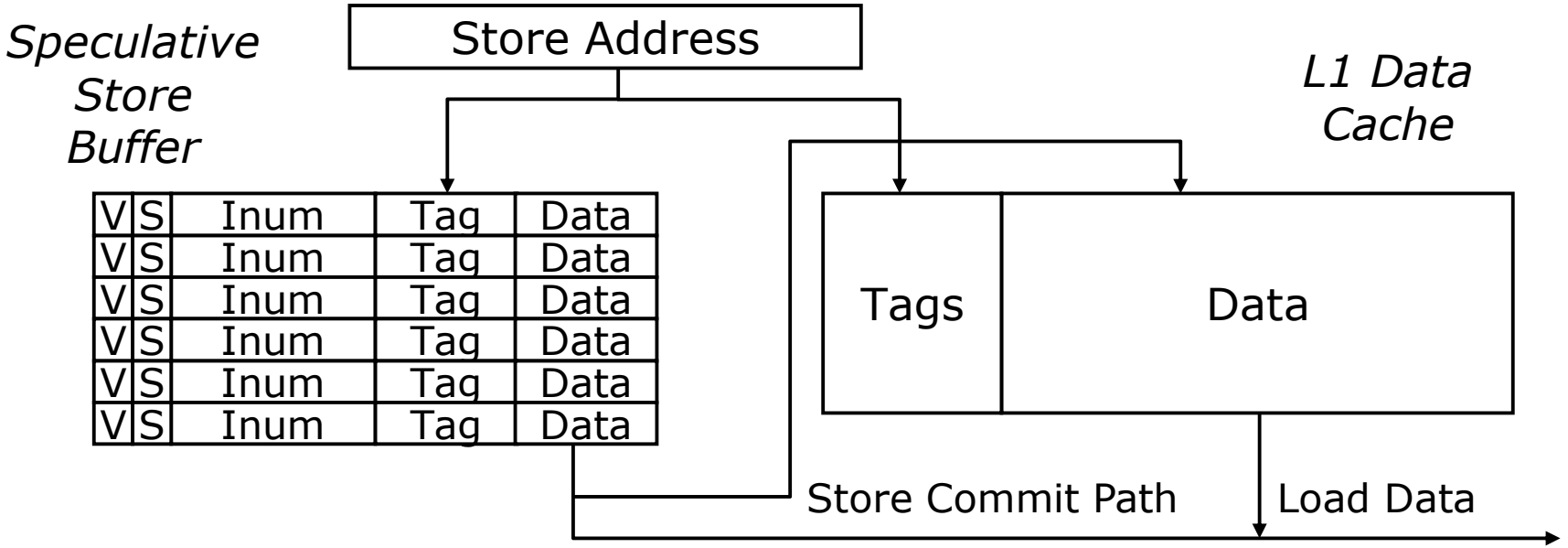
WAW Hazards

Store Buffer – Lazy data management



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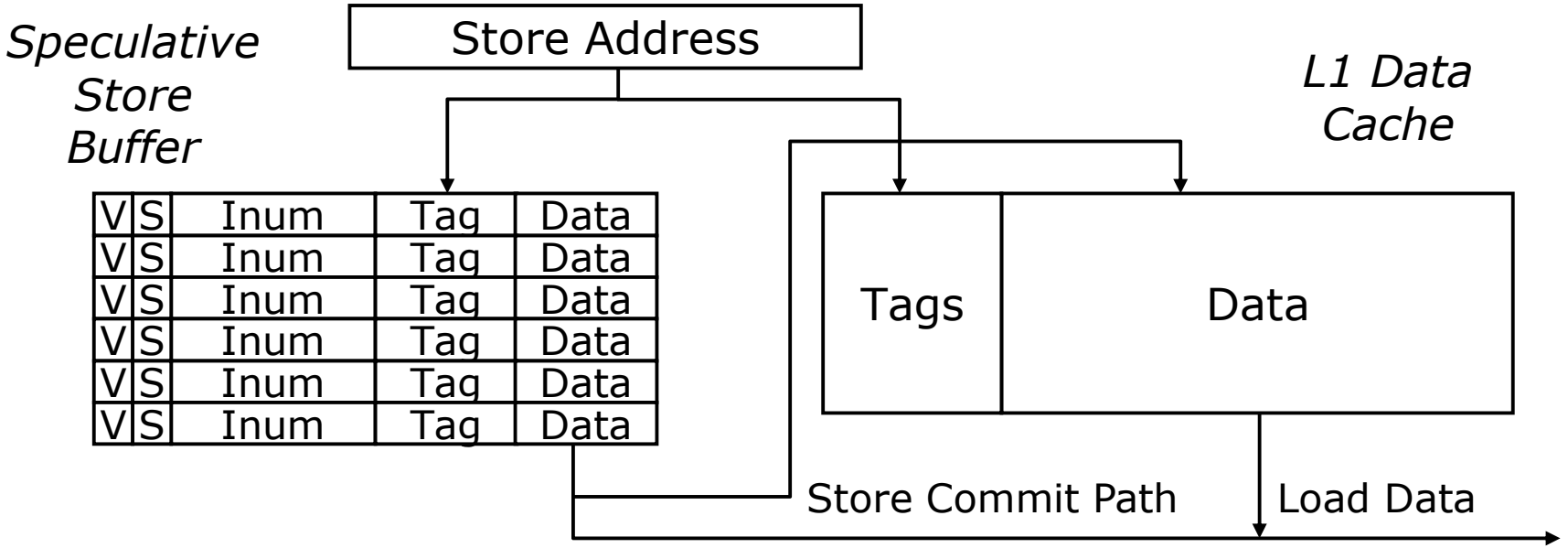

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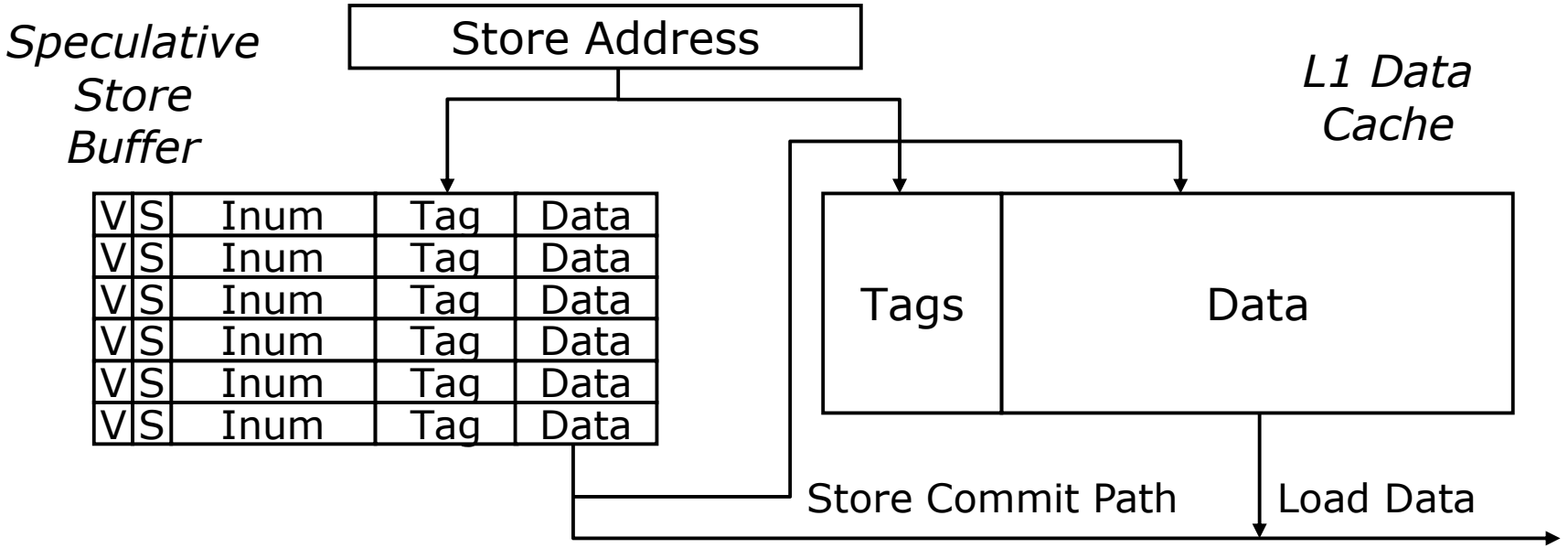

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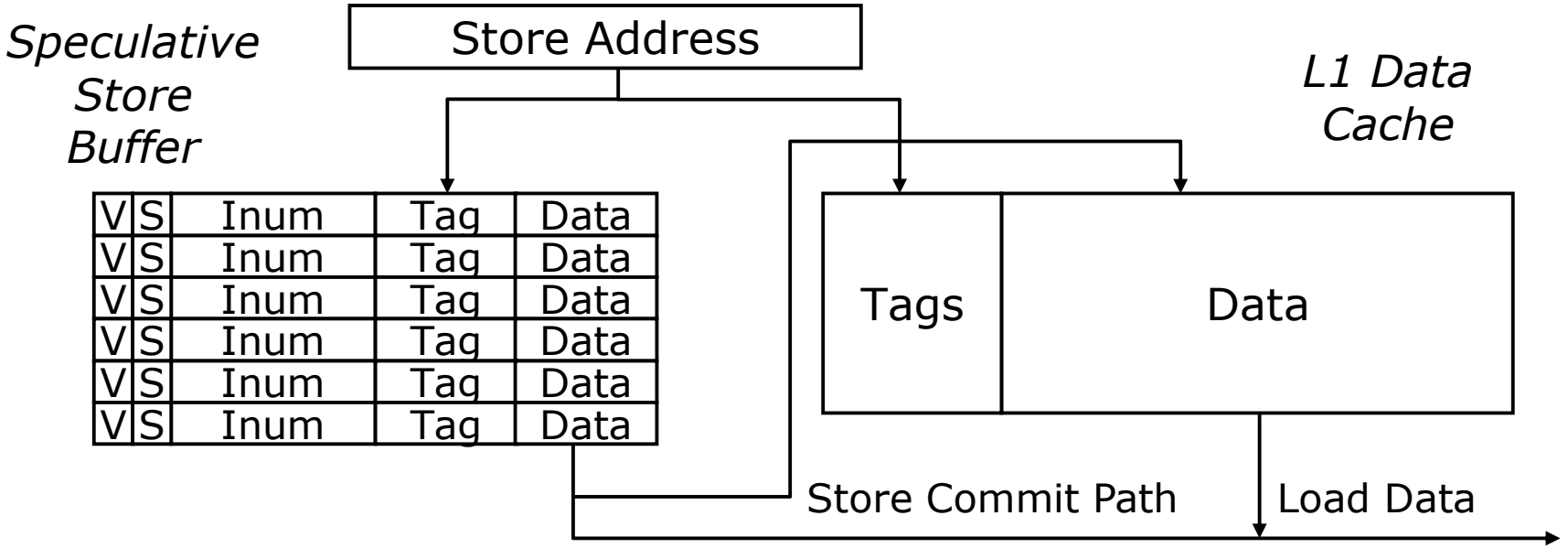

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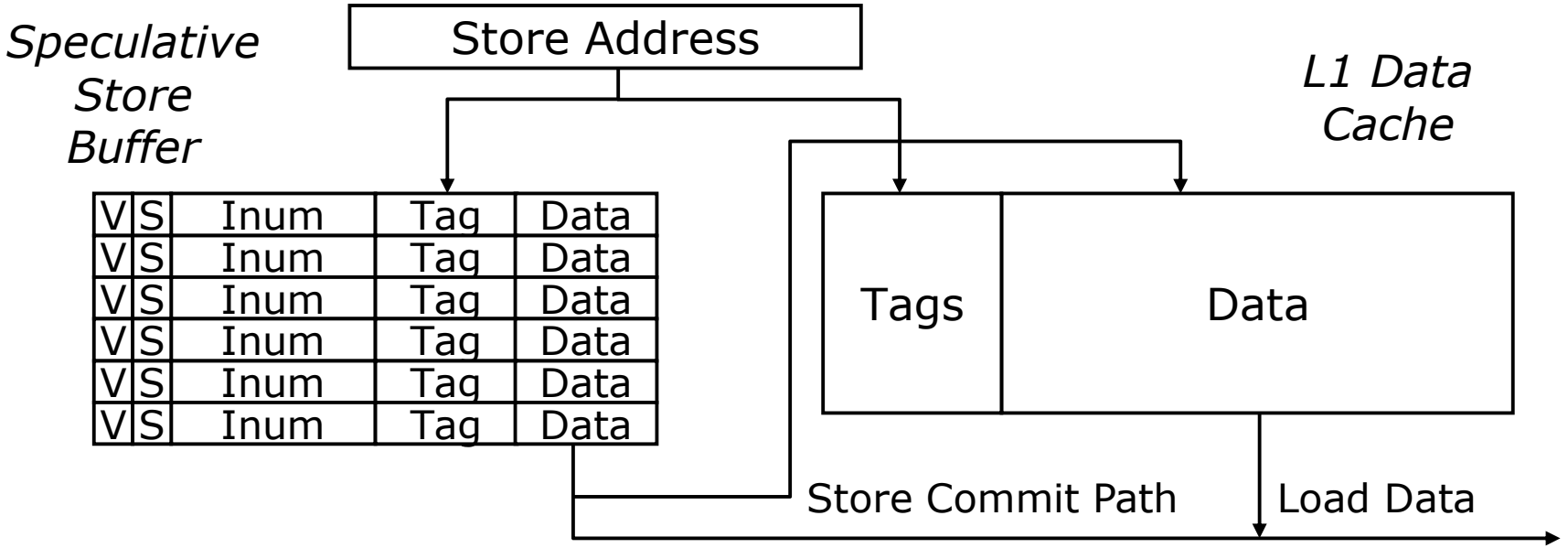

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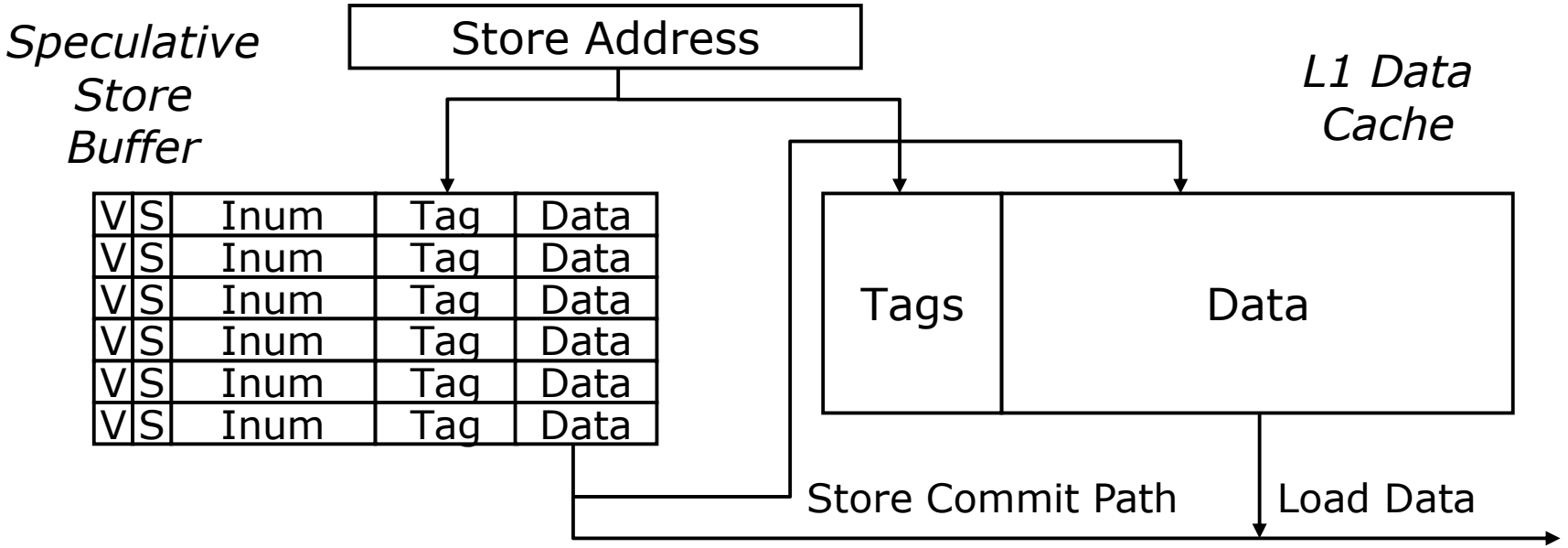

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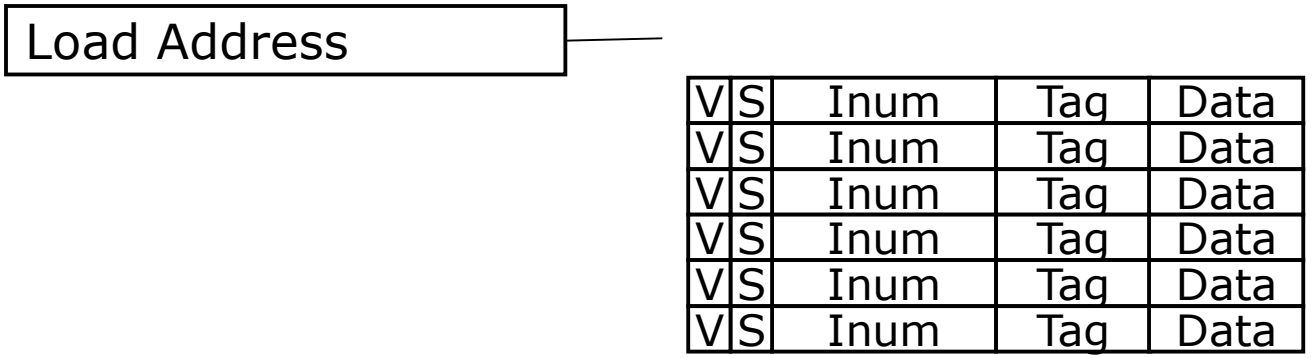

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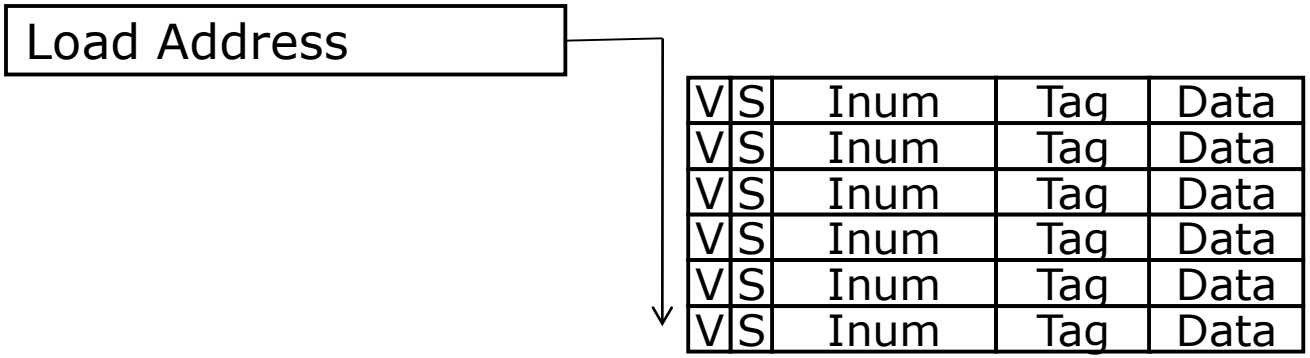

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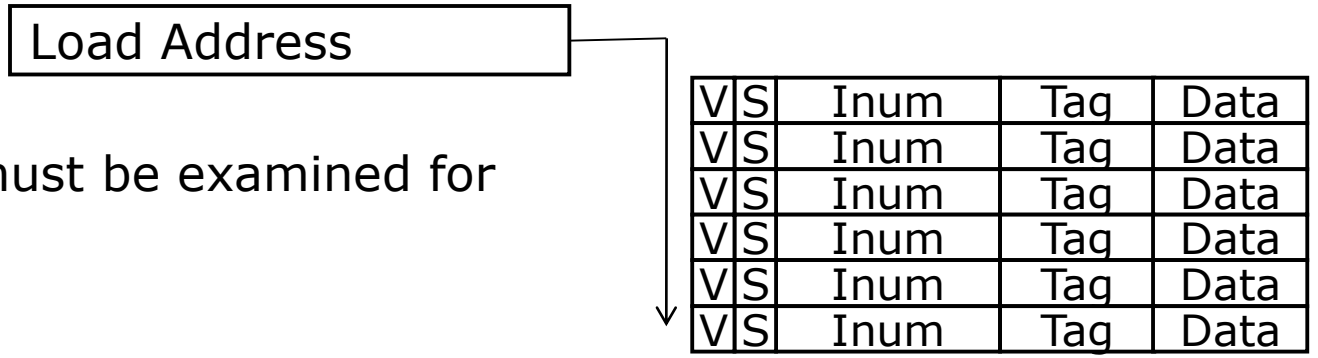

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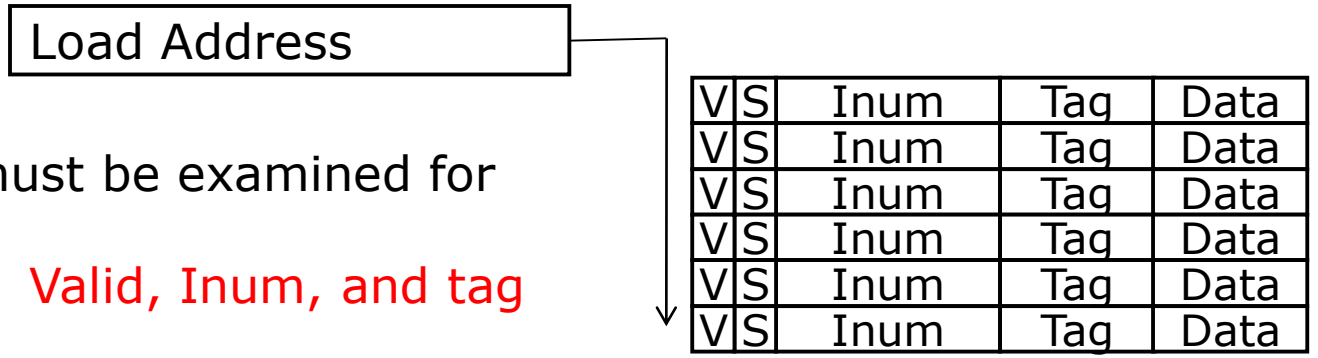

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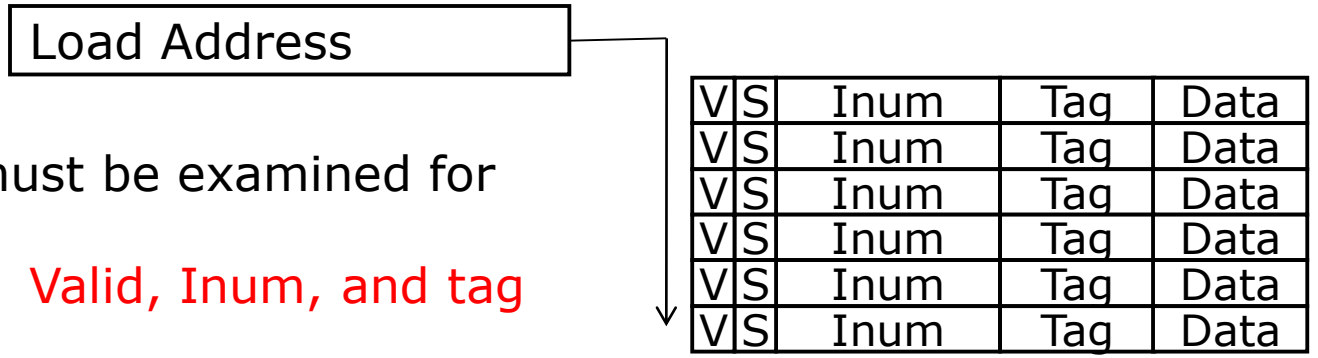

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- If data in both store buffer and cache, which should we use:

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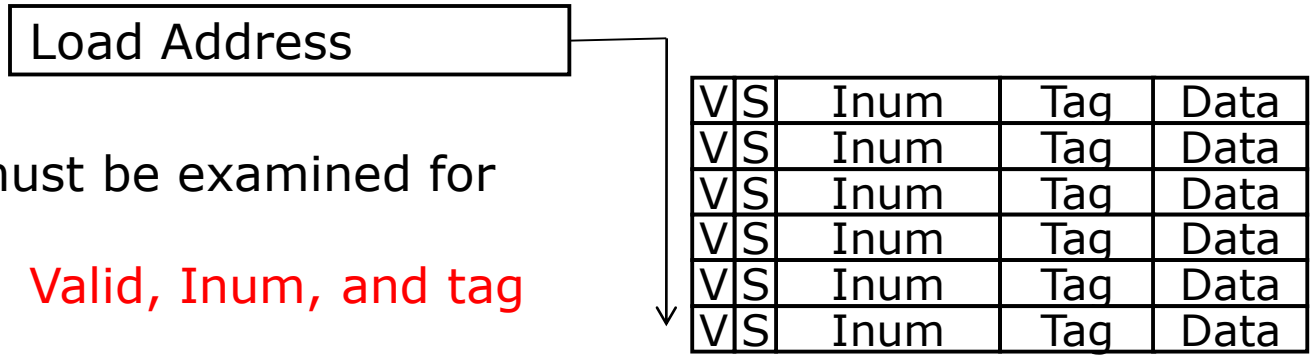

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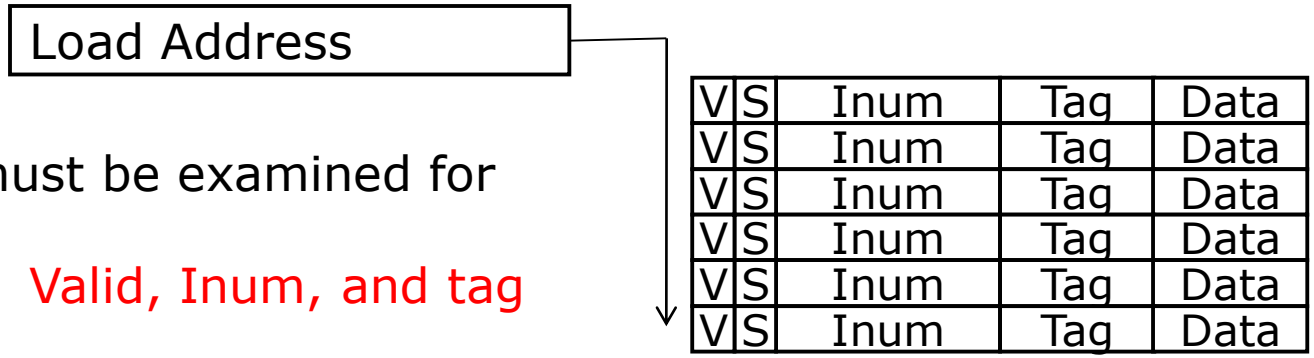

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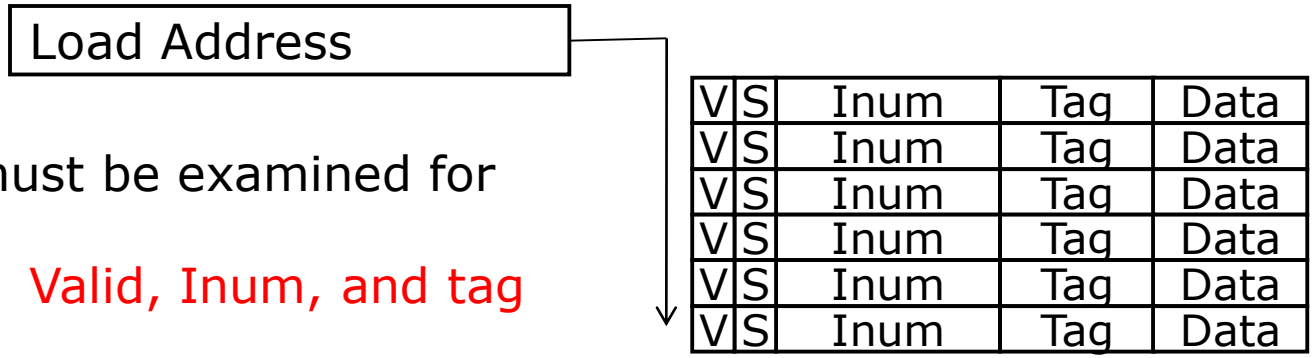

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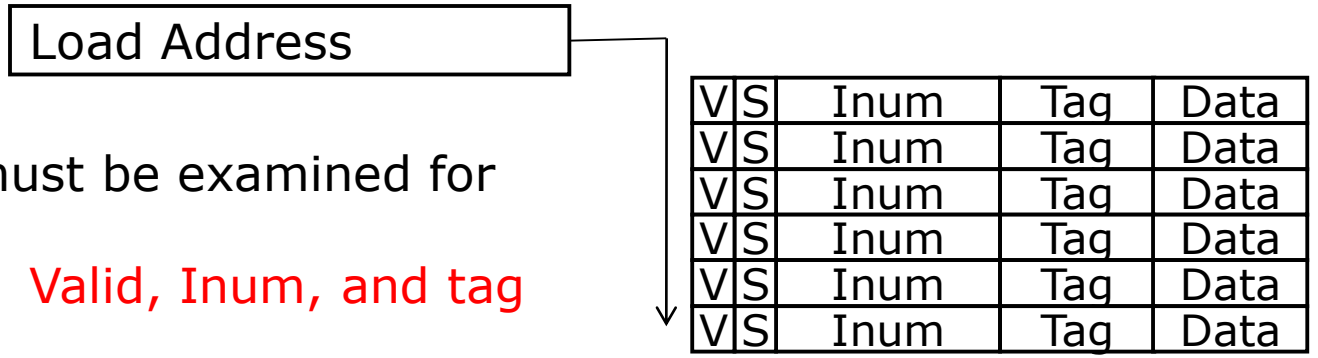

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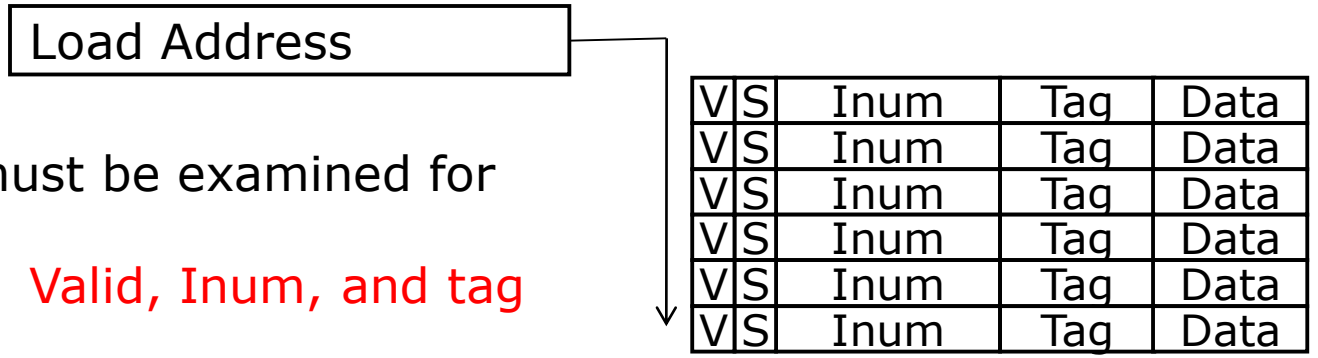

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  Declare a mis-speculation and abort.

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For registers, we used tags or physical register numbers to determine dependencies. What about memory operations?

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In-Order Memory Queue

st r1, (r2)
ld r3, (r4)

Stall naively:

- Execute all loads and stores in program order

=> Load and store cannot start execution until all previous loads and stores have completed execution

- Can still execute loads and stores speculatively, and out-of-order with respect to other instructions

Conservative O-o-O Load Execution

st r1, (r2)
ld r3, (r4)

Stall intelligently:

- Split execution of store instruction into two phases:
  address calculation and data write
- Can execute load before store, if addresses known and r4 != r2
- Each load address compared with addresses of all previous uncommitted stores *(can use partial conservative check, e.g., bottom 12 bits of address)*
- Don't execute load if any previous store address not known

(MIPS R10K, 16 entry address queue)

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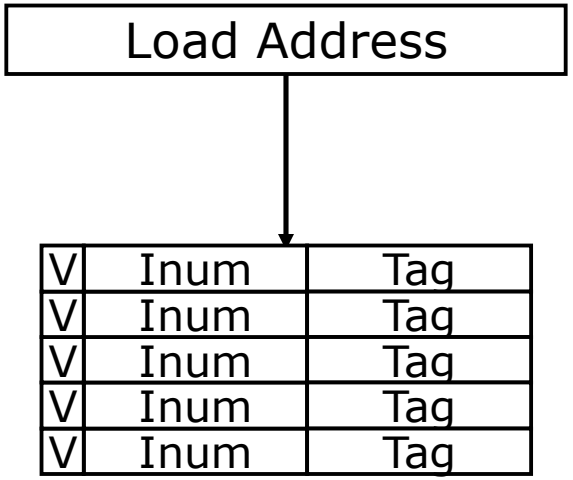
Watch for stores that arrive after load that needed its data

Speculative Load Buffer

Speculation check: Detect if a load has executed before an earlier store to the same address – missed RAW hazard

Speculative Load Buffer



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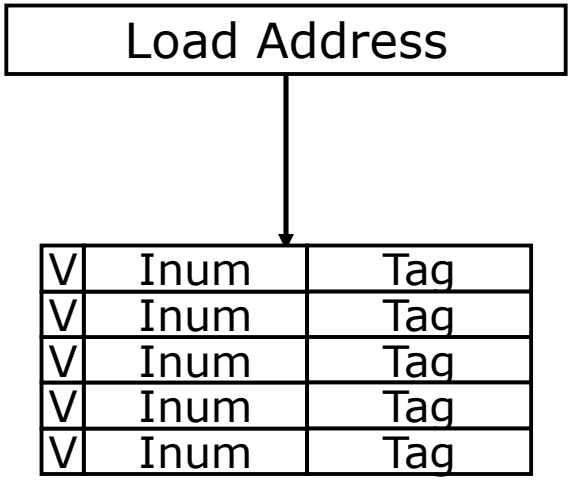

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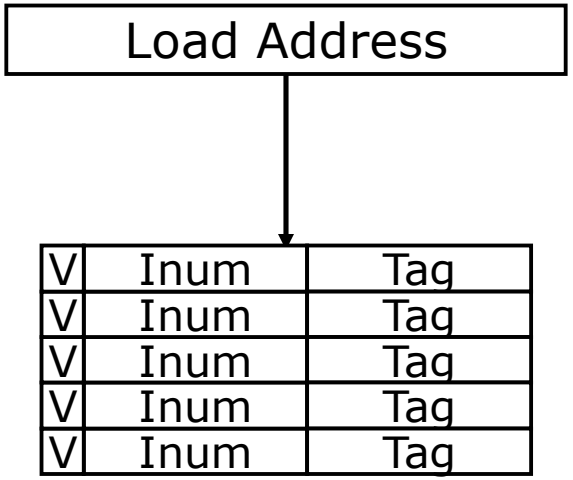

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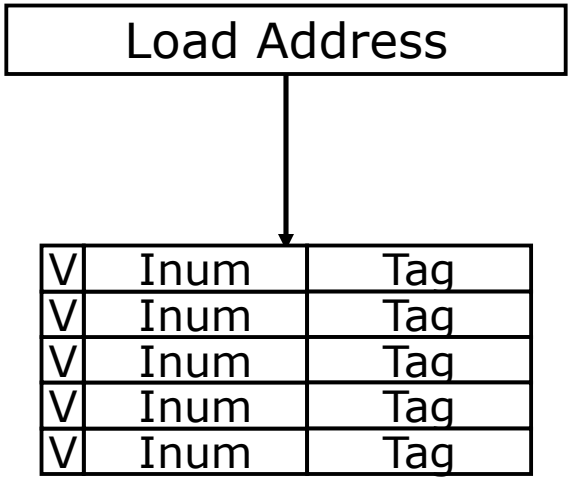

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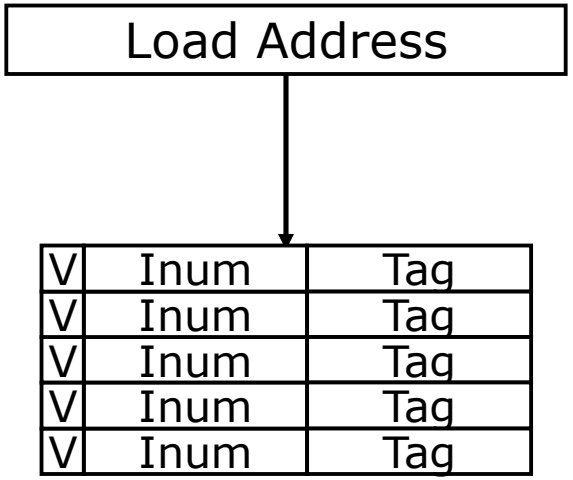

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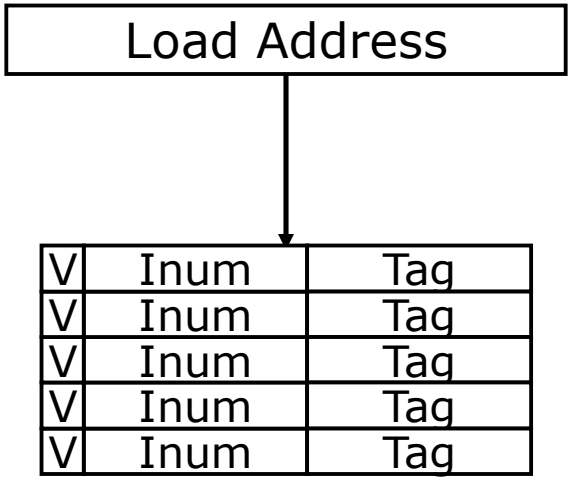

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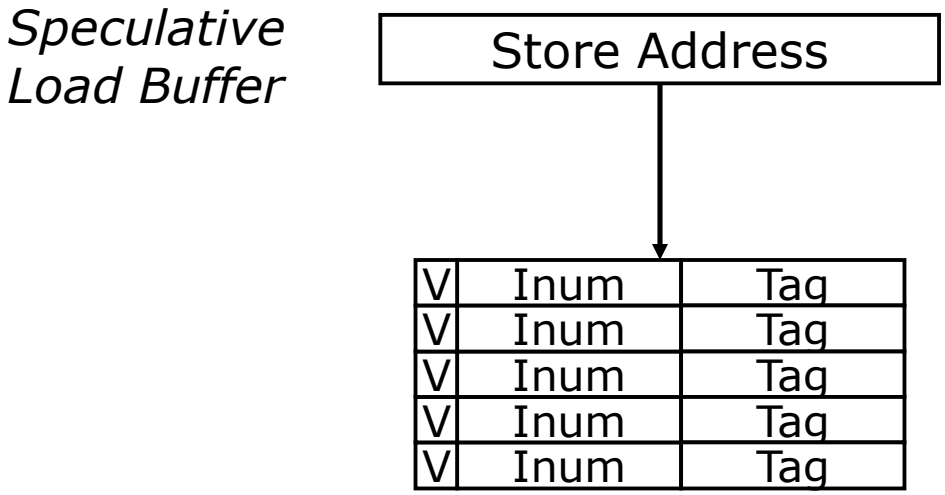

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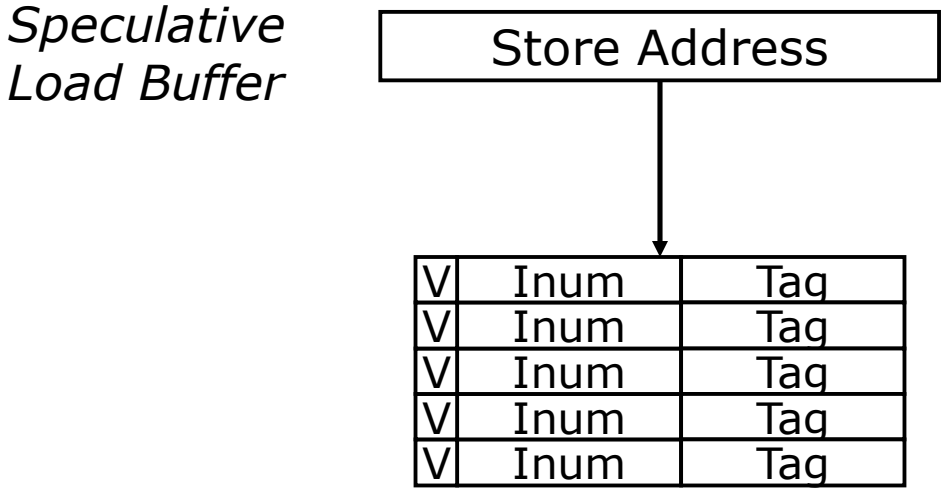

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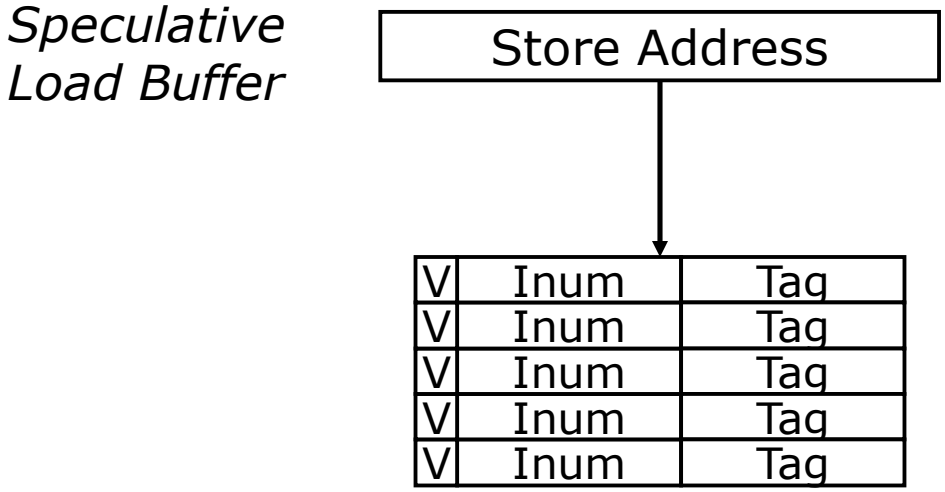

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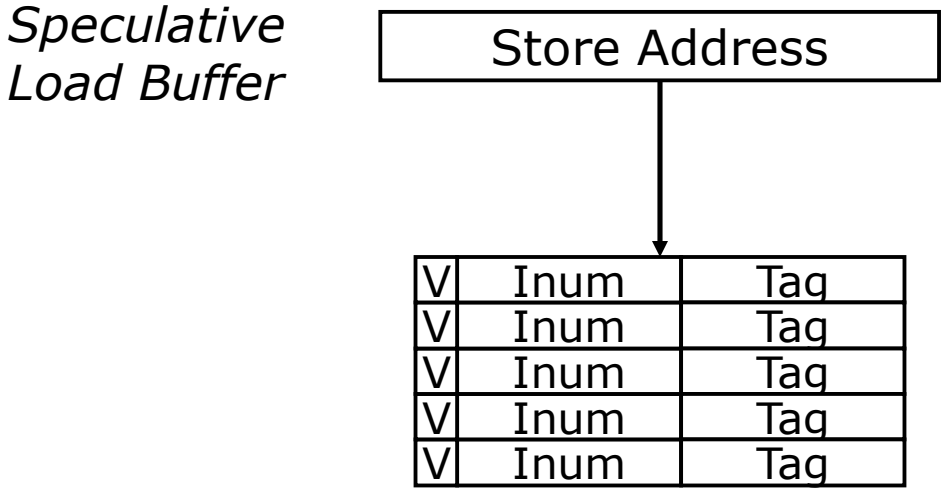

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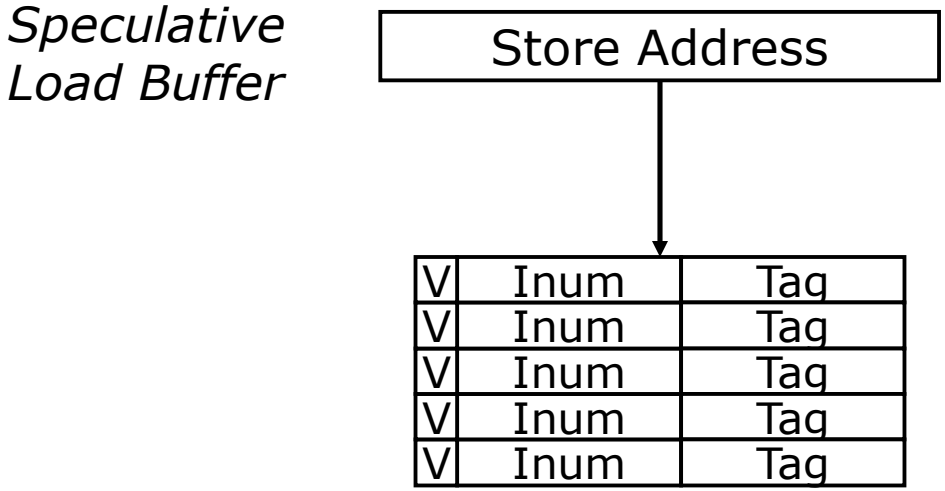

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Notice the general problem of predictors that learn something but can't unlearn it

Store Sets
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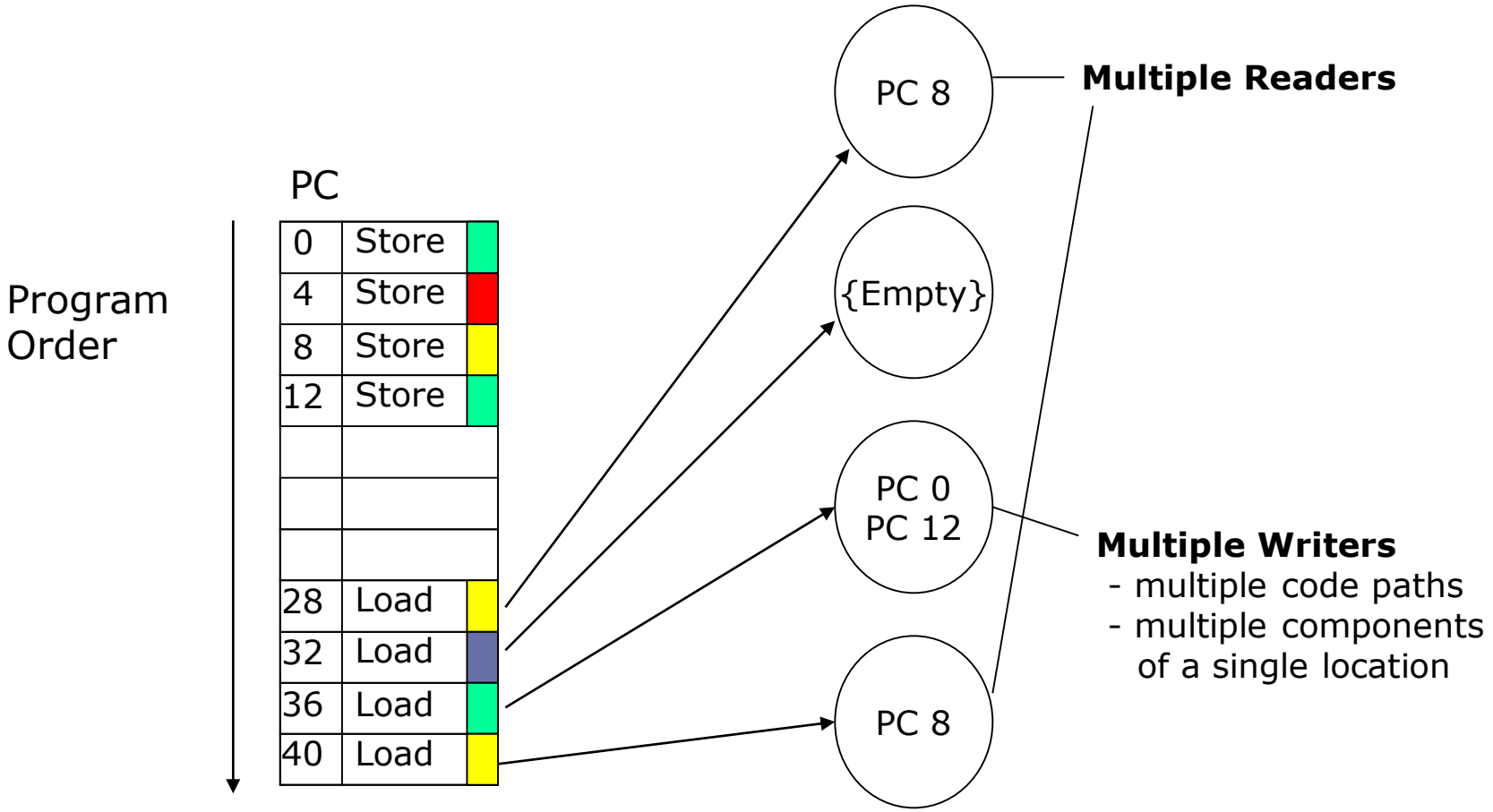
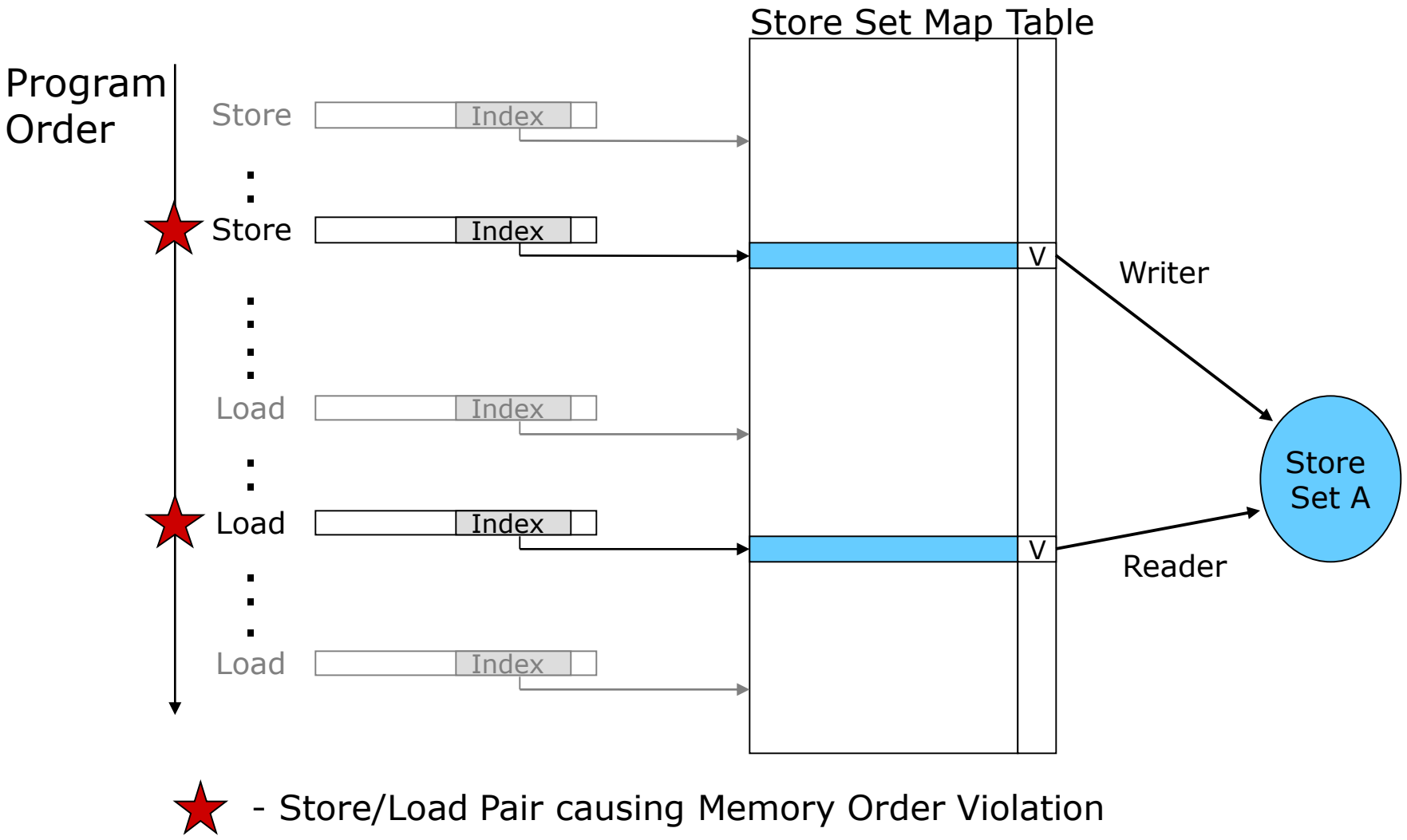


Memory Dependence Prediction using Store Sets

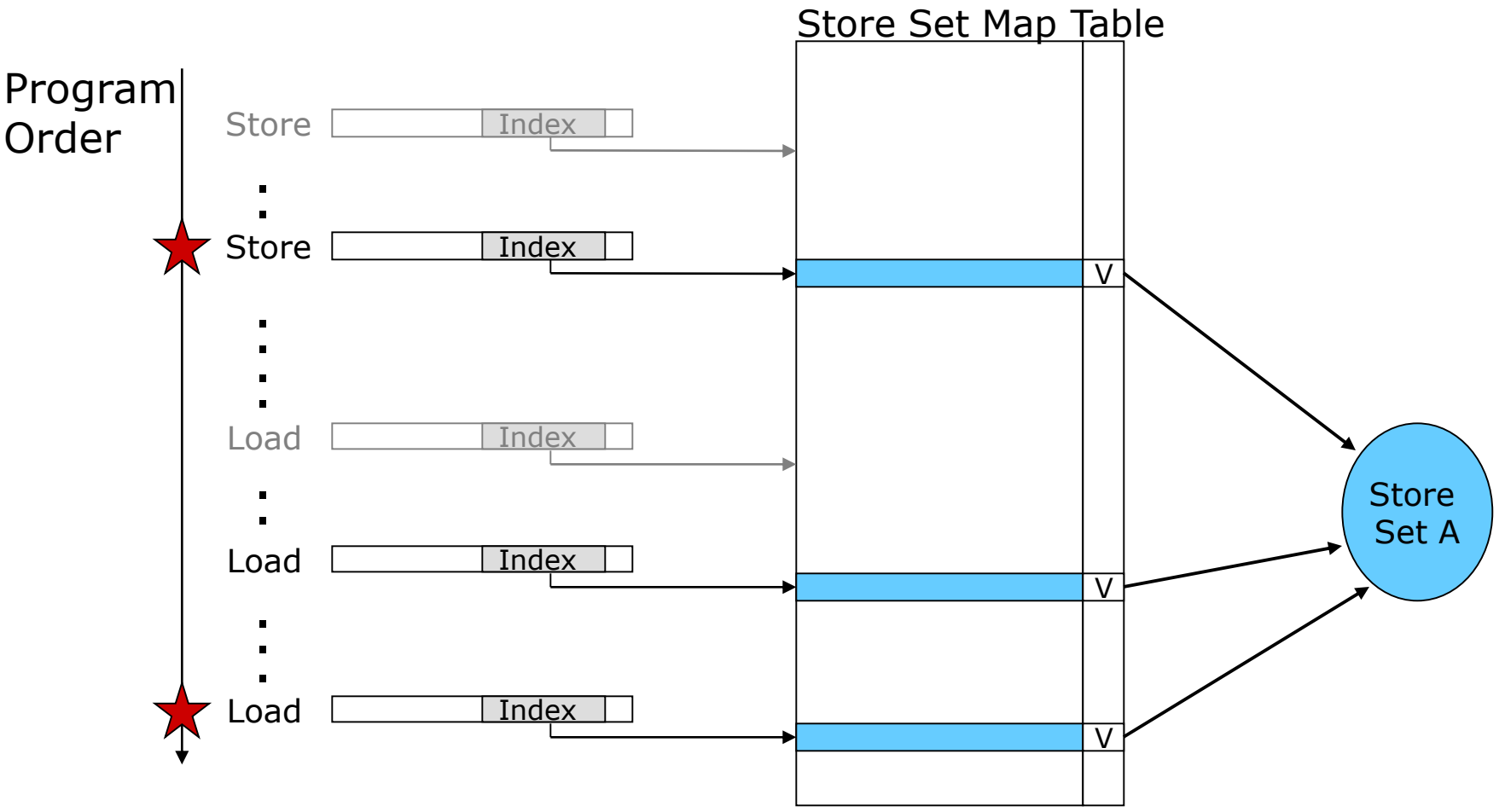
- A load must wait for any stores in its *store set* that have not yet executed

- The processor approximates each load's *store set* by initially allowing naïve speculation and recording memory-order violations

The Store Set Map Table



Store Set Sharing for Multiple Readers



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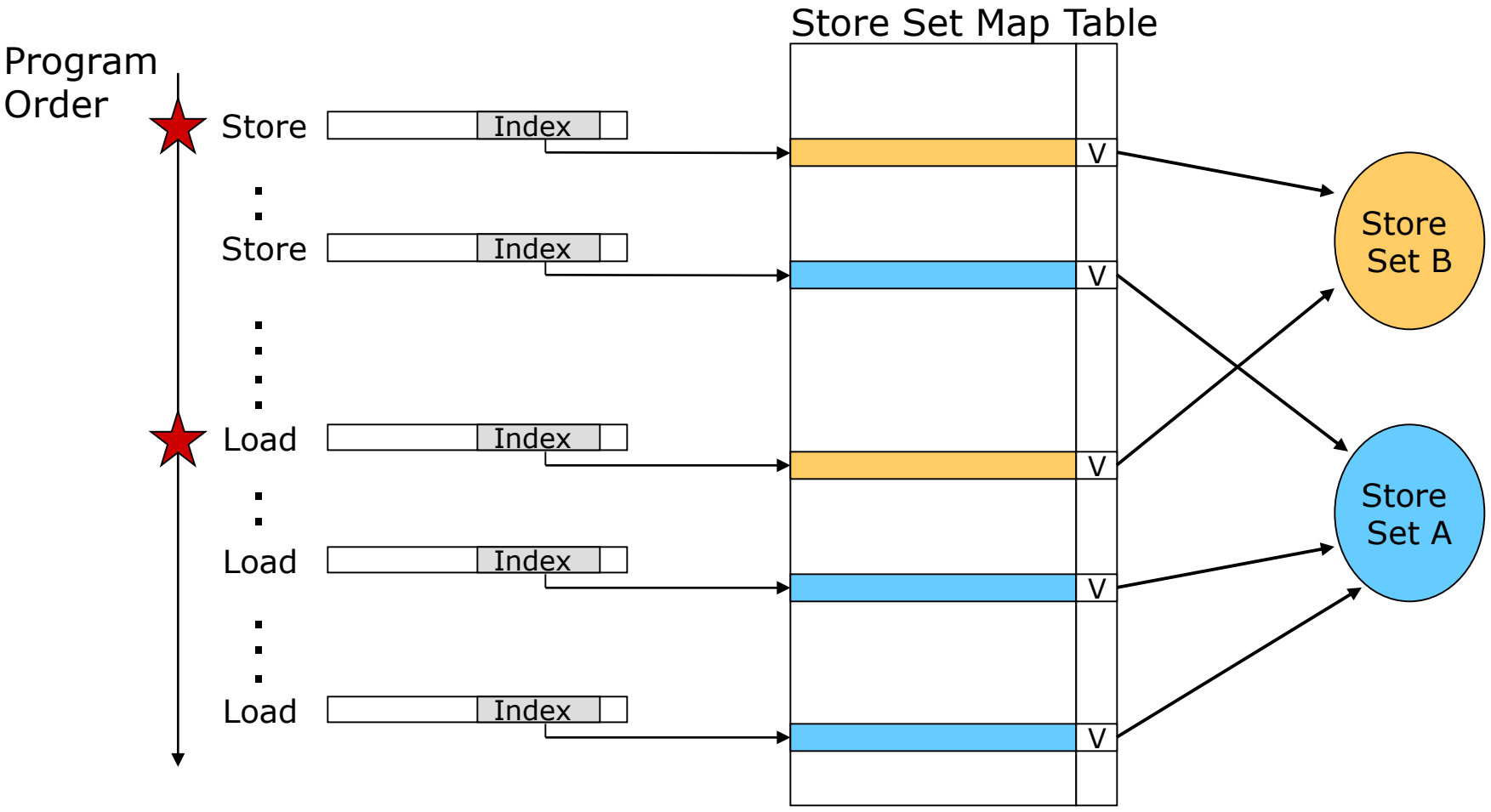

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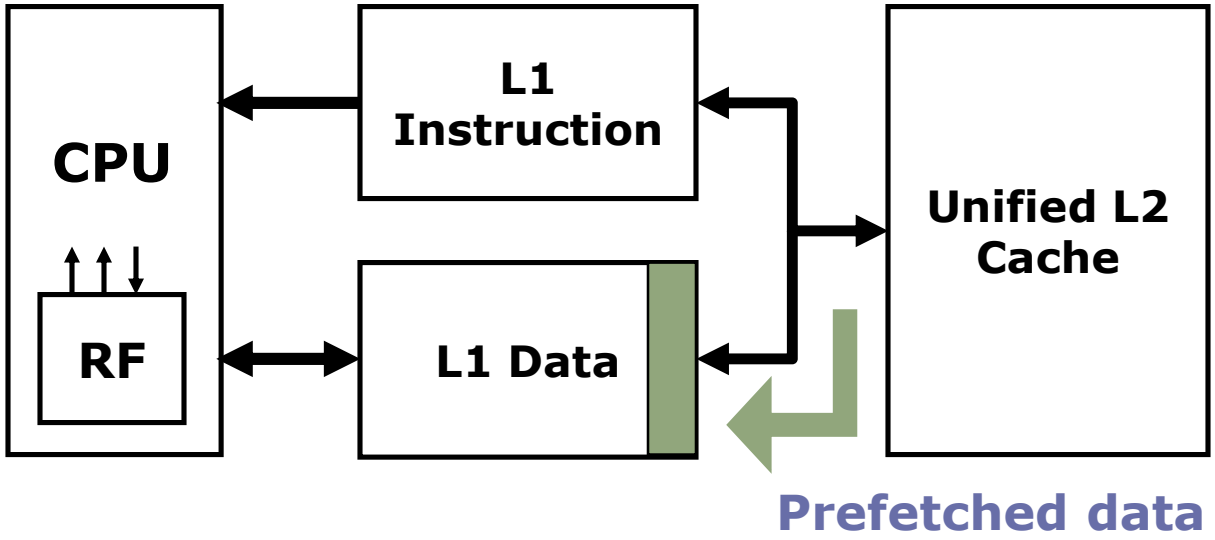
Issues in Prefetching

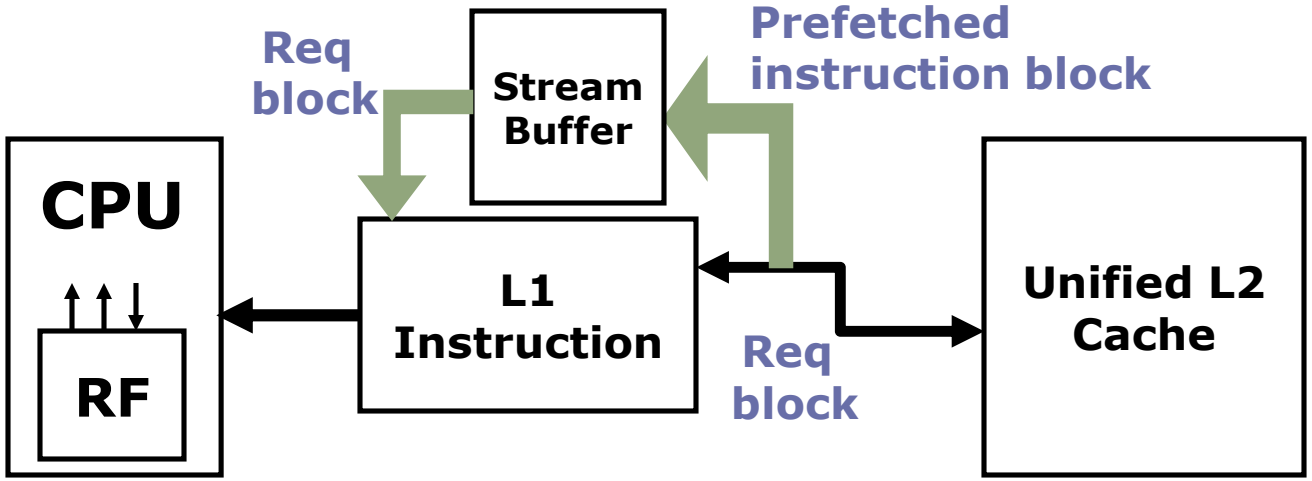
- Usefulness – should produce hits
- Timeliness – not late and not too early
- Cache and bandwidth pollution



Hardware Instruction Prefetching

Instruction prefetch in Alpha AXP 21064

- Fetch two blocks on a miss; the requested block (i) and the next consecutive block (i+1)
- Requested block placed in cache, and next block in instruction stream buffer
- If miss in cache but hit in stream buffer, move stream buffer block into cache and prefetch next block (i+2)



Hardware Data Prefetching

- Prefetch-on-miss:
  - Prefetch b + 1 upon miss on b
- One Block Lookahead (OBL) scheme
  - Initiate prefetch for block b + 1 when block b is accessed
  - *Why is this different from doubling block size?*
  - Can extend to N-block lookahead (called *stream prefetching*)
- Strided prefetch
  - If observe sequence of accesses to block b, b+N, b+2N, then prefetch b+3N etc.

Example: IBM Power 5 [2003] supports eight independent streams of strided prefetch per processor, prefetching 12 lines ahead of current access

Thank you!

Next lecture:
Multithreading