

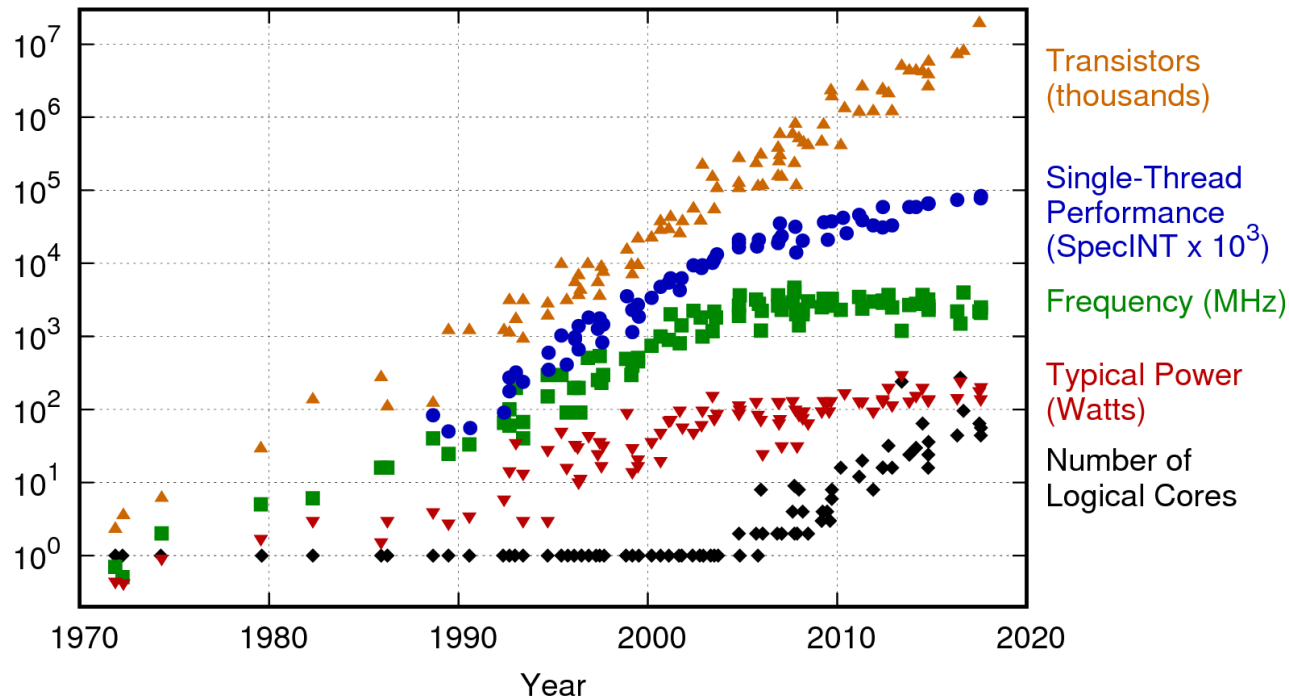
# Cache Coherence

*Mengjia Yan*

Computer Science & Artificial Intelligence Lab  
M.I.T.

*Based on slides from Daniel Sanchez*

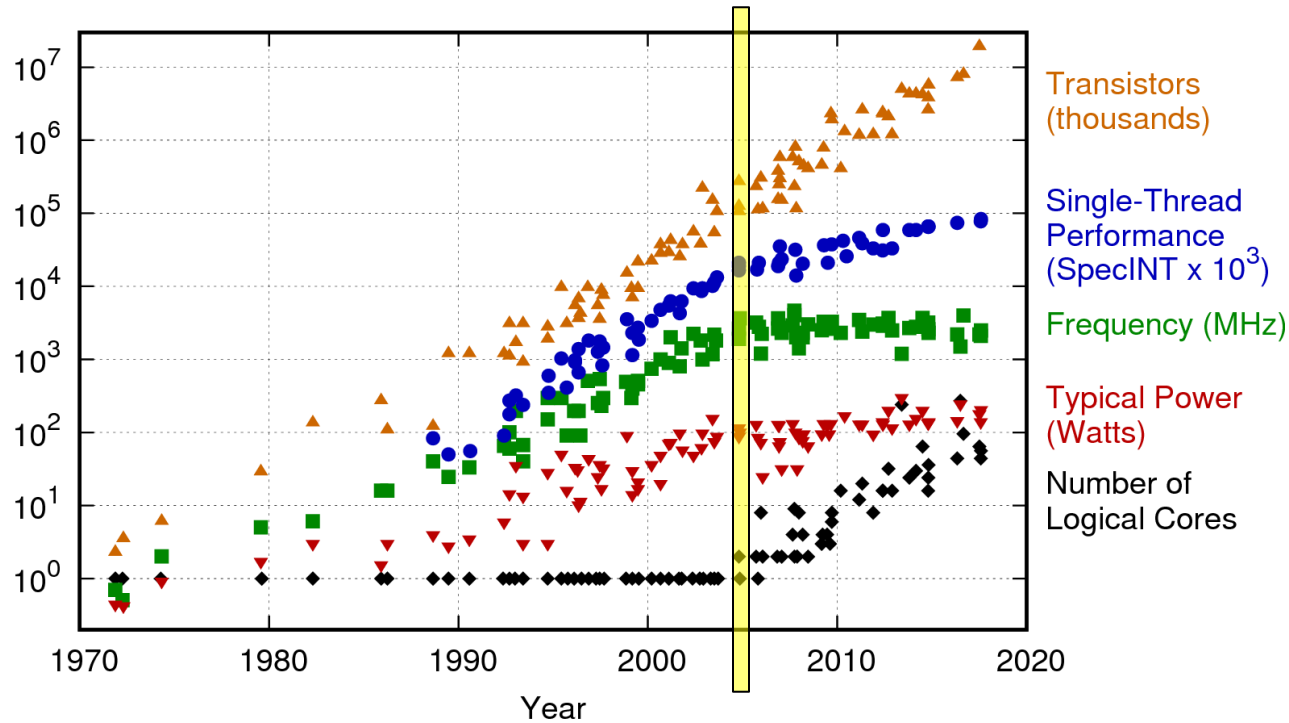
# The Shift to Multicore



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten

New plot and data collected for 2010-2017 by K. Rupp [<https://www.karlsruhp.net/2018/02/42-years-of-microprocessor-trend-data/>]

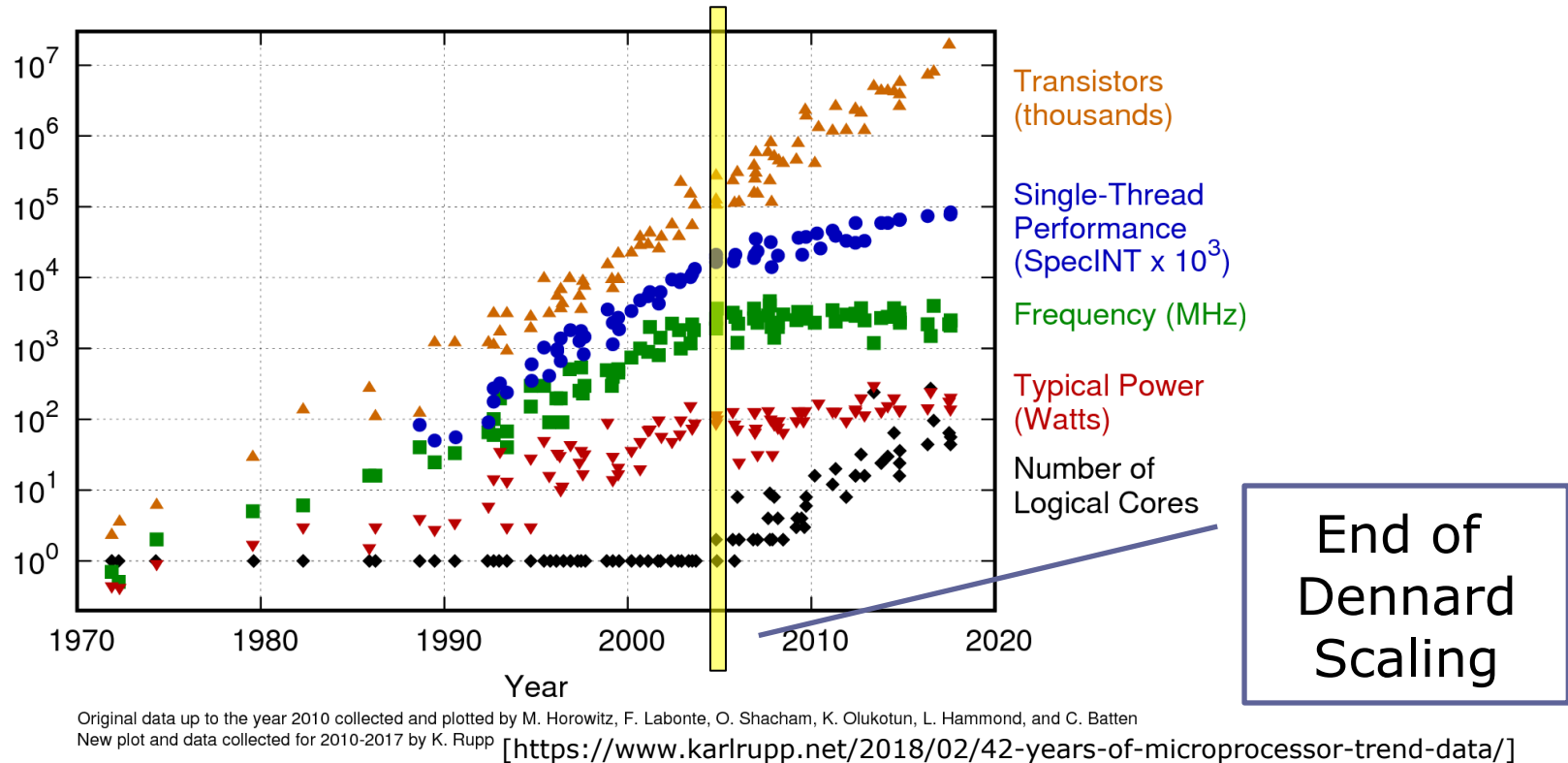
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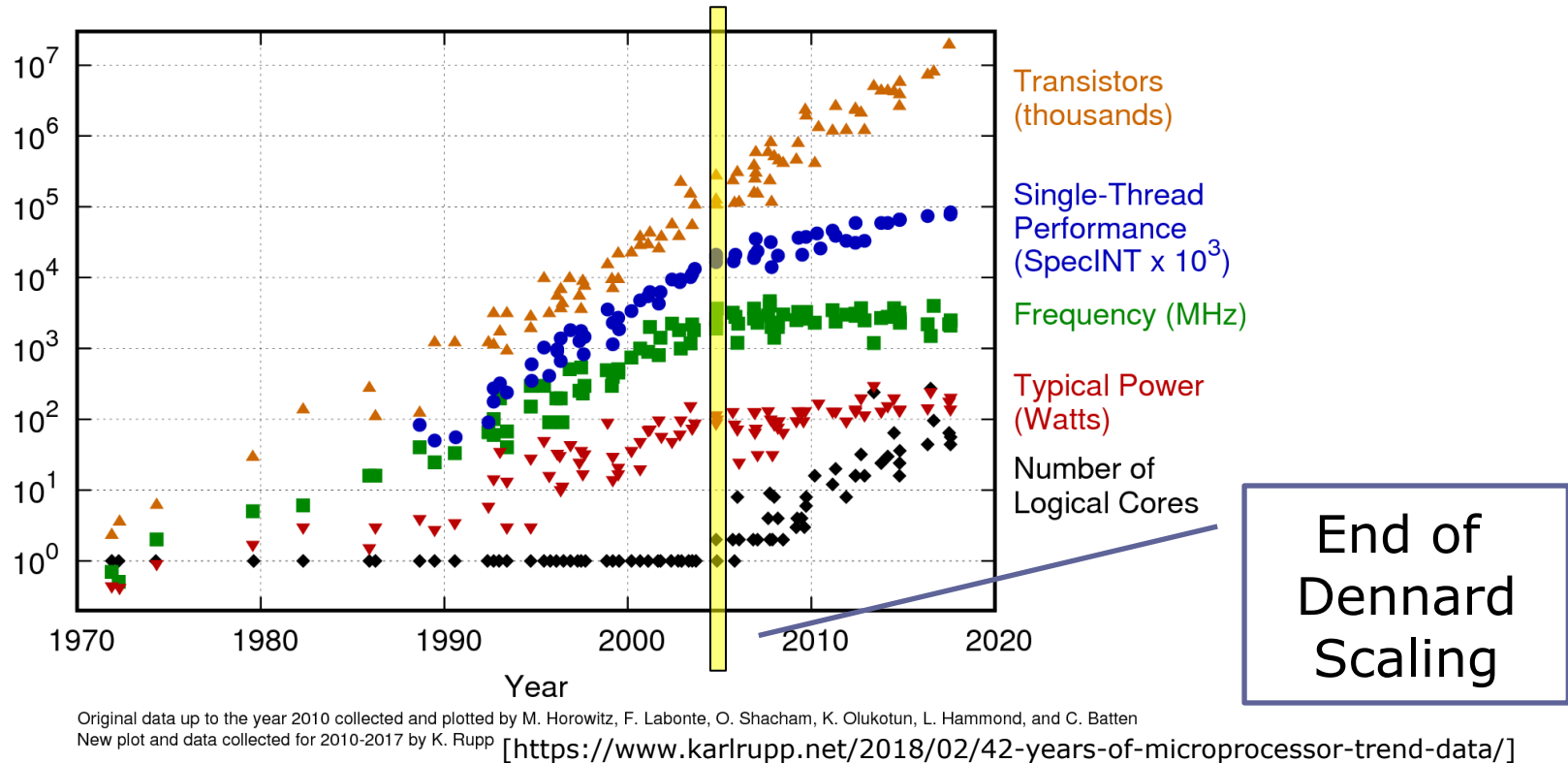
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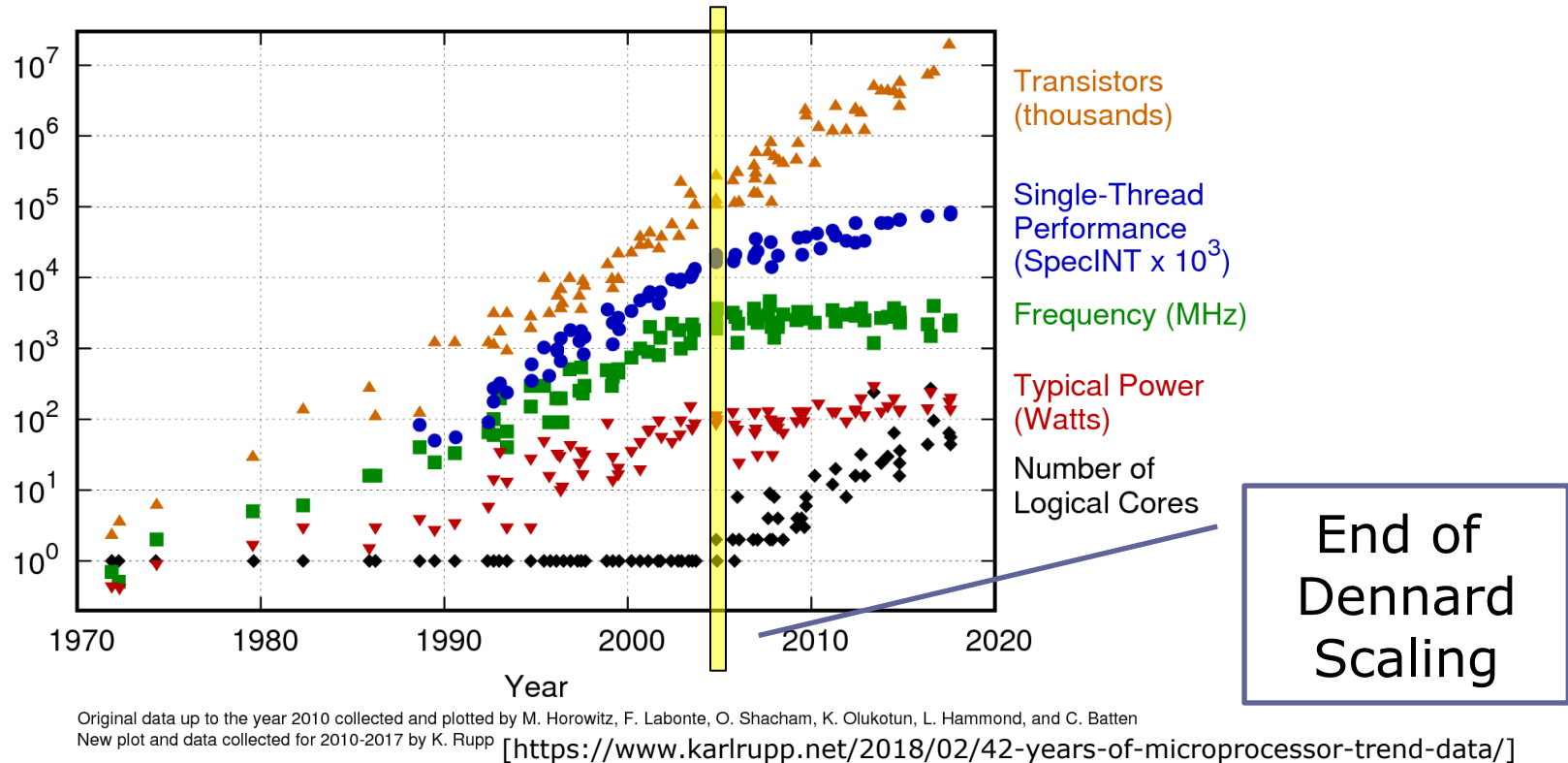


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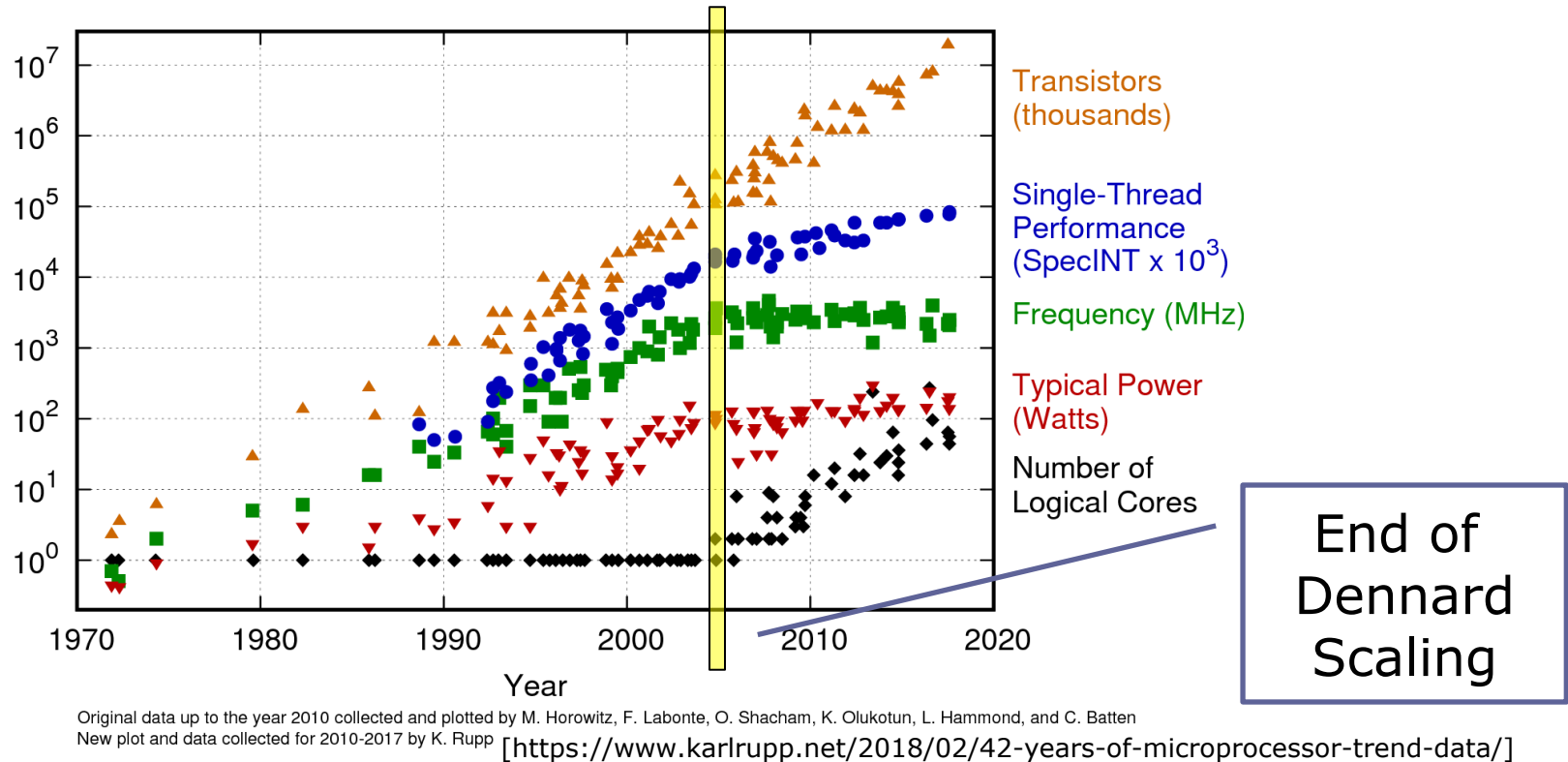
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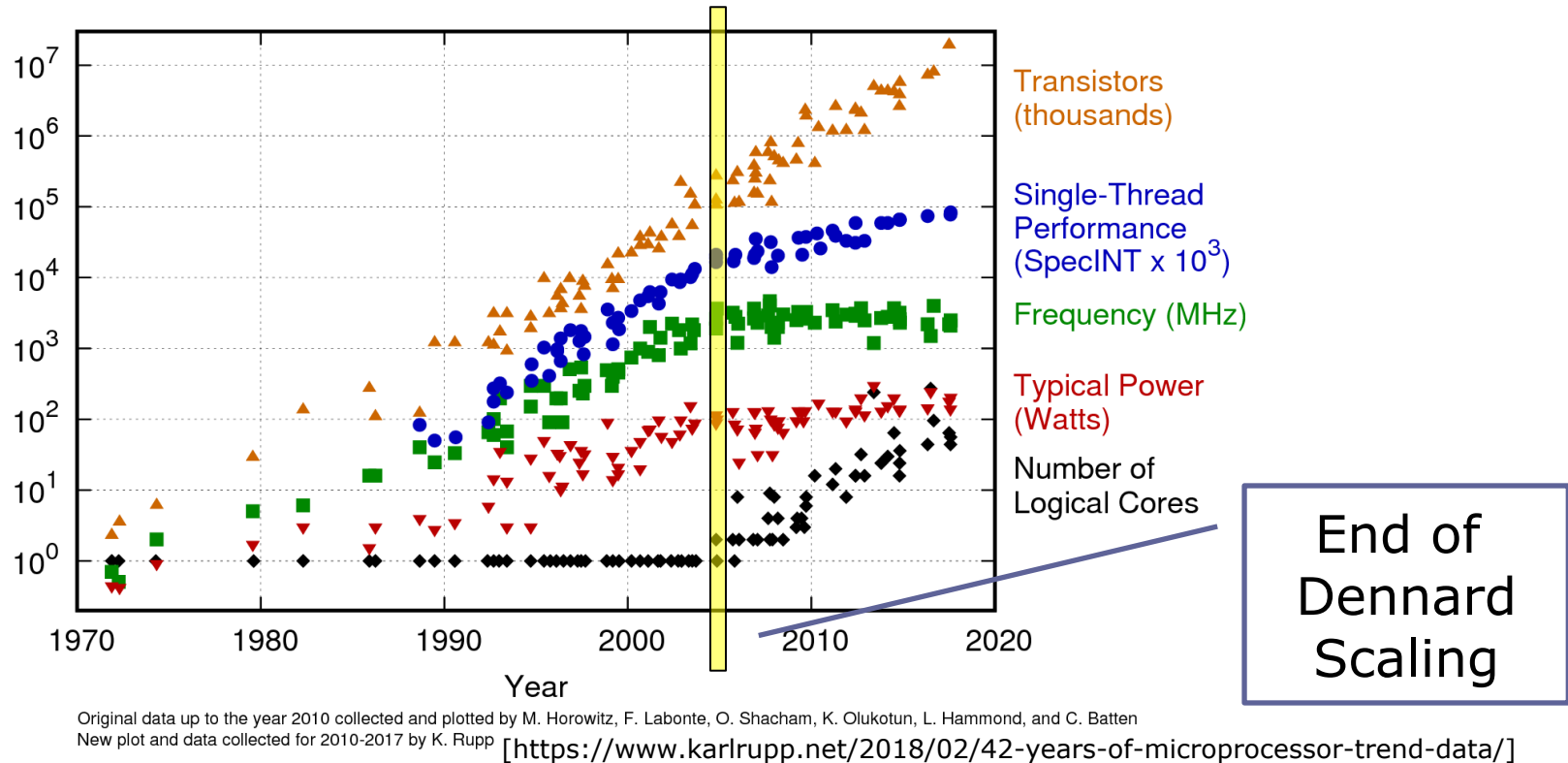
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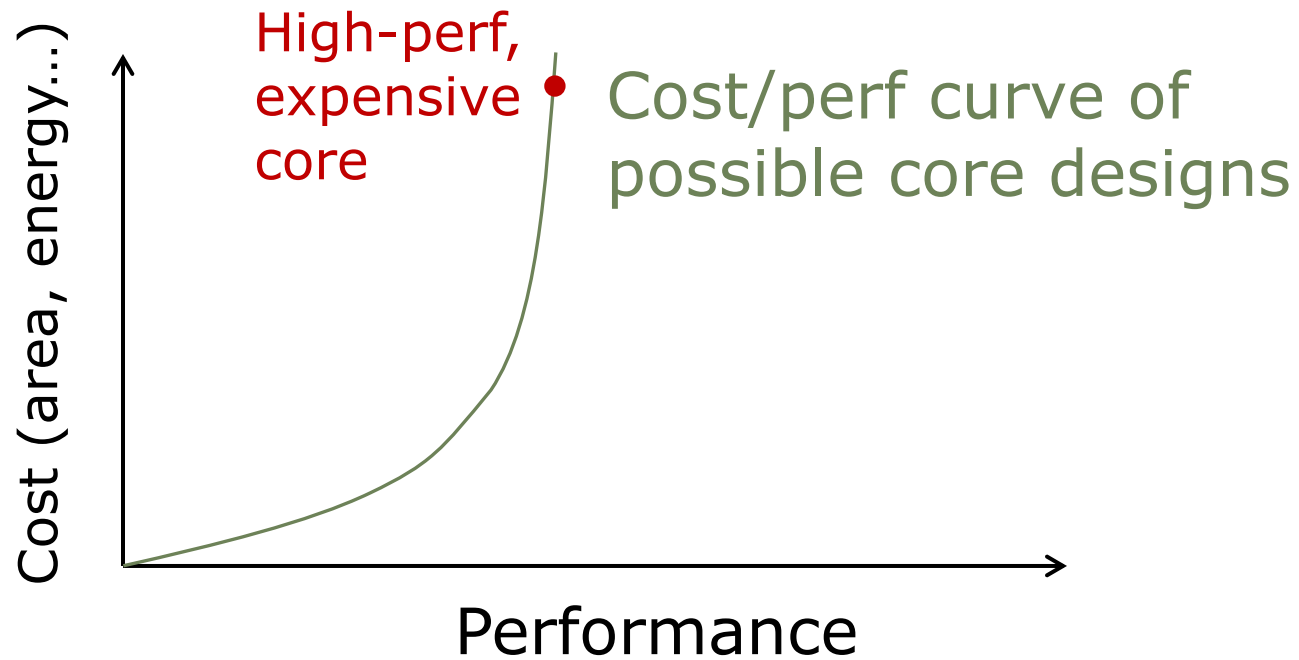


- Since 2005, improvements in system performance mainly due to increasing cores per chip
- Why? **Technology scaling**  
**Limited instruction-level parallelism**



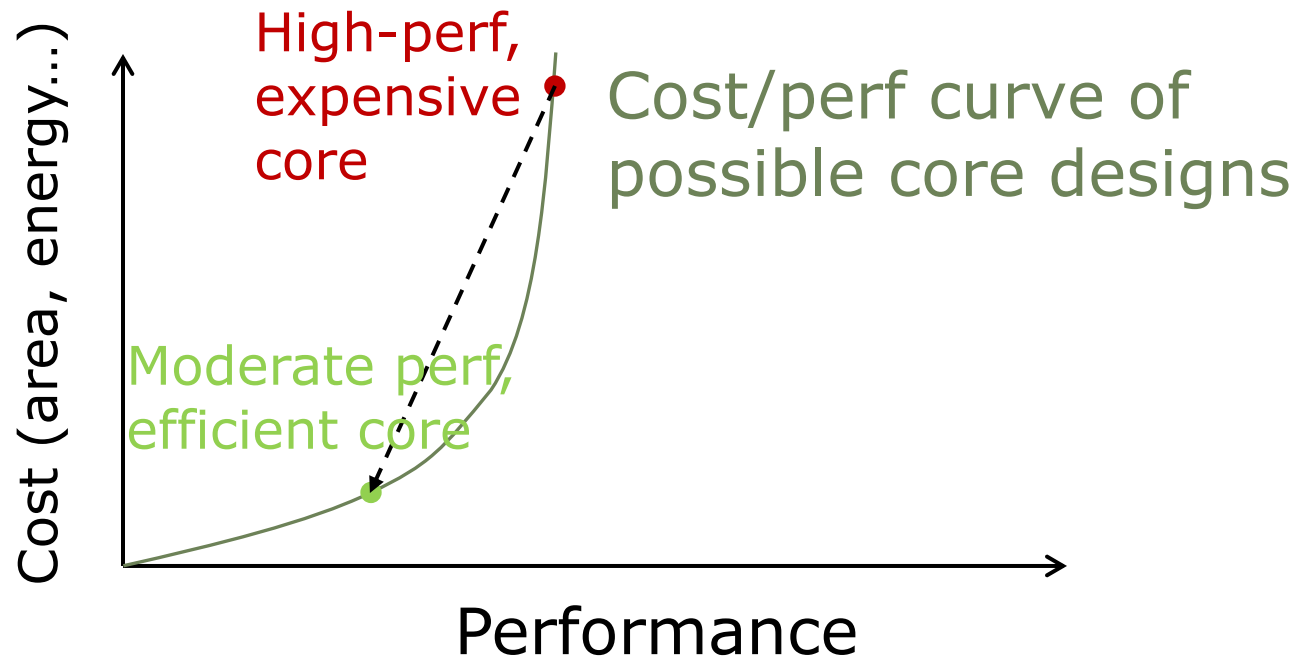
# Multicore Performance

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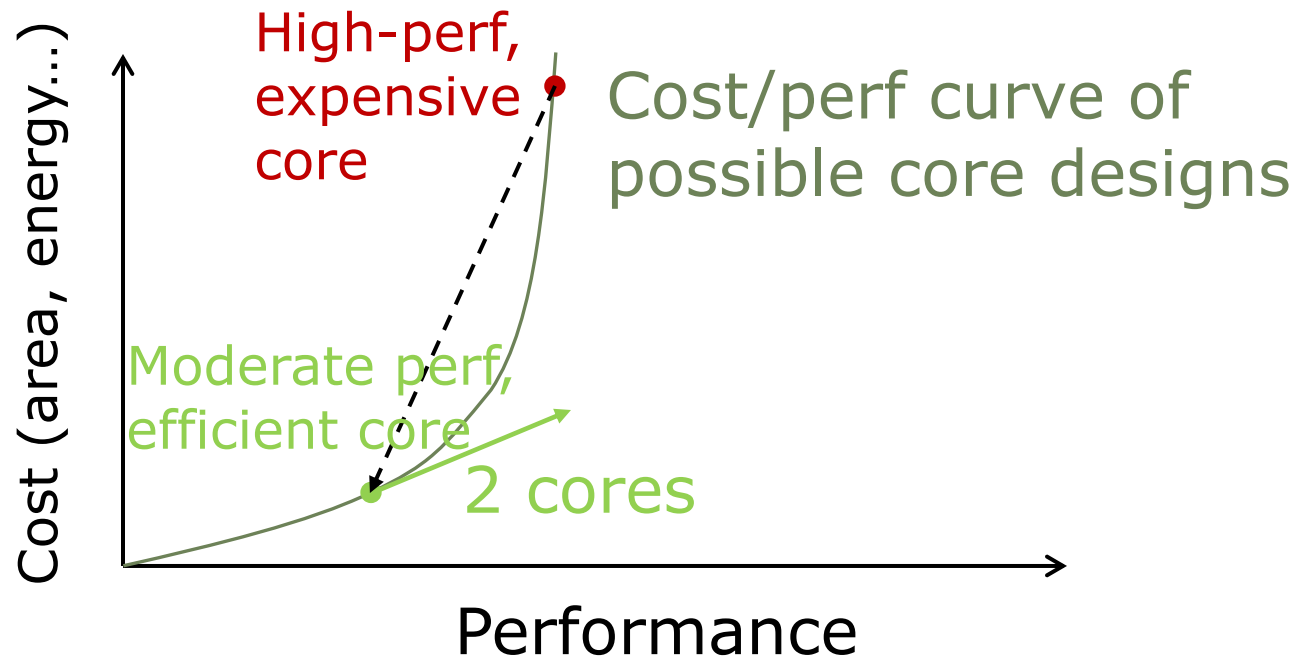
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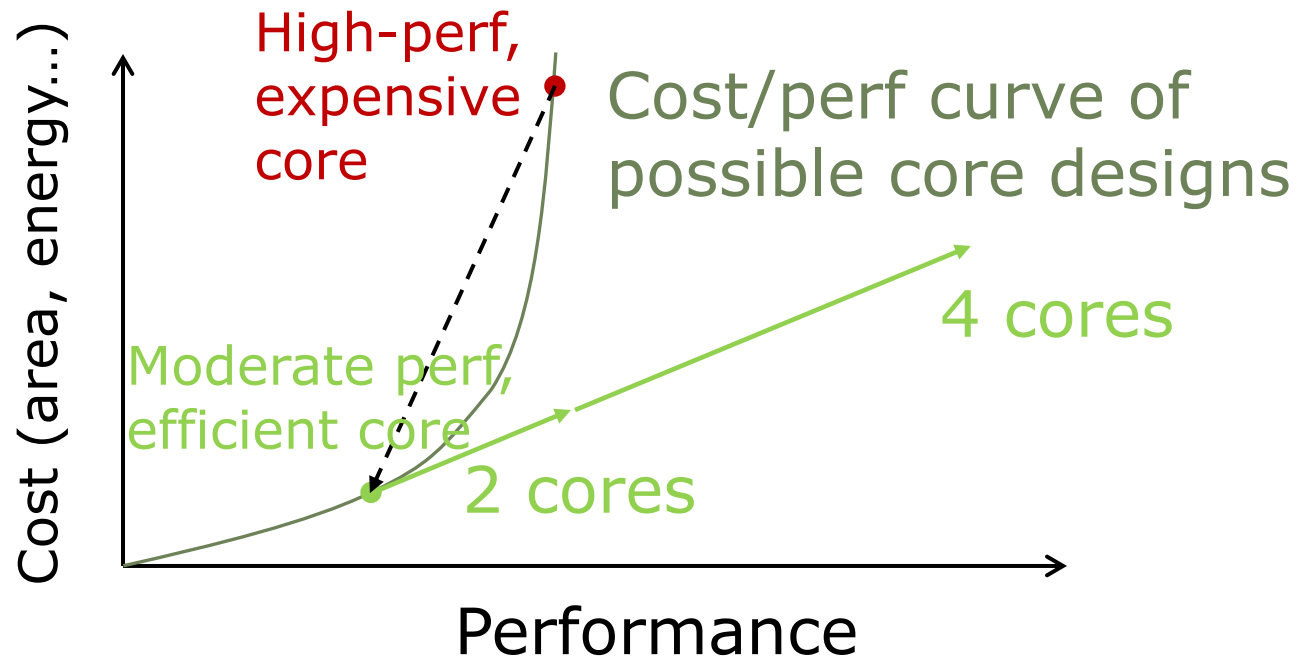
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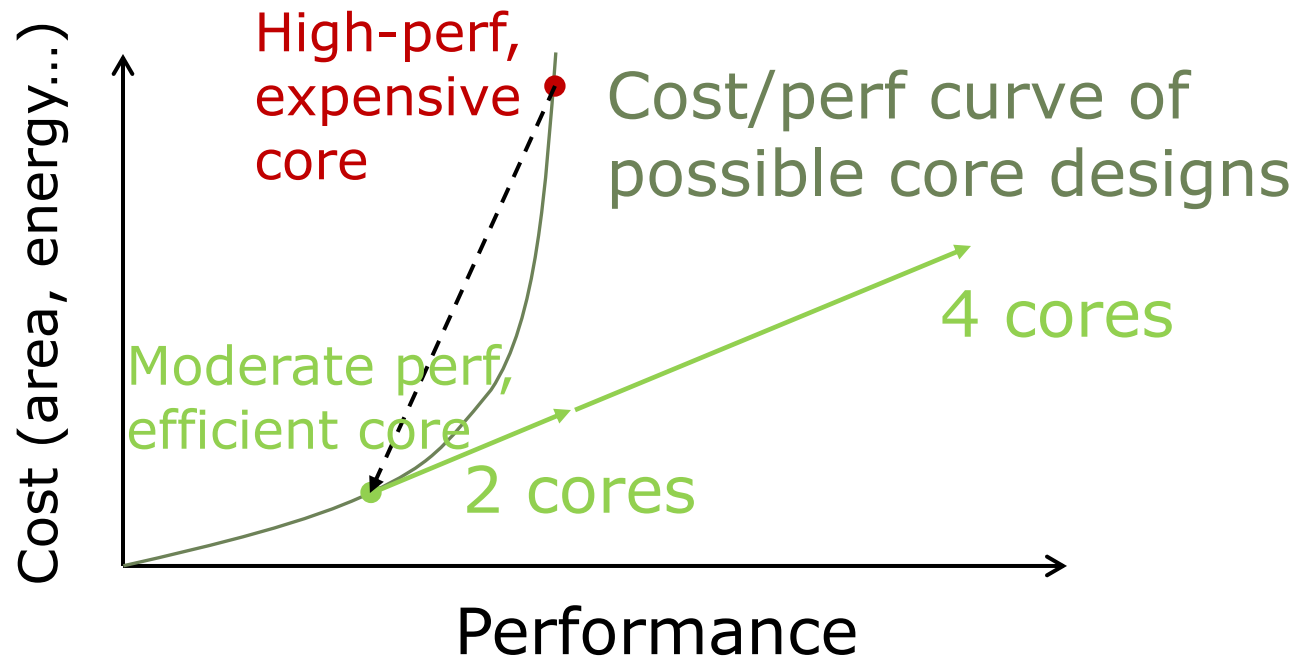
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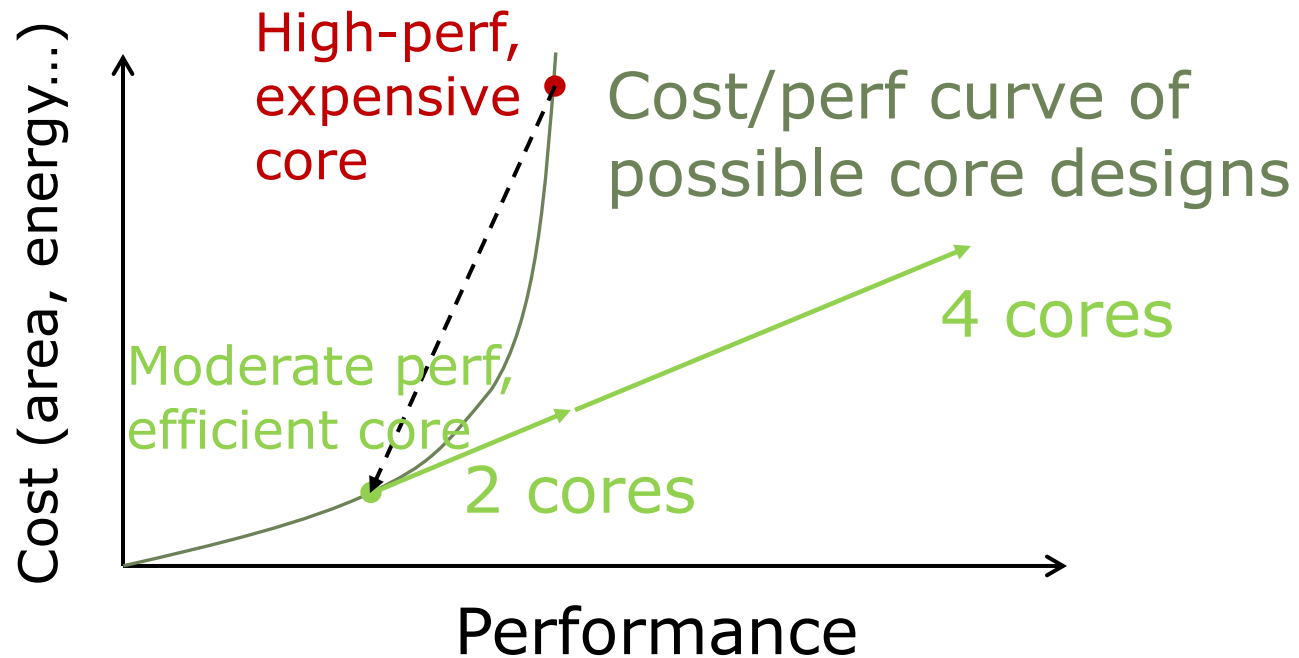
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*What factors may limit multicore performance?*

# Multicore Performance

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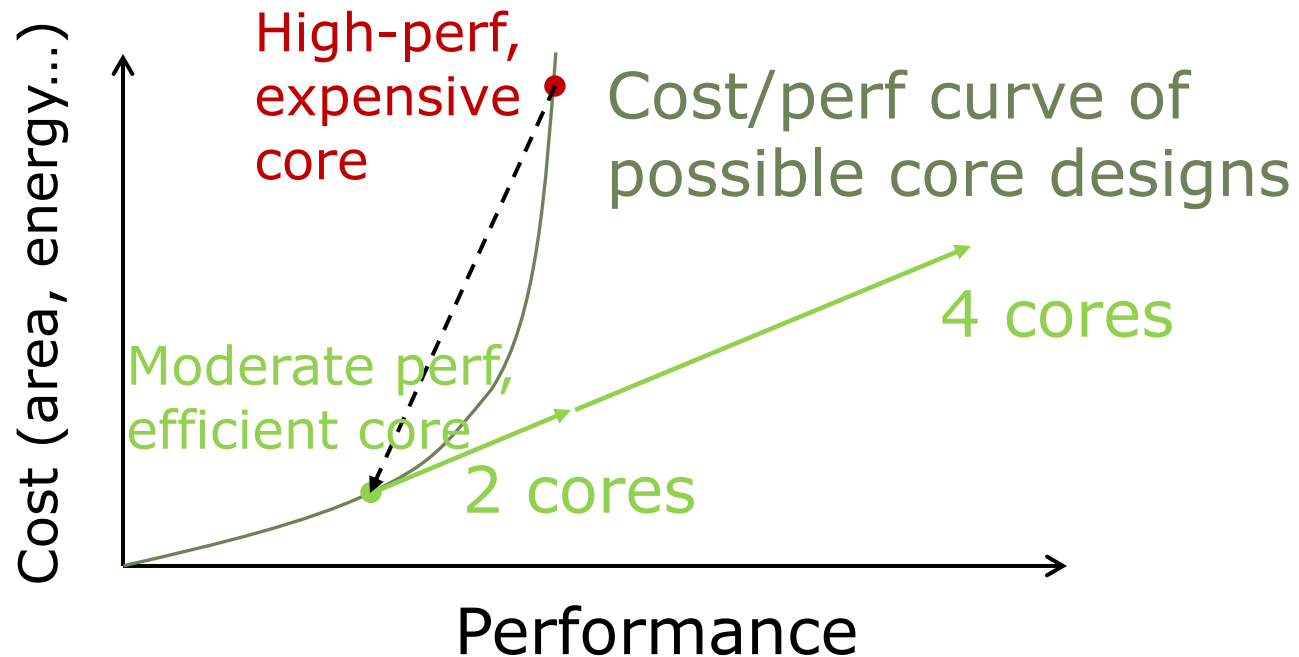


*What factors may limit multicore performance?*

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# Multicore Performance

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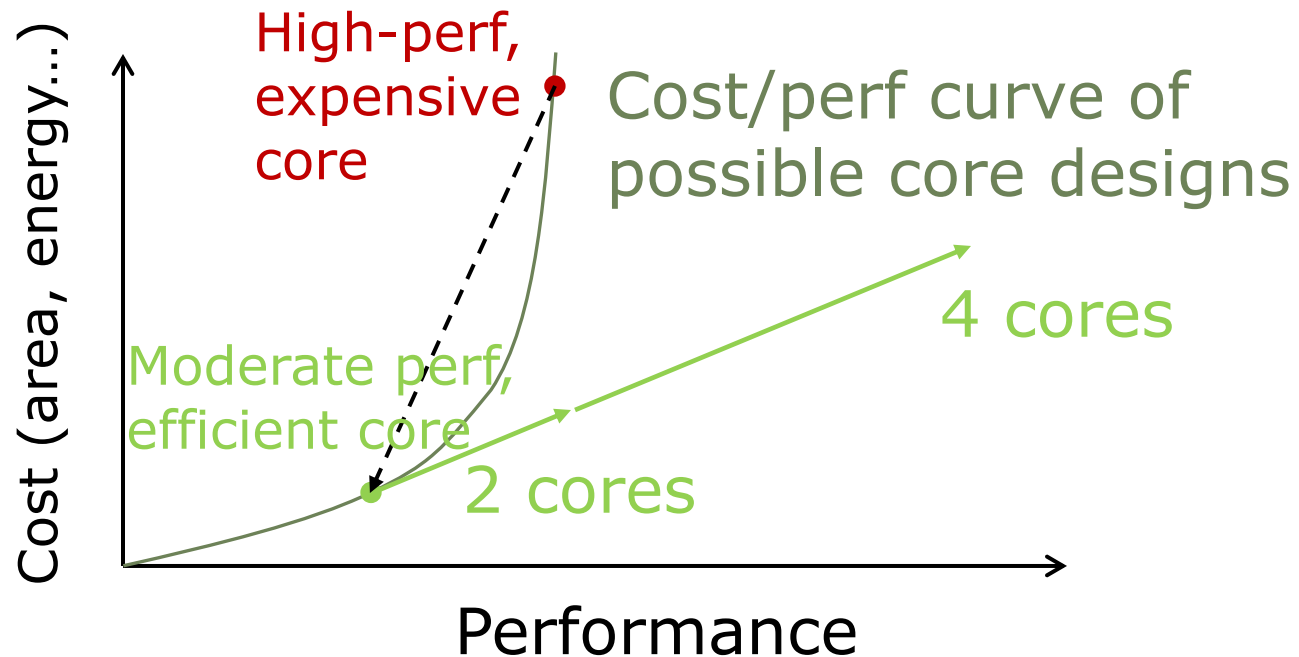


*What factors may limit multicore performance?*

- Limited application parallelism
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# Multicore Performance

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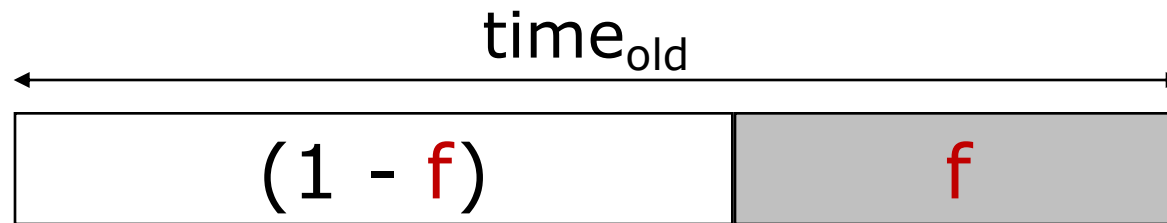
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- Programming complexity



# Amdahl's Law

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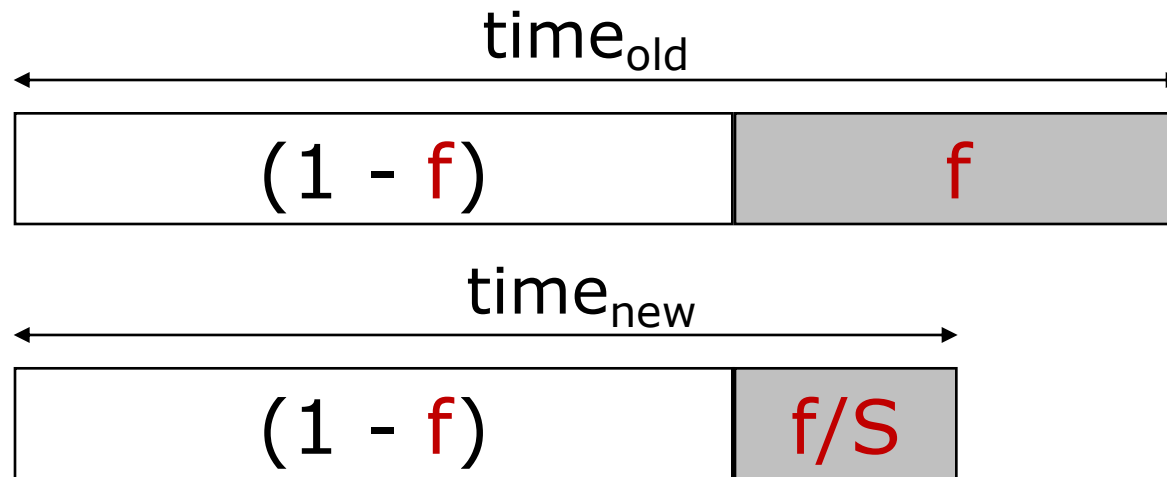
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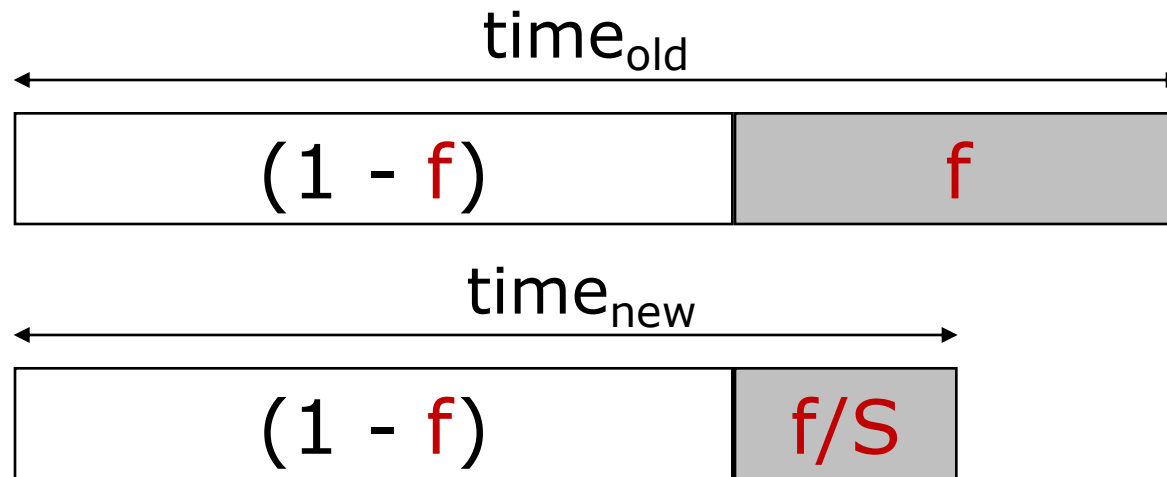


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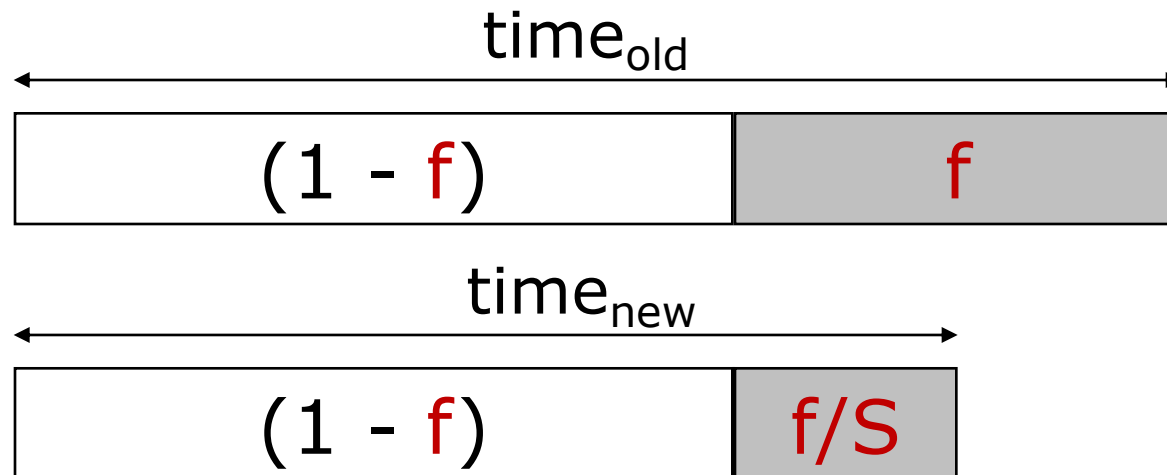
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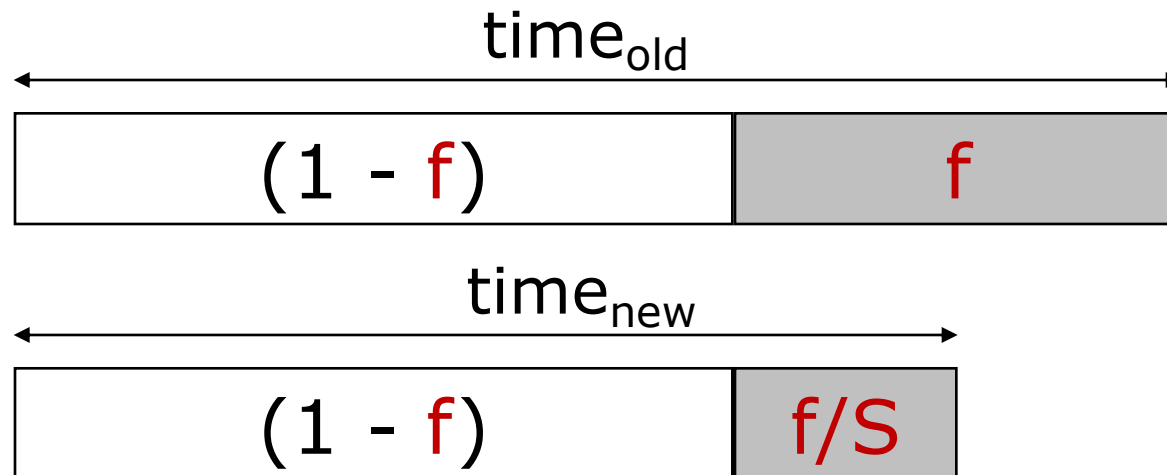
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**Corollary: Make the common case fast**

# Amdahl's Law and Parallelism

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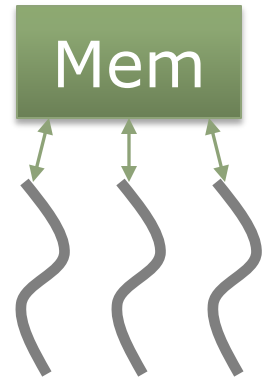
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What  $f$  do you need to use a 1000-core machine well?

# Communication Models

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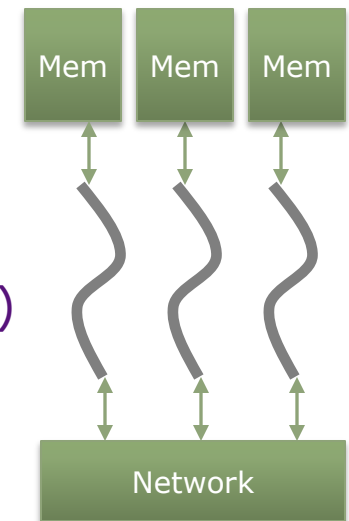
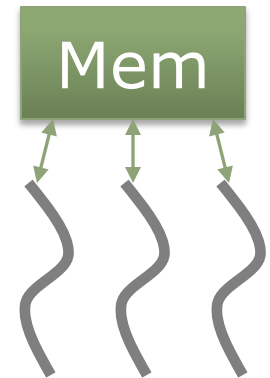
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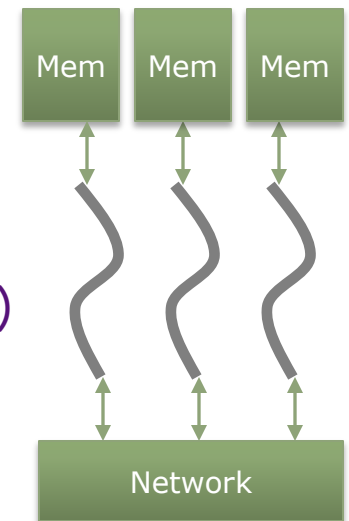
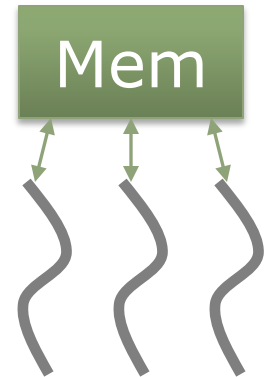
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- Pros/cons of each model?



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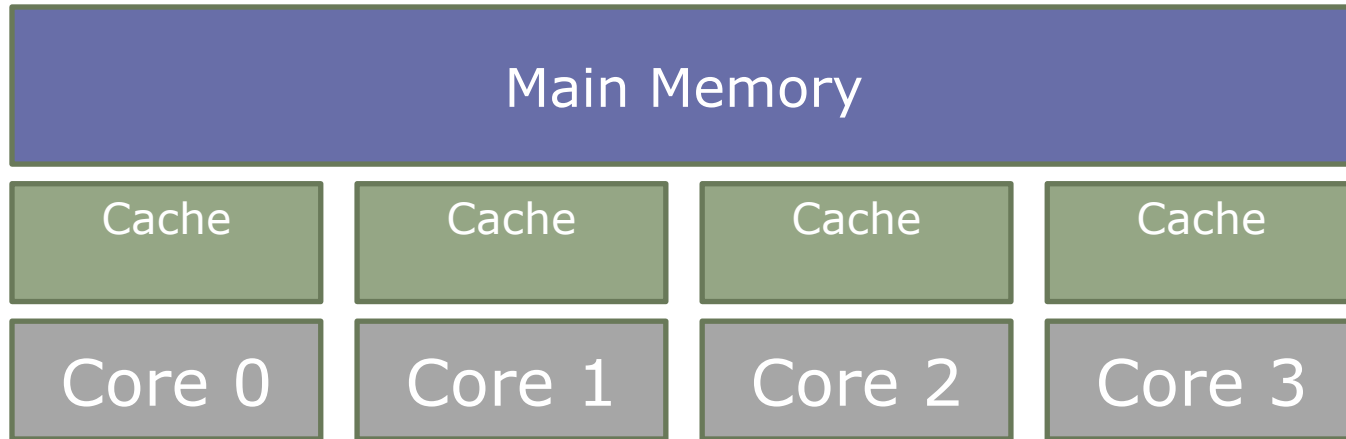
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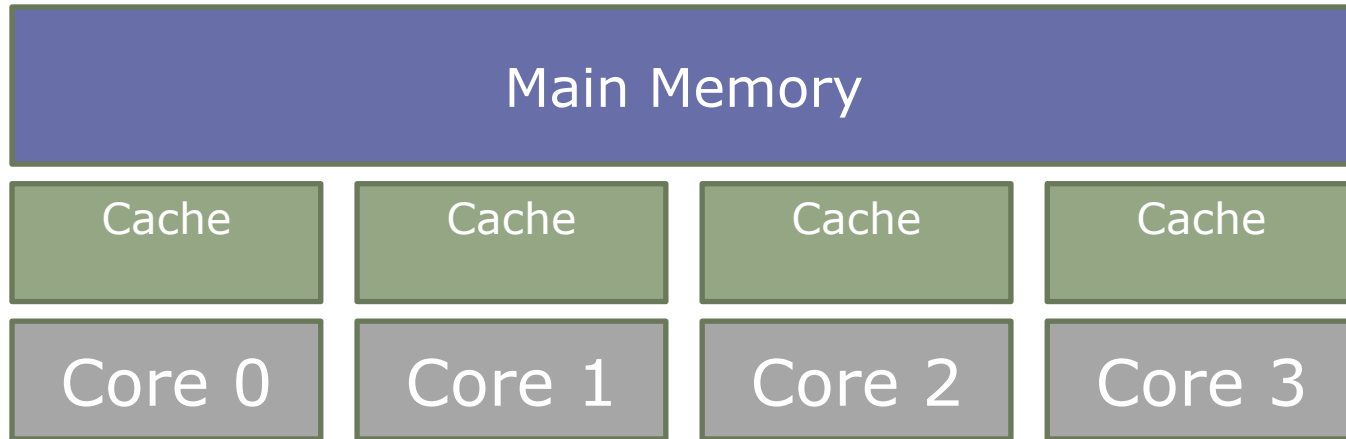
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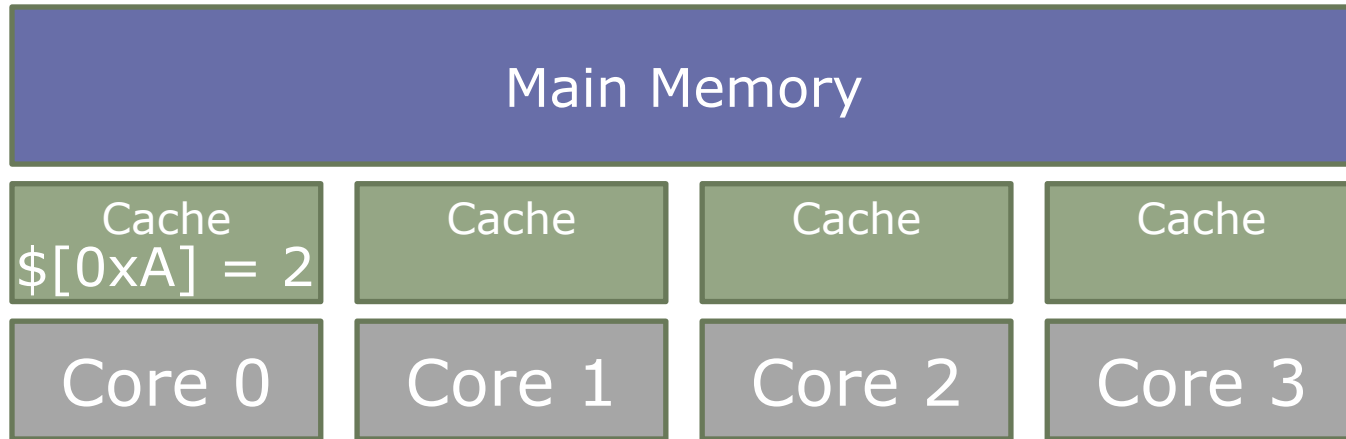
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**1** LD 0xA → 2

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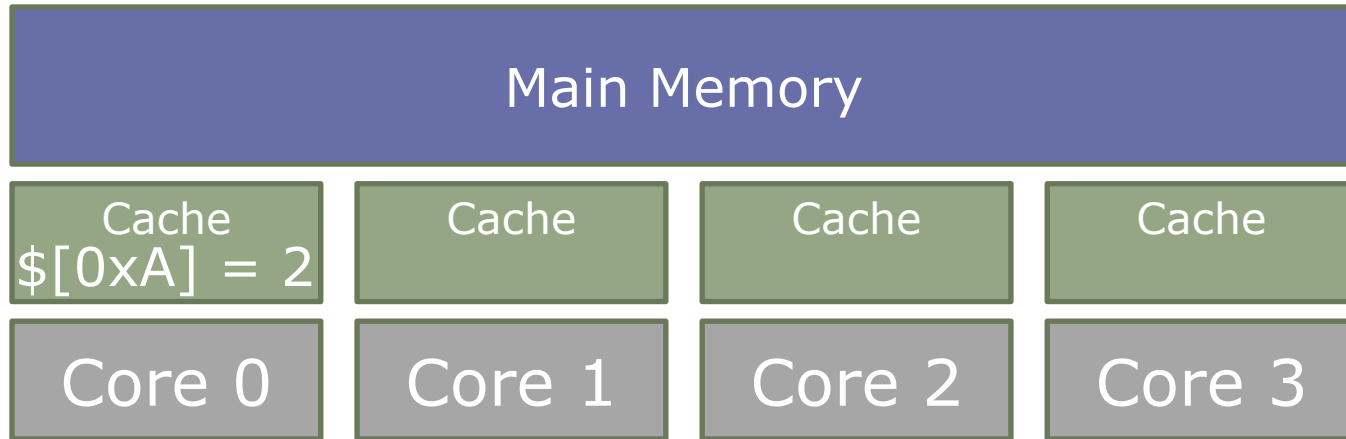
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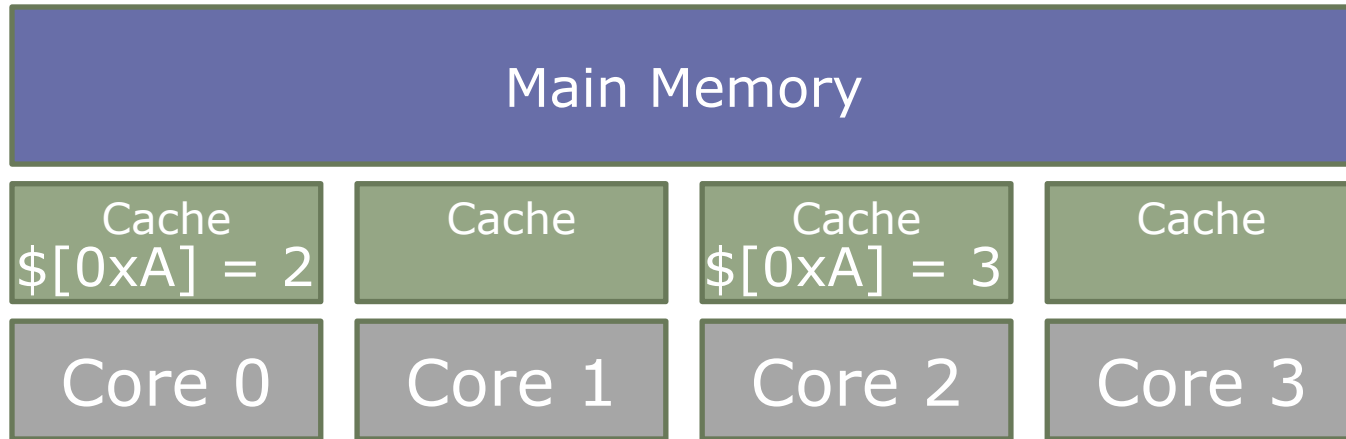


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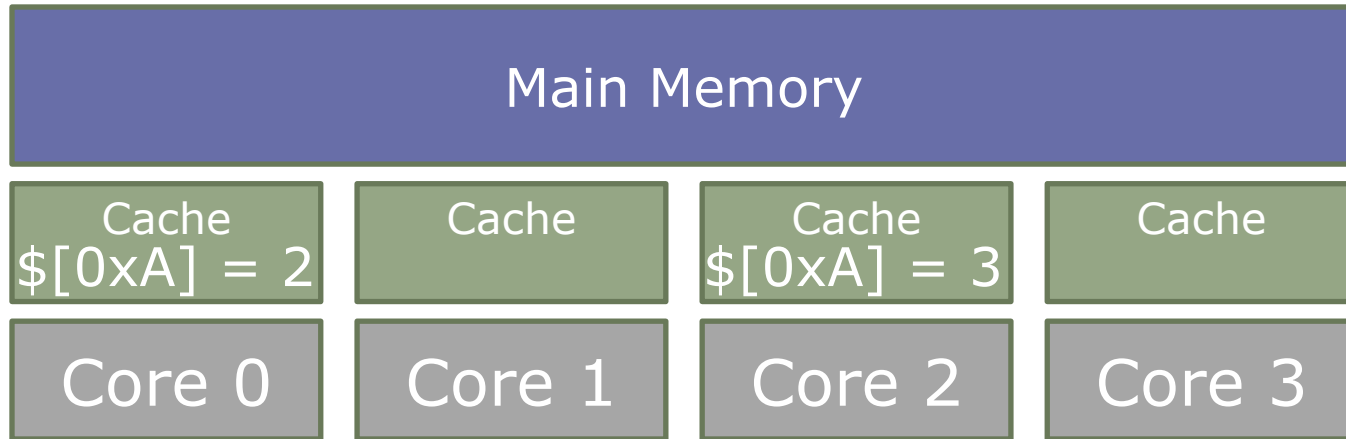


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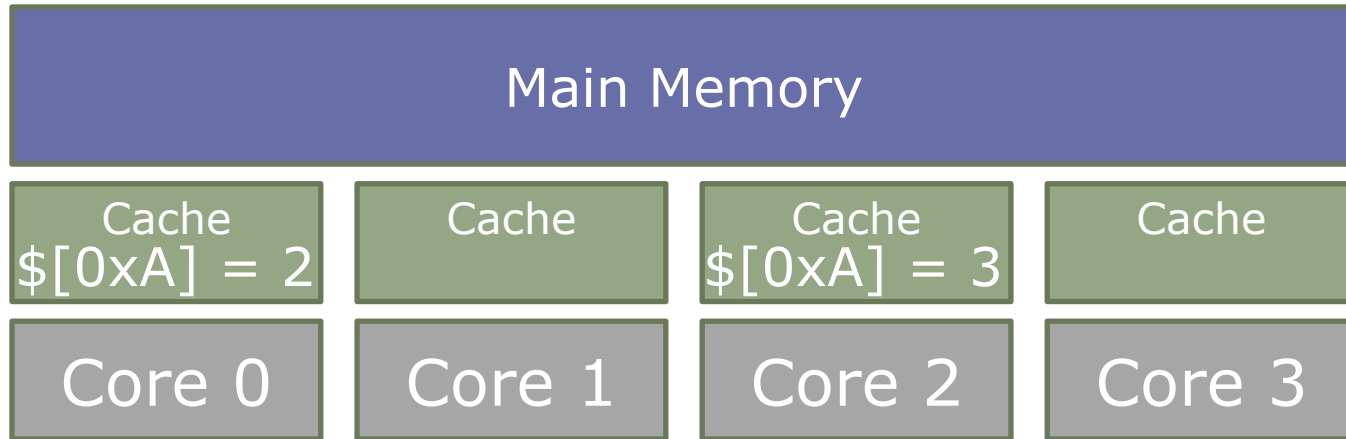
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① LD 0xA → 2

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- A **cache coherence protocol** controls cache contents to avoid stale cache lines



# Implementing Cache Coherence

---

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  - *Write propagation*: Writes eventually become visible to all processors
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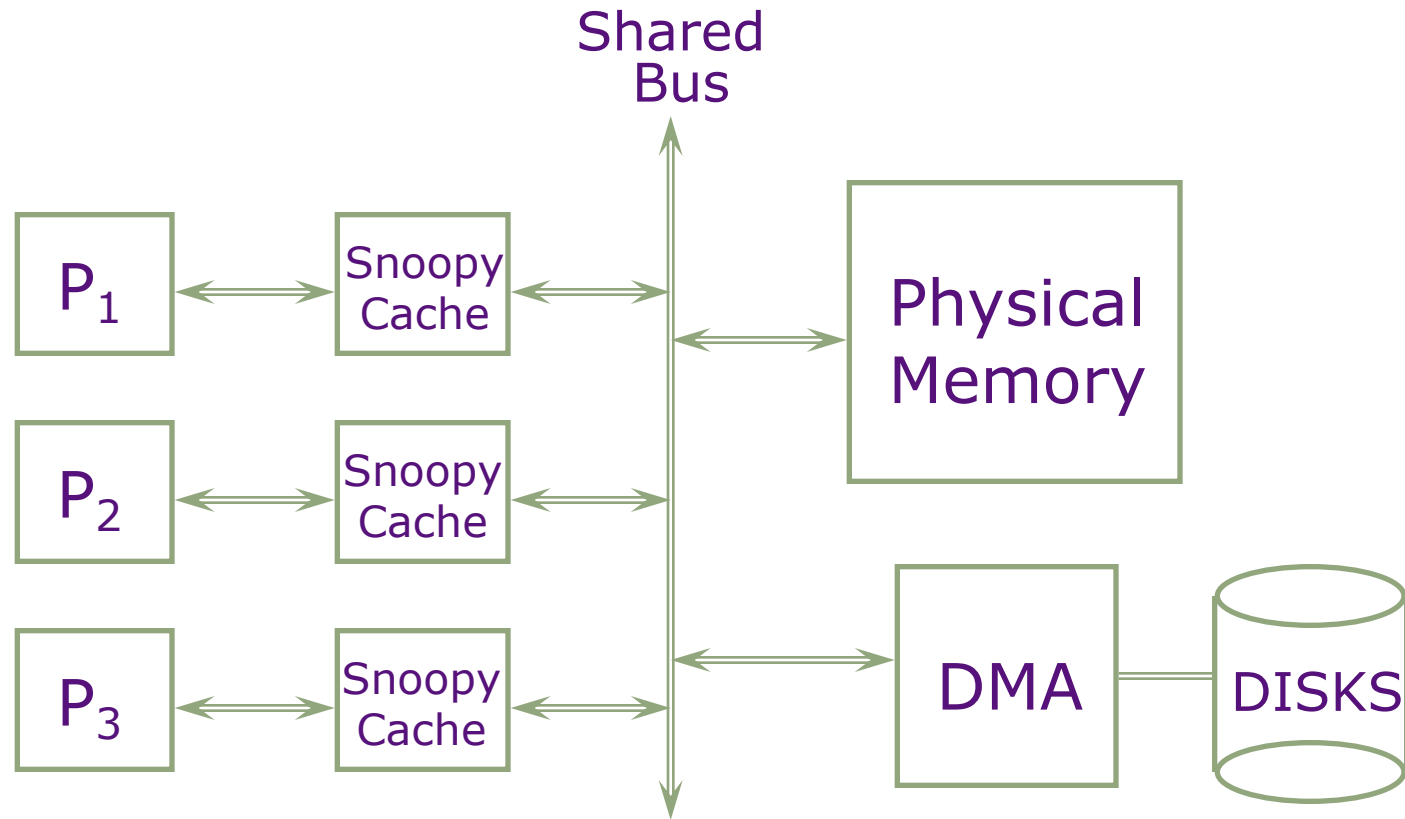
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- How to track sharing state of cached data and serialize requests to the same address?
  - *Snooping-based protocols*: All caches observe each other's actions through a shared bus (bus is the serialization point)
  - *Directory-based protocols*: A coherence directory tracks contents of private caches and serializes requests (directory is the serialization point)

# Snooping-Based Coherence

(Goodman, 1983)

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Caches watch (snoop on) bus to keep all processors' view of memory coherent

# Snooping-Based Coherence

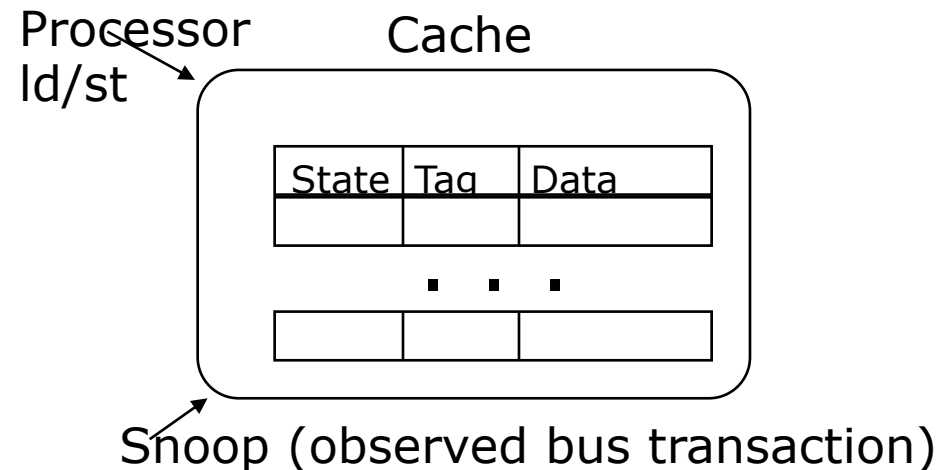
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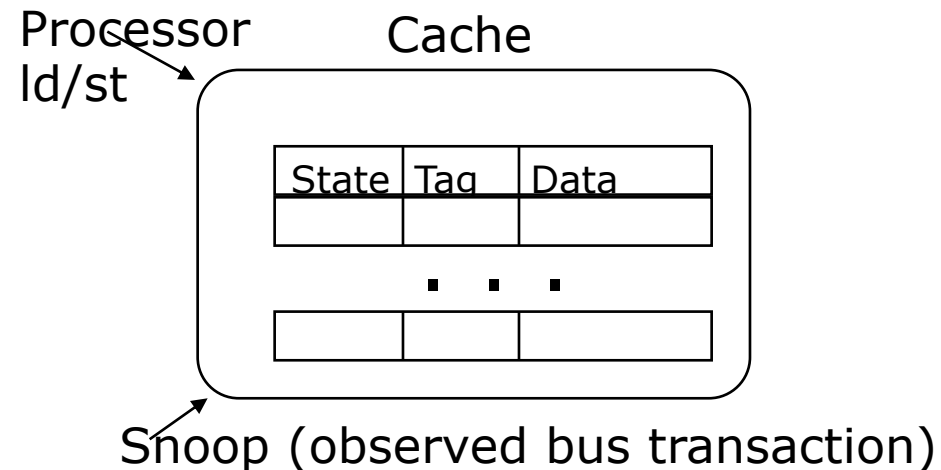
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  - One cache controller for each core “snoops” all bus transactions
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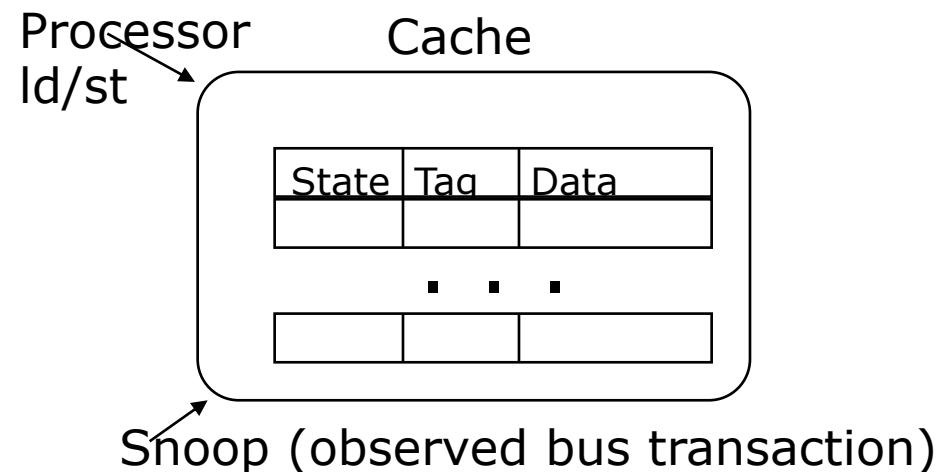
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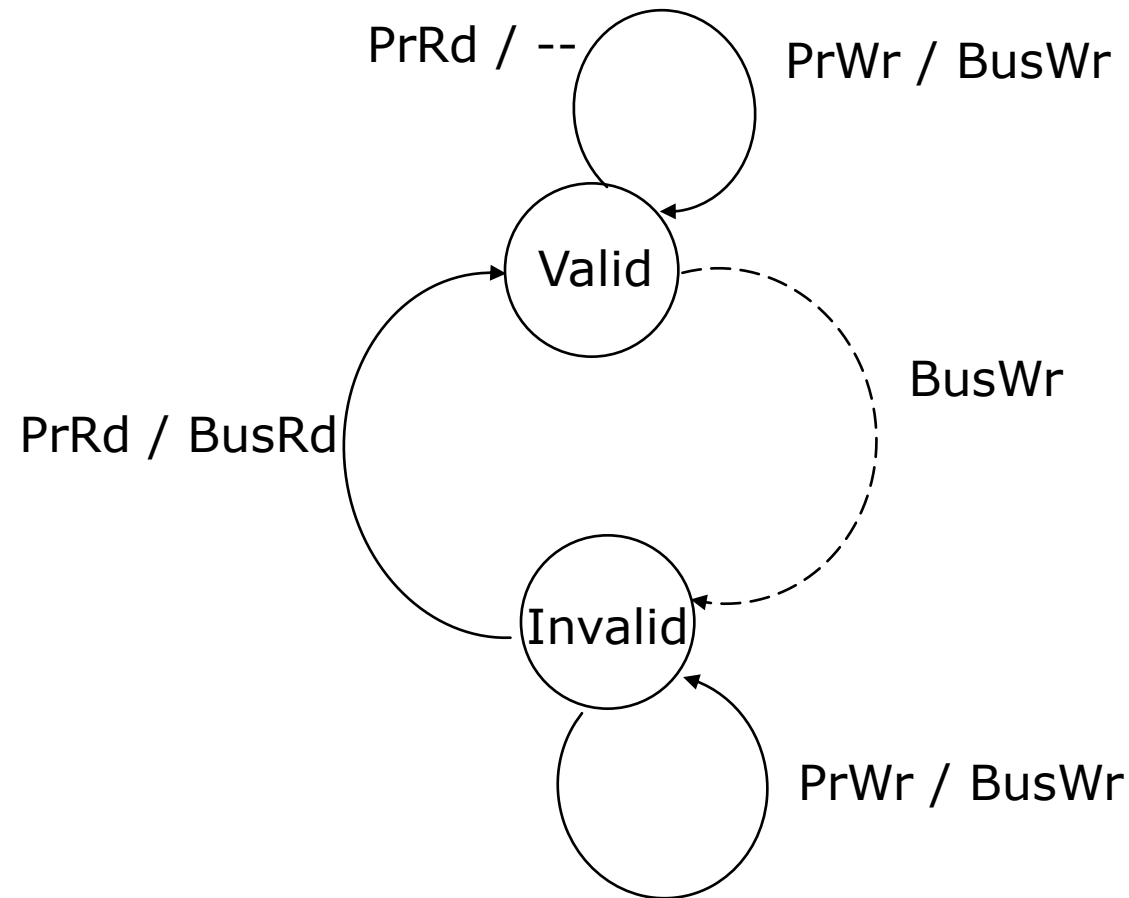
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- Handling writes:
  - Write-invalidate
  - Write-update





# A Simple Protocol: Valid/Invalid (VI)

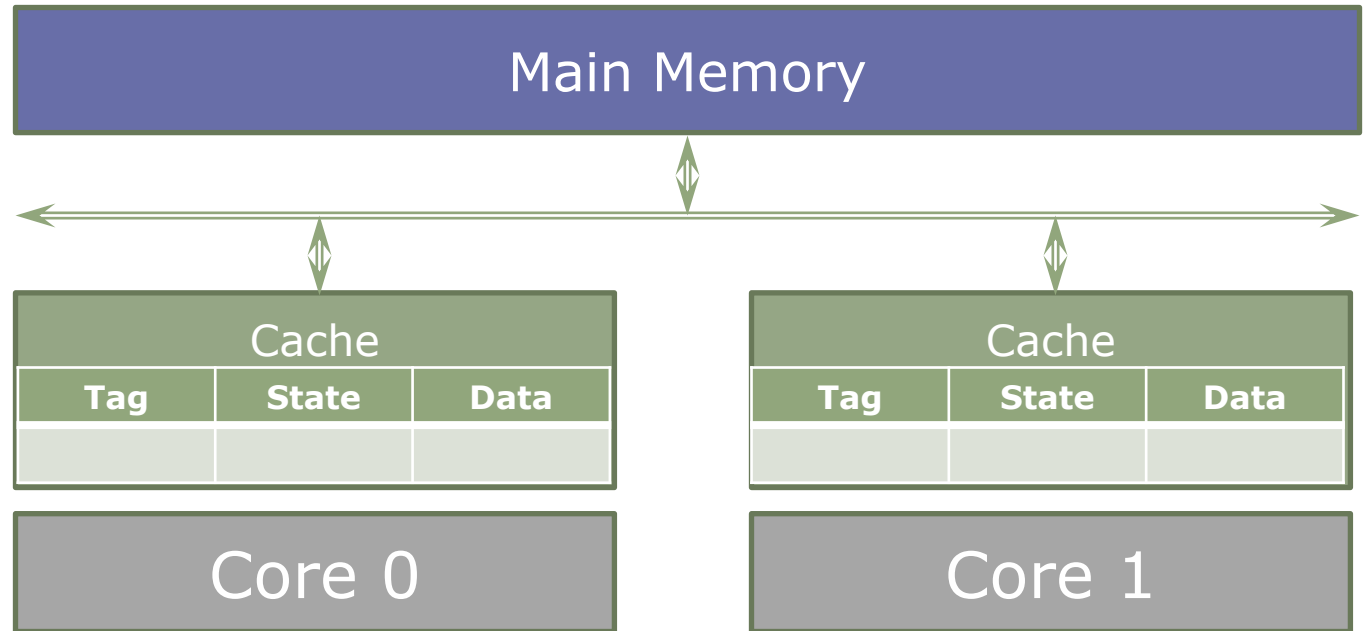


- Assume write-through caches
- Transition:  
*received action / generate action*

Actions
Processor Read (PrRd)
Processor Write (PrWr)
Bus Read (BusRd)
Bus Write (BusWr)

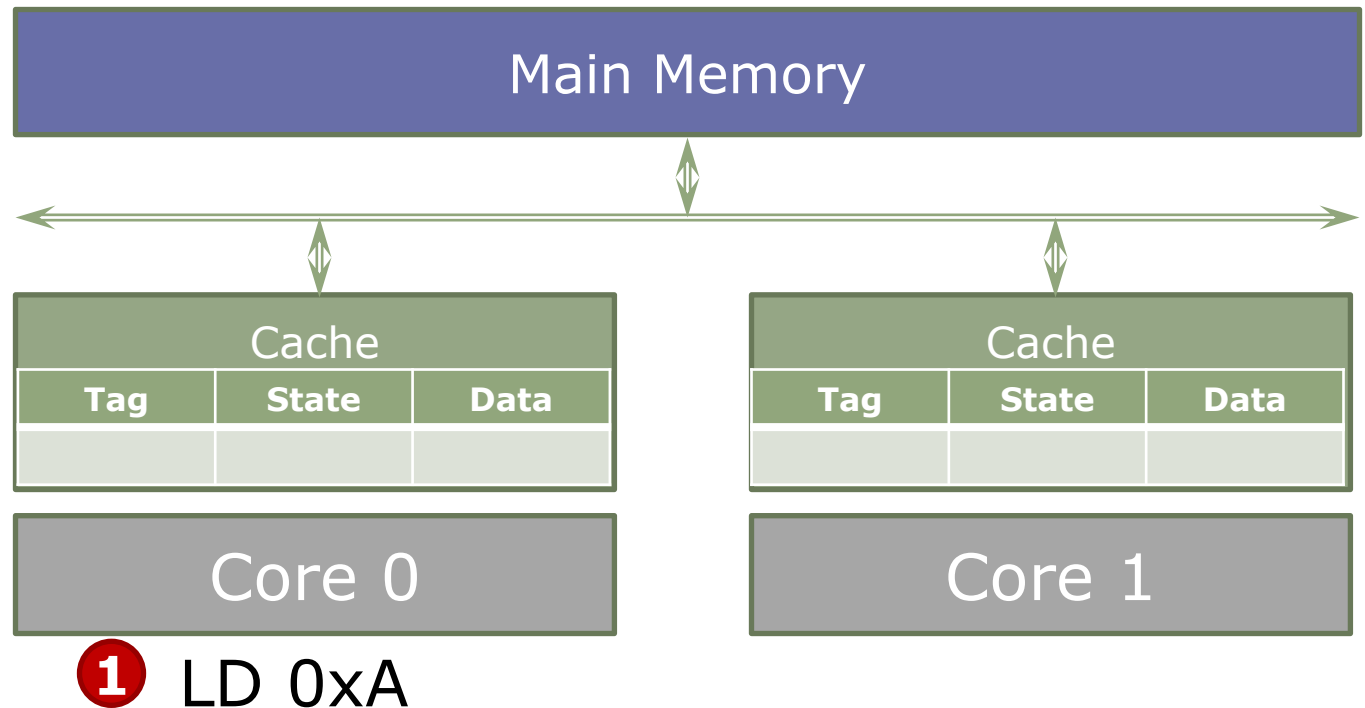
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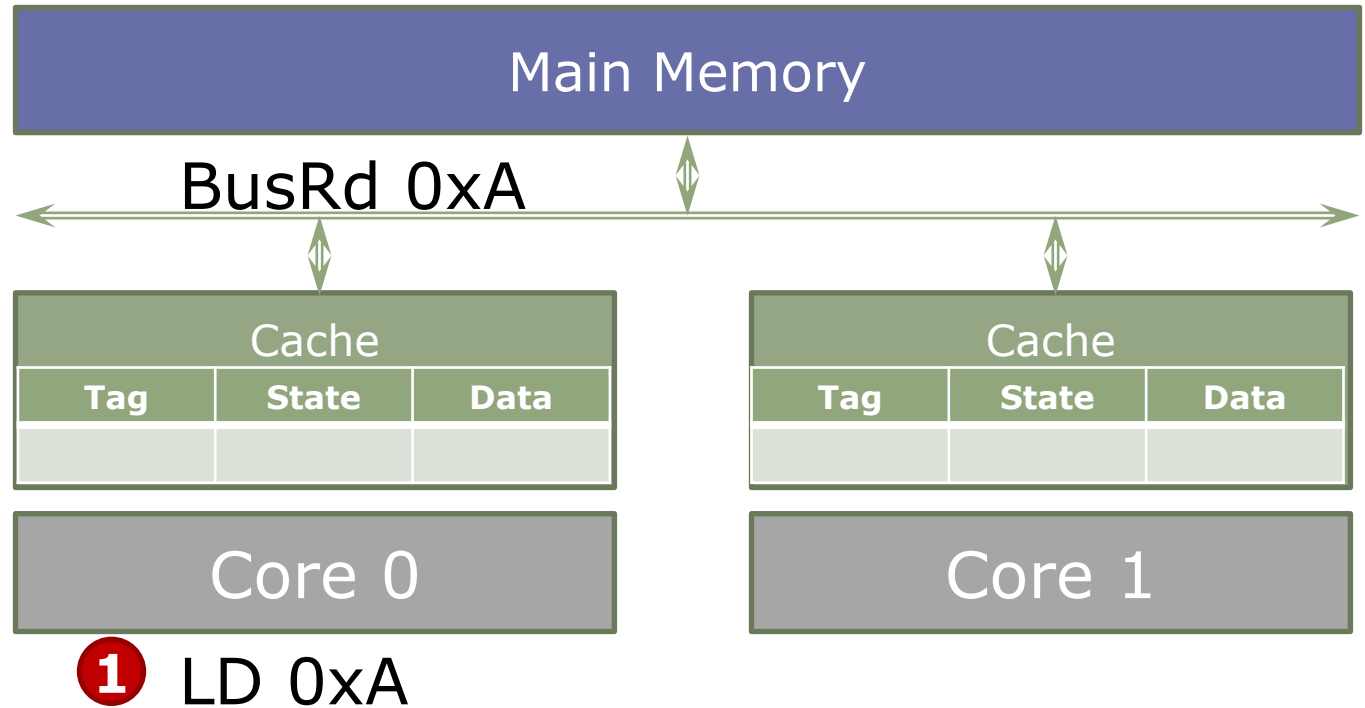
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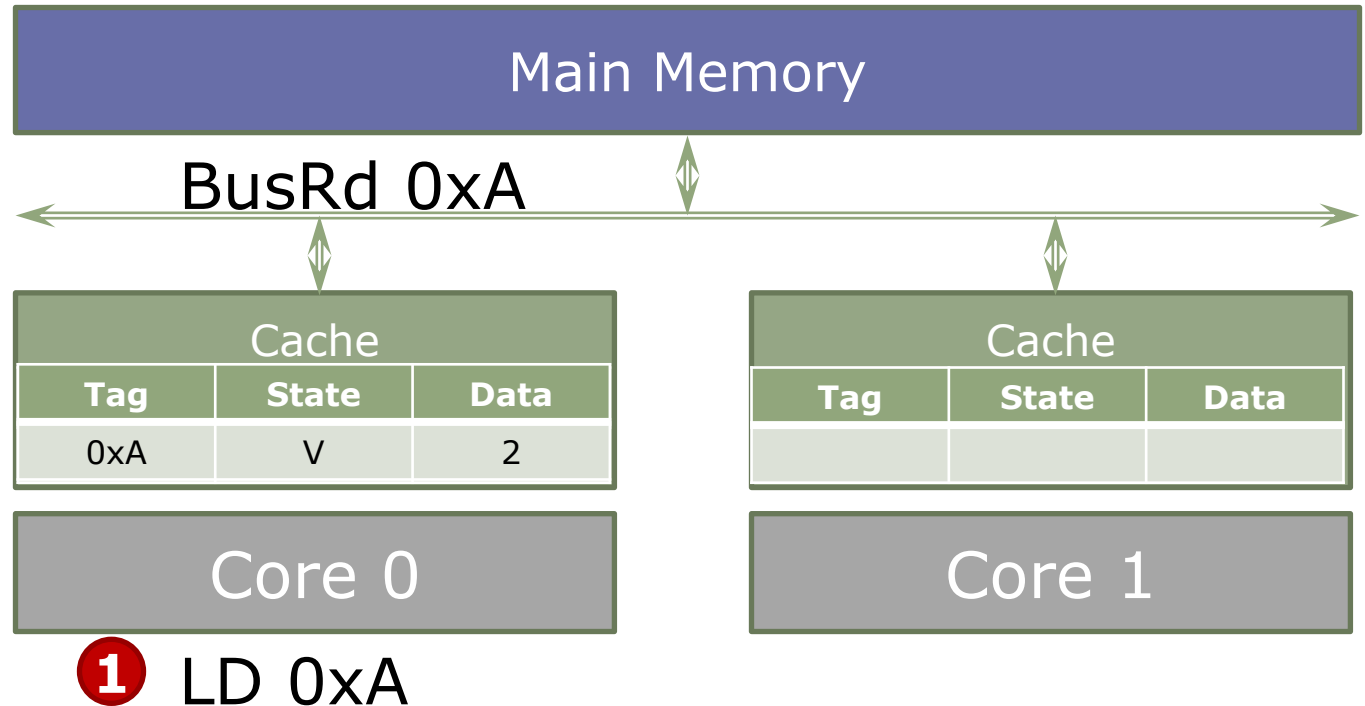


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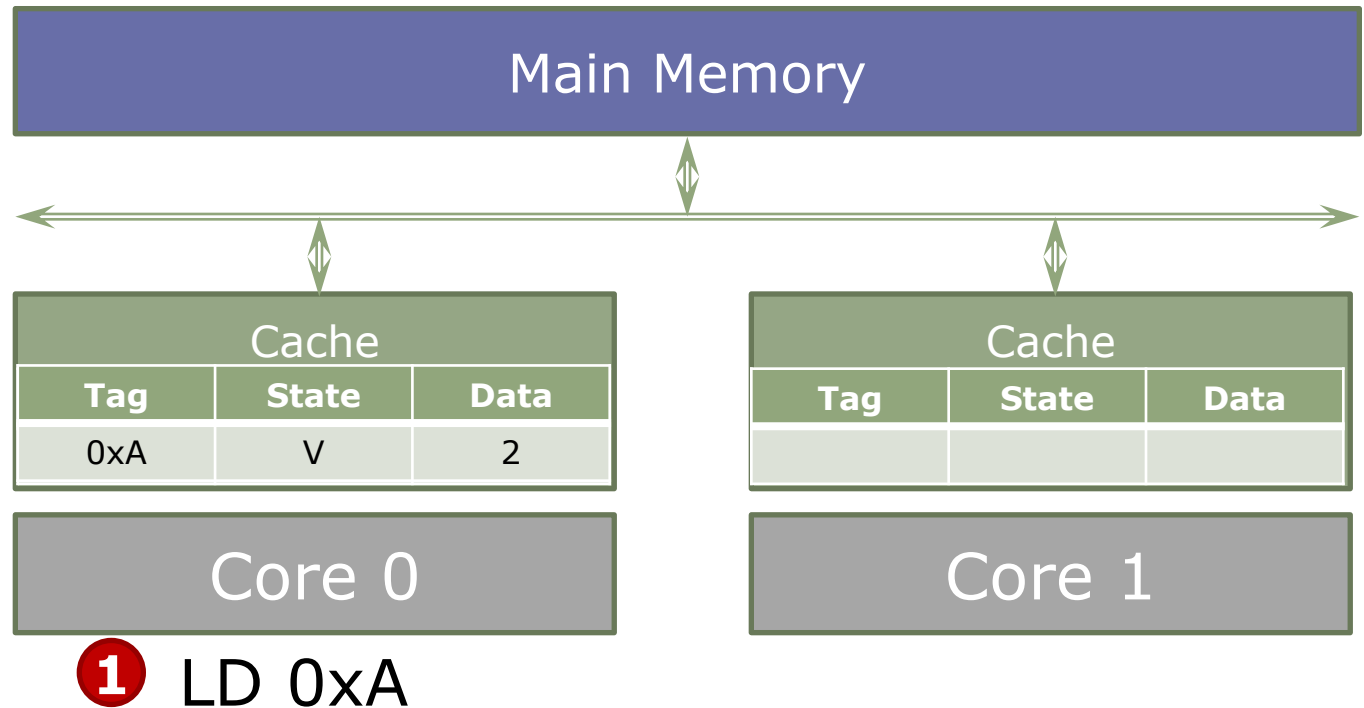
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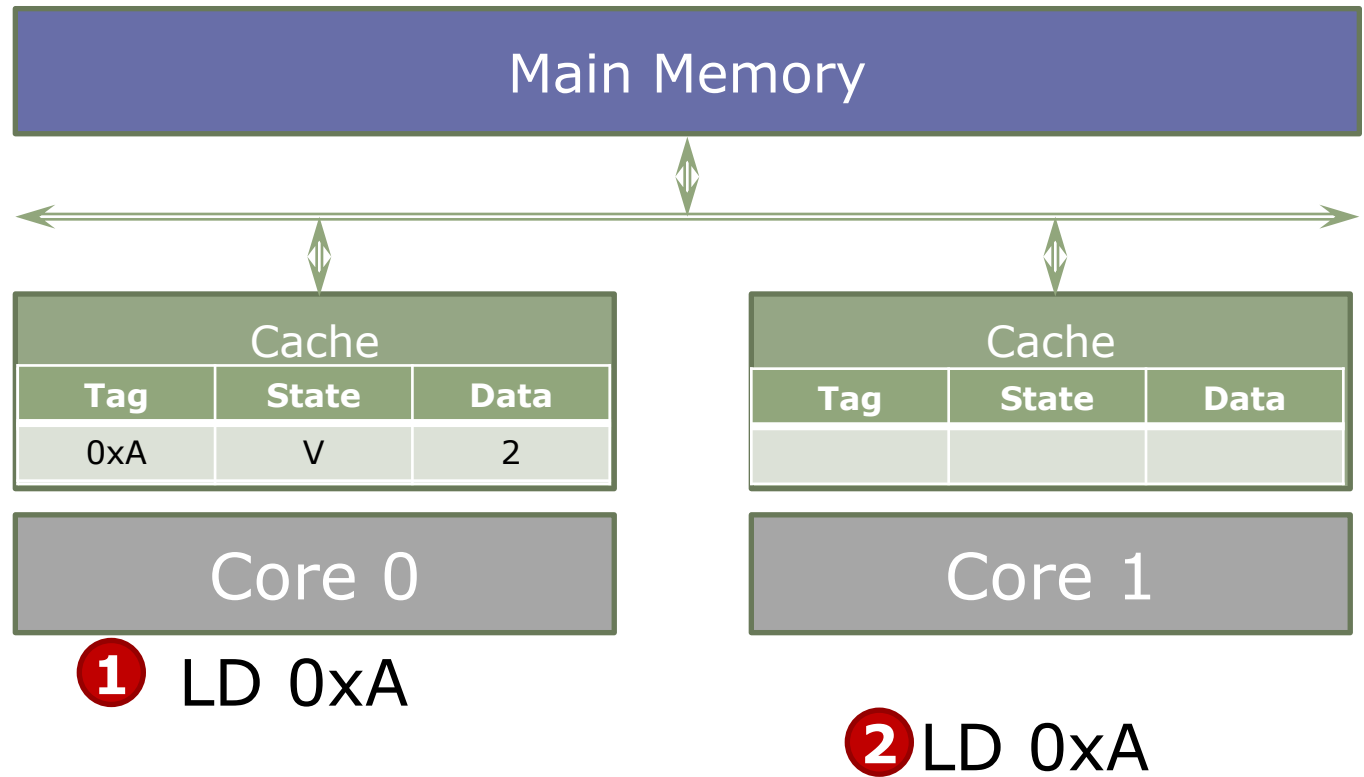
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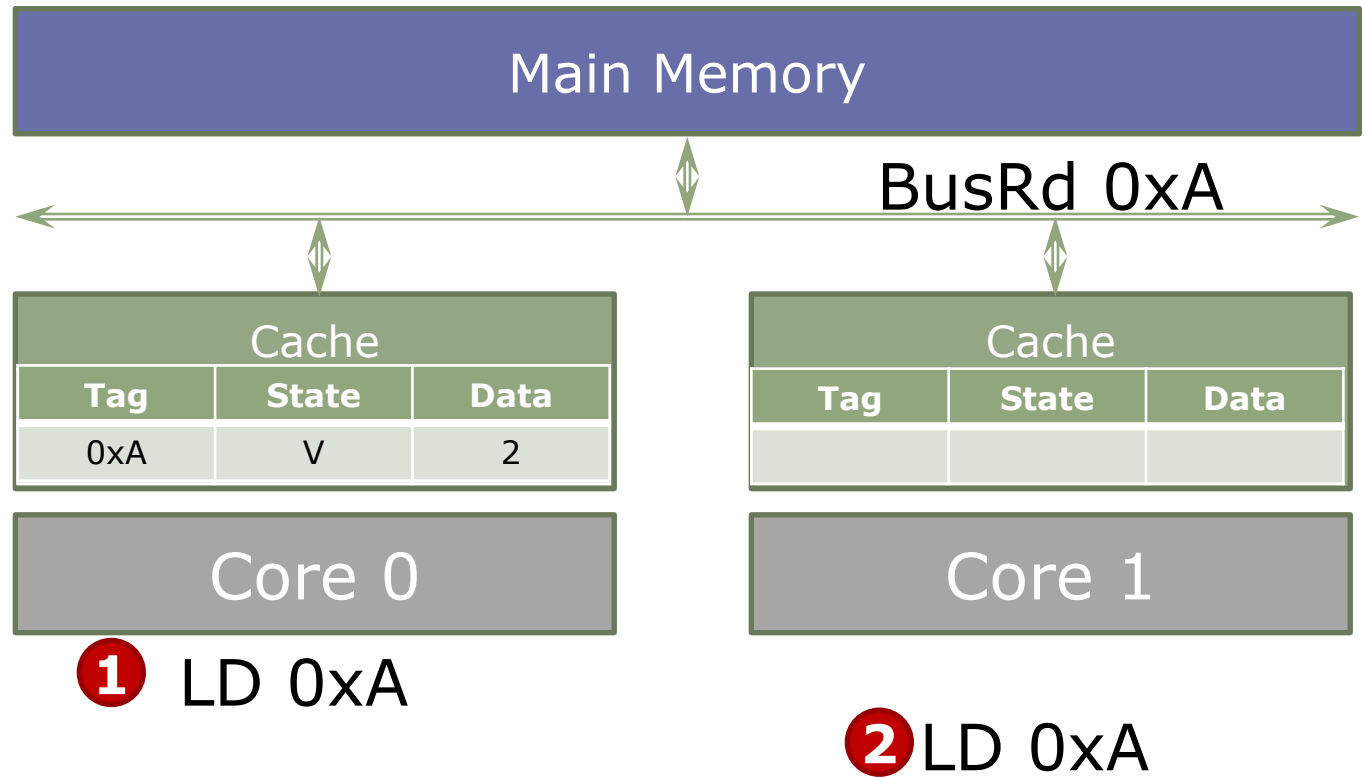
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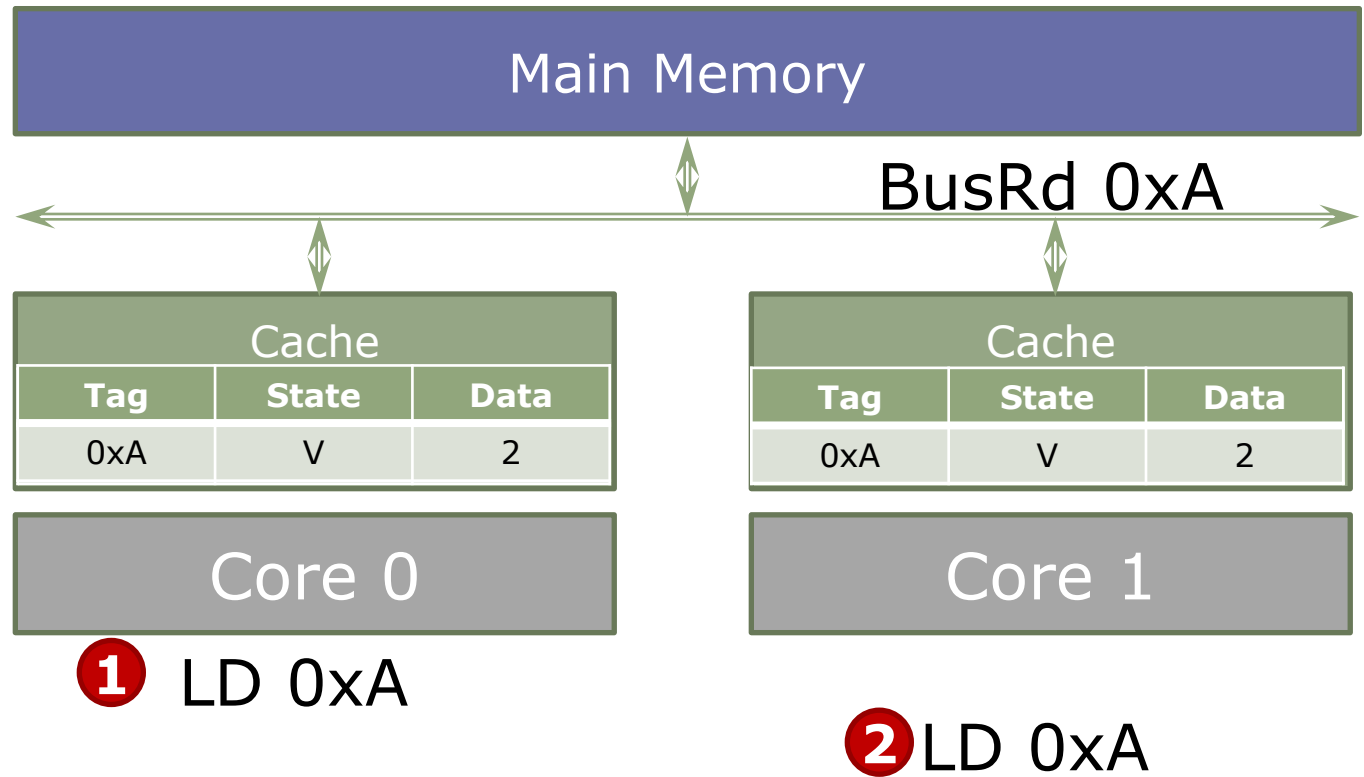


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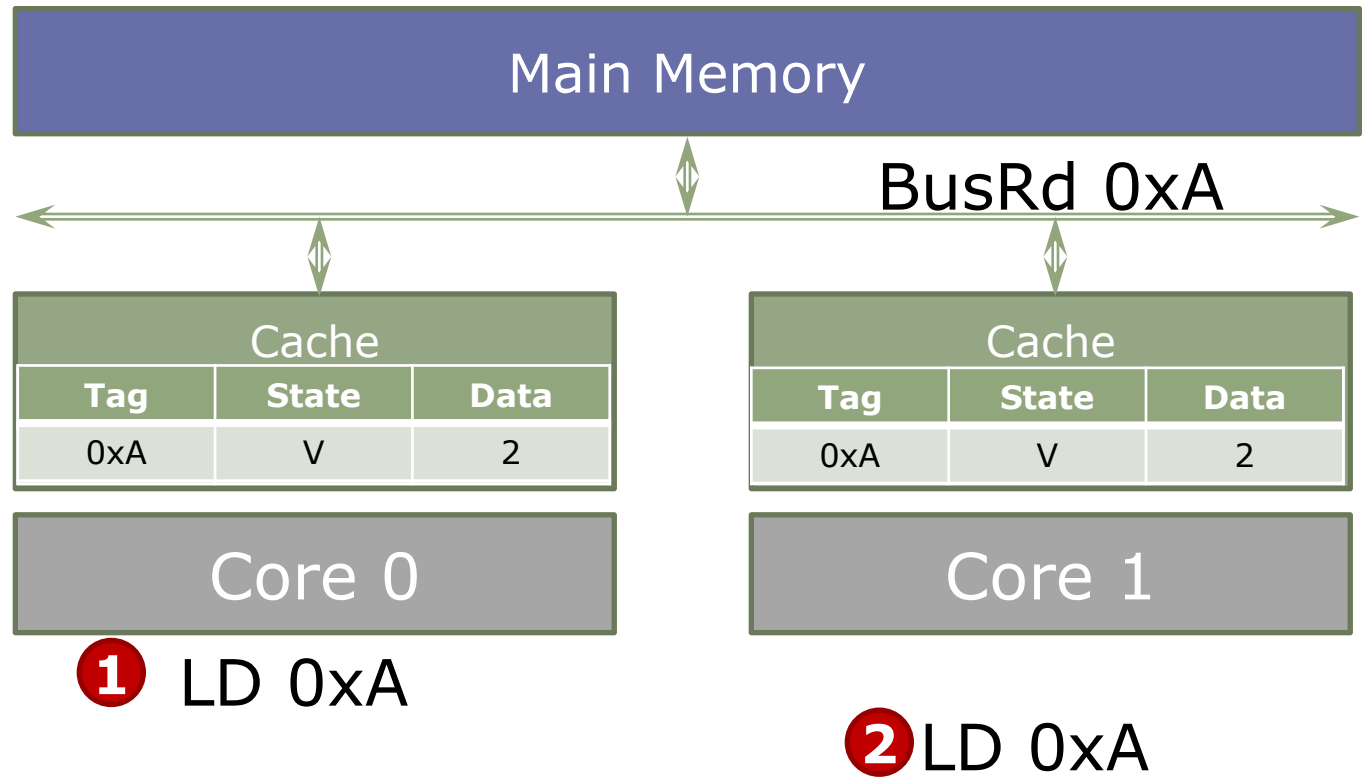




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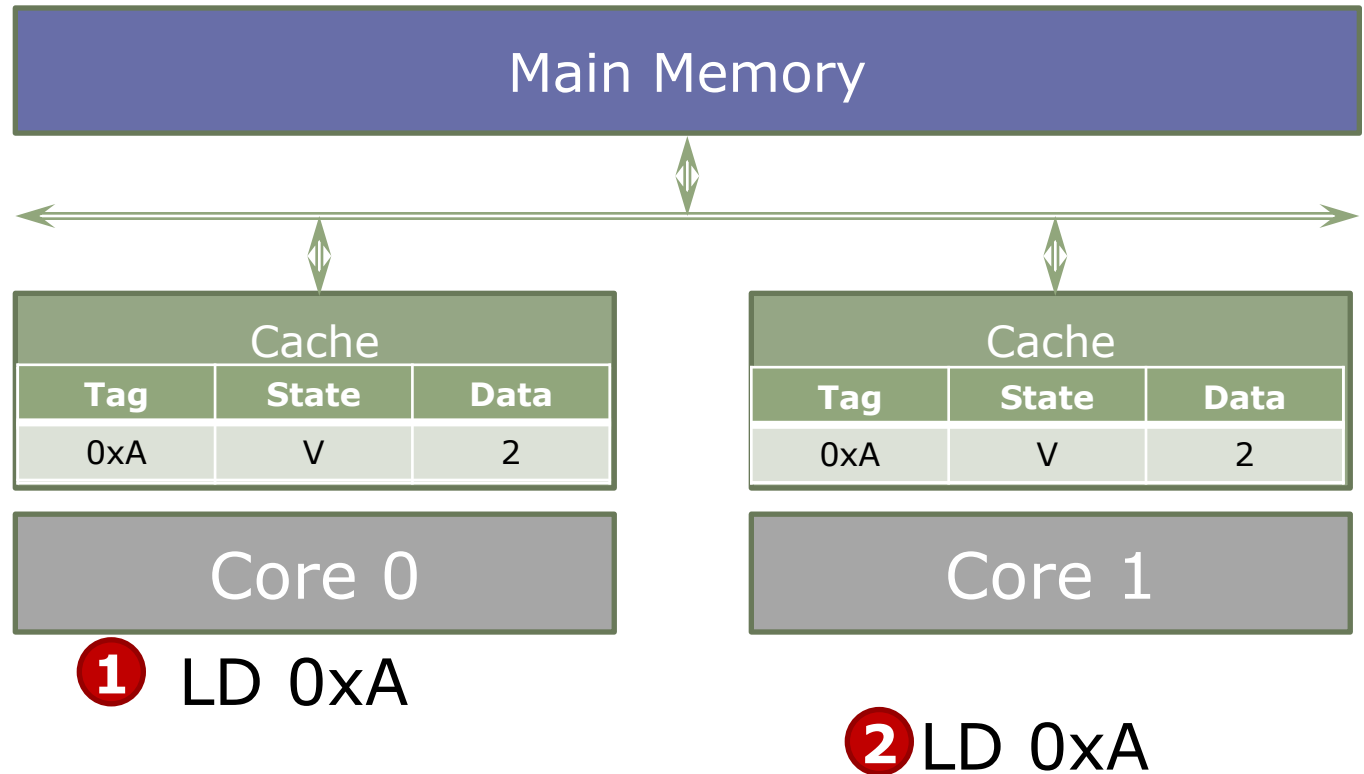


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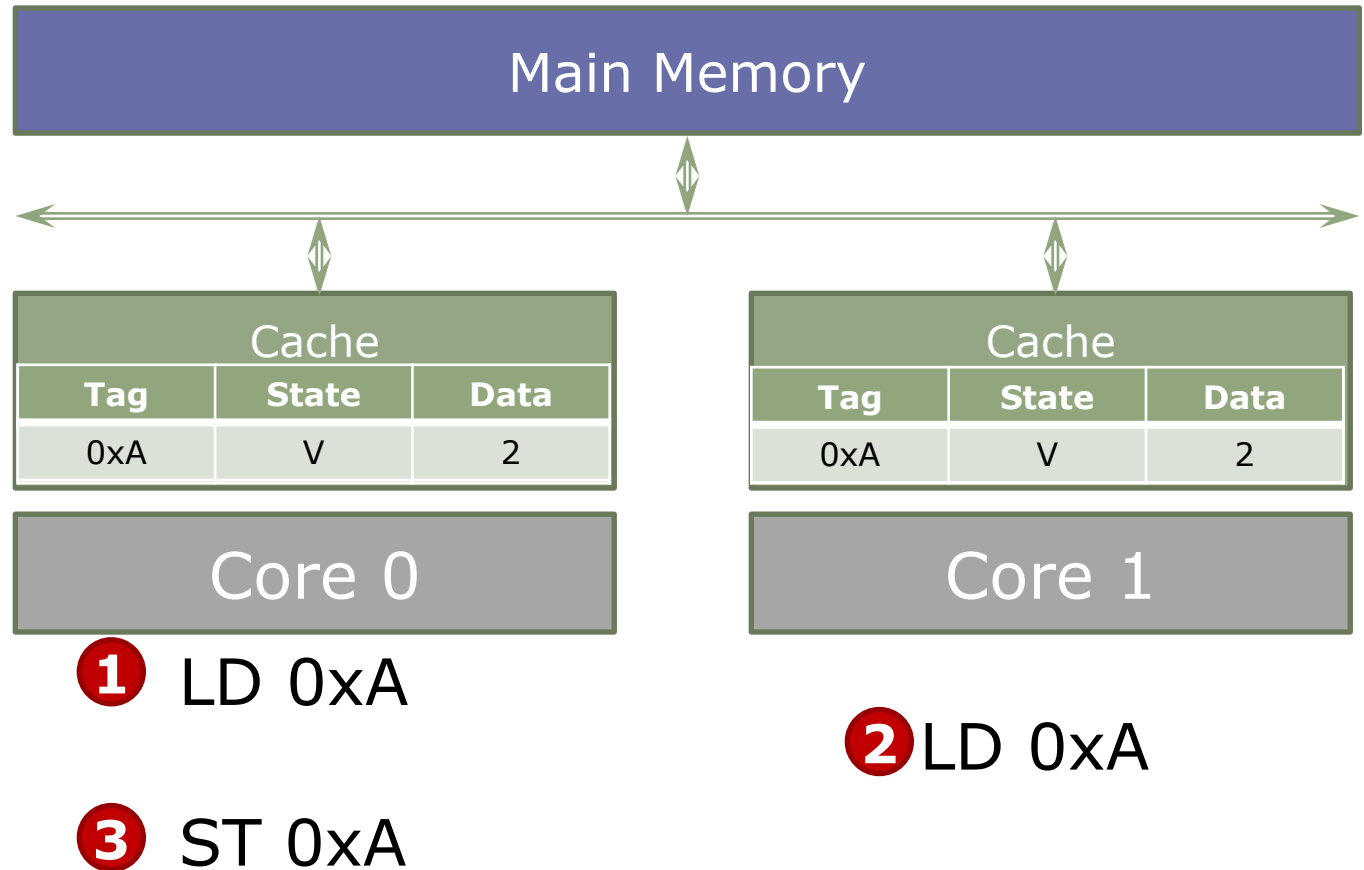


Additional loads satisfied locally, without BusRd

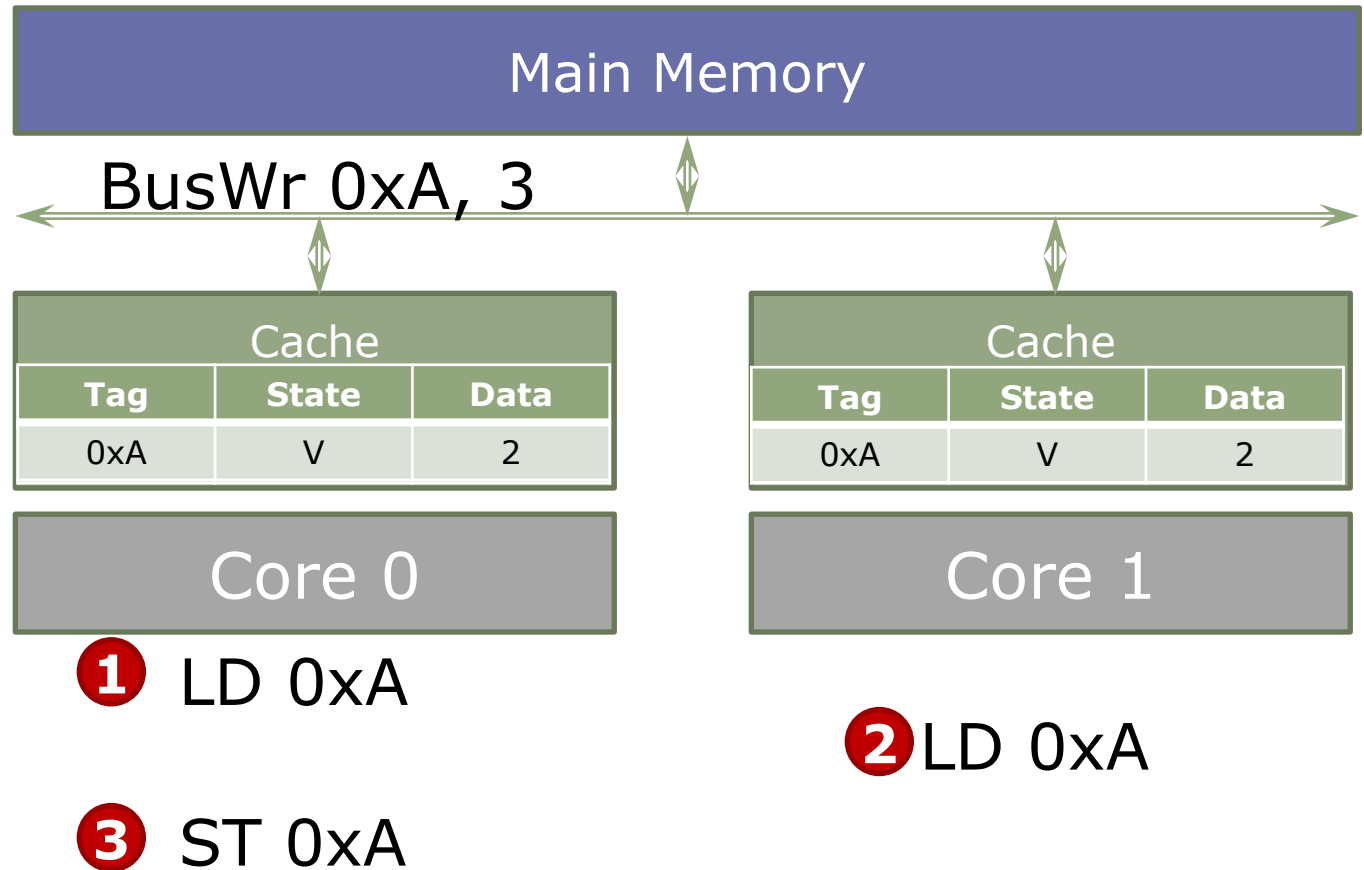
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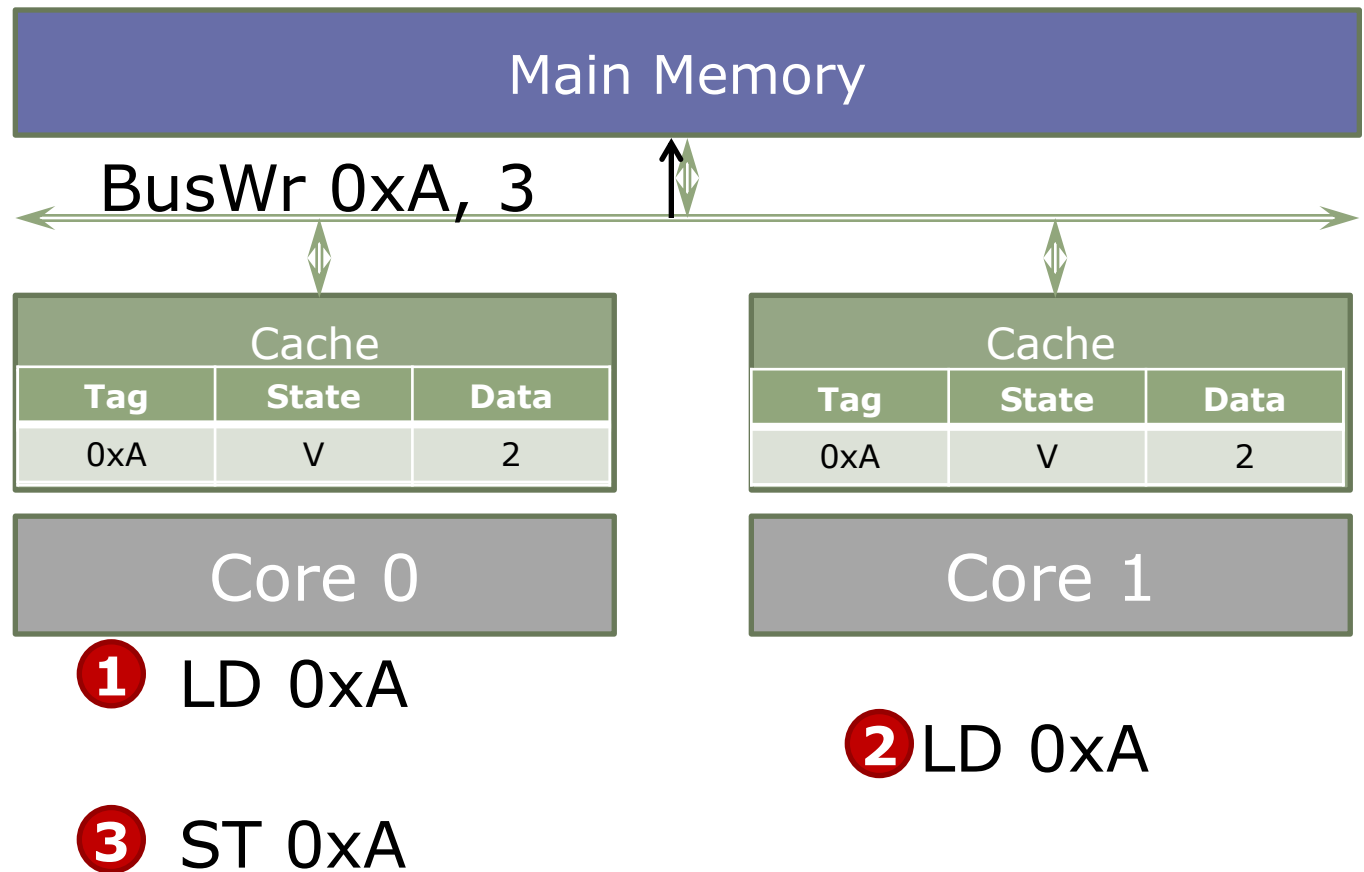
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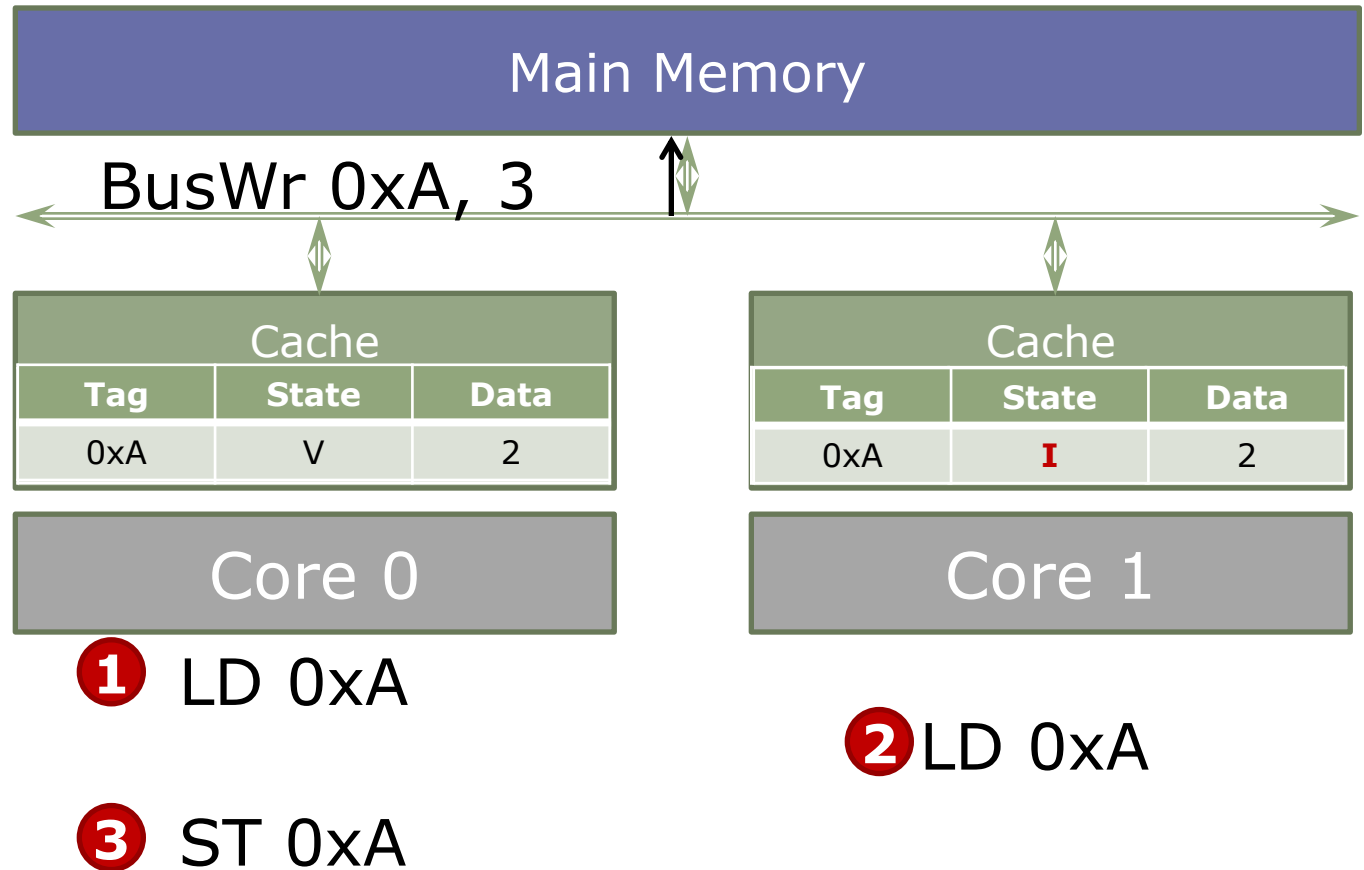
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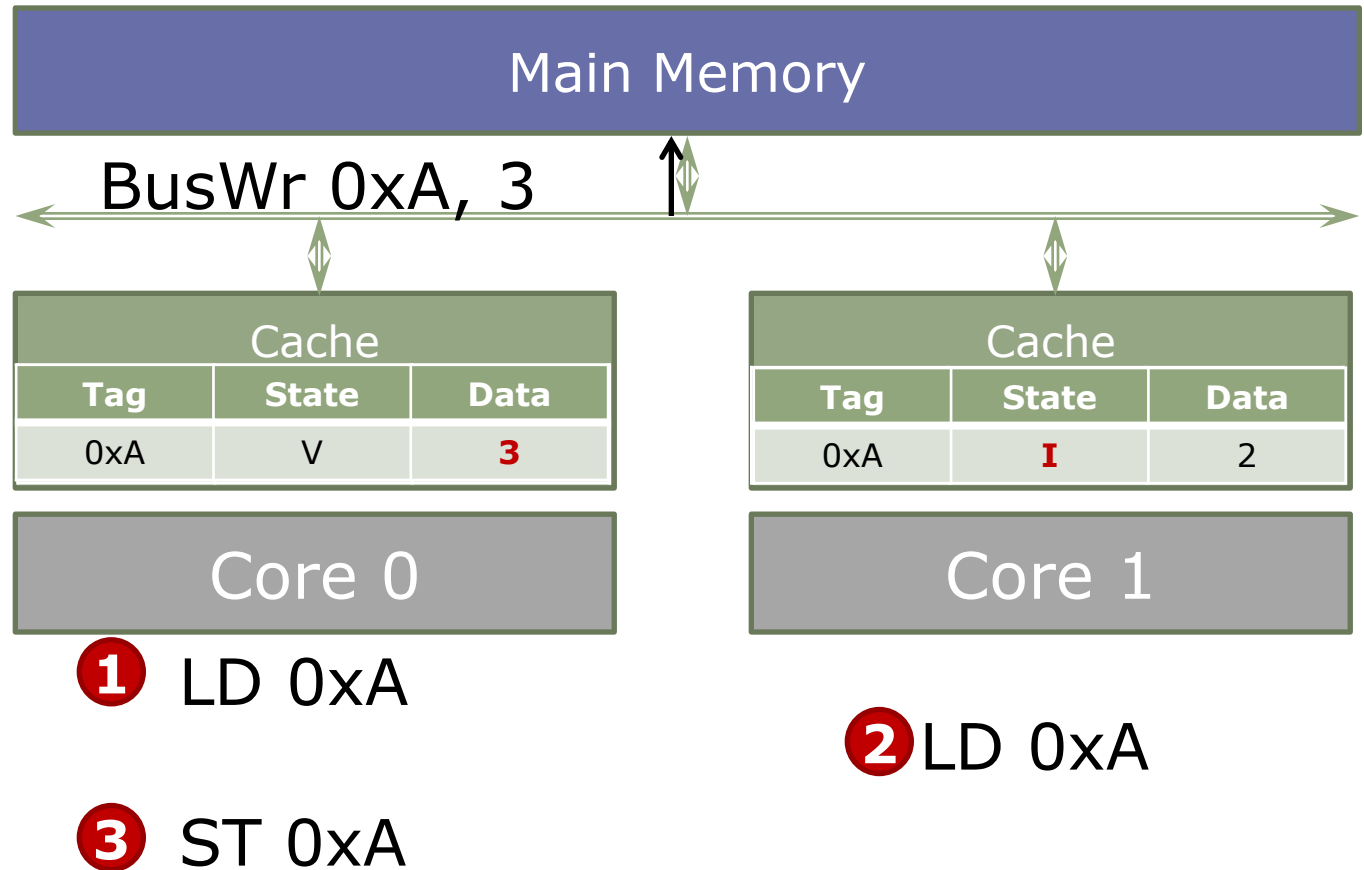
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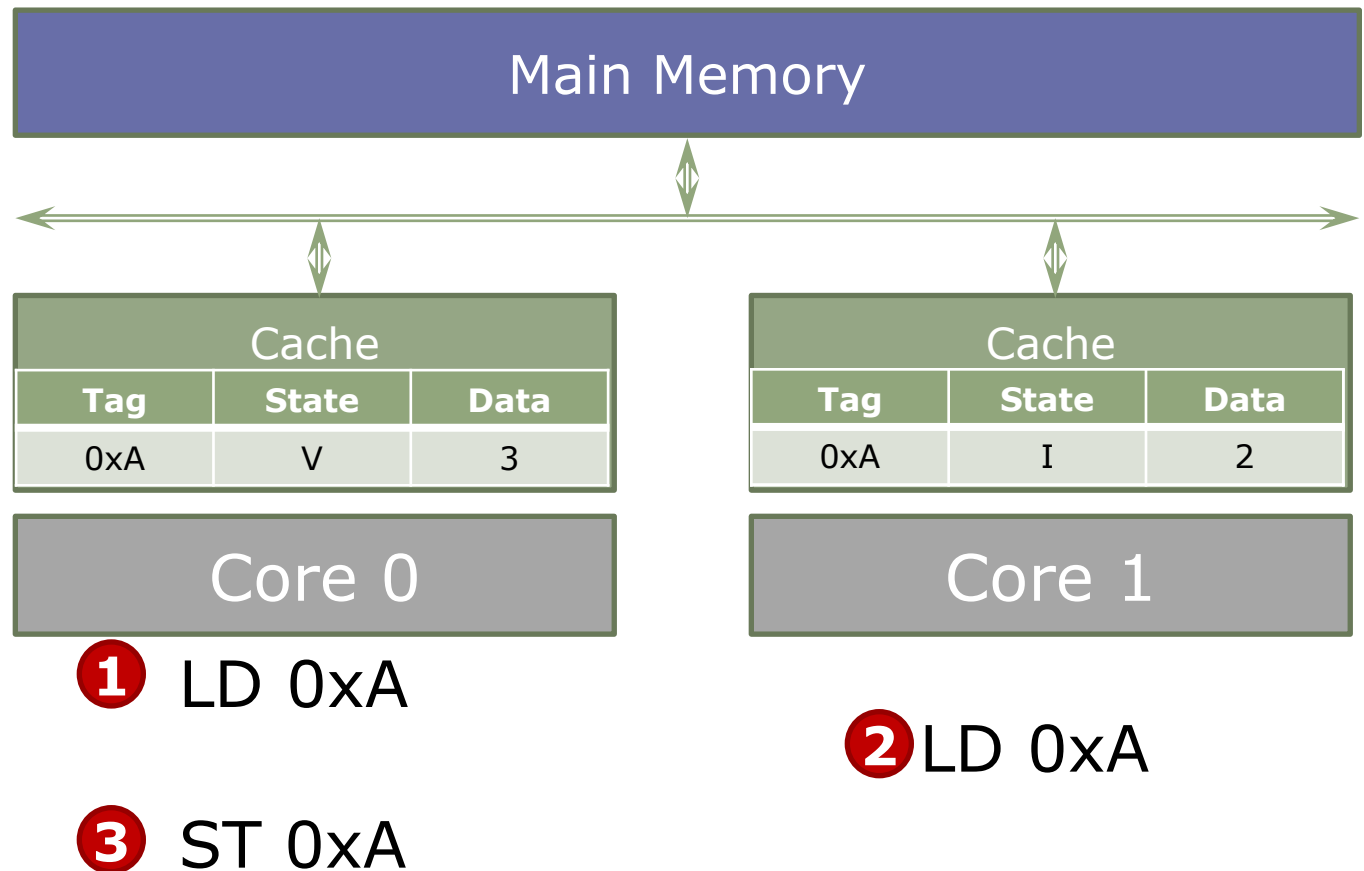


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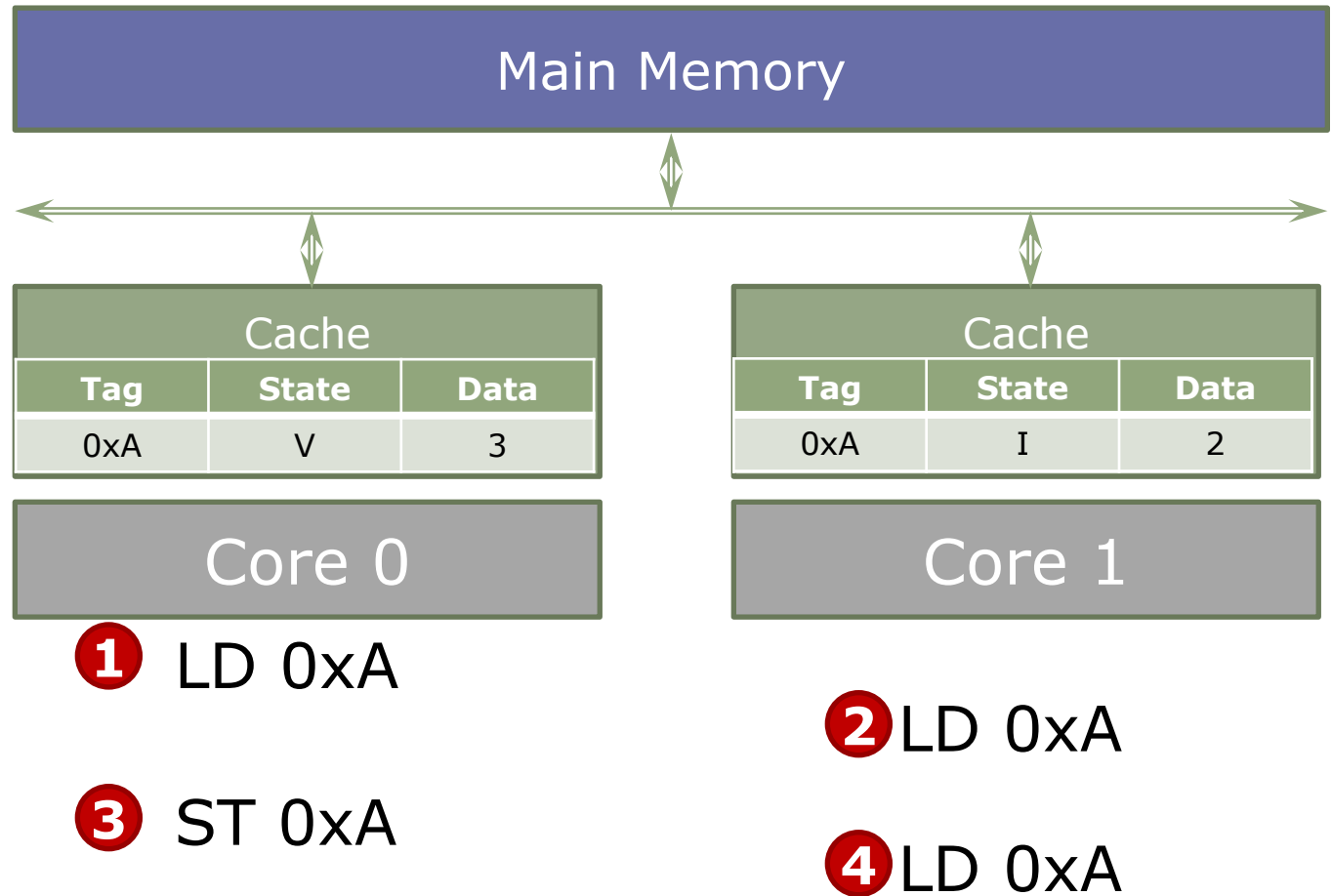




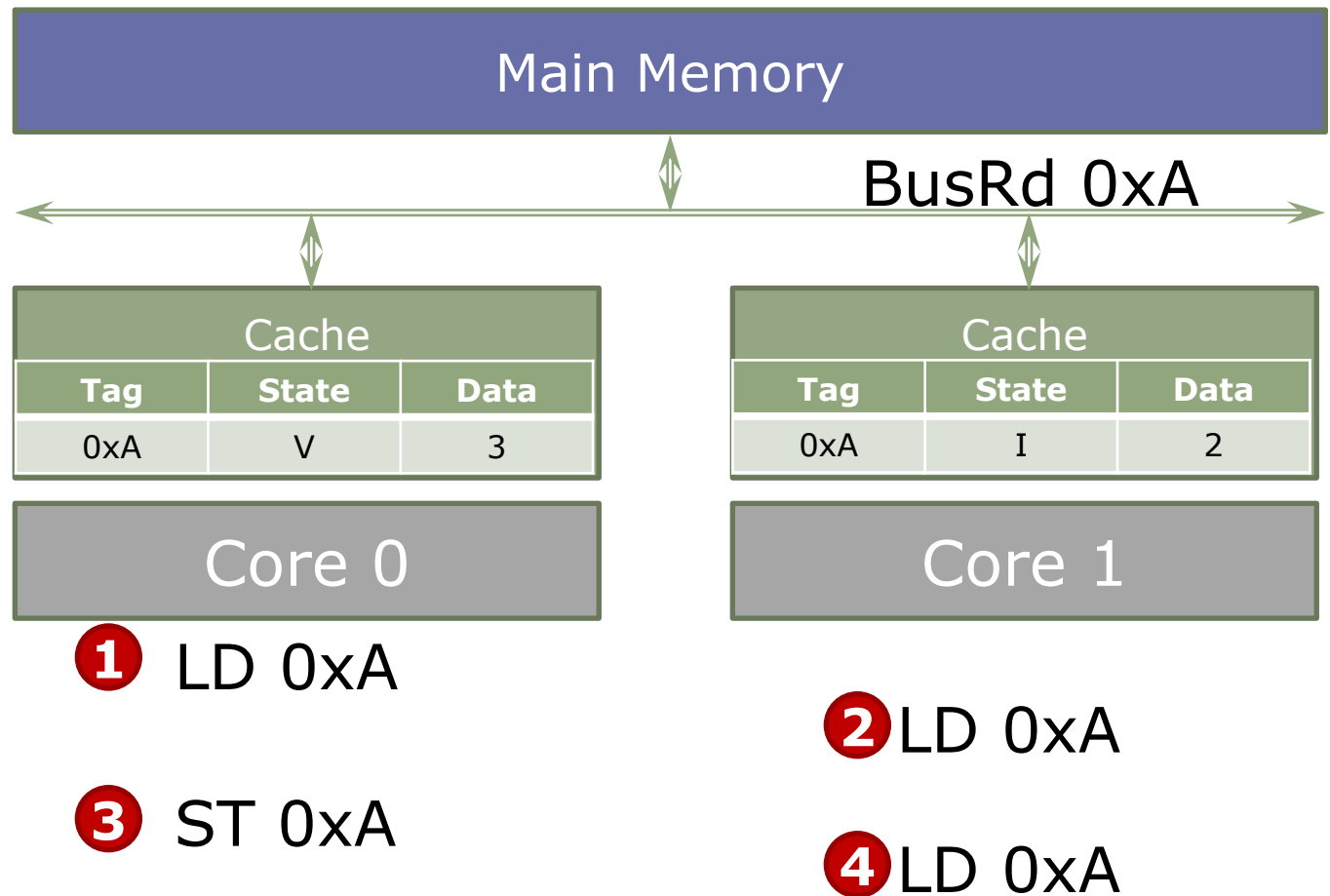
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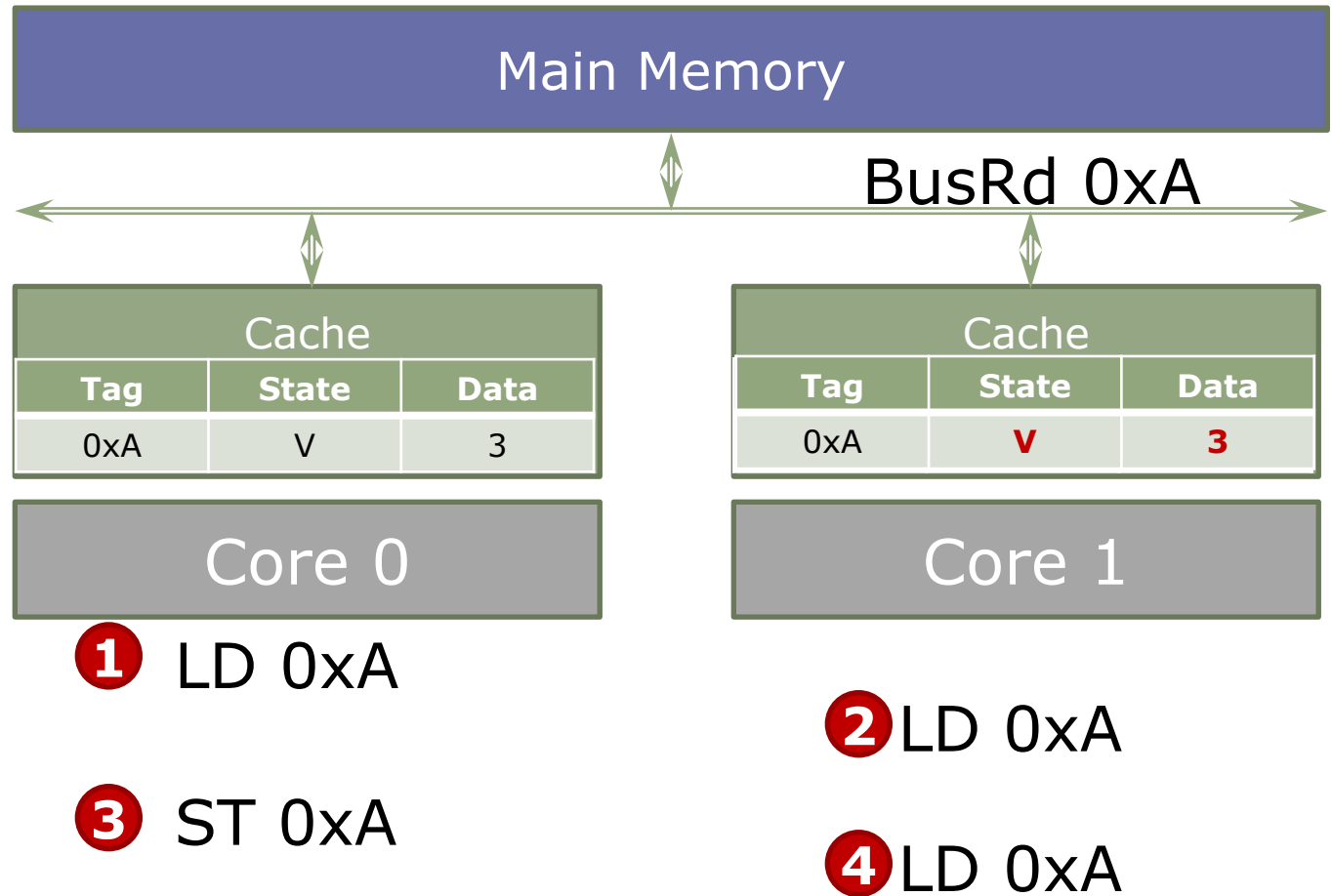
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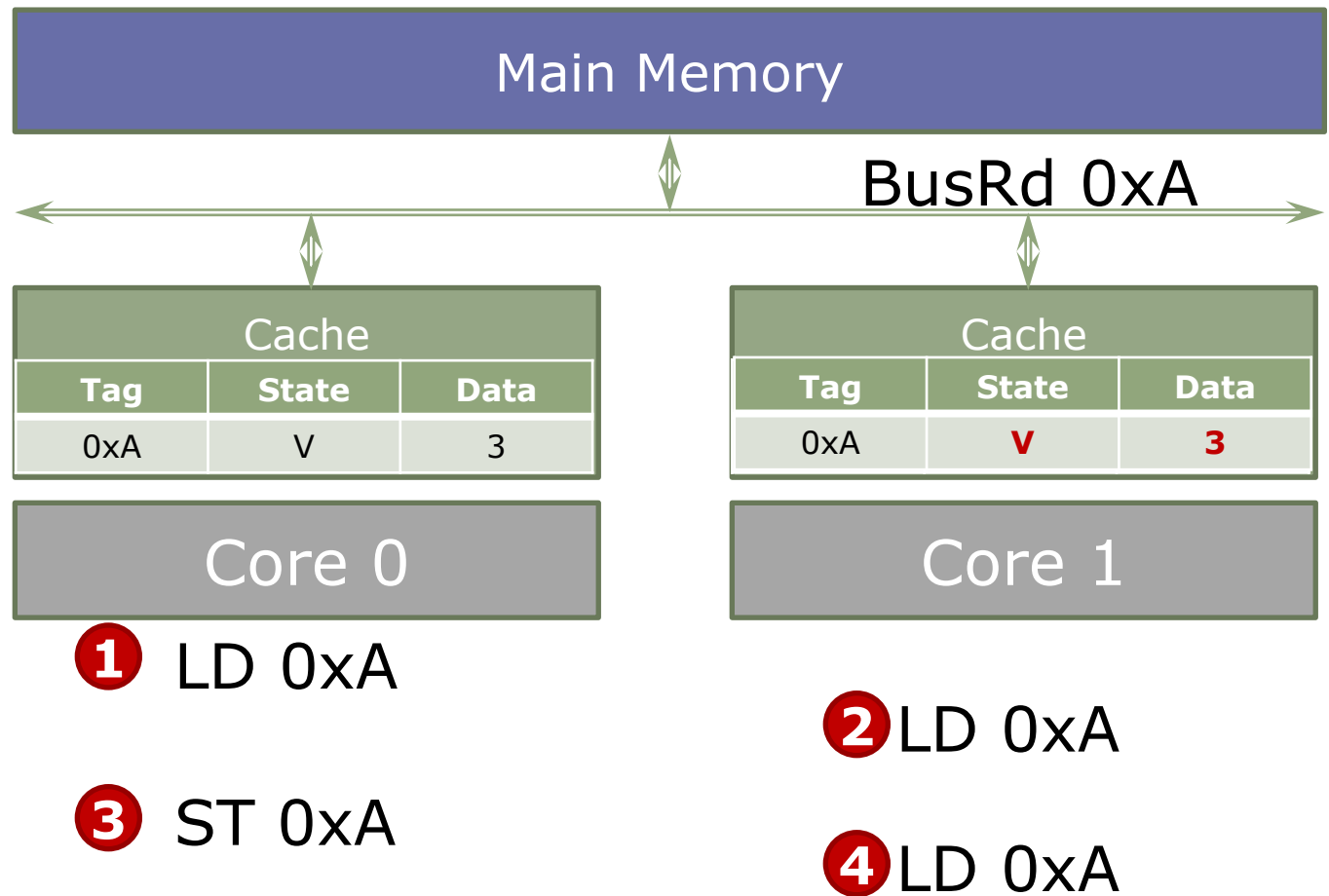
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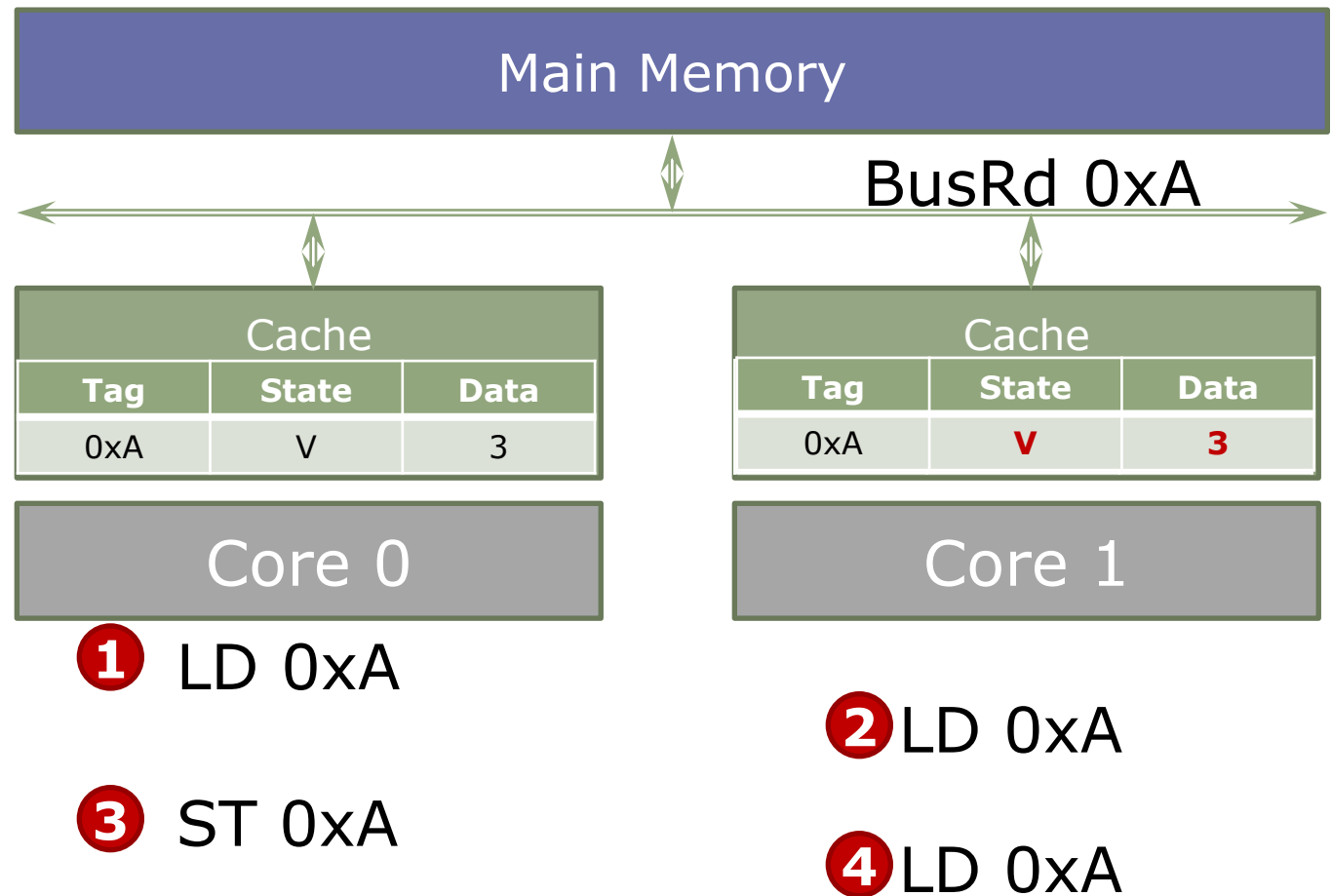


# Valid/Invalid Example



VI Problems?

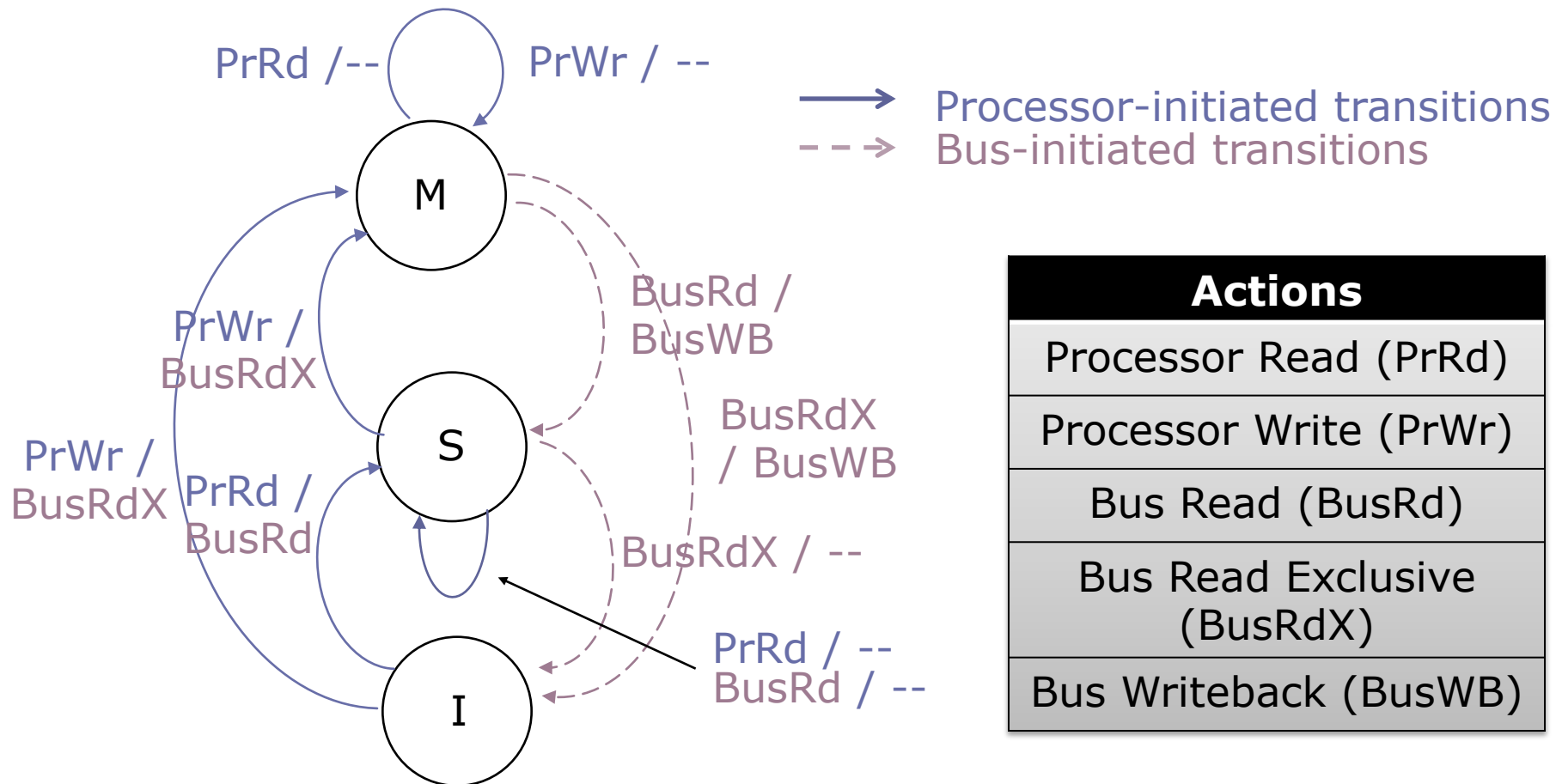
# Valid/Invalid Example



VI Problems? **Every write updates main memory**  
**Every write requires broadcast & snoop**

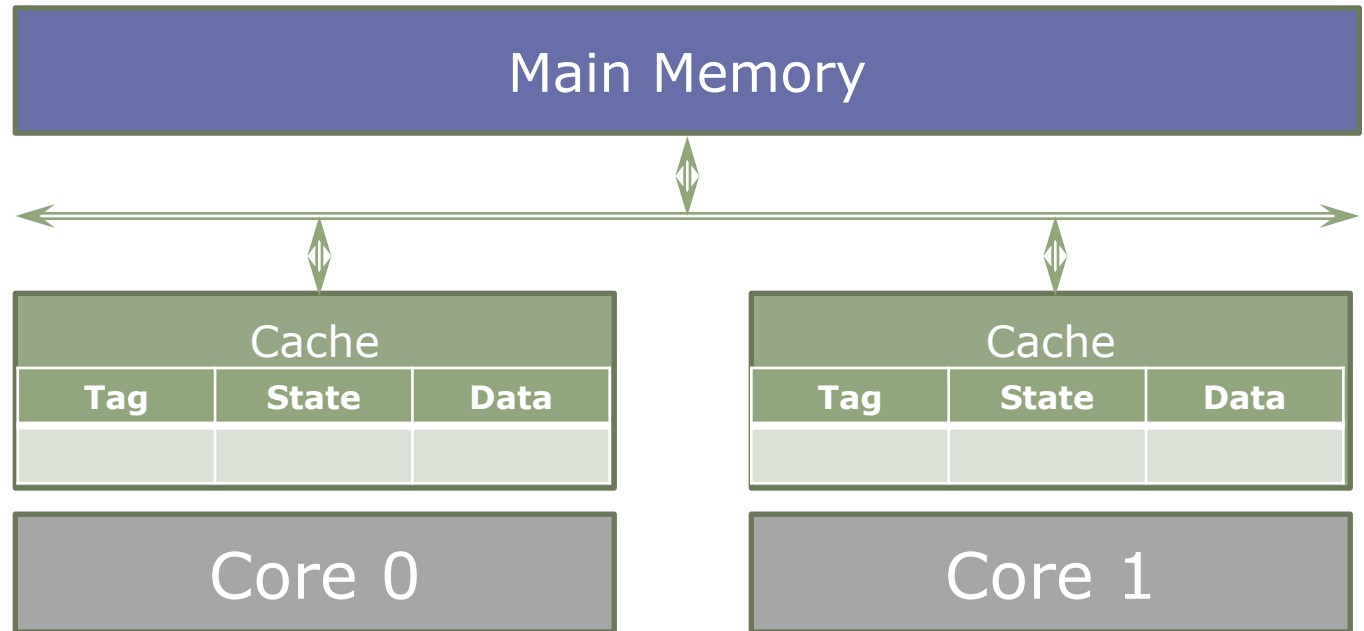
# Modified/Shared/Invalid (MSI) Protocol

- Allows writeback caches + satisfying writes locally



# MSI Example

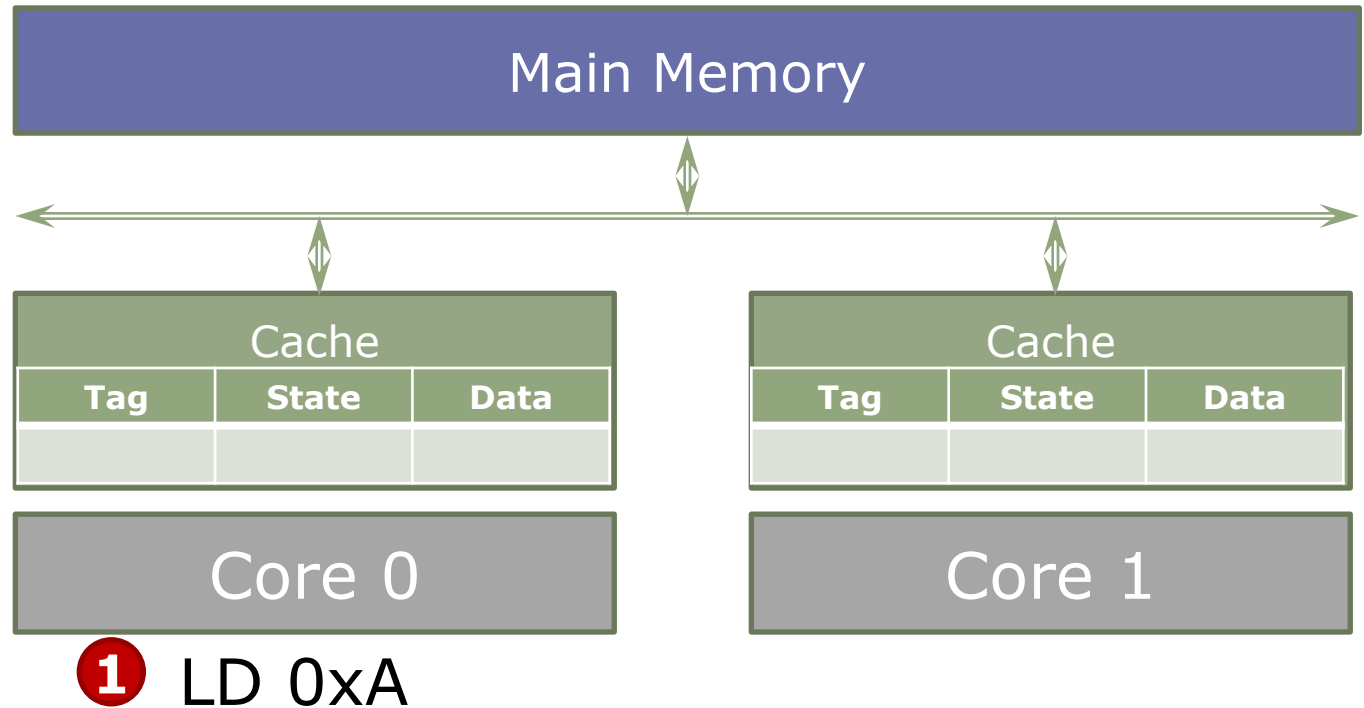
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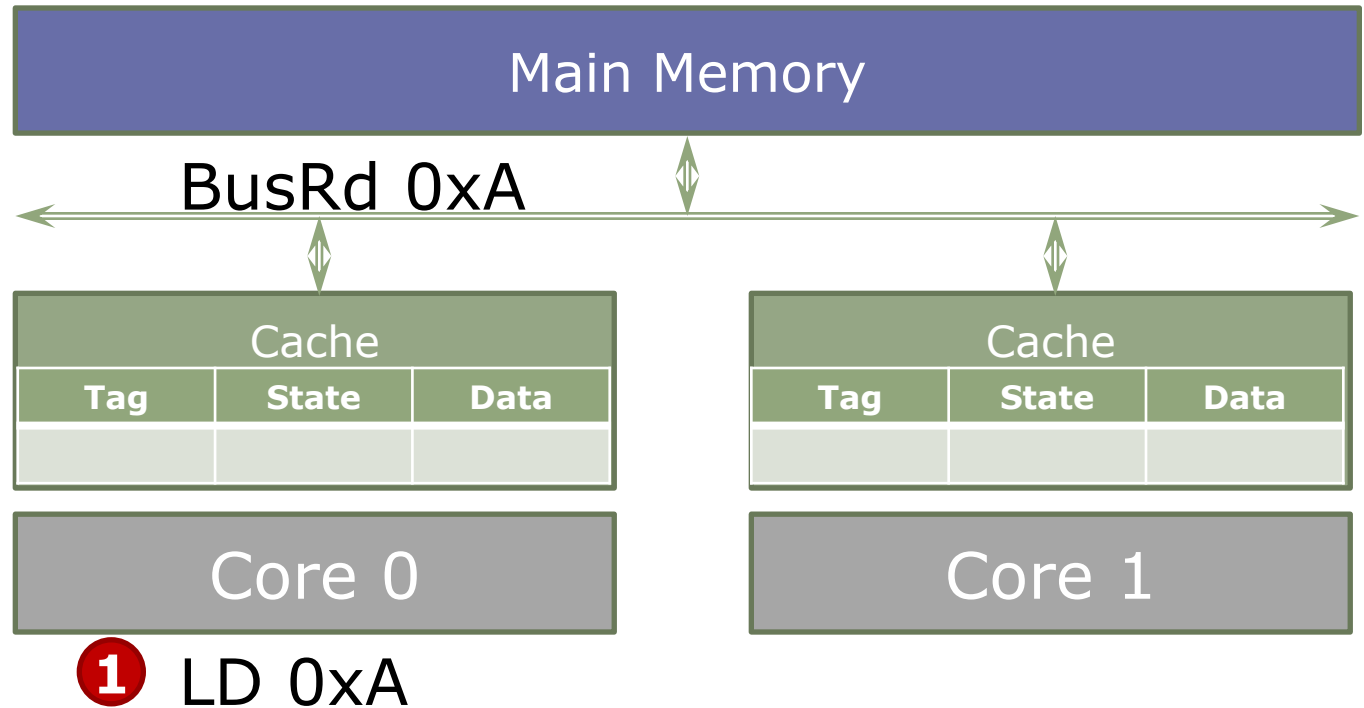


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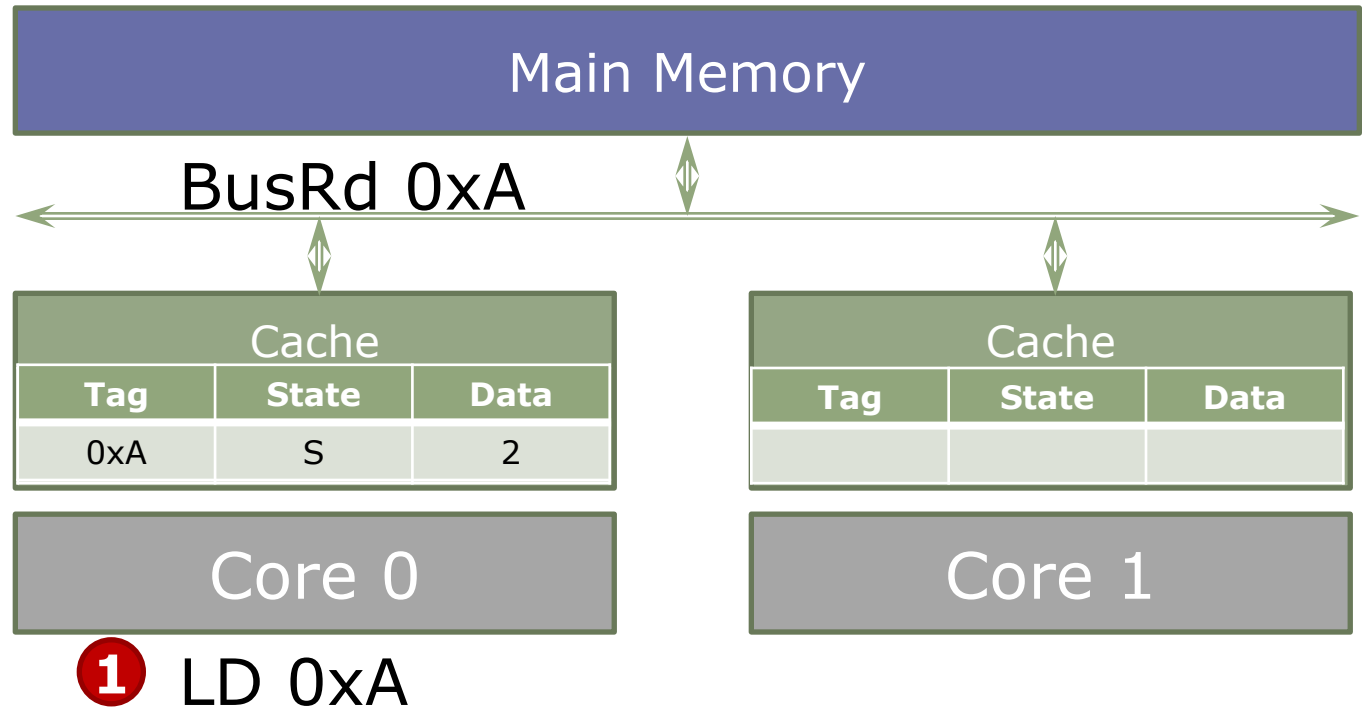
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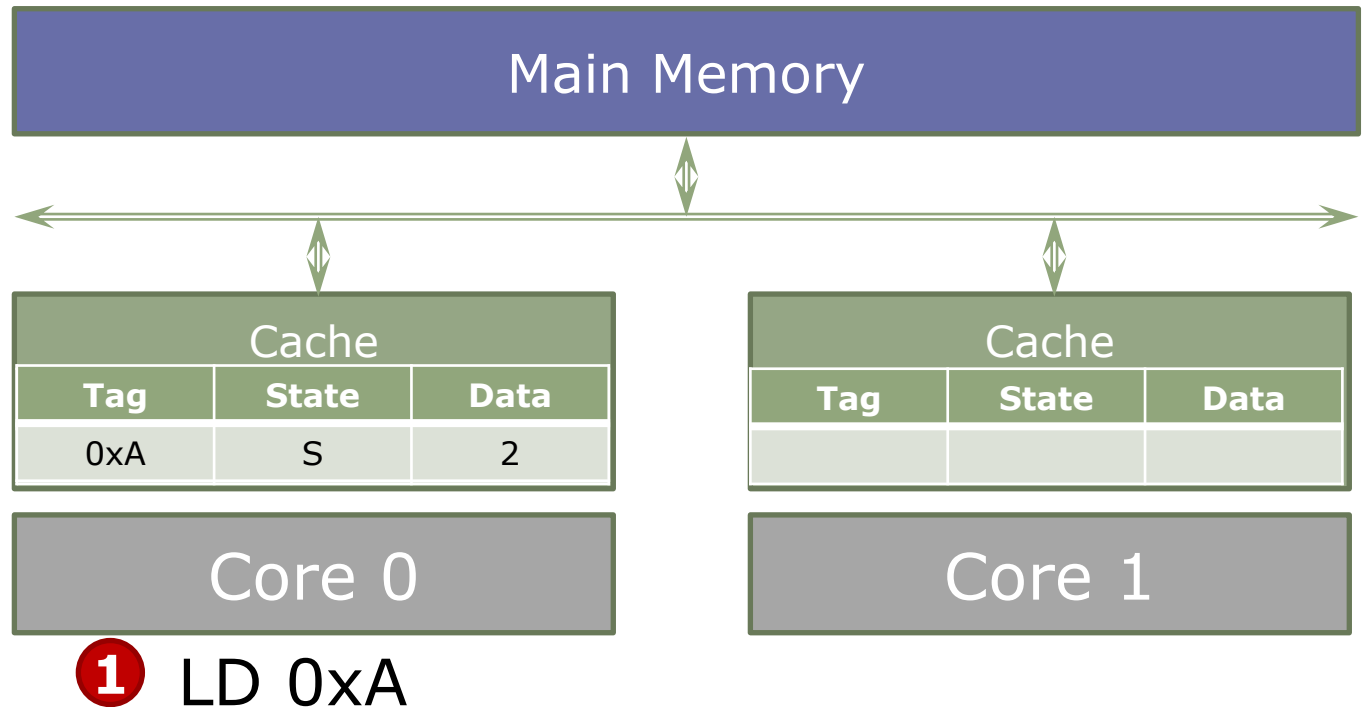
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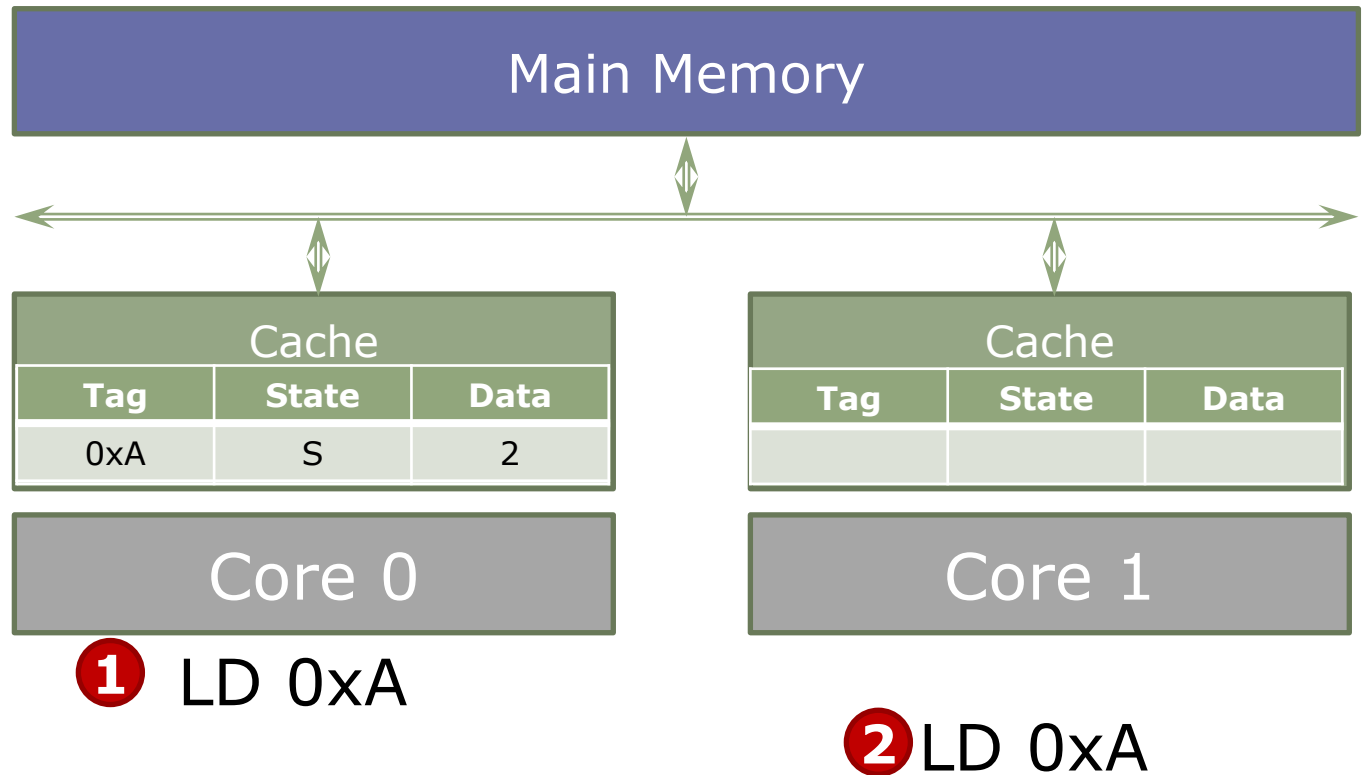
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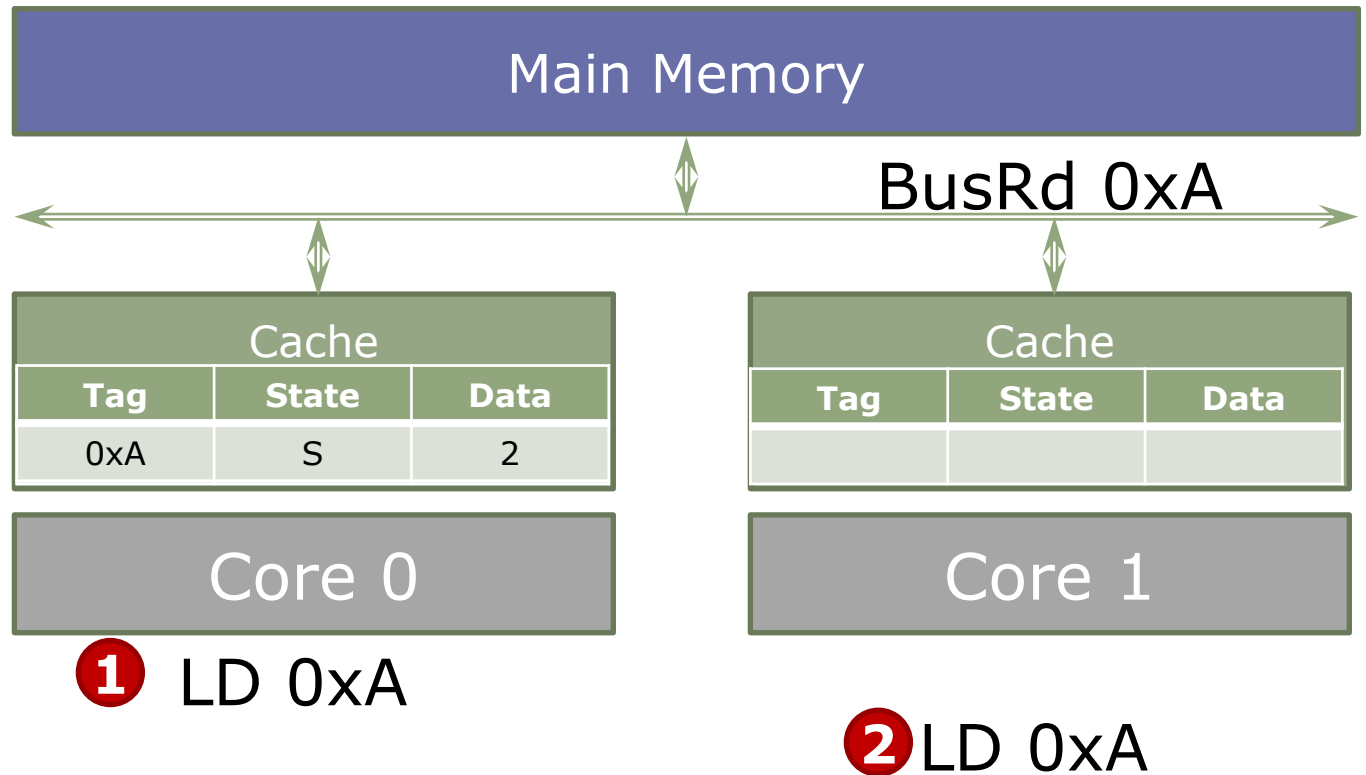
# MSI Example



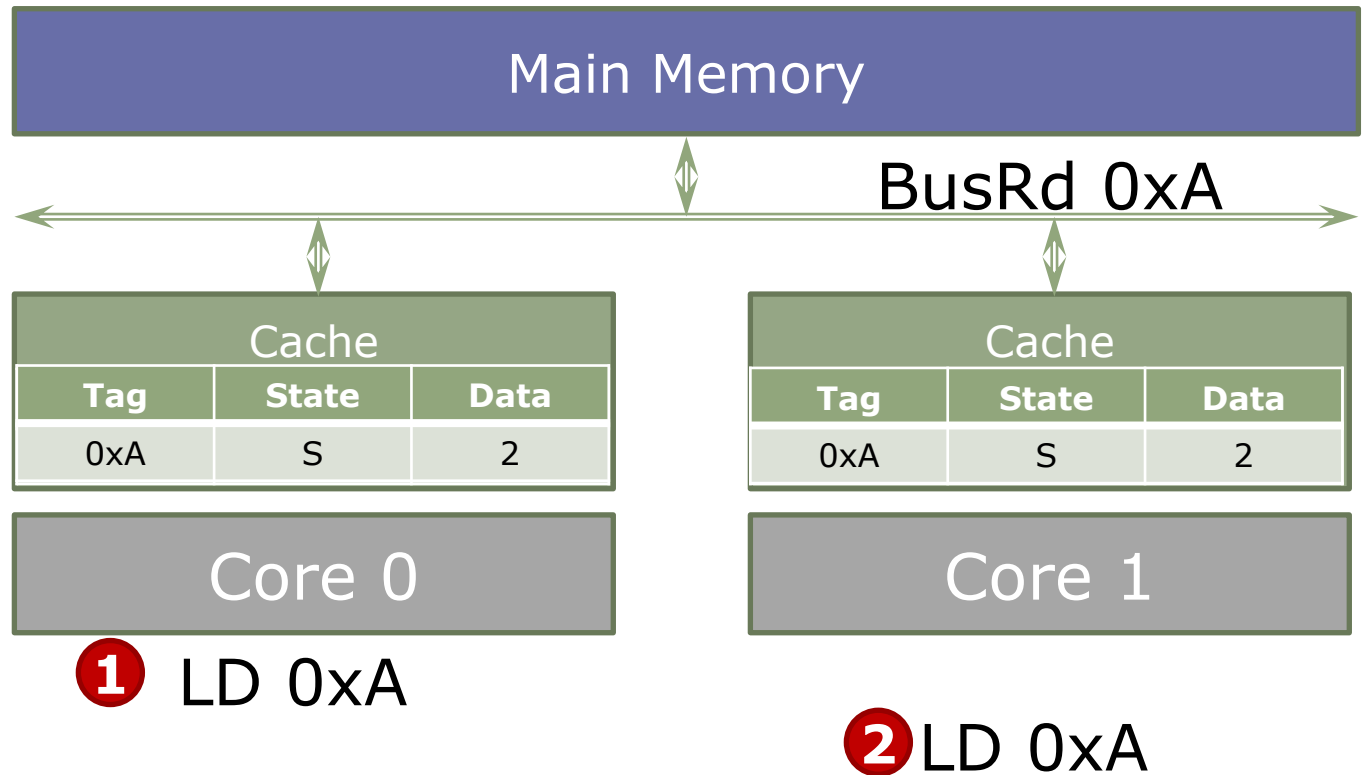
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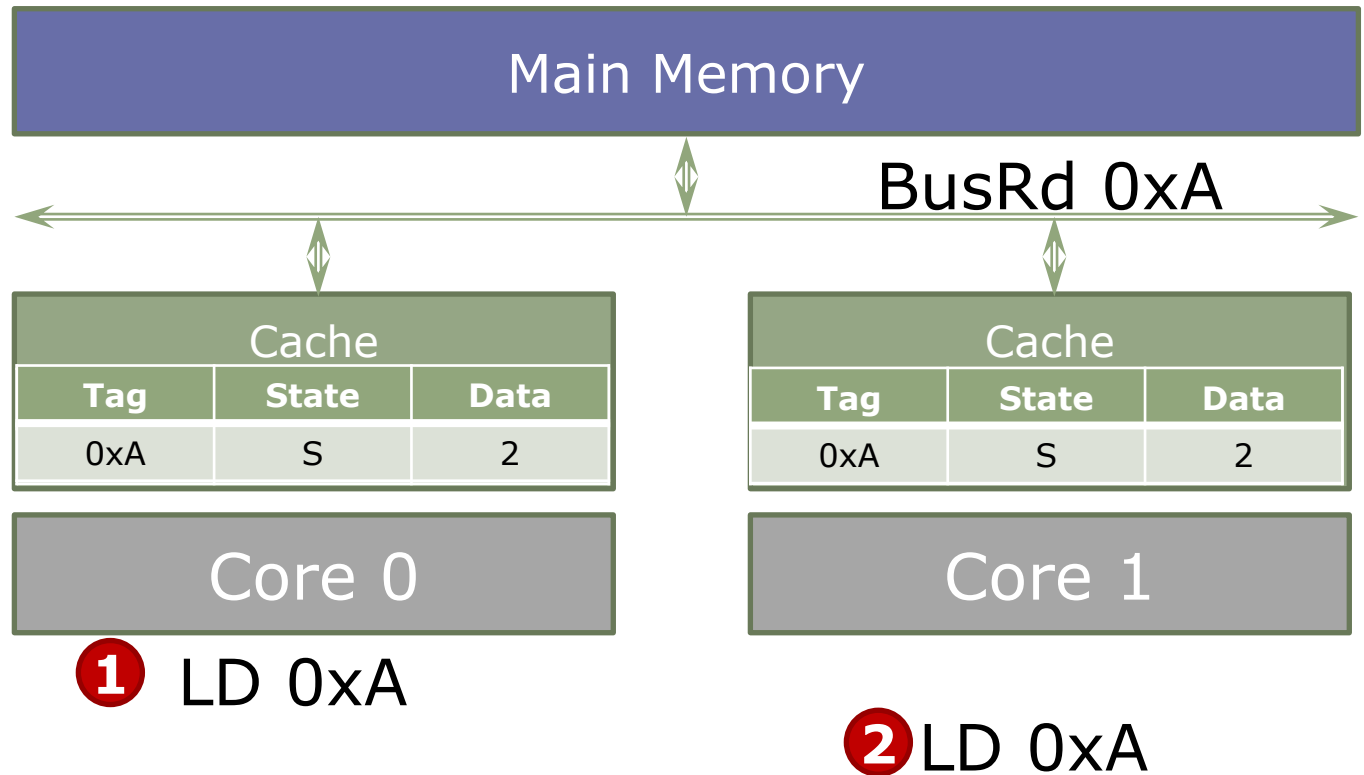
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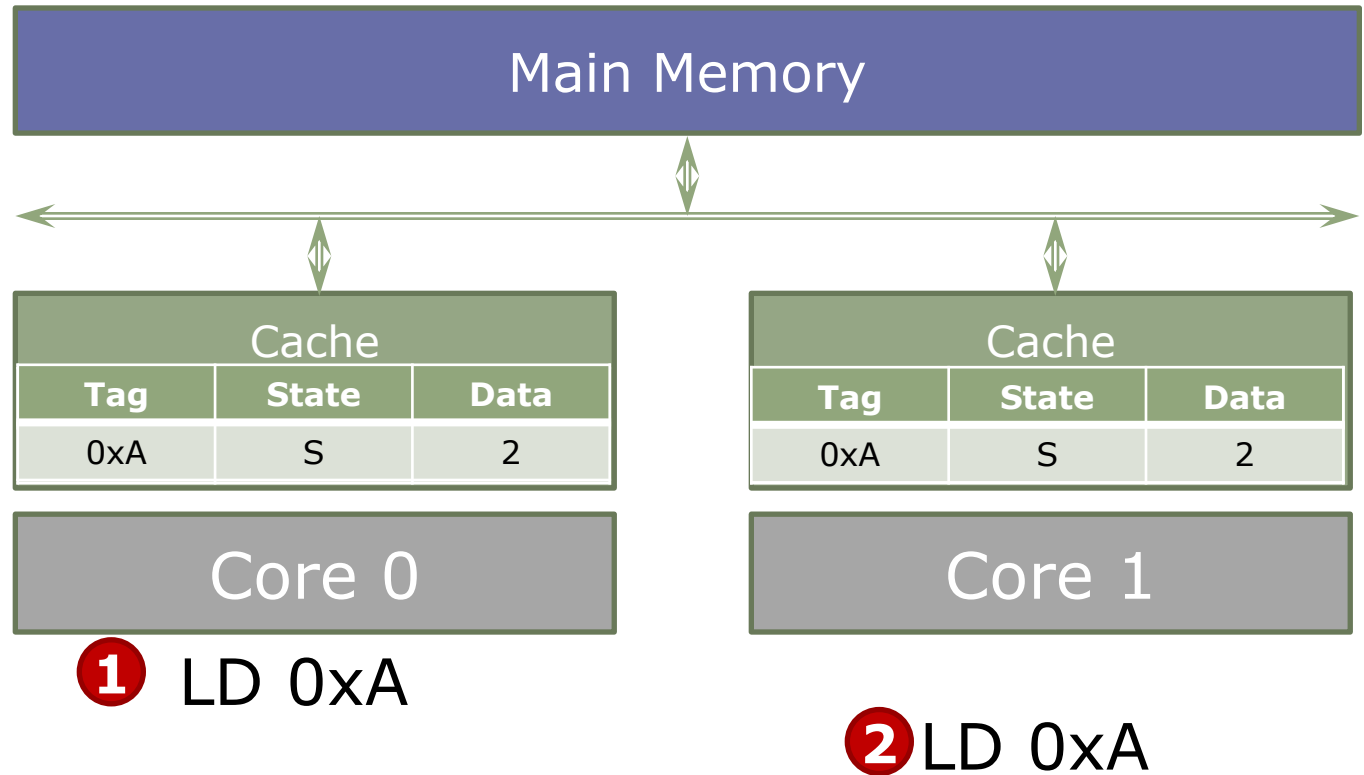
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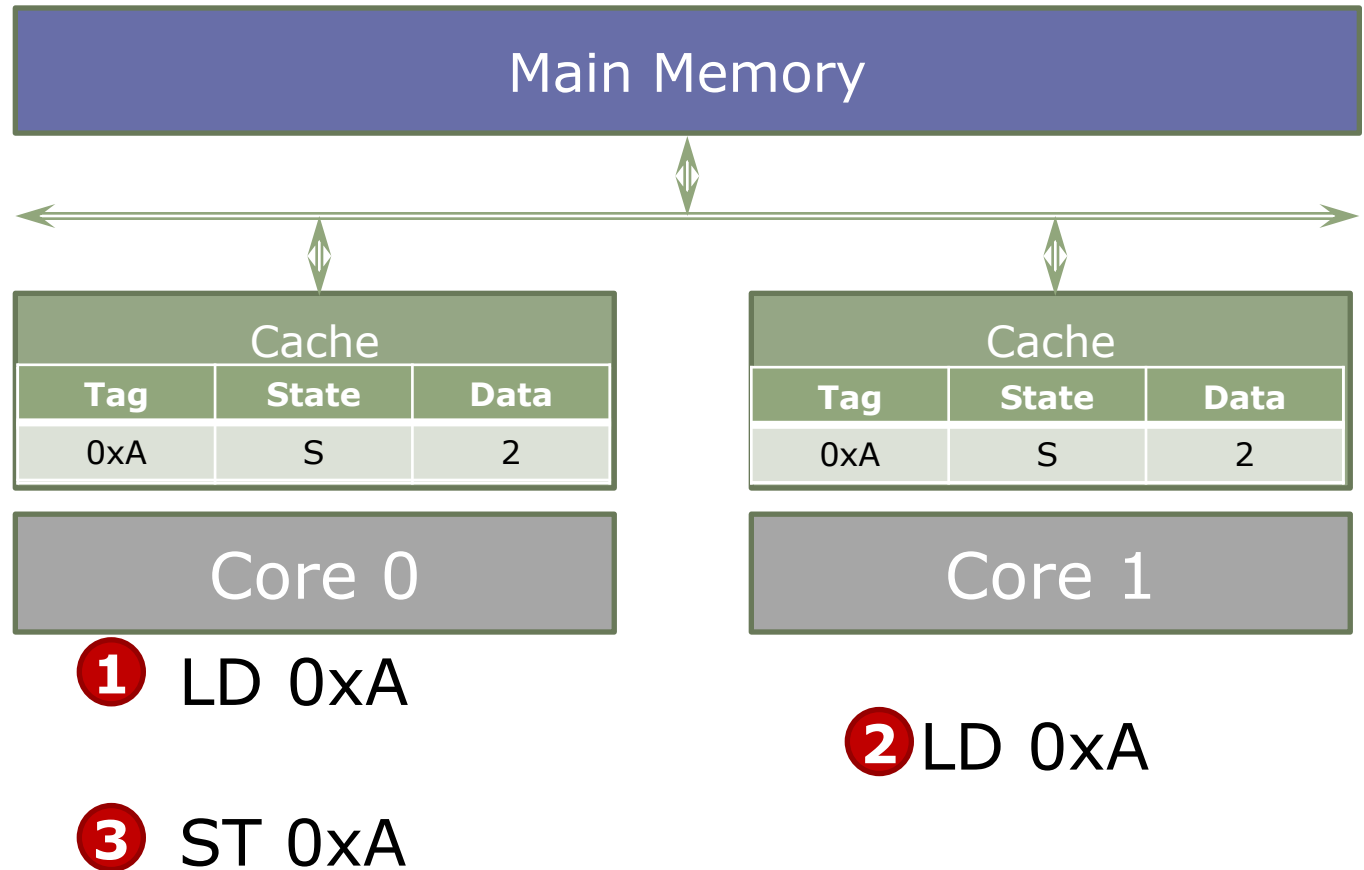
Additional loads satisfied locally, without BusRd (like in VI)



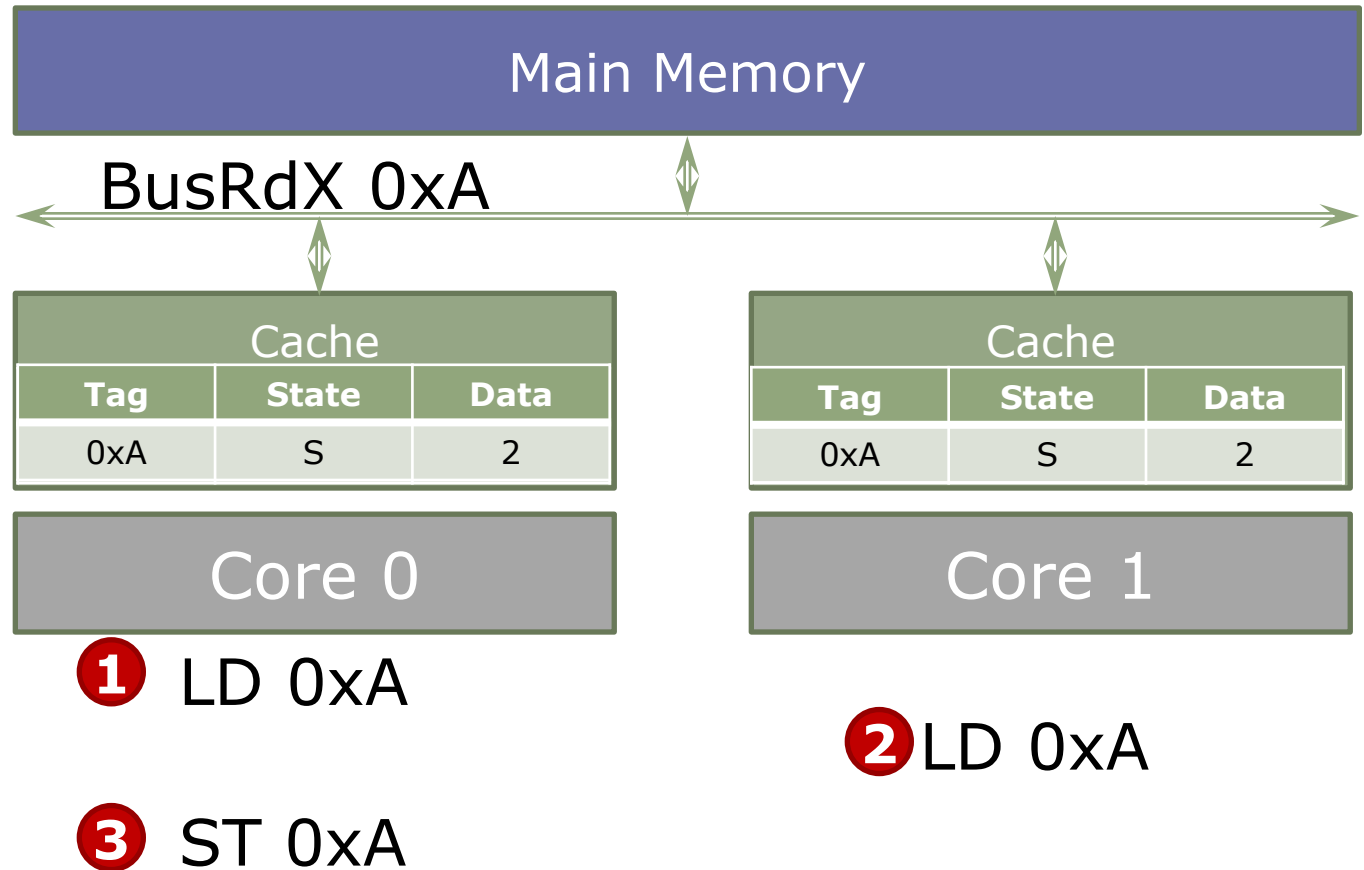
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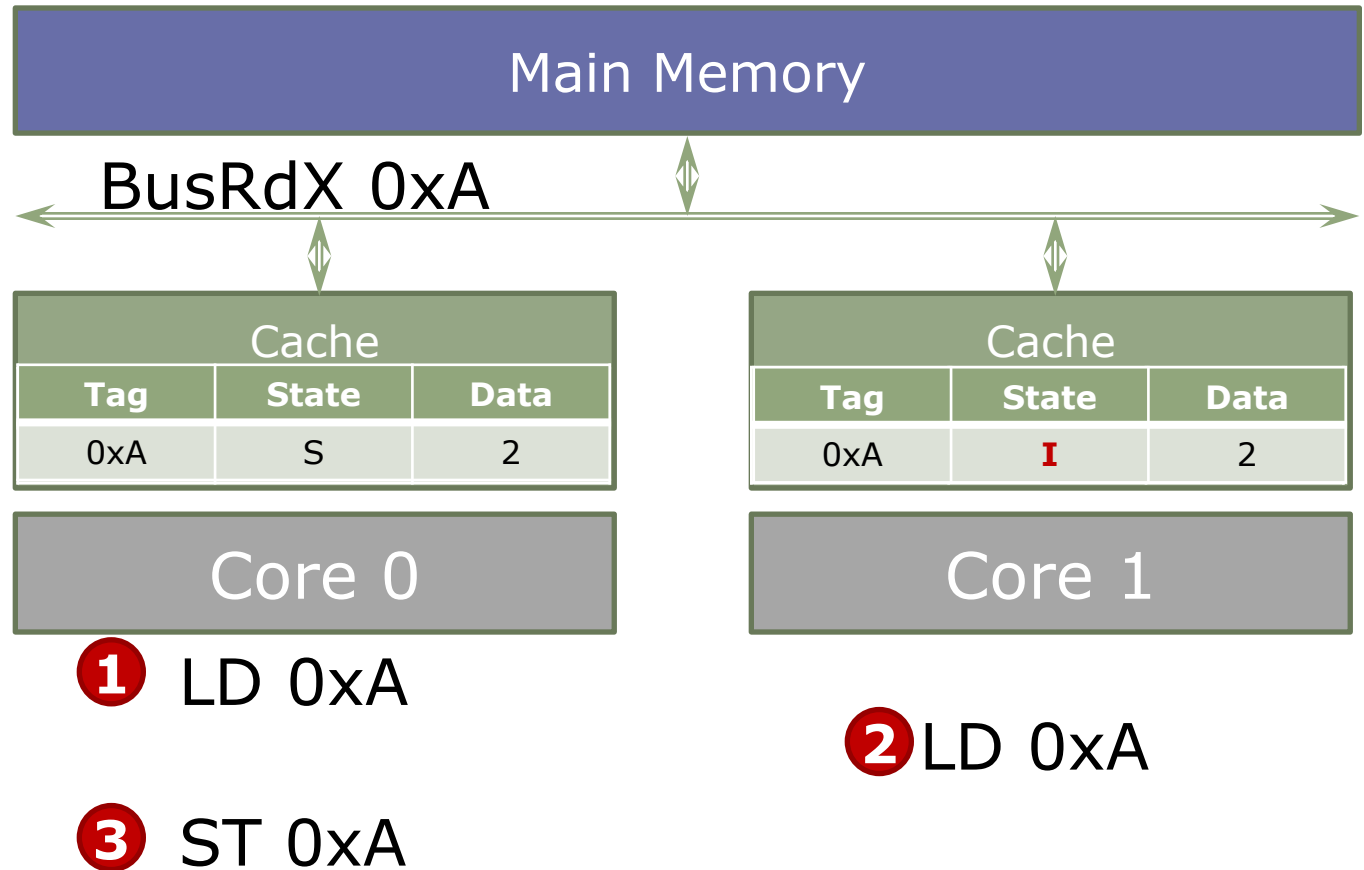
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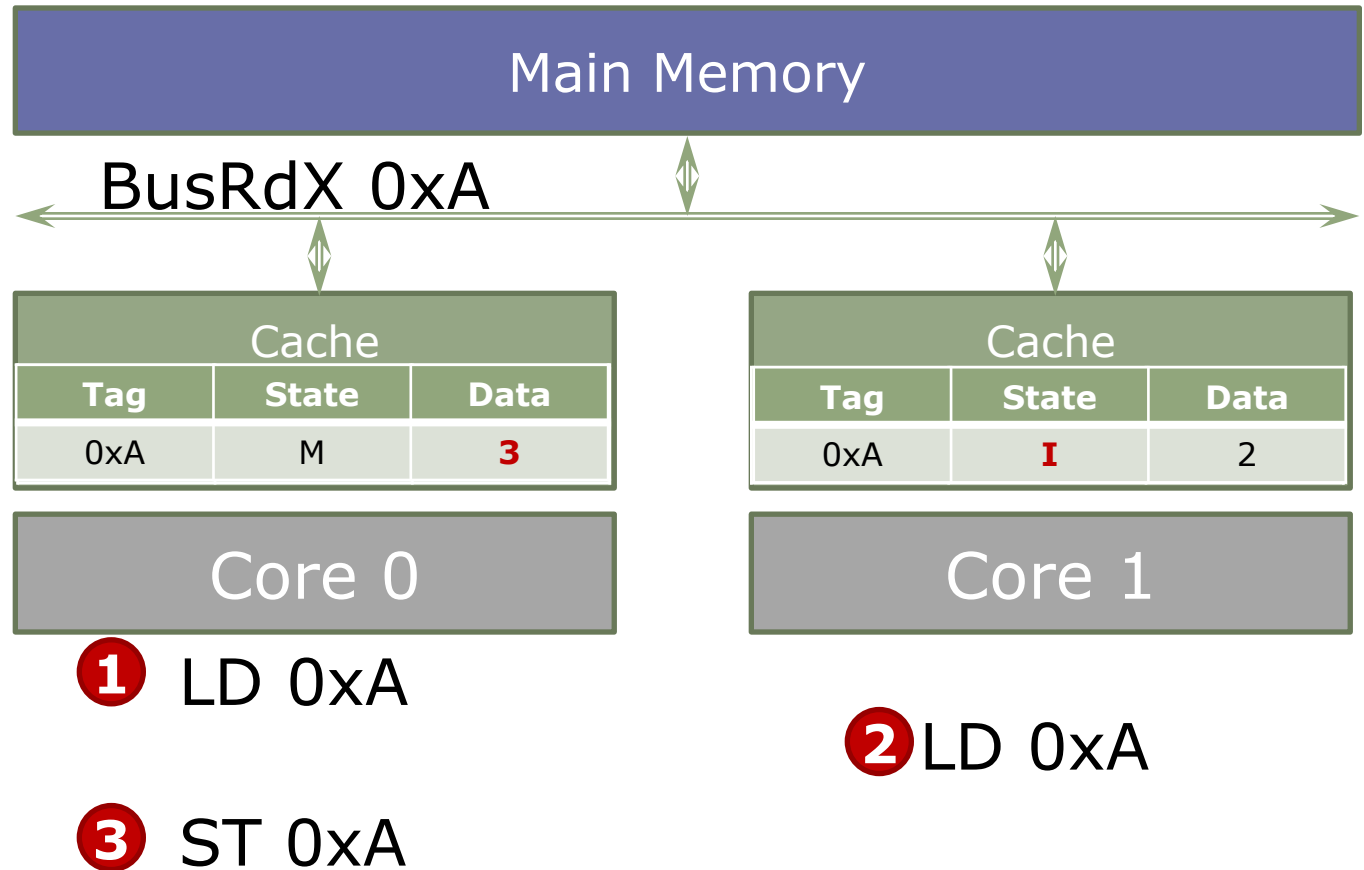
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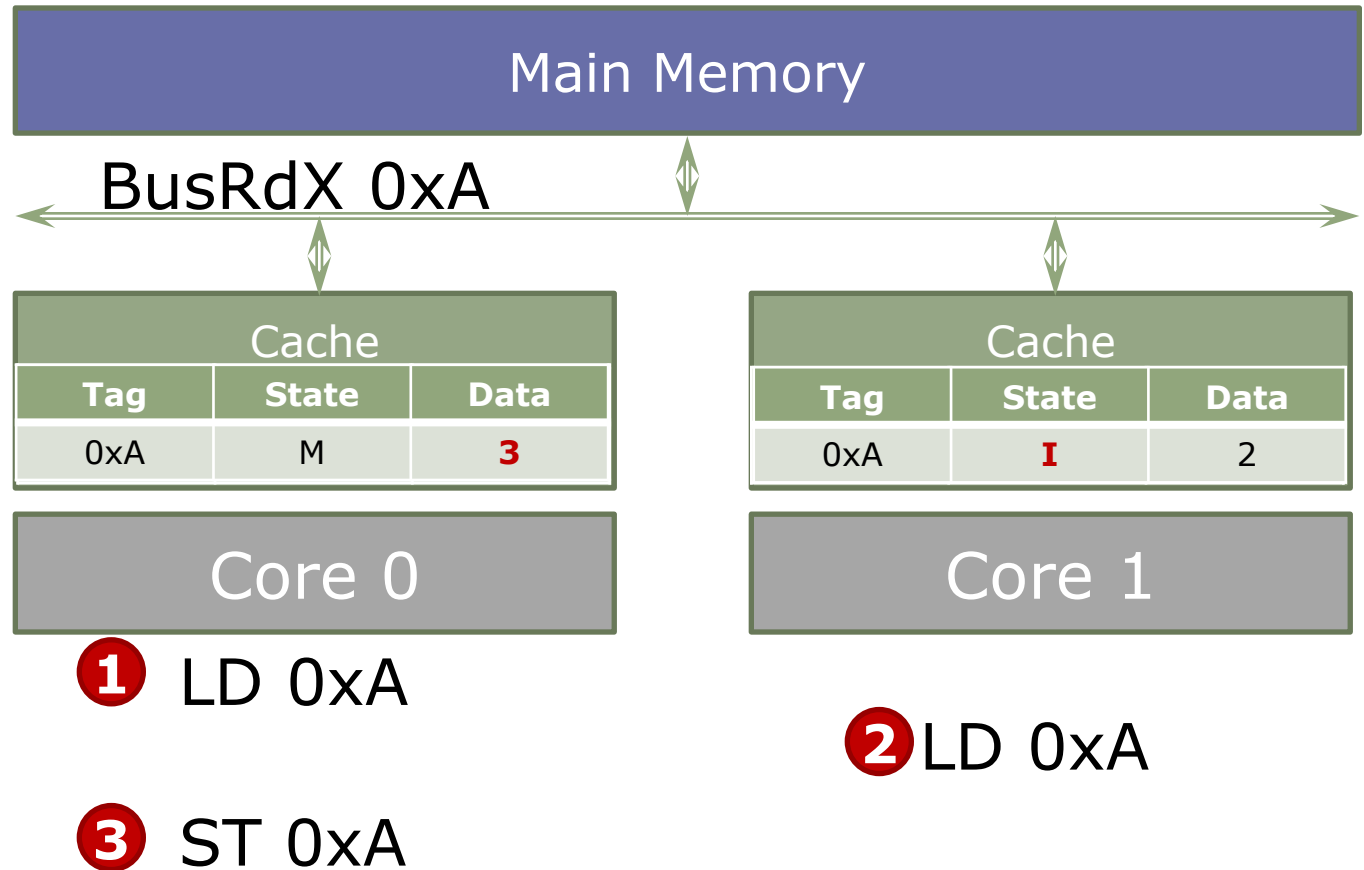
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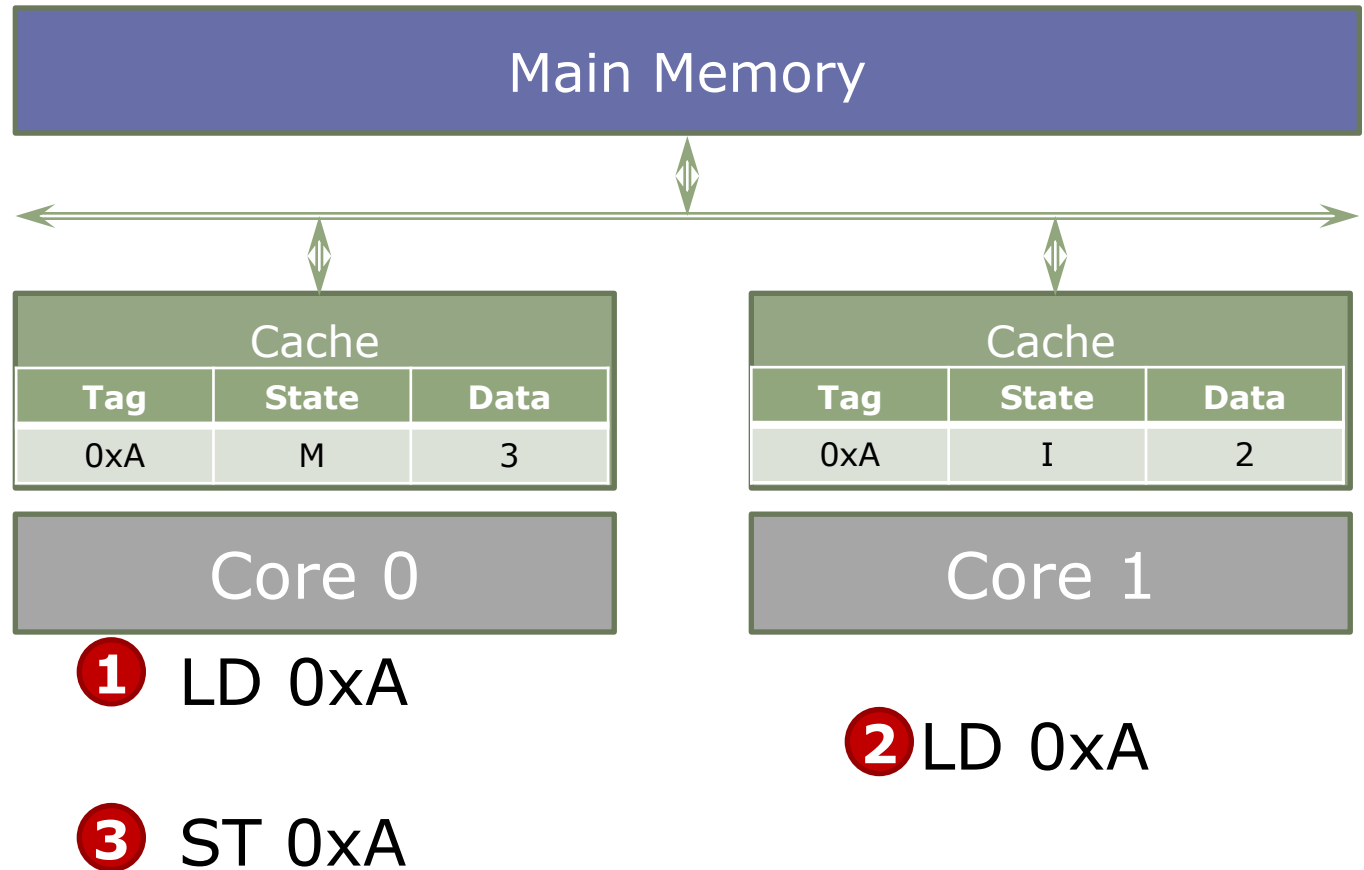


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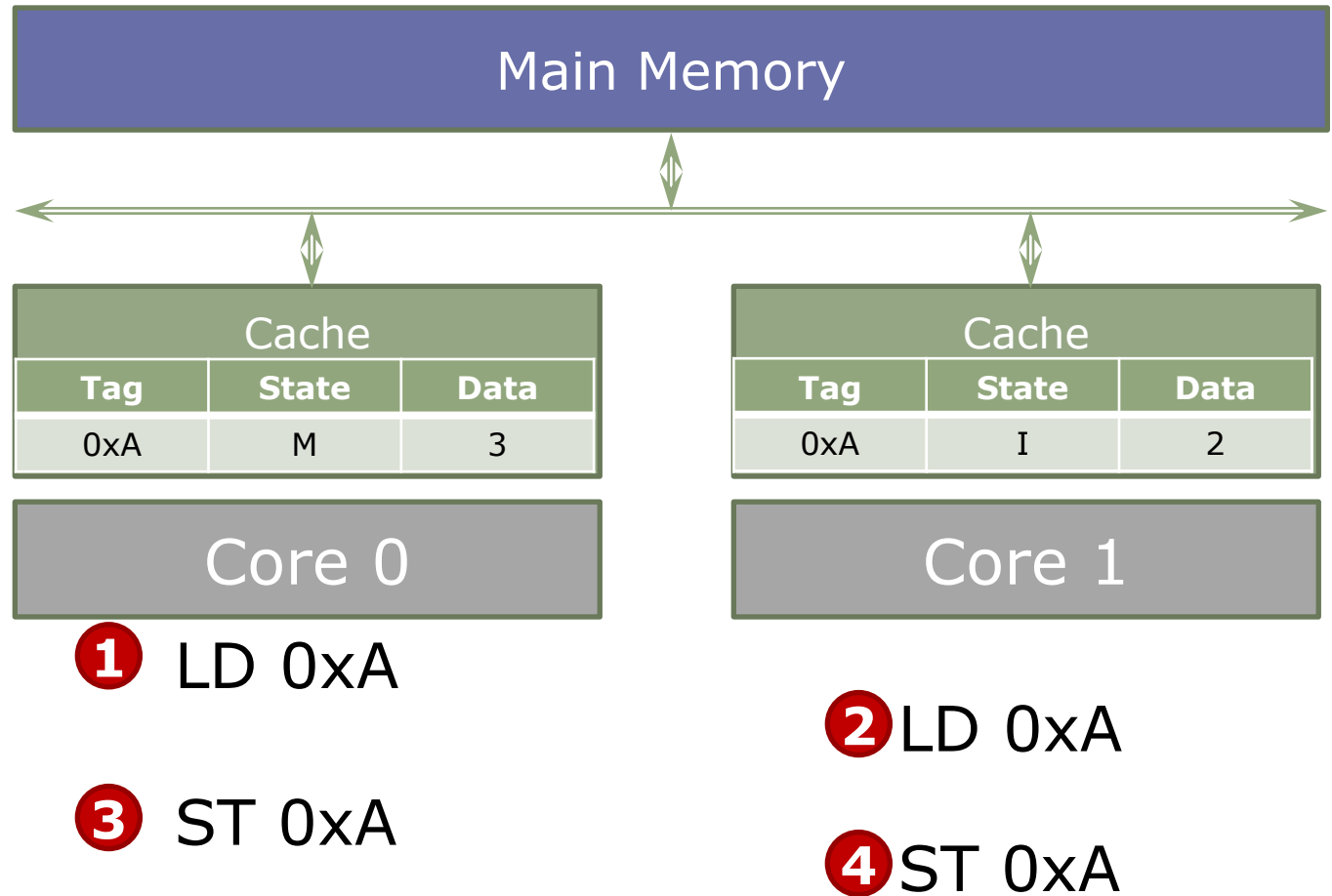


Additional loads *and* stores from core 0 satisfied locally, without bus transactions (unlike in VI)

# MSI Example

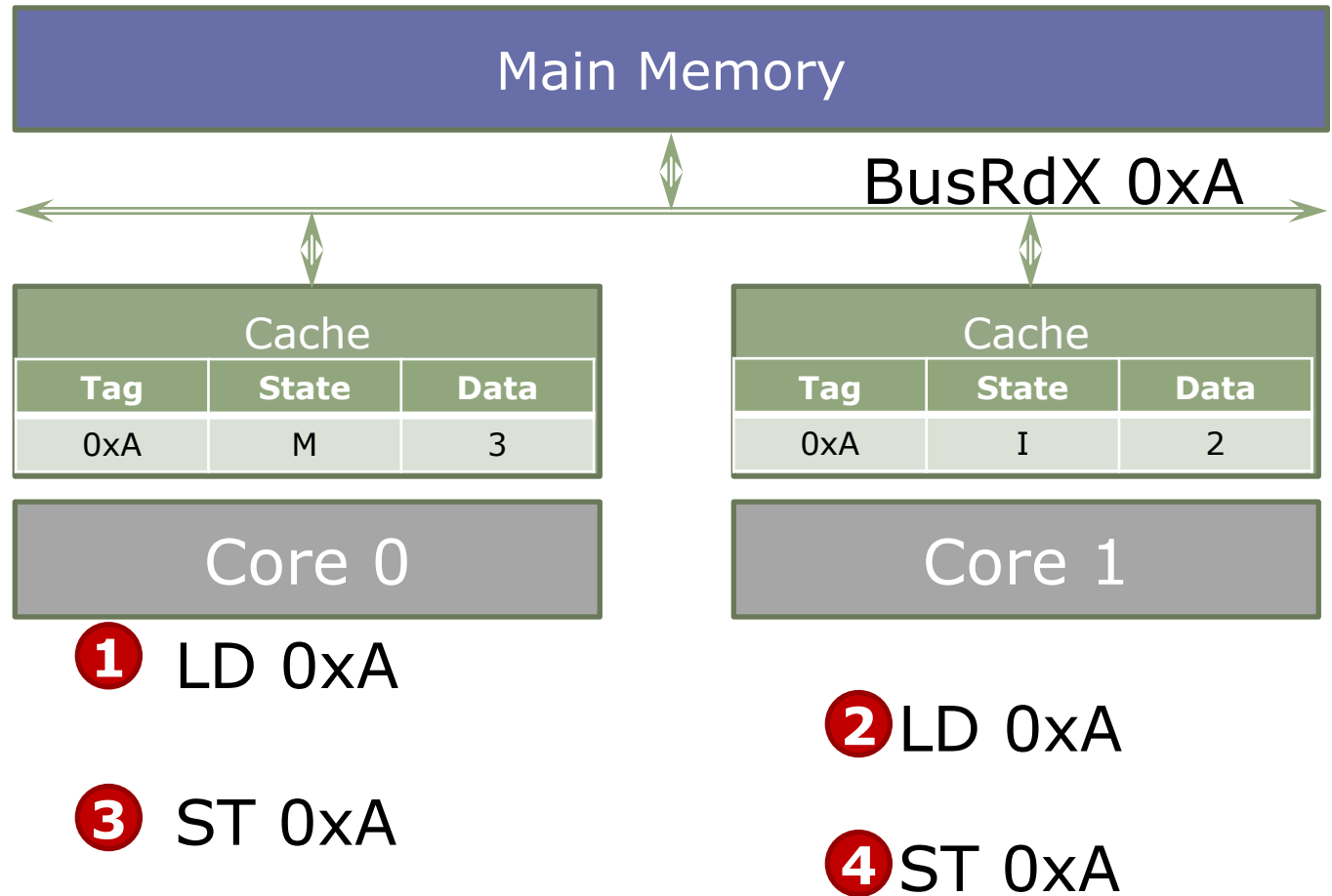


# MSI Example

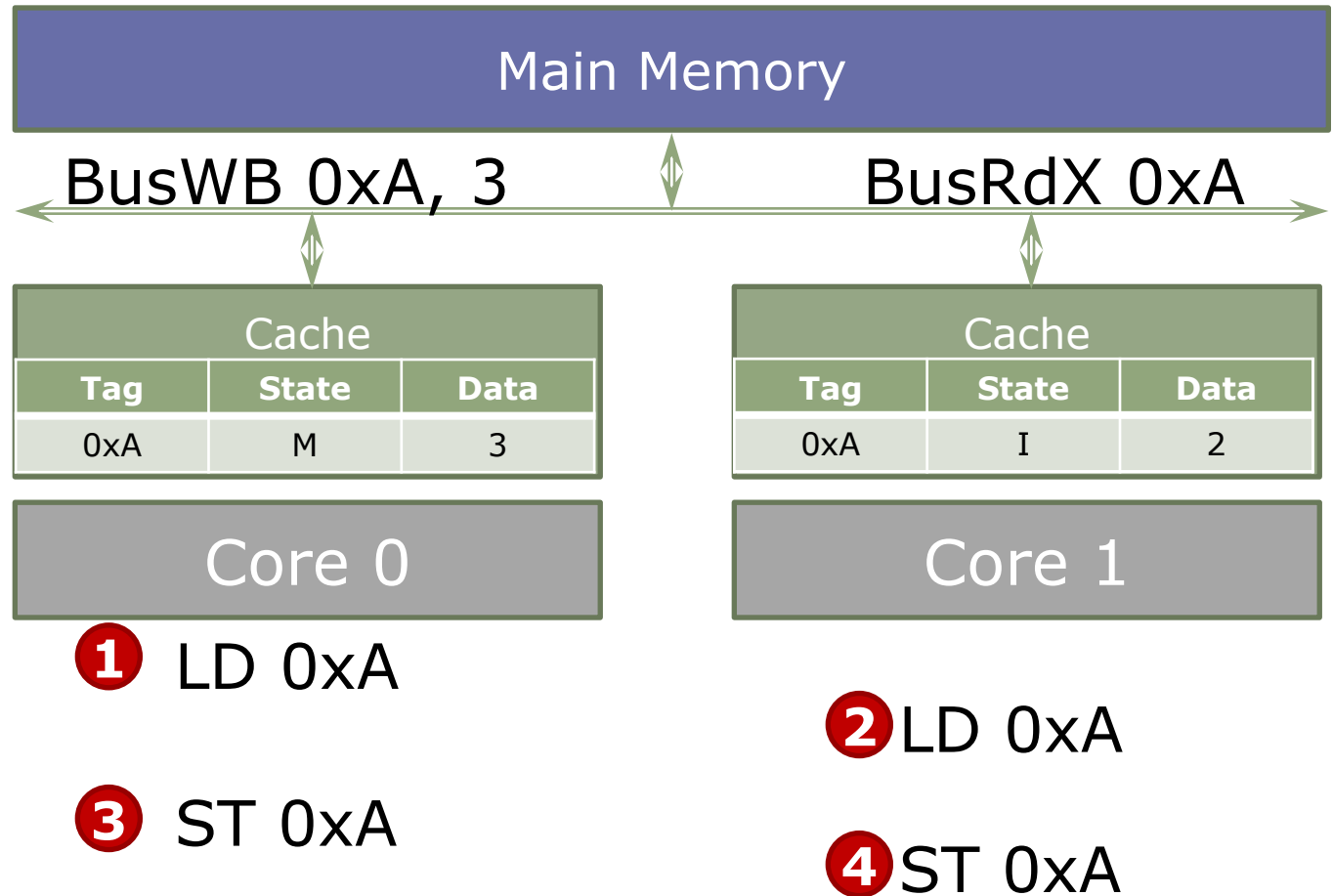




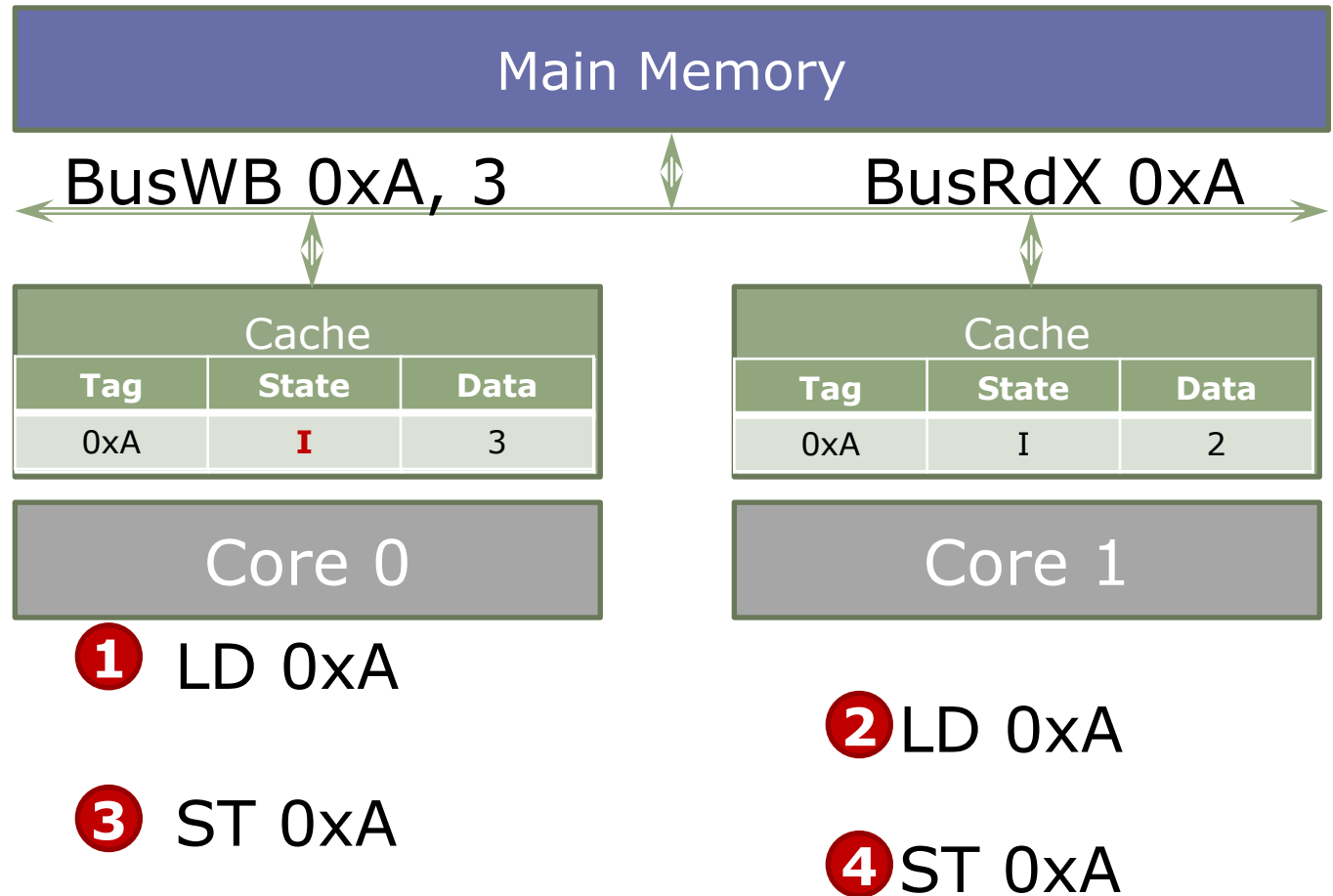
# MSI Example



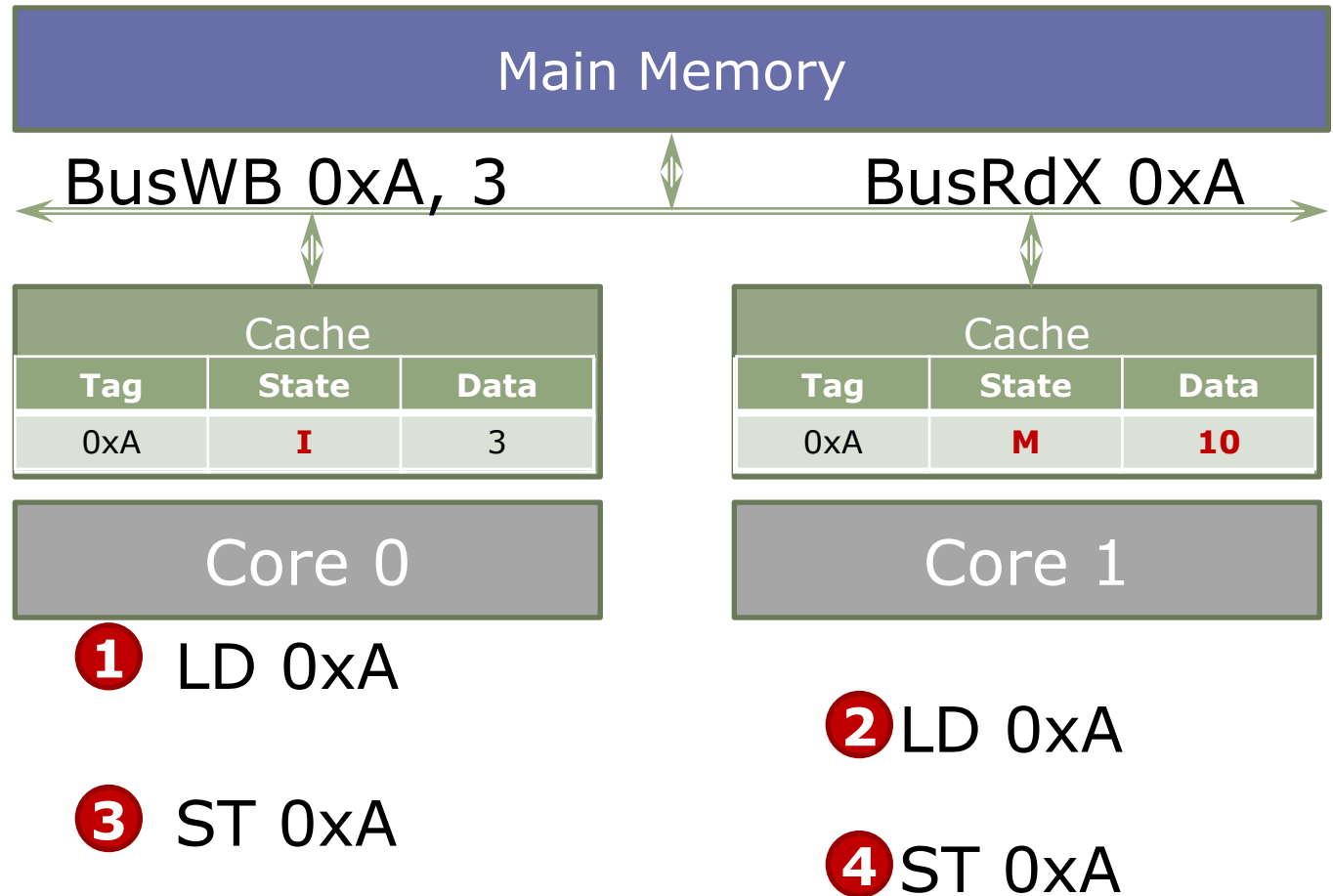
# MSI Example



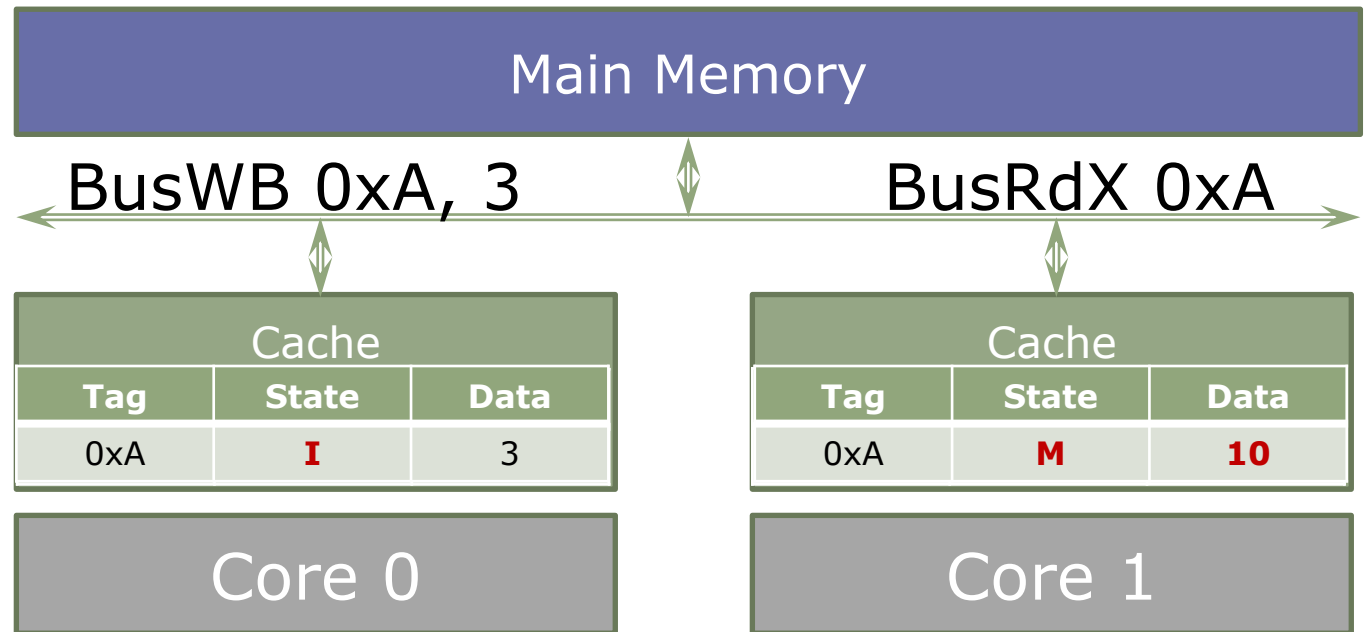
# MSI Example



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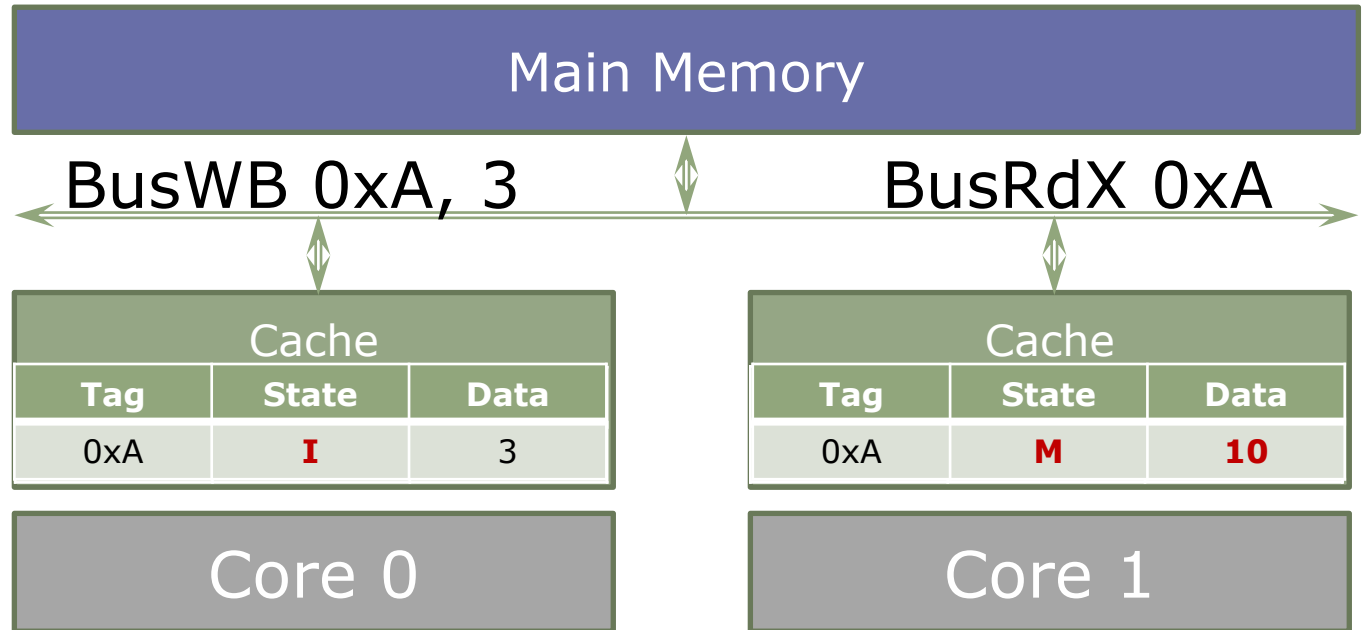


# Cache interventions



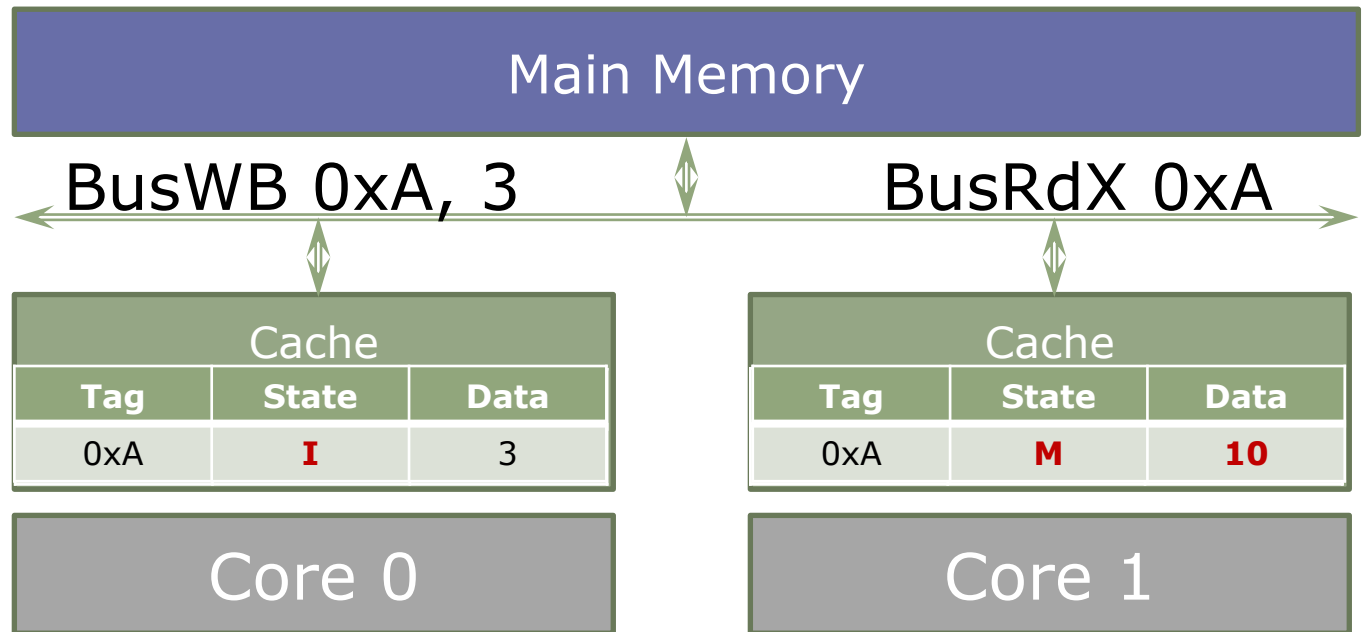
- MSI allows caches to serve writes without updating memory, so main memory can have stale data

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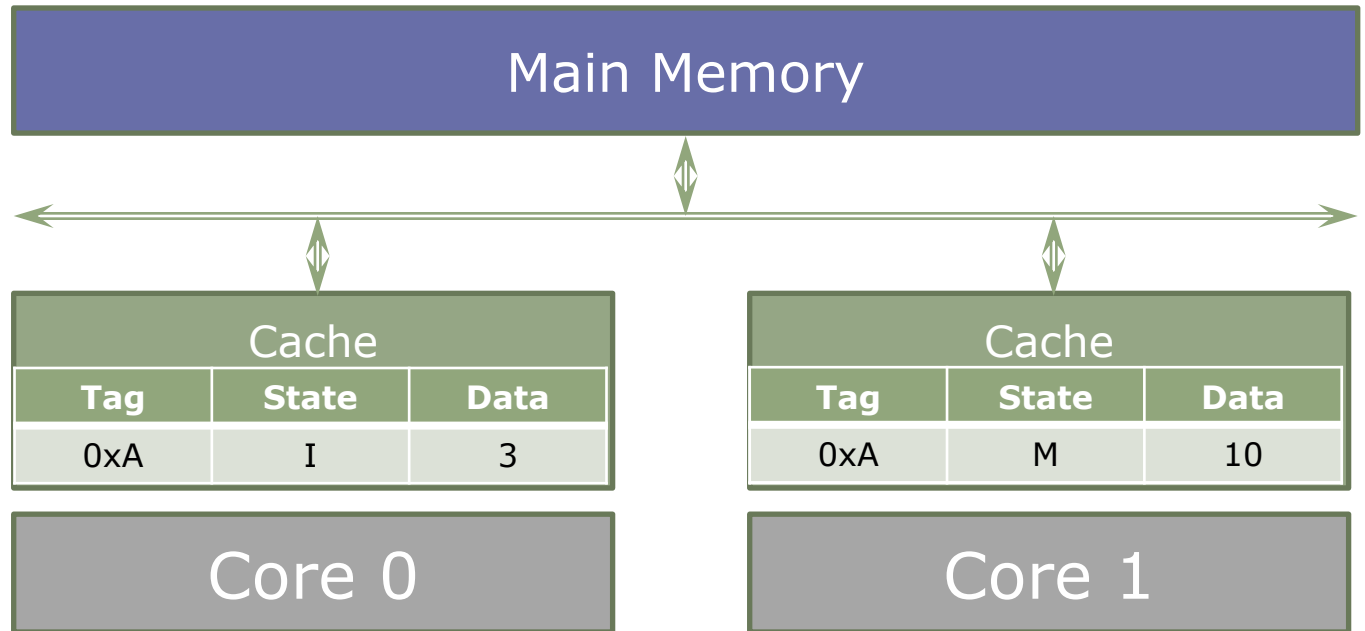
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  - But main memory may also respond!

# Cache interventions



- MSI allows caches to serve writes without updating memory, so main memory can have stale data
  - Core 0's cache needs to supply data
  - But main memory may also respond!
- Cache must override response from main memory

# MSI Example



**1** LD 0xA

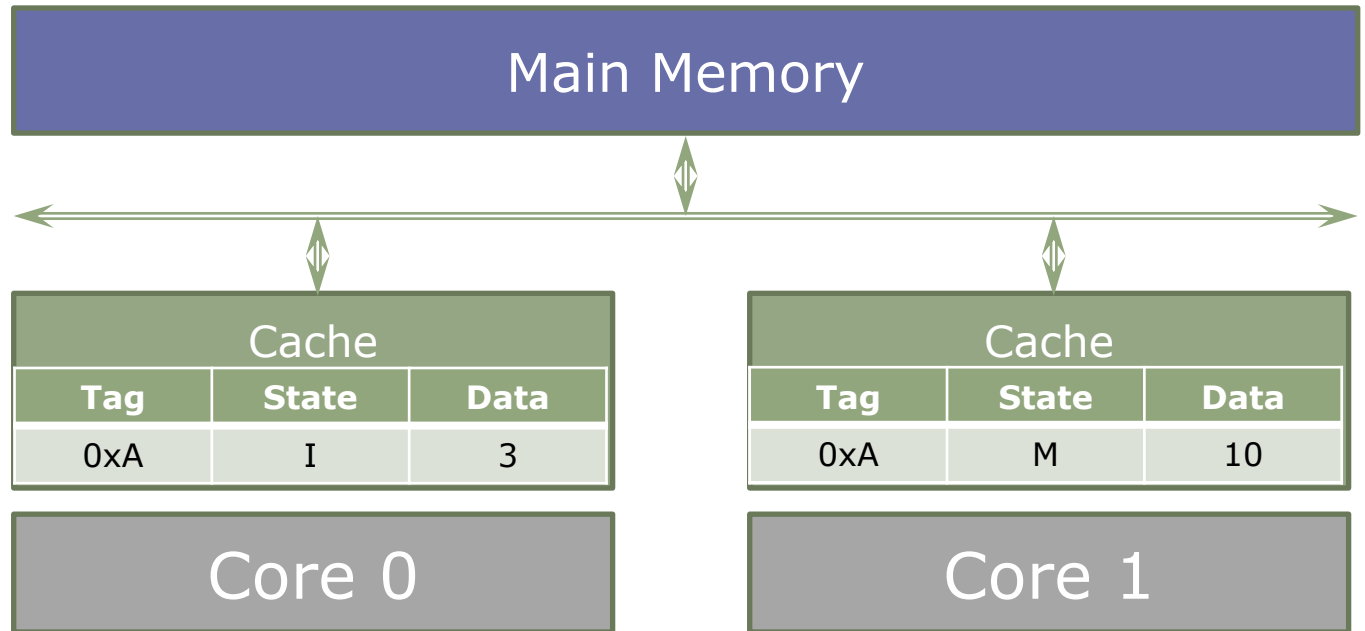
**3** ST 0xA

**2** LD 0xA

**4** ST 0xA



# MSI Example



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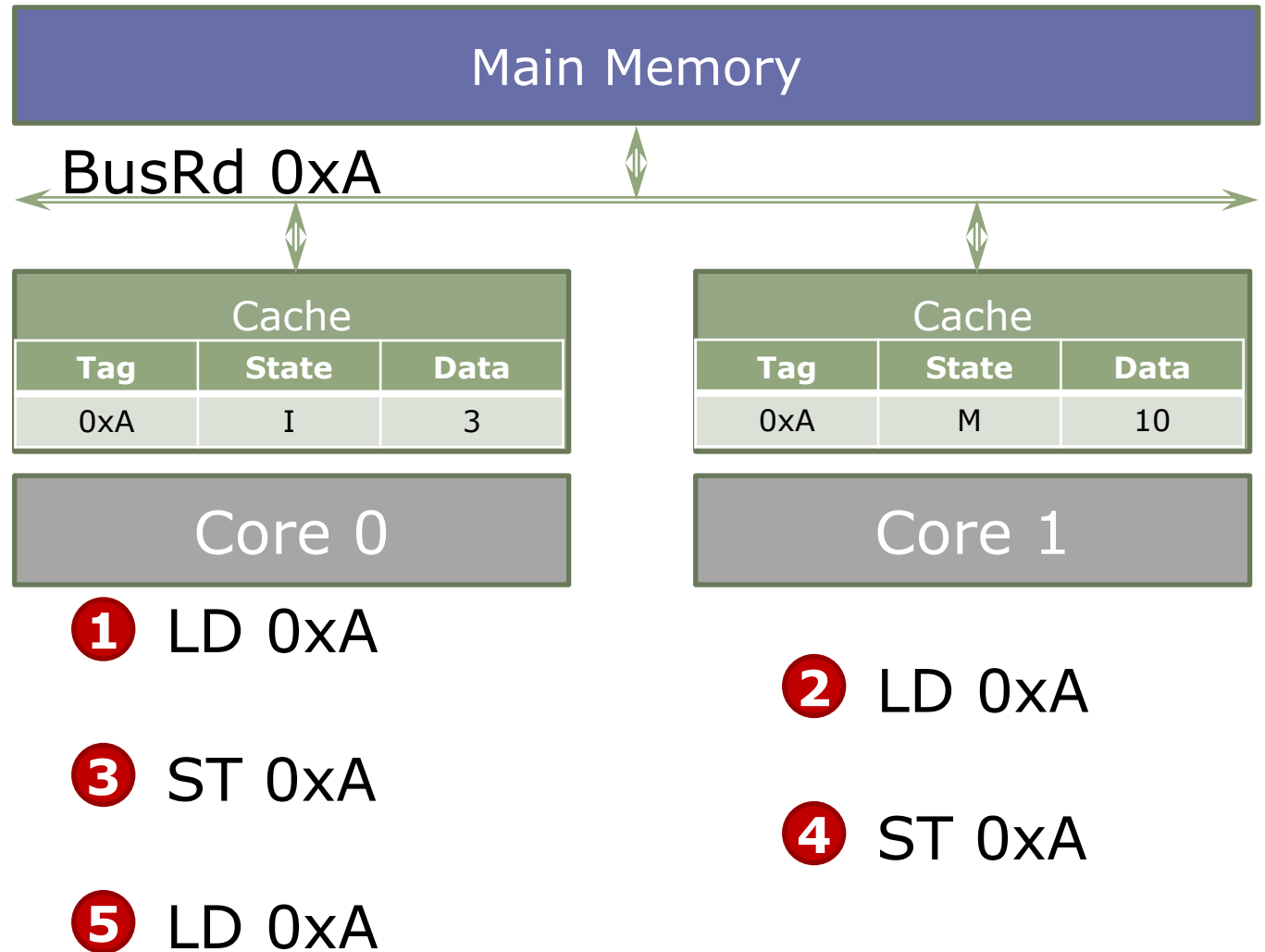
**3** ST 0xA

**5** LD 0xA

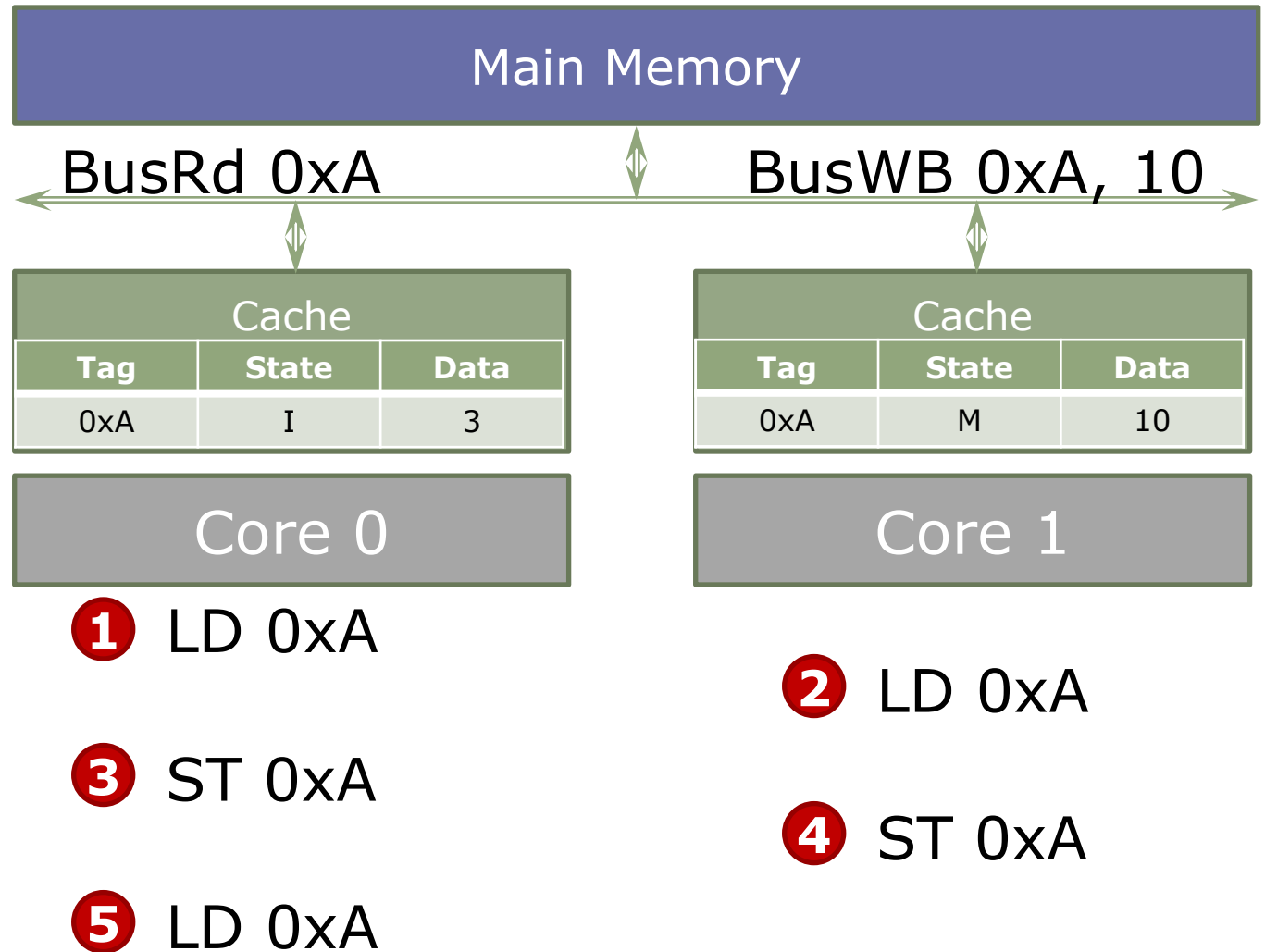
**2** LD 0xA

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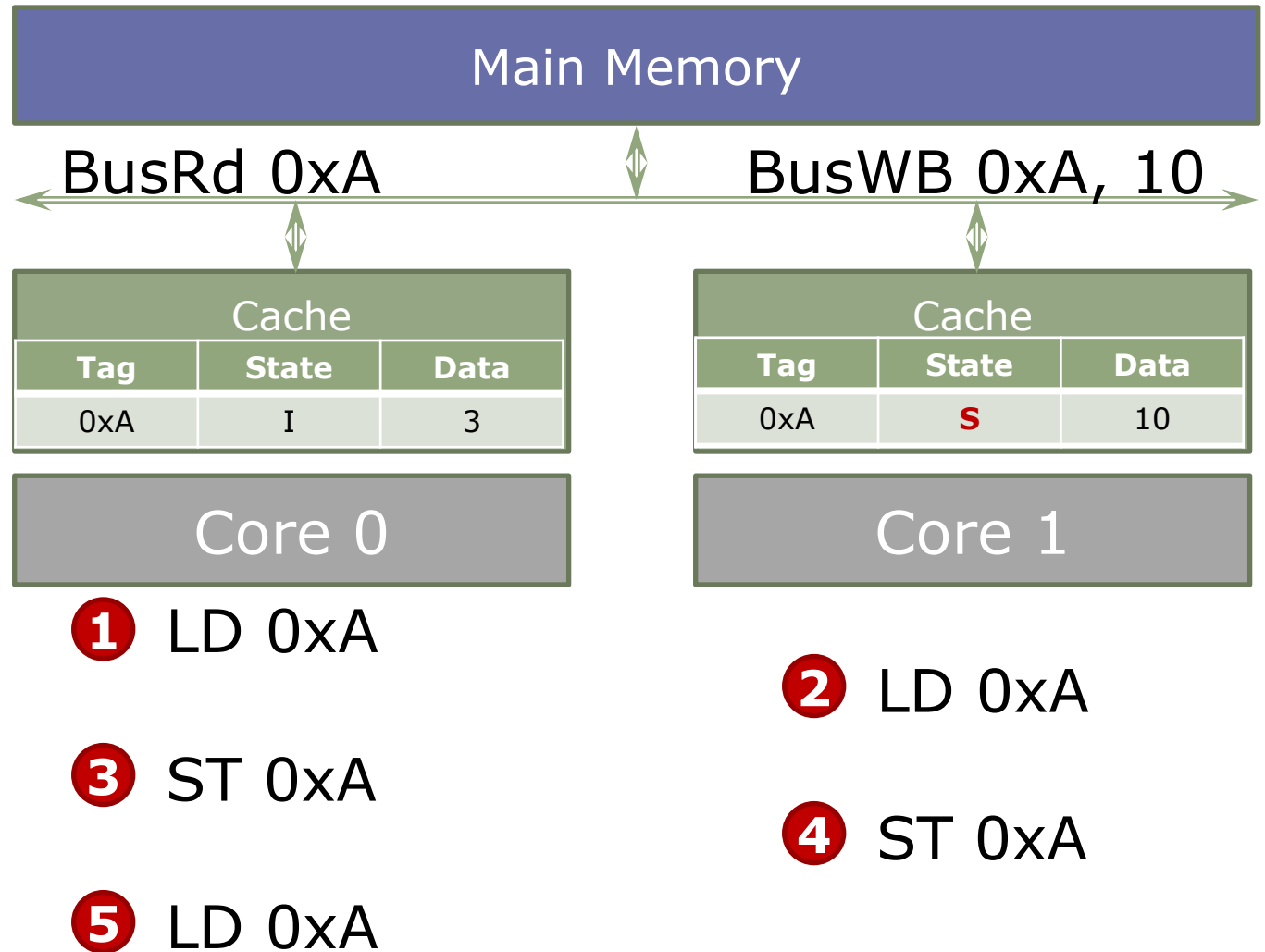
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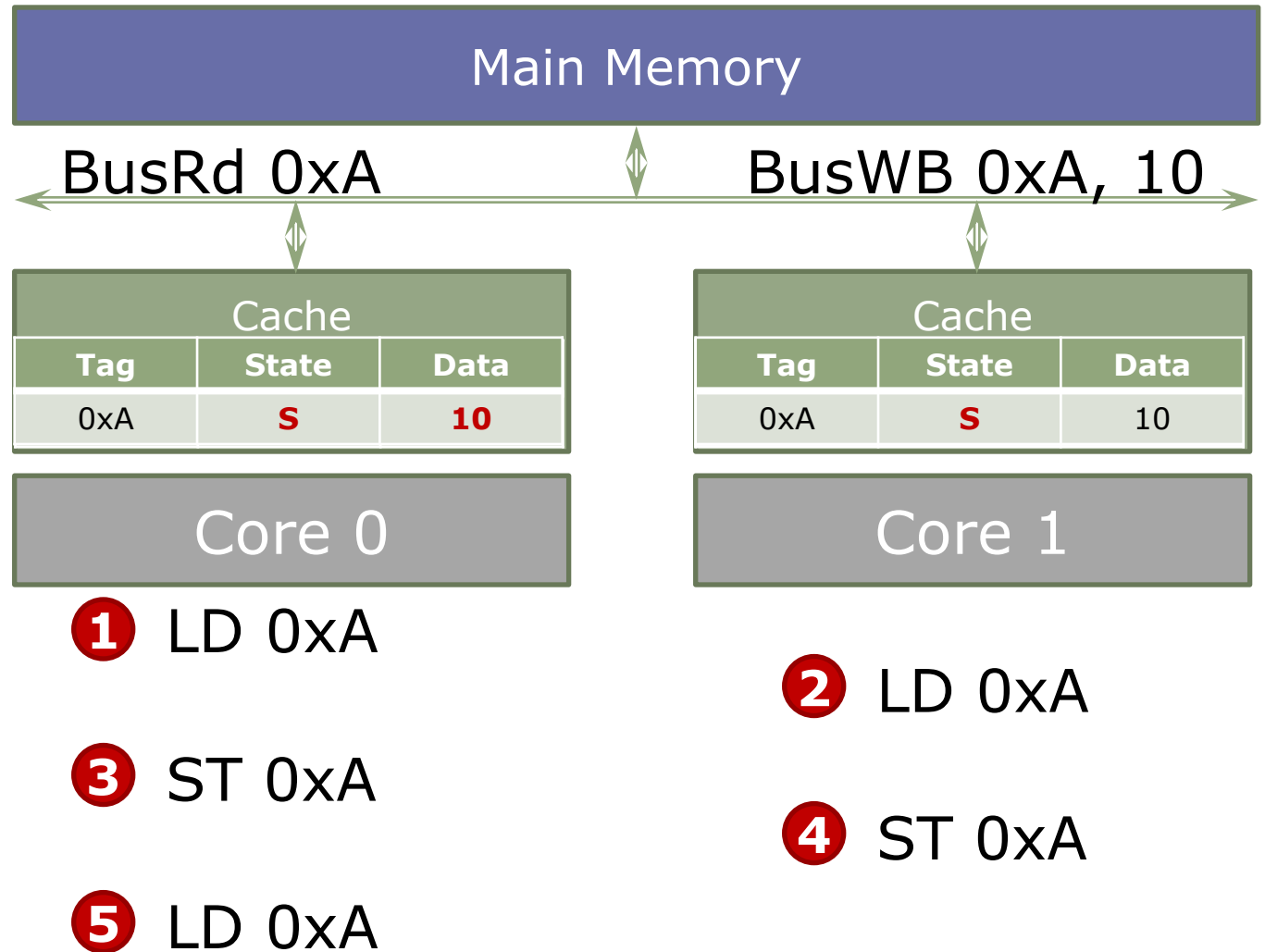
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# MSI Example



# MSI Optimizations: Exclusive State

---

- Observation: Doing read-modify-write sequences on private data is common
  - What's the problem with MSI?

# MSI Optimizations: Exclusive State

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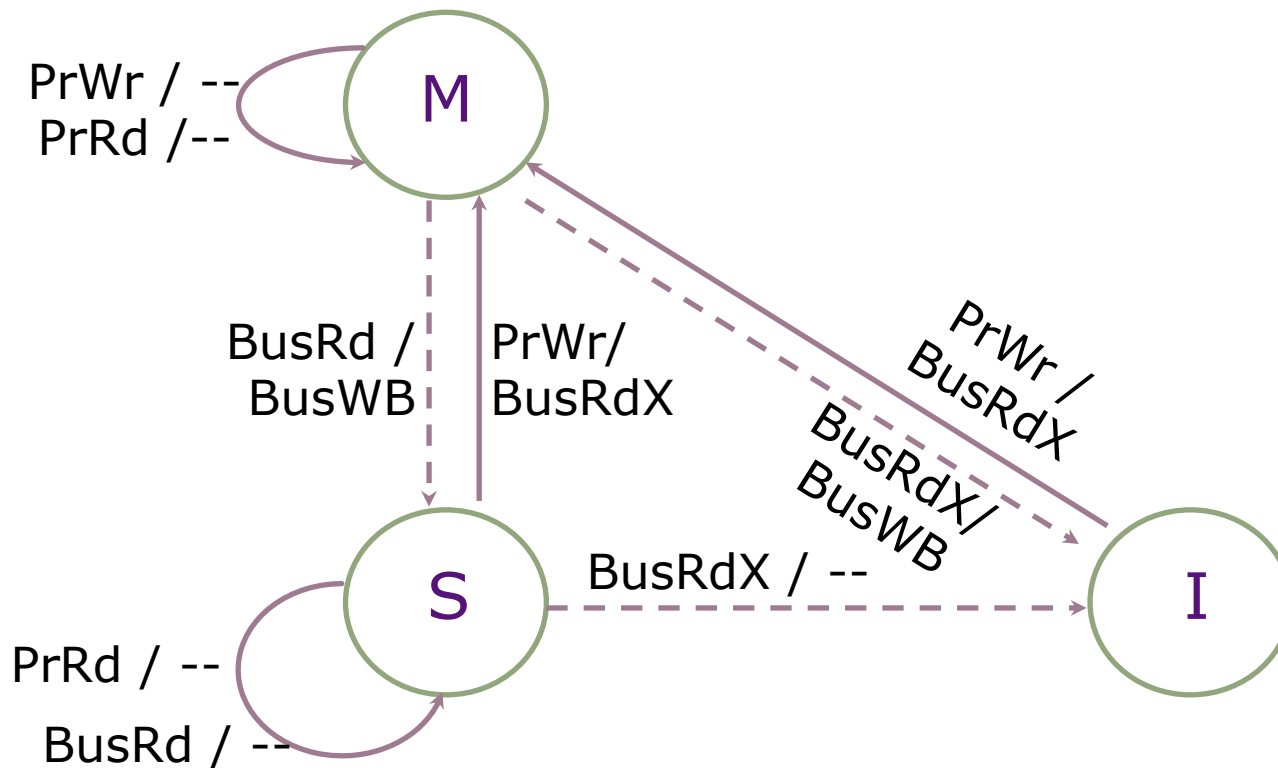
- Observation: Doing read-modify-write sequences on private data is common
  - What's the problem with MSI?
- Solution: E state (exclusive, clean)
  - If no other sharers, a read acquires line in E instead of S
  - Writes silently cause E→M (exclusive, dirty)

# MESI: An Enhanced MSI protocol

increased performance for private read-write data

---

M: Modified Exclusive  
E: Exclusive, unmodified  
S: Shared  
I: Invalid



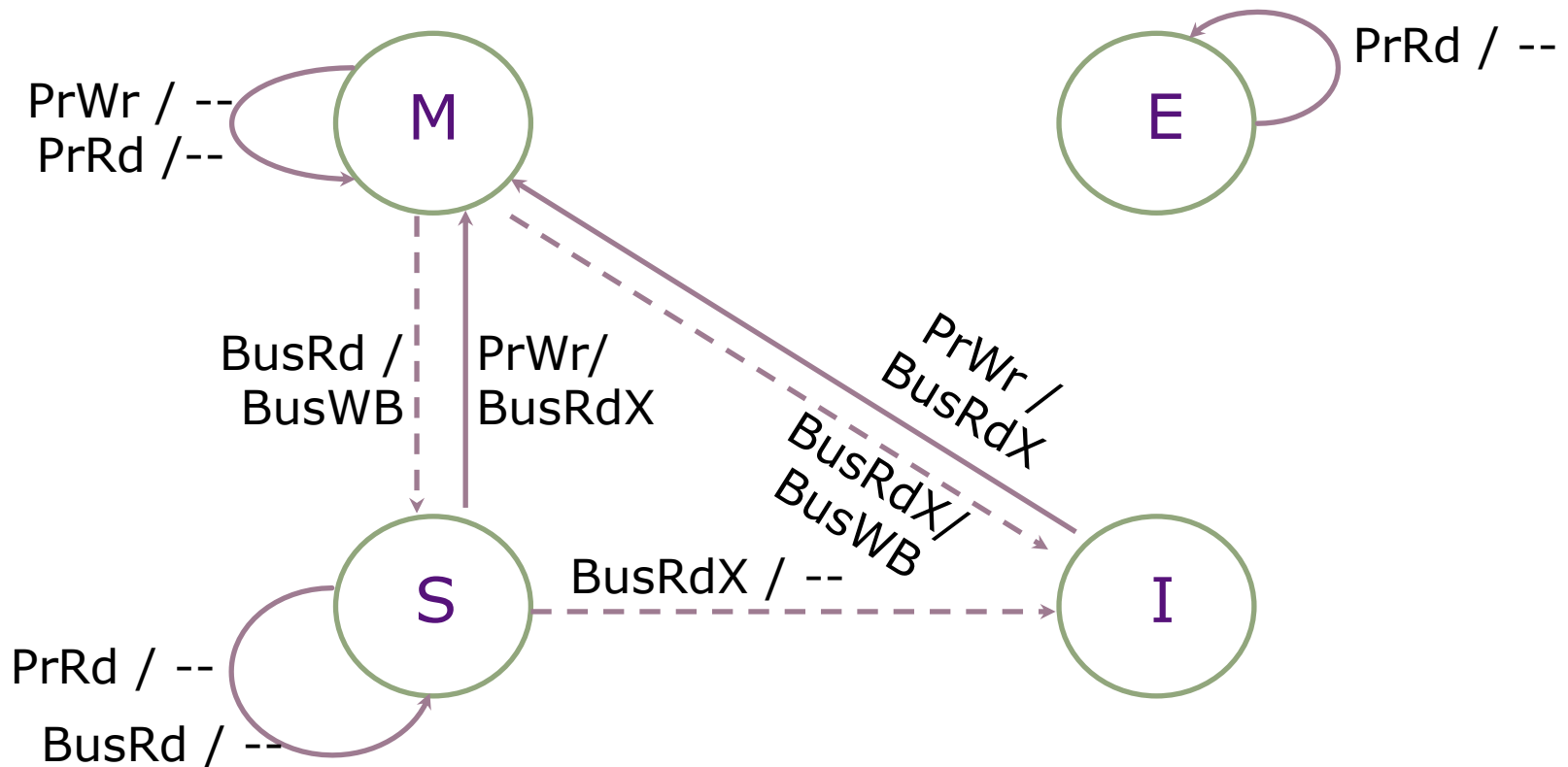


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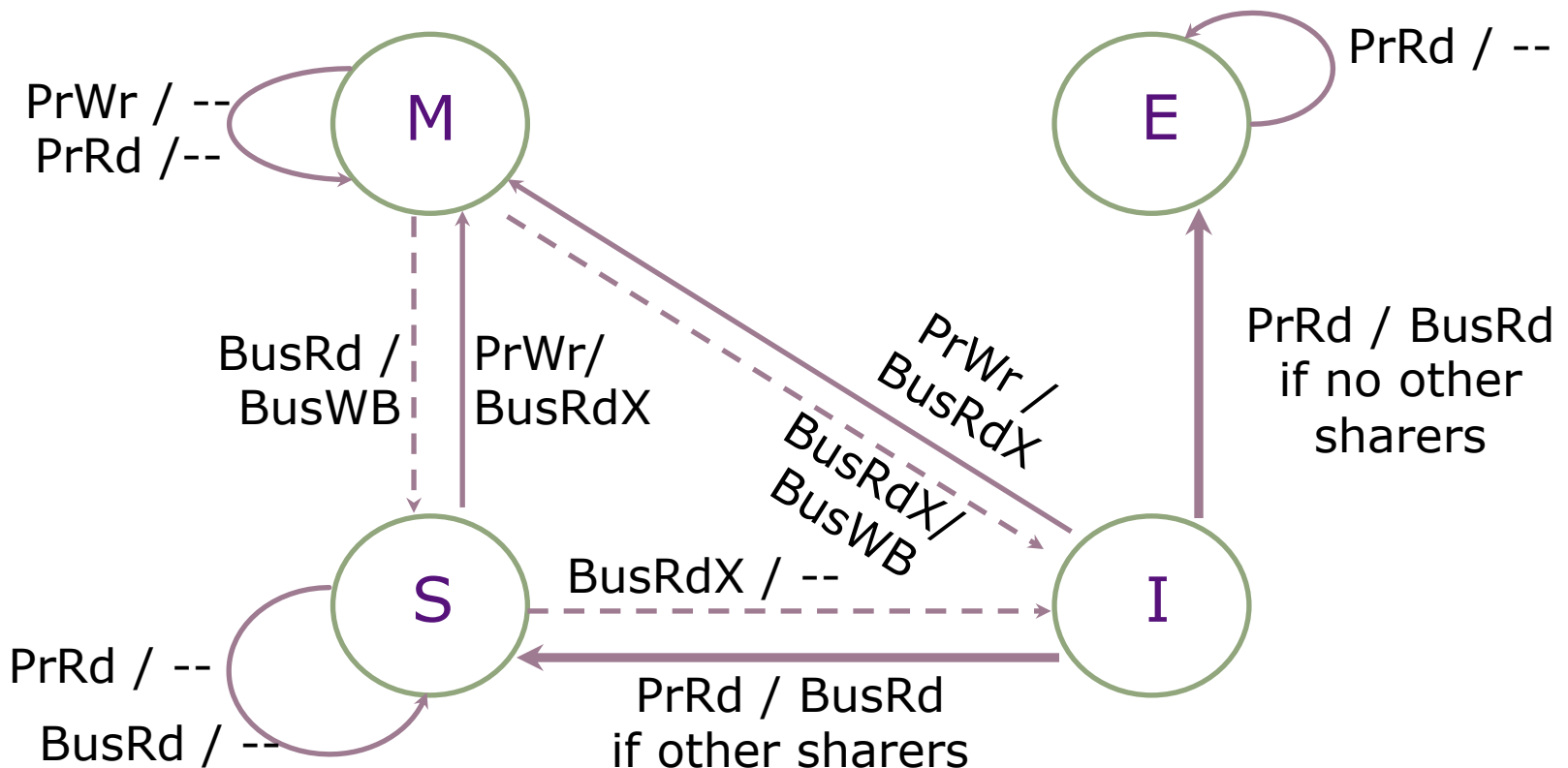
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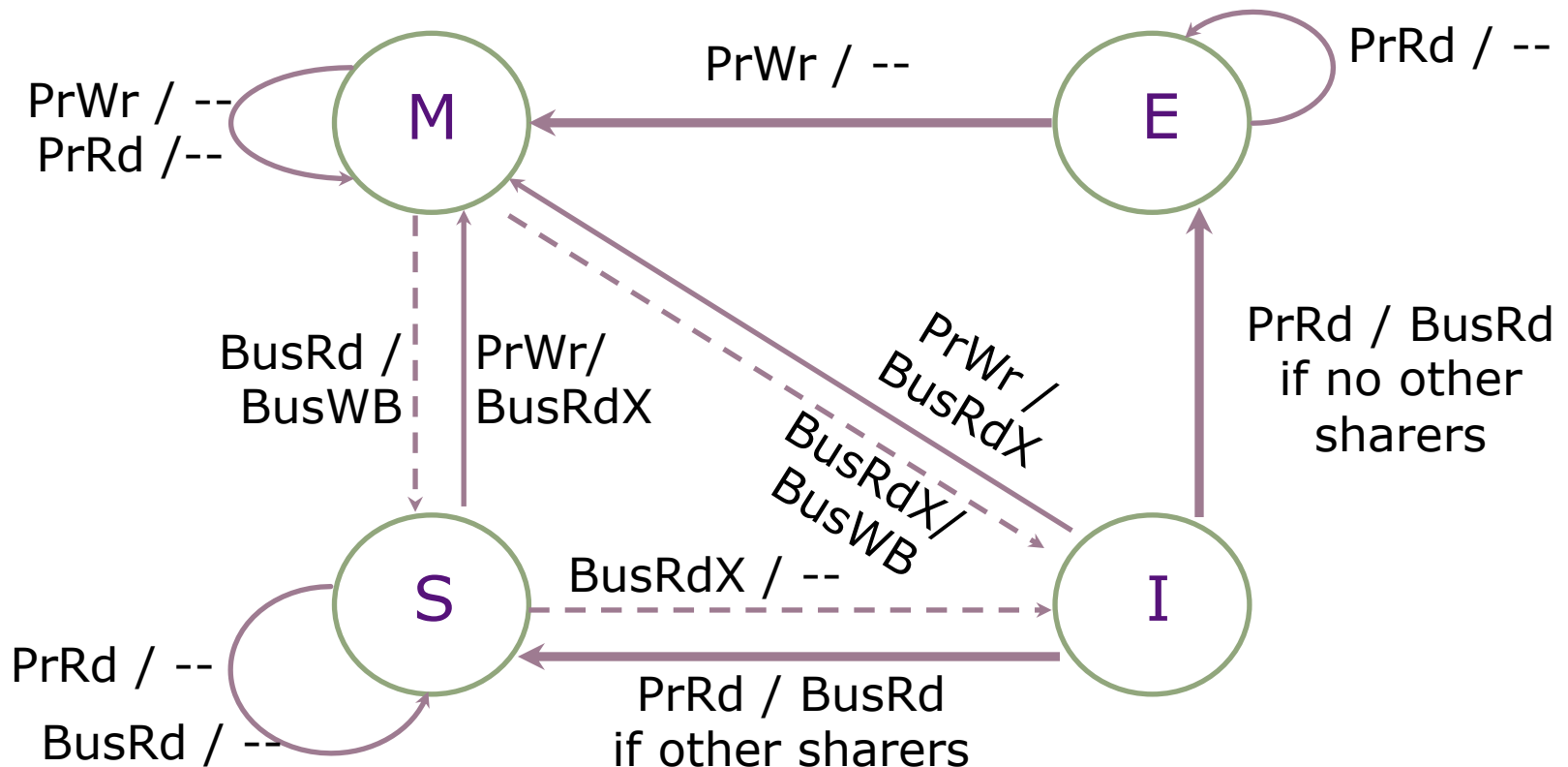
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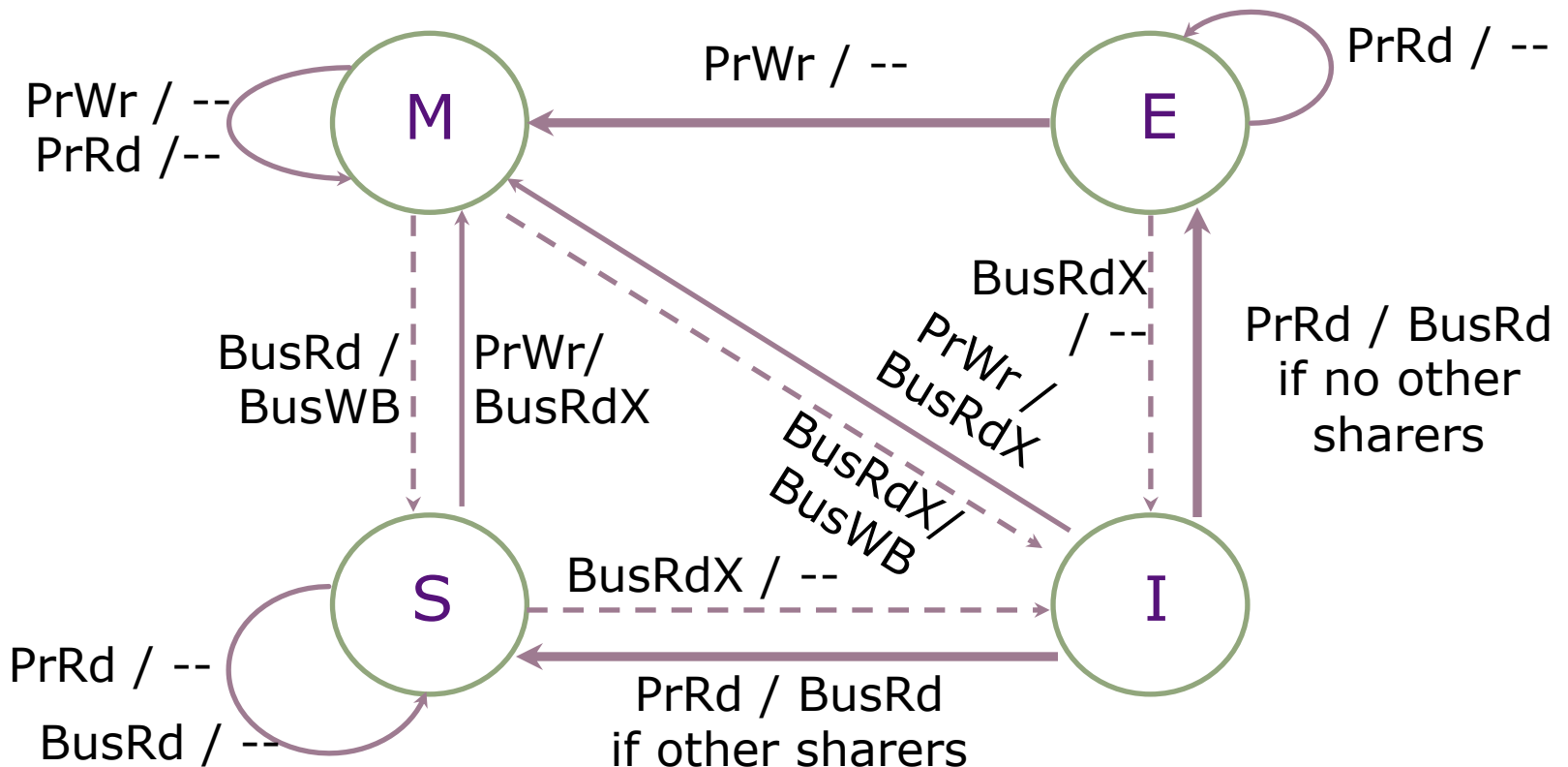
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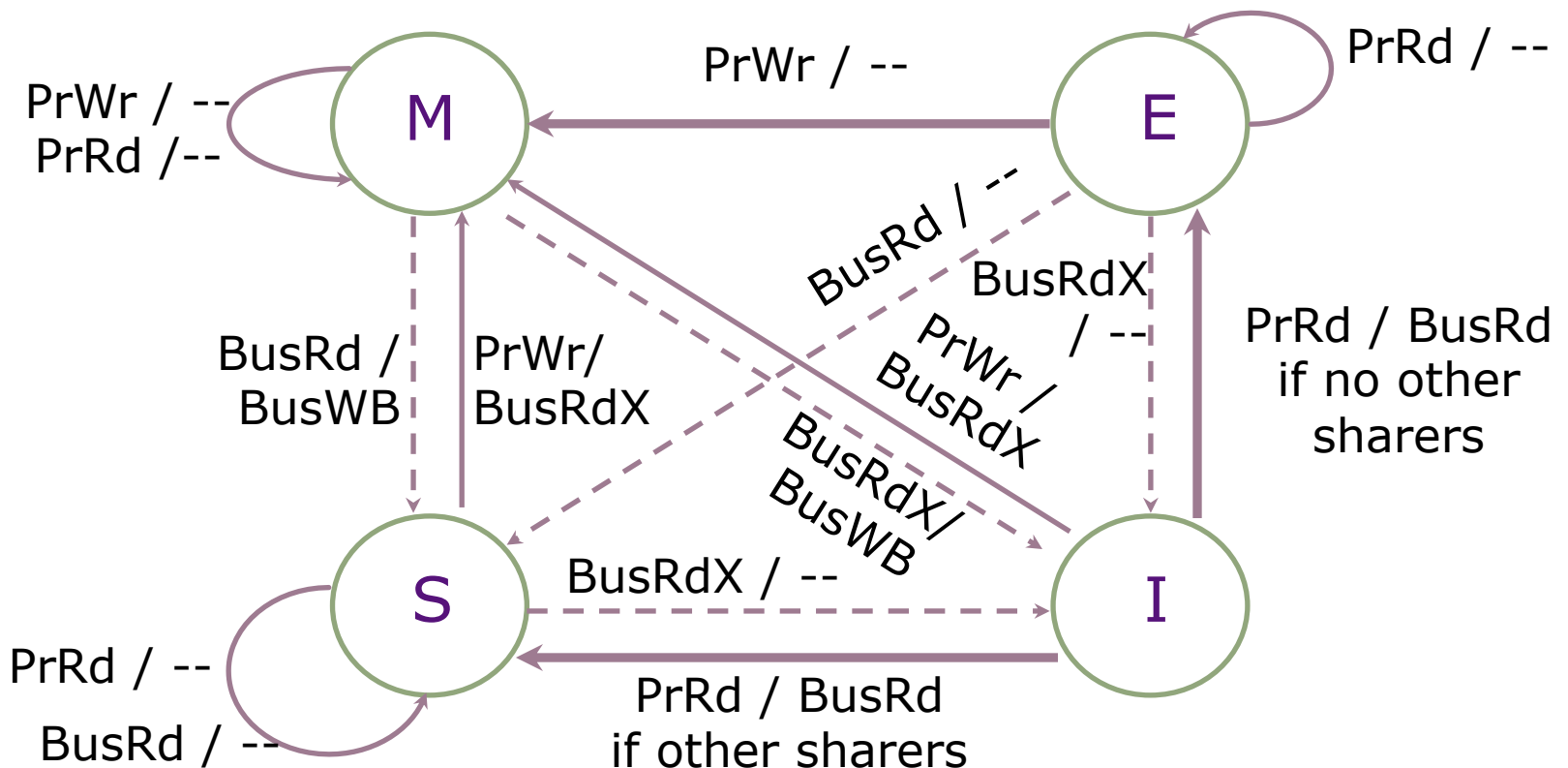
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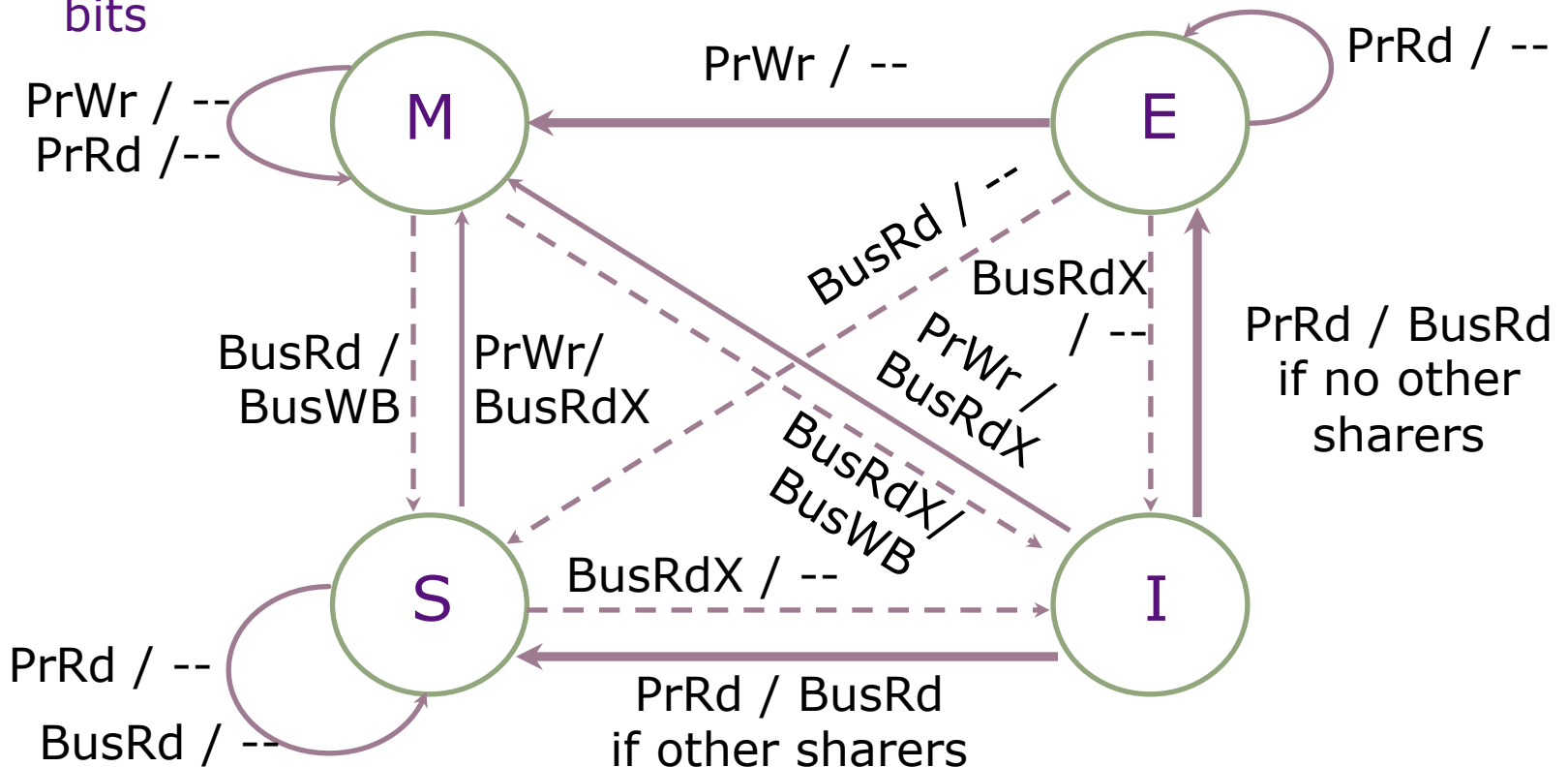
# MESI: An Enhanced MSI protocol

increased performance for private read-write data

Each cache line has a tag



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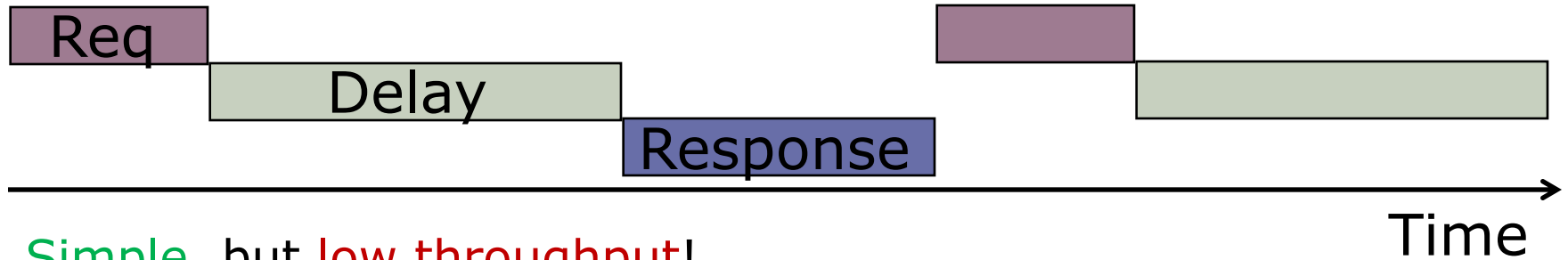
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- MSI, MESI, MOSI, MOESI...
  - Typically  $E$  if private read-write  $\gg$  shared read-only (common)
  - Typically  $O$  only if writebacks are expensive (main mem vs  $L3$ )

# Split-Transaction and Pipelined Buses

---

## Atomic Transaction Bus



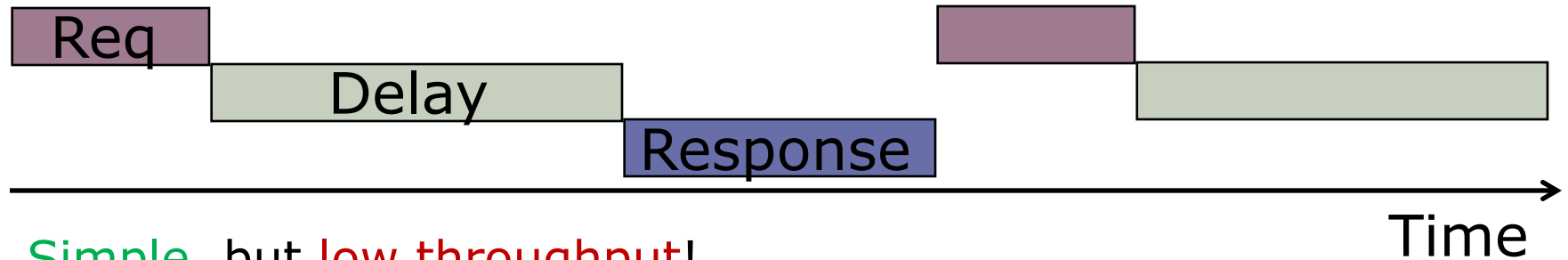
Simple, but low throughput!

Time

# Split-Transaction and Pipelined Buses

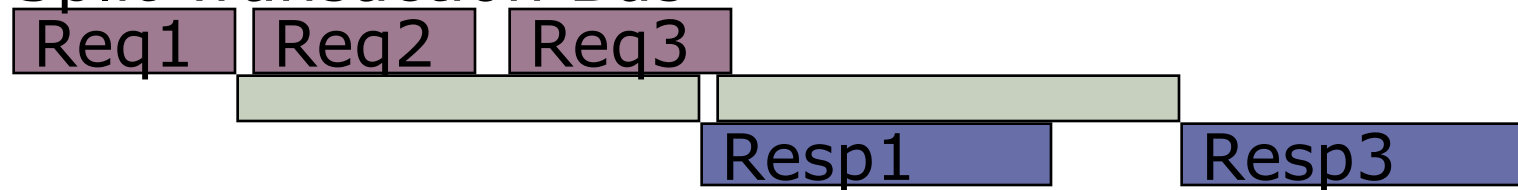
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## Atomic Transaction Bus



Simple, but low throughput!

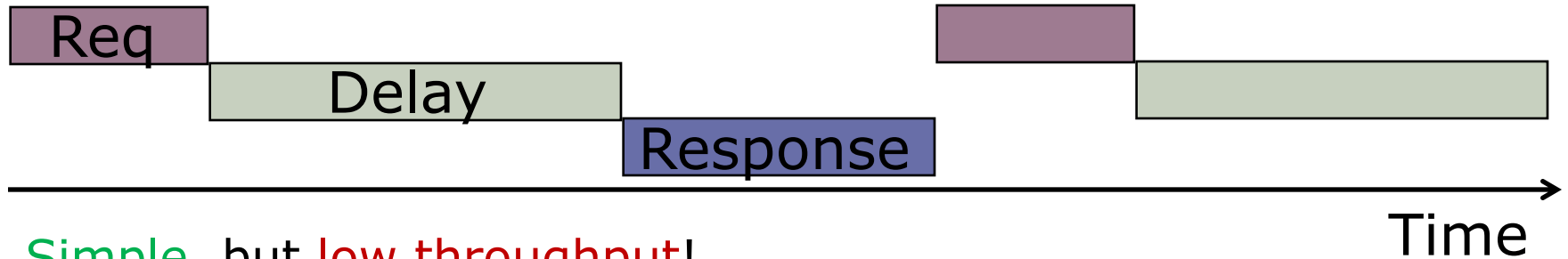
## Split-Transaction Bus



# Split-Transaction and Pipelined Buses

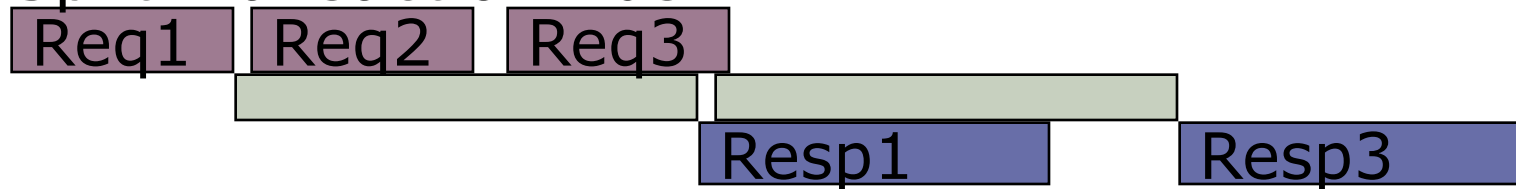
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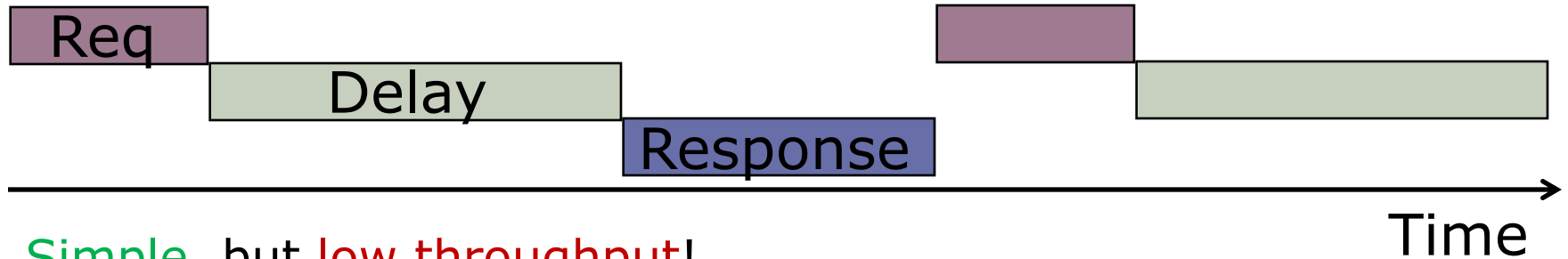


- Supports multiple simultaneous transactions

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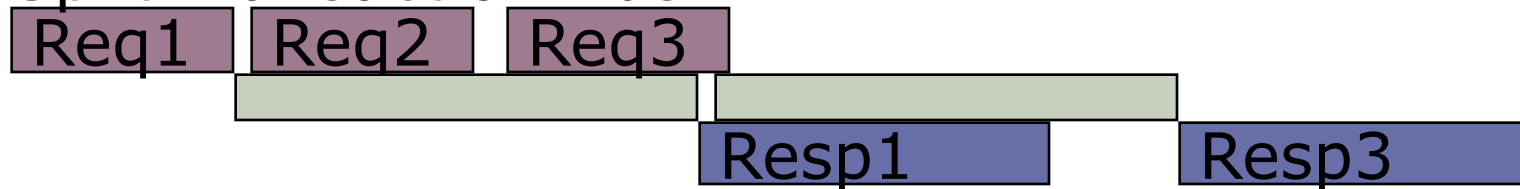
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## Atomic Transaction Bus



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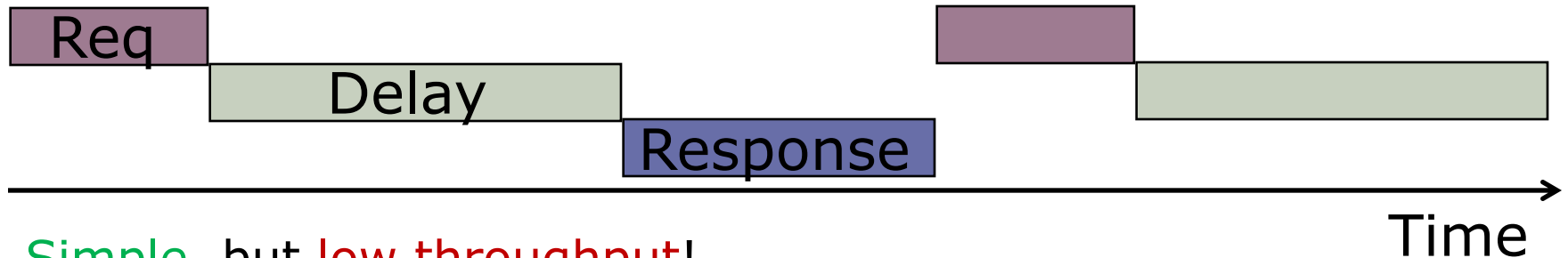


- Supports multiple simultaneous transactions
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  - Responses may arrive out of order

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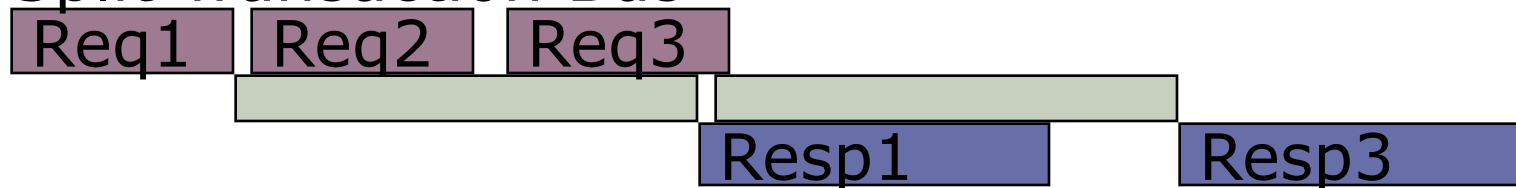
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## Atomic Transaction Bus



Simple, but low throughput!

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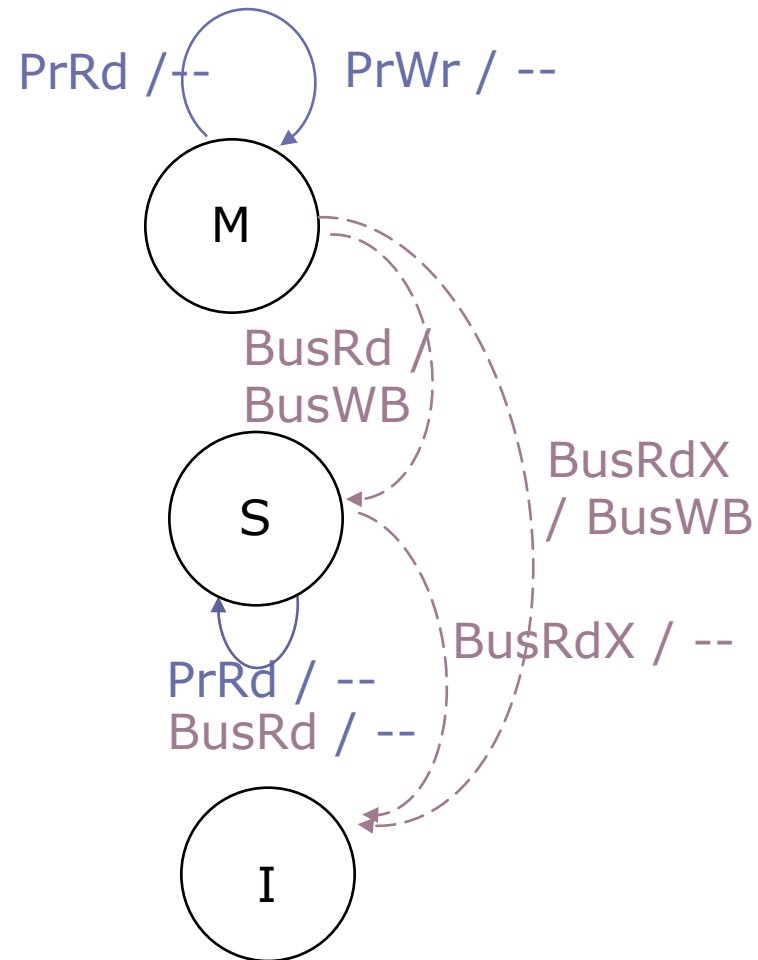


- Supports multiple simultaneous transactions
  - Higher throughput
  - Responses may arrive out of order
- Often implemented as multiple buses (req+resp)

# Non-Atomicity → Transient States

- Protocol must handle lack of atomicity
- Two types of states
  - Stable (e.g. MSI)
  - Transient
- Split + race transitions
- More complex

Actions
Bus Request (BusReq)
Bus Grant (BusGnt)

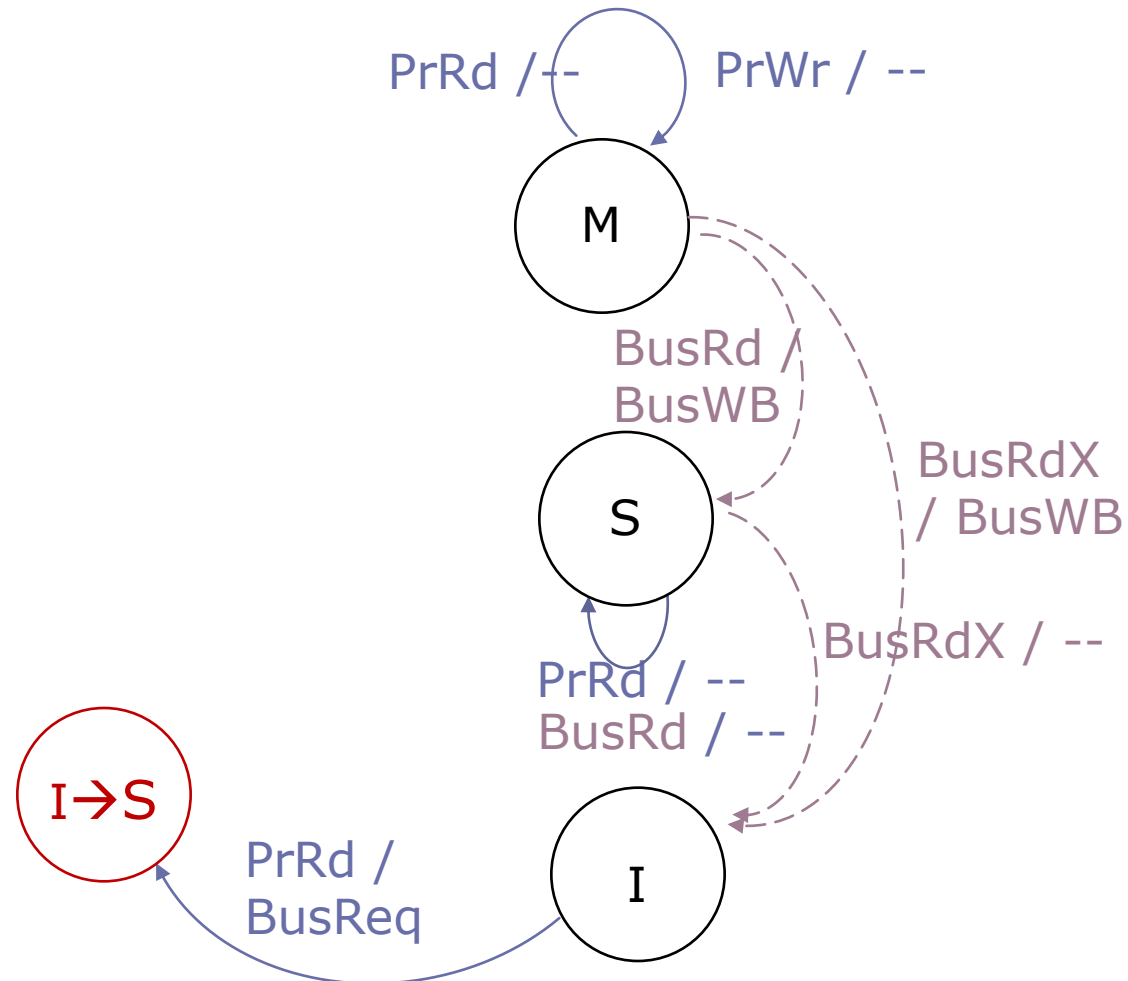




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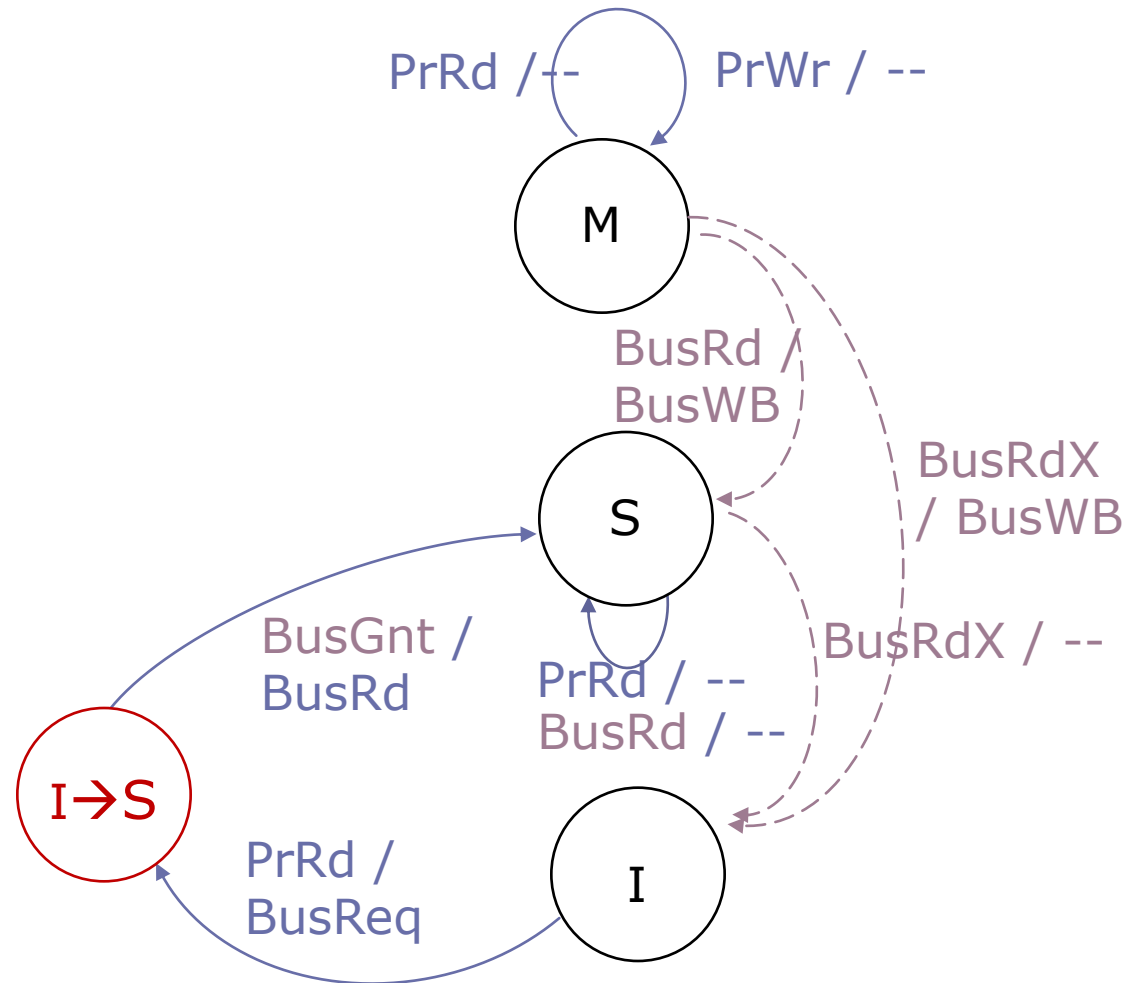
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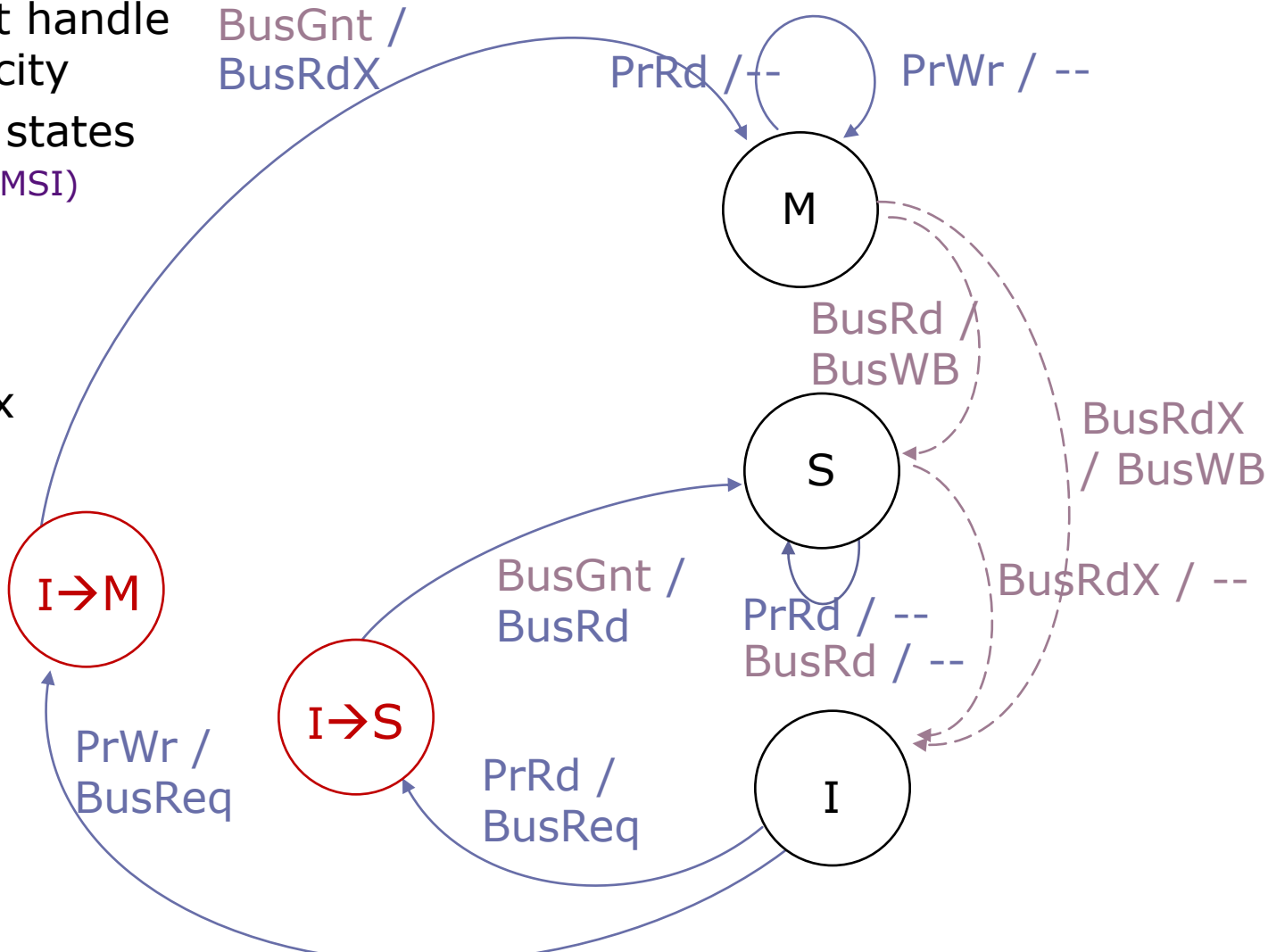
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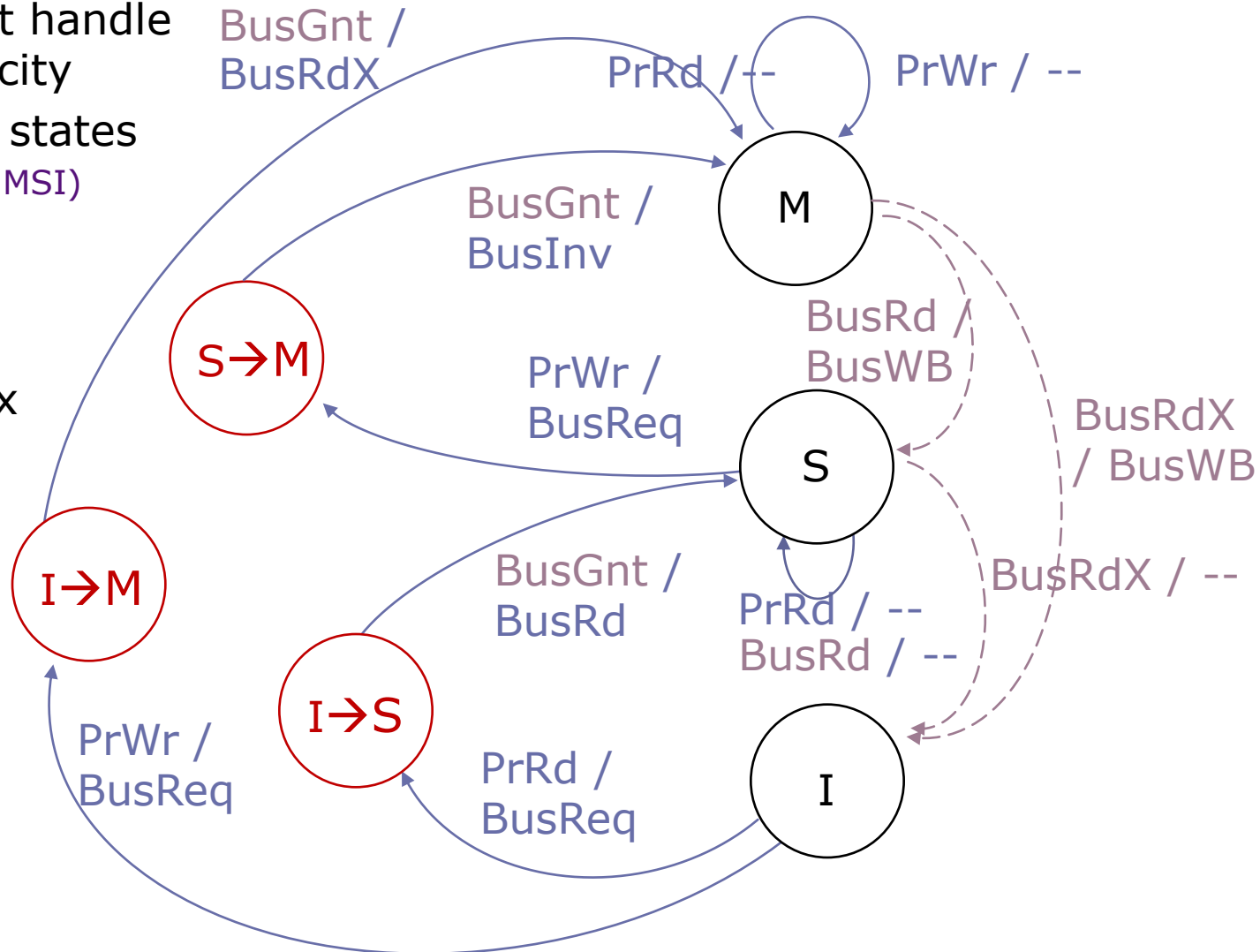
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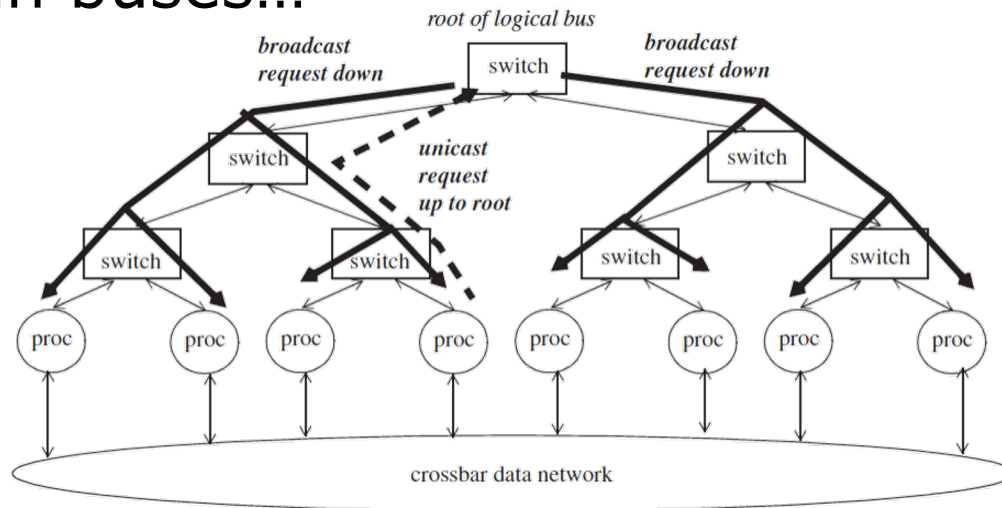
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# Scaling Cache Coherence

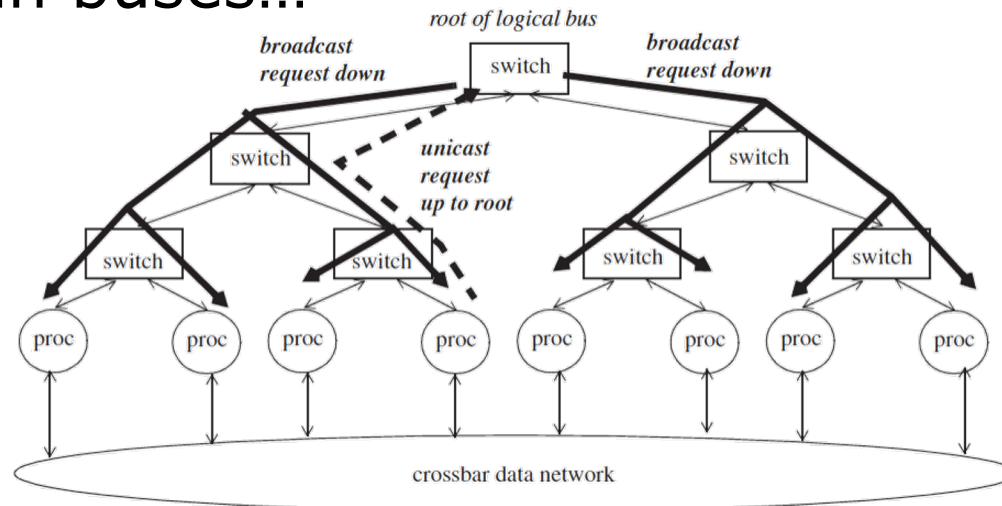
- Can implement ordered interconnects that scale better than buses...



Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors

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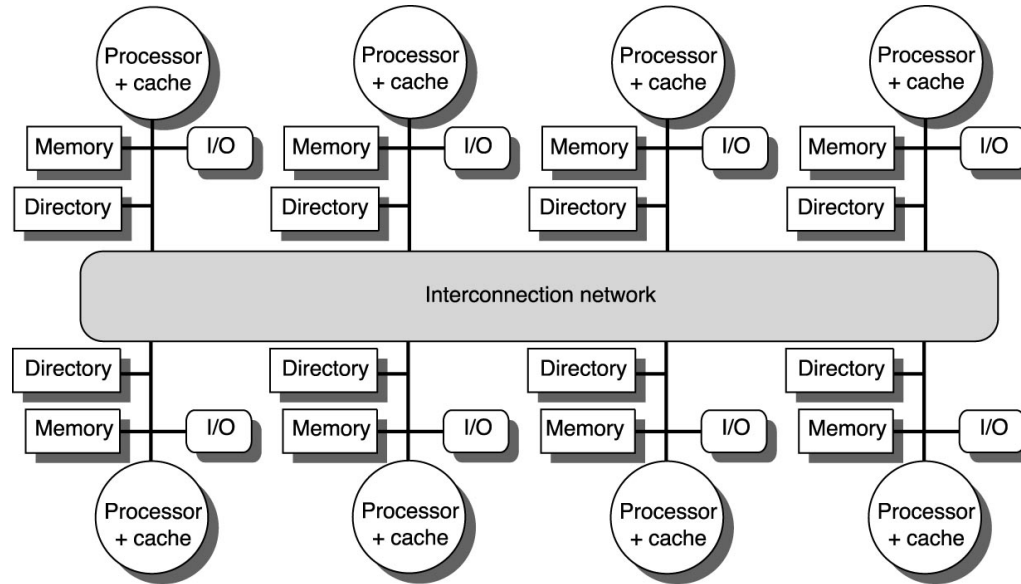


Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors

- ... but broadcast is fundamentally unscalable
  - Bandwidth, energy of transactions with 100s of cache snoops?

# Directory-Based Coherence

---



- Route all coherence transactions through a directory
  - Tracks contents of private caches → No broadcasts
  - Serves as ordering point for conflicting requests → Unordered networks

*(more on next lecture)*

# Coherence and False Sharing

## *Performance Issue #1*

---



A cache block contains more than one word and cache coherence is done at the block-level and not word-level



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Suppose  $P_1$  writes  $word_i$  and  $P_2$  writes  $word_k$  and both words have the same block address.

*What can happen?*

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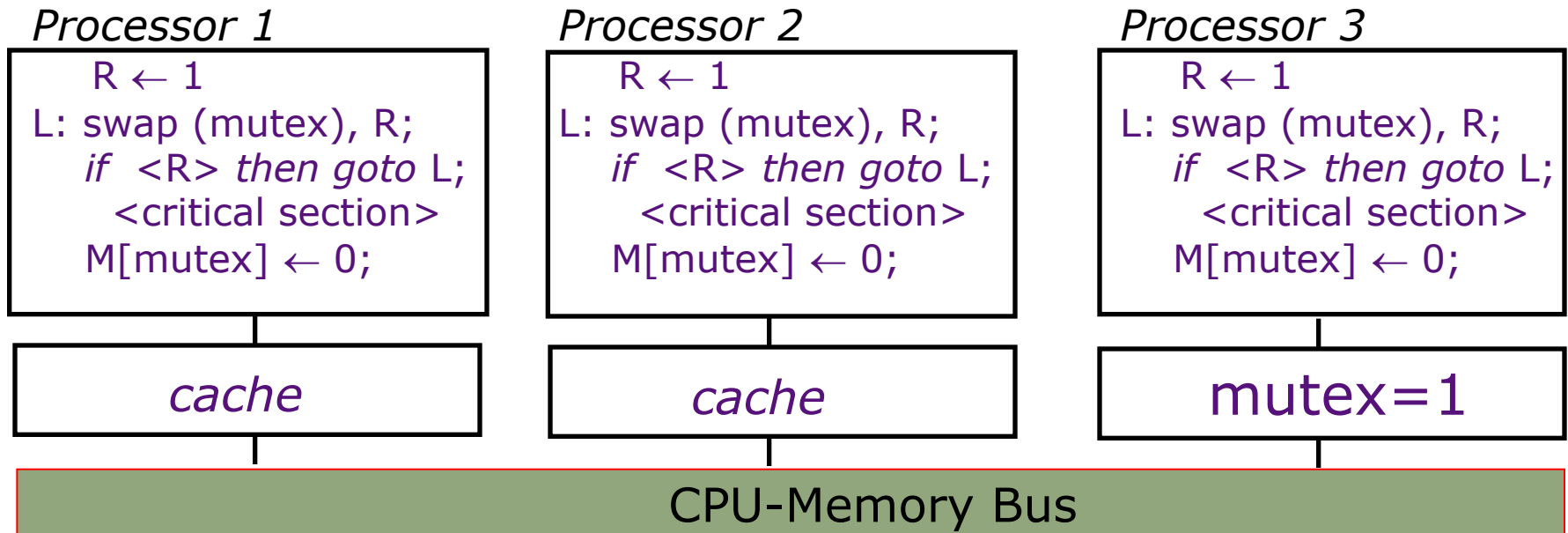
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*How to address this problem?*

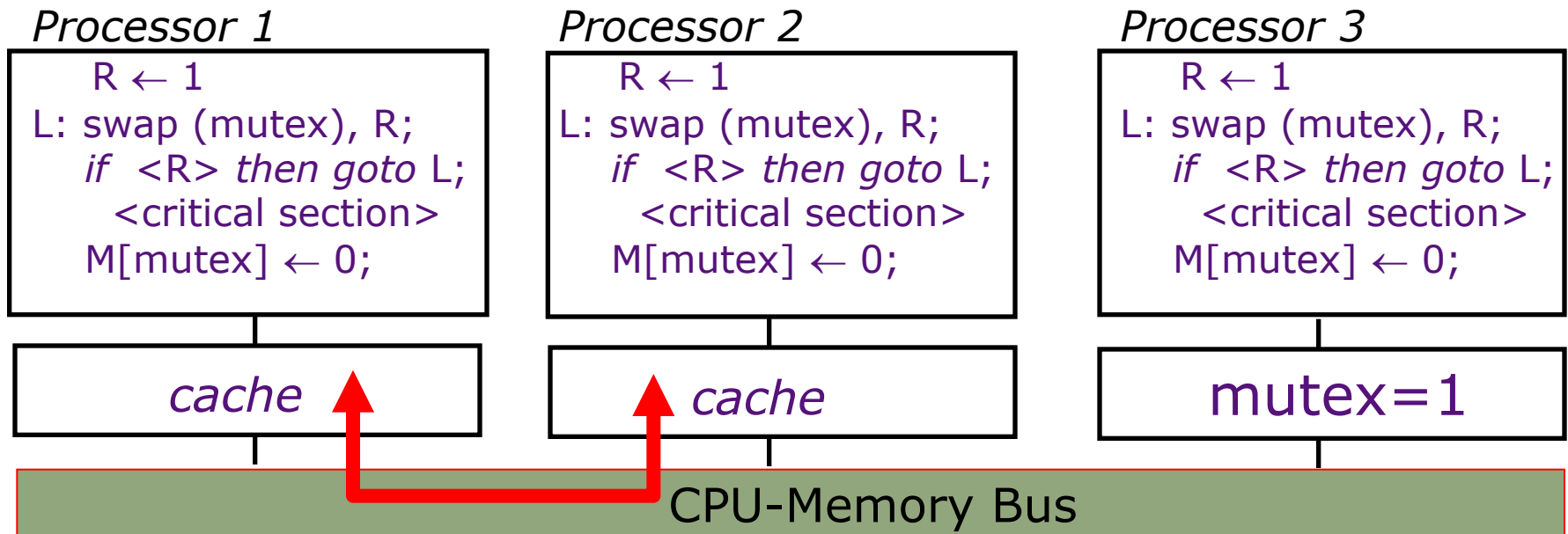
# Coherence and Synchronization

## Performance Issue #2



# Coherence and Synchronization

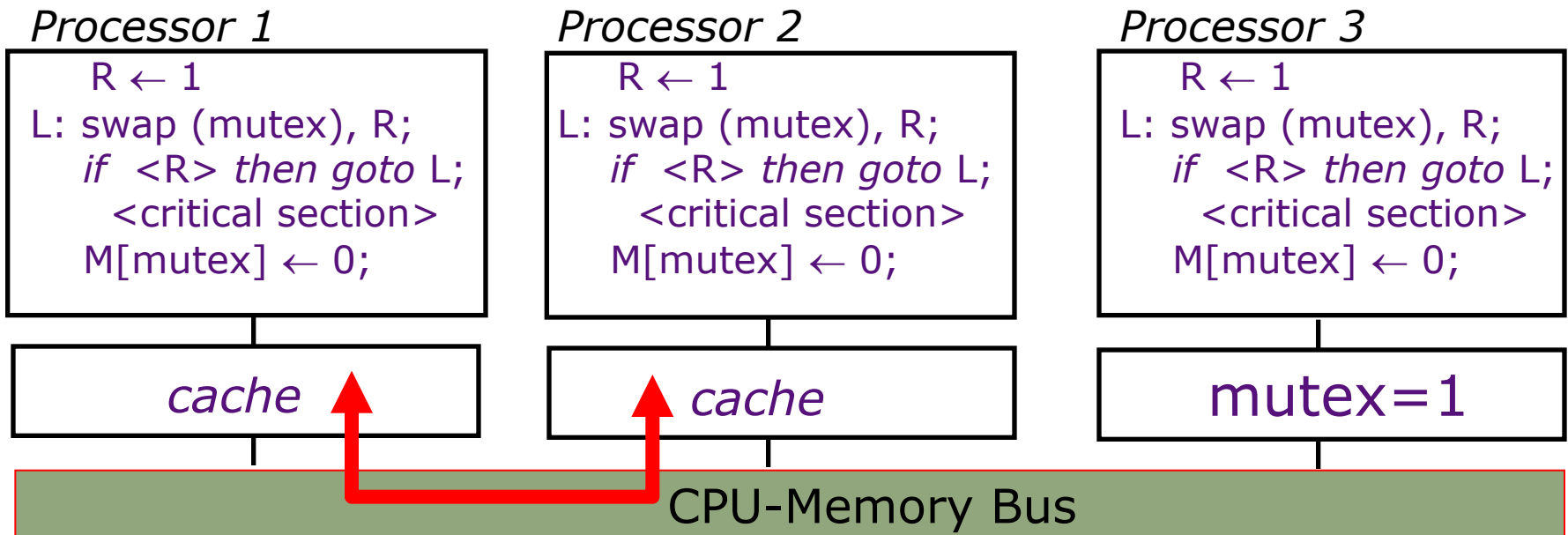
## Performance Issue #2



Cache coherence protocols will cause **mutex** to *ping-pong* between P1's and P2's caches.

# Coherence and Synchronization

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Cache coherence protocols will cause **mutex** to *ping-pong* between P1's and P2's caches.

Ping-ponging can be reduced by first reading the **mutex** location (*non-atomically*) and executing a swap only if it is found to be zero (test&test&set).

# Coherence and Bus Occupancy

## Performance Issue #3

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  - ⇒ *very expensive* for split-transaction buses



# Coherence and Bus Occupancy

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- In general, an *atomic read-modify-write* instruction requires two memory (bus) operations without intervening memory operations by other processors
- In a multiprocessor setting, bus needs to be locked for the entire duration of the atomic read and write operation
  - ⇒ expensive for simple buses
  - ⇒ *very expensive* for split-transaction buses
- modern processors use
  - load-reserve*
  - store-conditional*

# Load-reserve & Store-conditional

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Special register(s) to hold reservation flag and address, and the outcome of store-conditional

```
Load-reserve R, (a):  
  <flag, adr> ← <1, a>;  
  R ← M[a];
```

```
Store-conditional (a), R:  
  if <flag, adr> == <1, a>  
  then cancel other procs'  
    reservation on a;  
    M[a] ← <R>;  
    status ← succeed;  
  else status ← fail;
```

If the snooper sees a store transaction to the address in the reserve register, the reserve bit is set to **0**

- Several processors may reserve 'a' simultaneously
- These instructions are like ordinary loads and stores with respect to the bus traffic

# Performance:

## *Load-reserve & Store-conditional*

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The total number of memory (bus) transactions is not necessarily reduced, but splitting an atomic instruction into load-reserve & store-conditional:

- *increases bus utilization* (and reduces processor stall time), especially in split-transaction buses
- *reduces cache ping-pong effect* because processors trying to acquire a mutex do not have to perform stores each time

*Thank you!*

*Next lecture: Directory-based  
Cache Coherence*