Virtualization and Security

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Based on slides from Daniel Sanchez

Evolution in Number of Users

IBM 1620
1959

Single User

Runtime loaded with program

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IBM 360
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Multiple Users

OS for sharing resources

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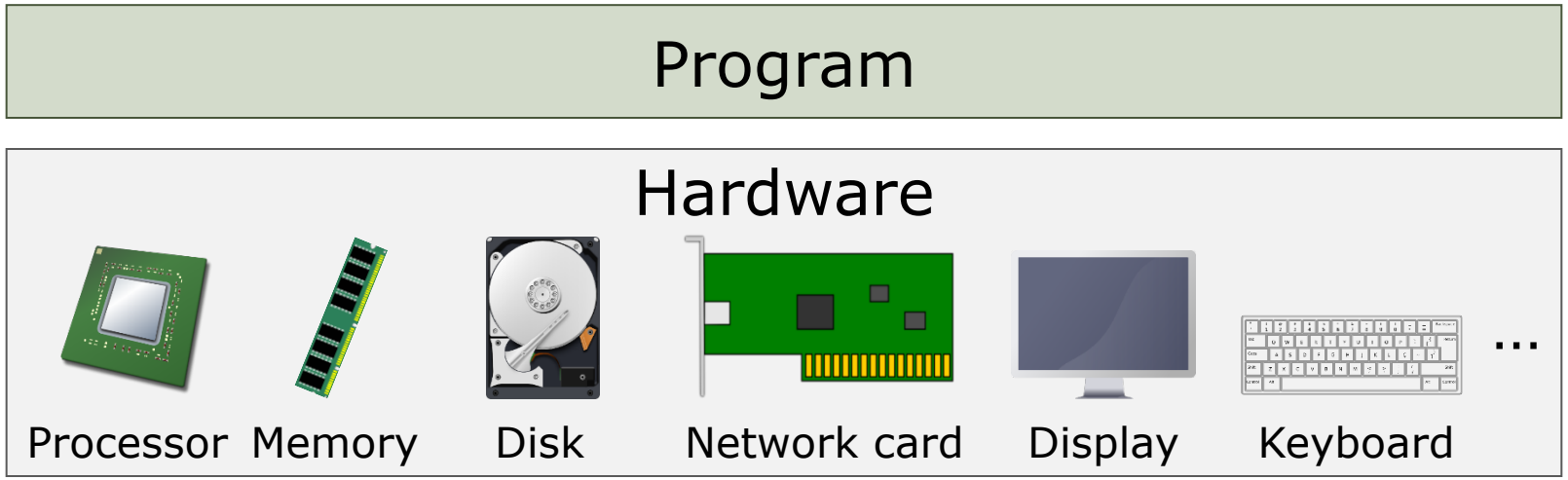
Runtime loaded with program	OS for sharing resources	OS for sharing resources	Multiple OSs

Single-Program Machine



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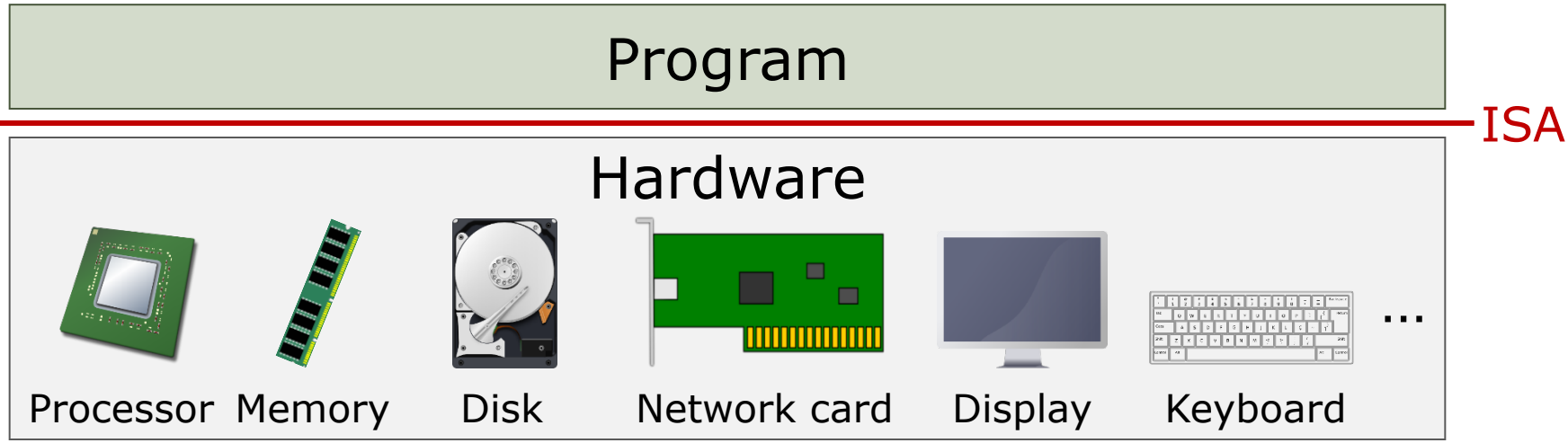

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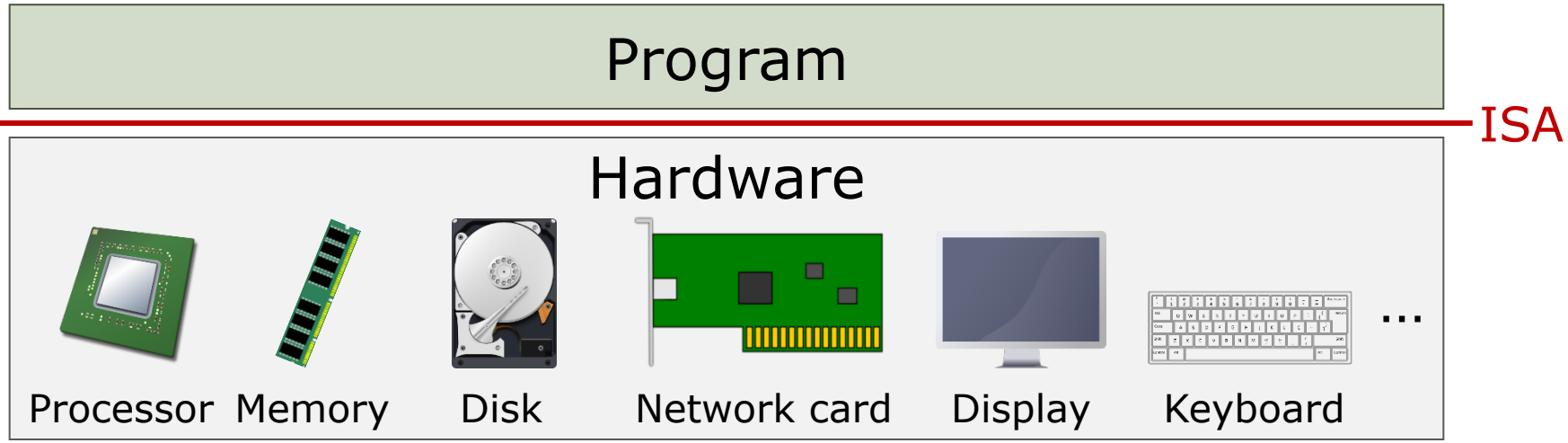

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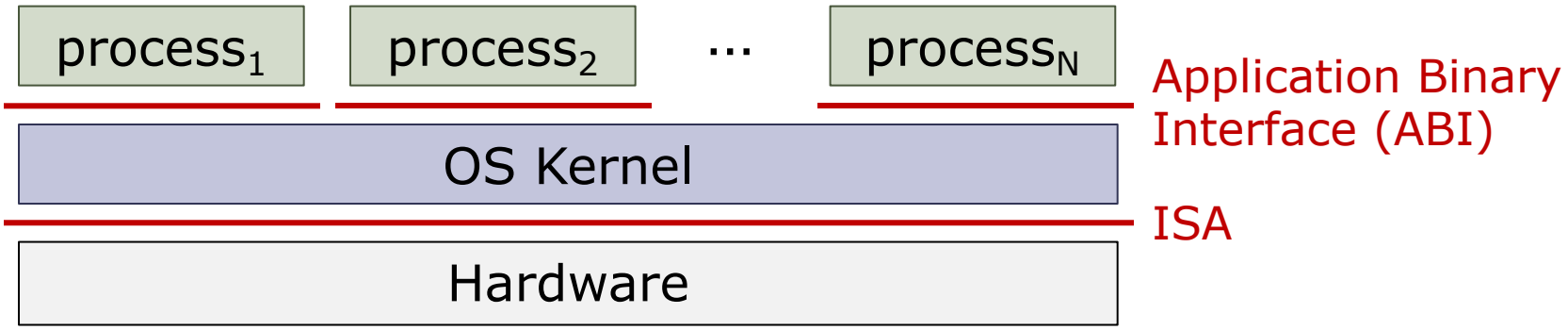
- This program has direct and complete access to all hardware resources in the machine
- The instruction set architecture (ISA) is the interface between software and hardware

Operating Systems



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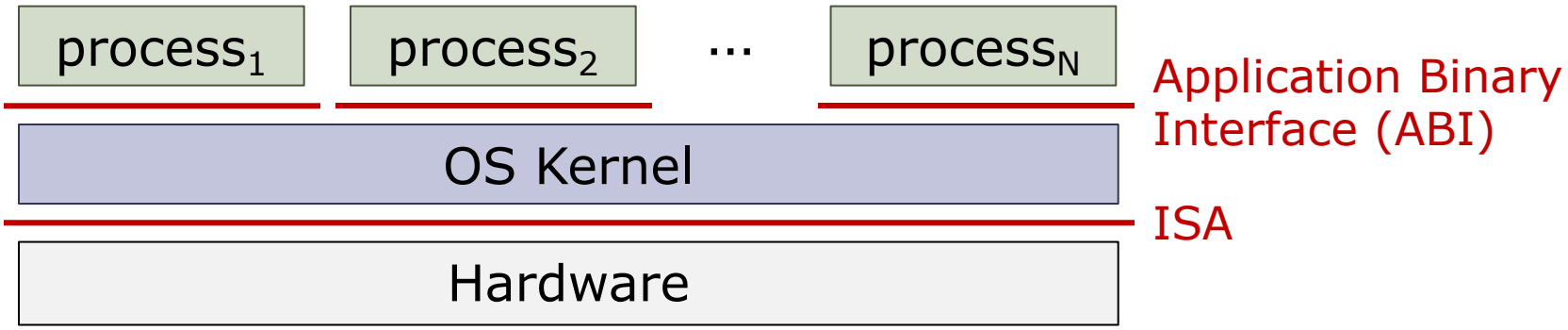

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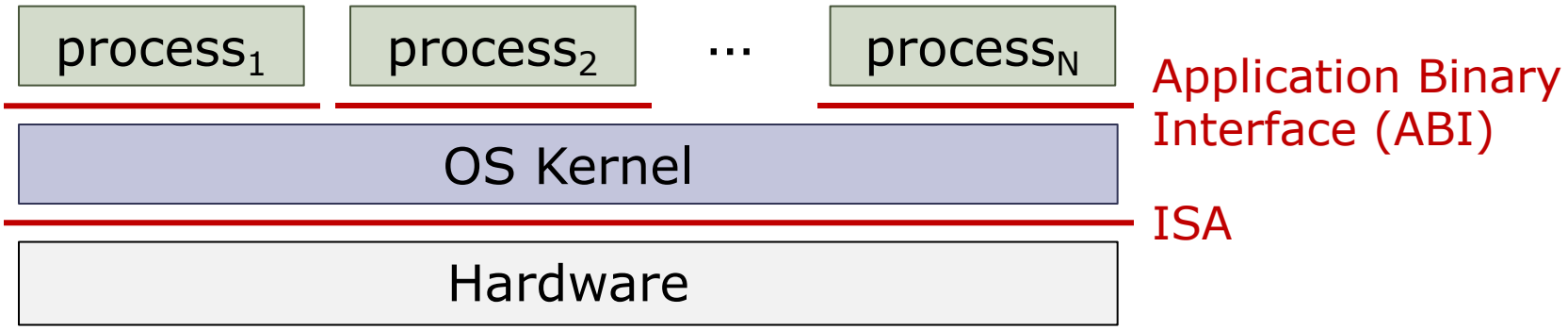

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  - Protection and privacy: Processes cannot access each other's data
  - Abstraction: OS hides details of underlying hardware
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  - Resource management: OS controls how processes share hardware (CPU, memory, disk, etc.)

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- The OS kernel provides a private address space to each process
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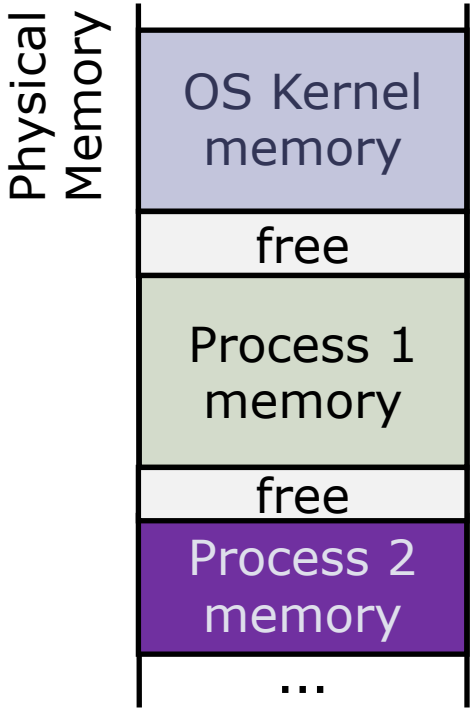

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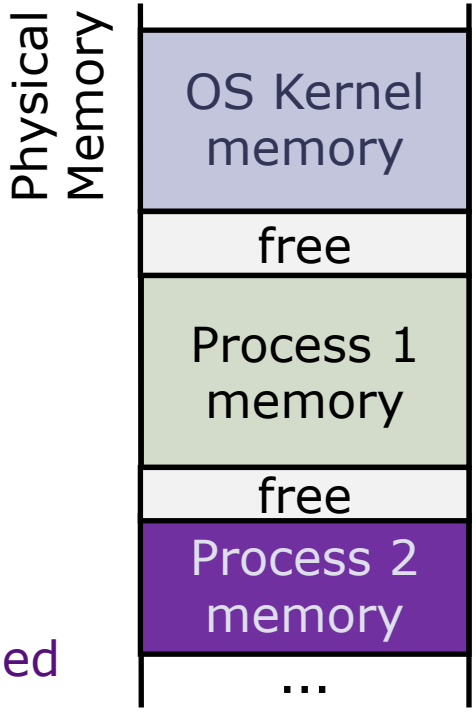

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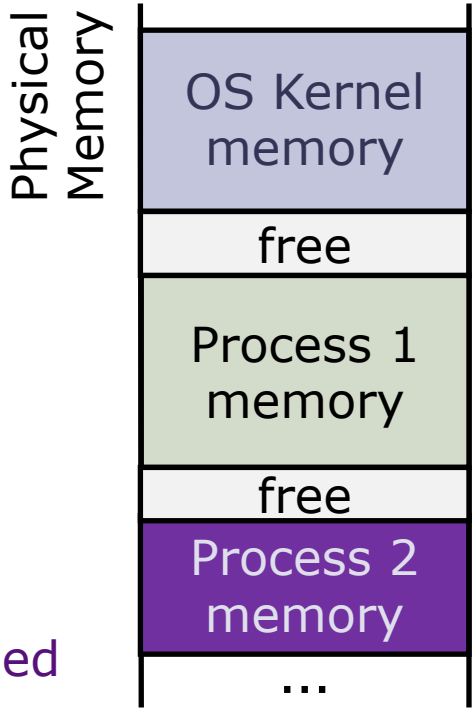

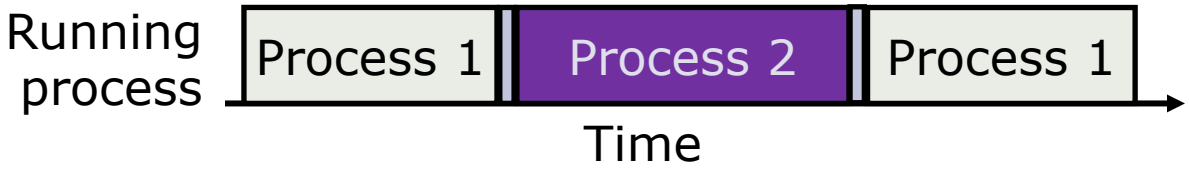

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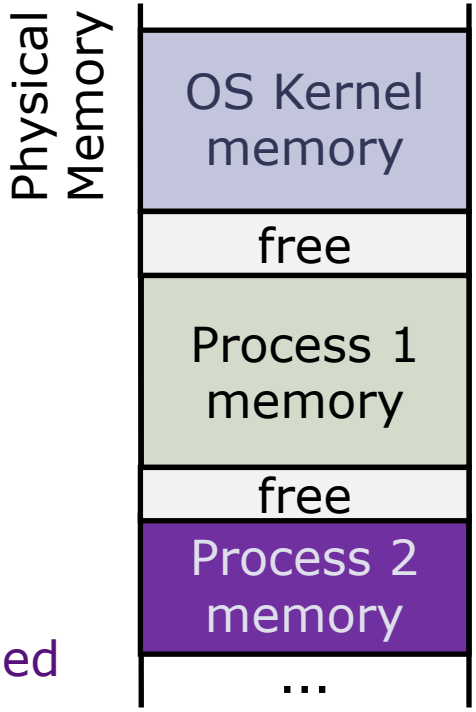

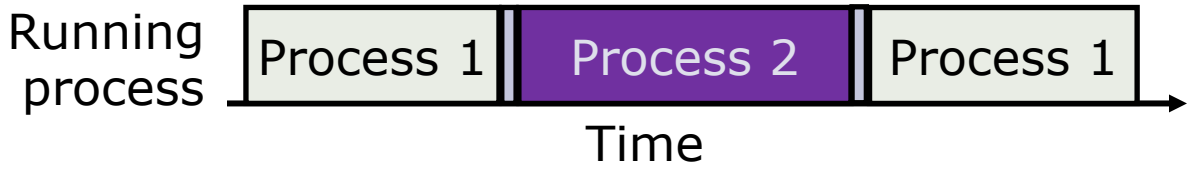

- The OS kernel lets processes invoke system services (e.g., access files or network sockets) via system calls

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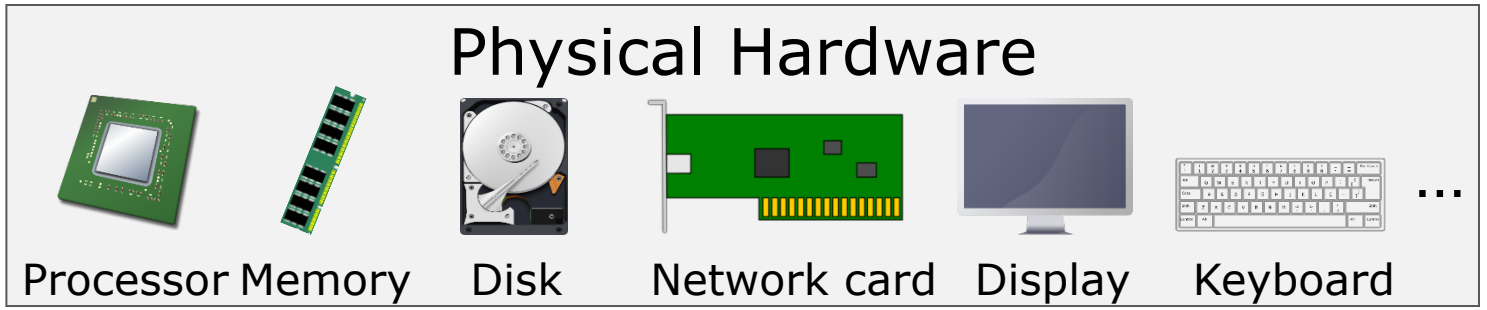

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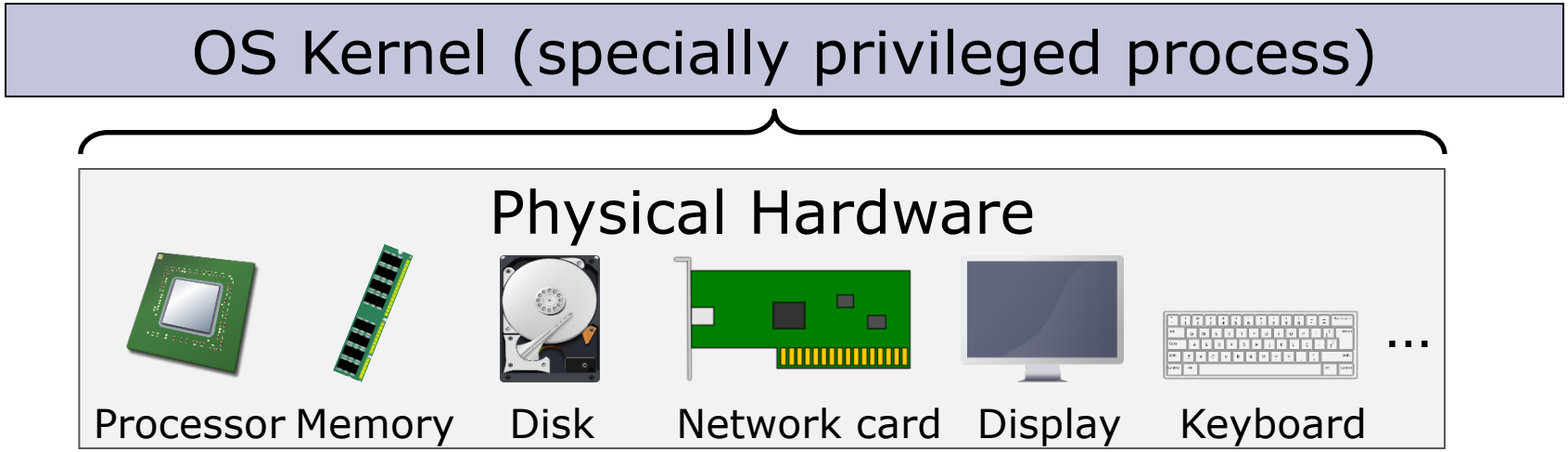

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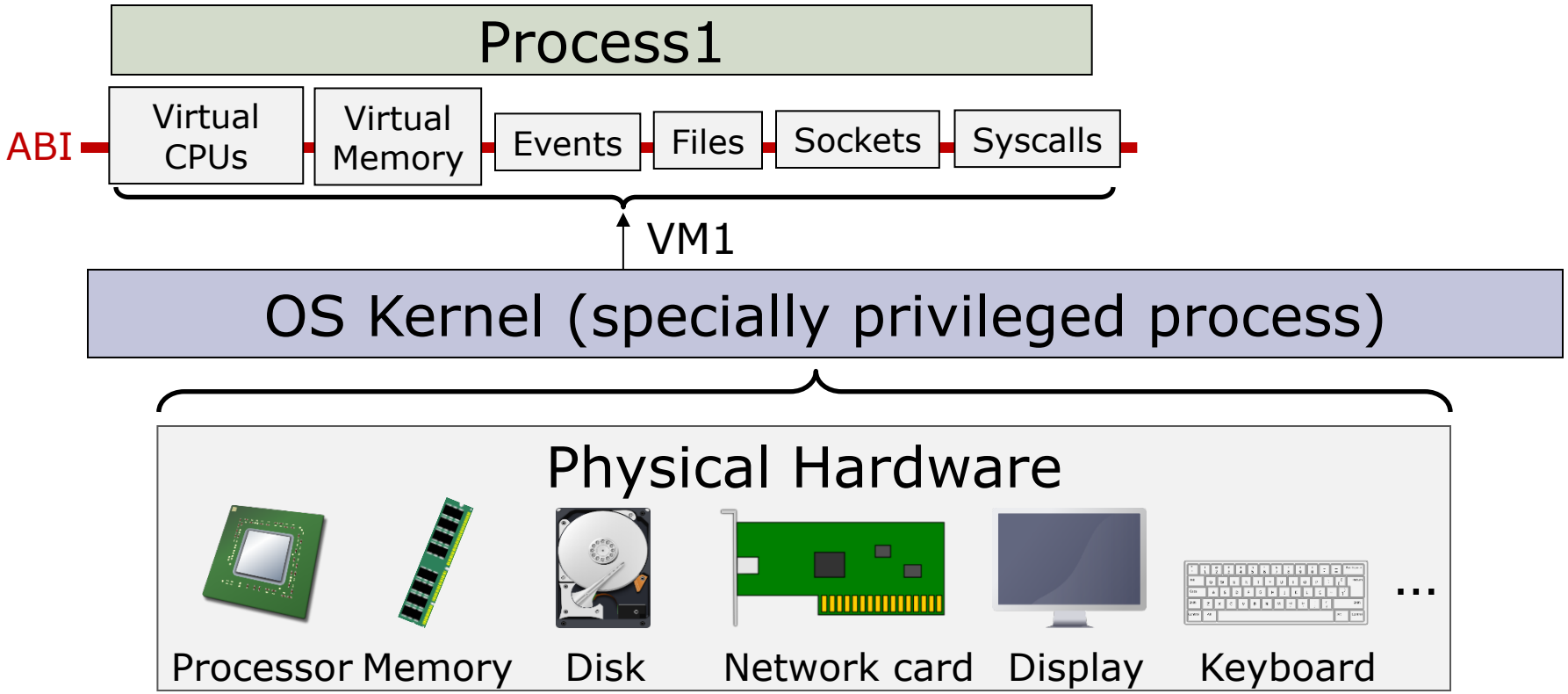

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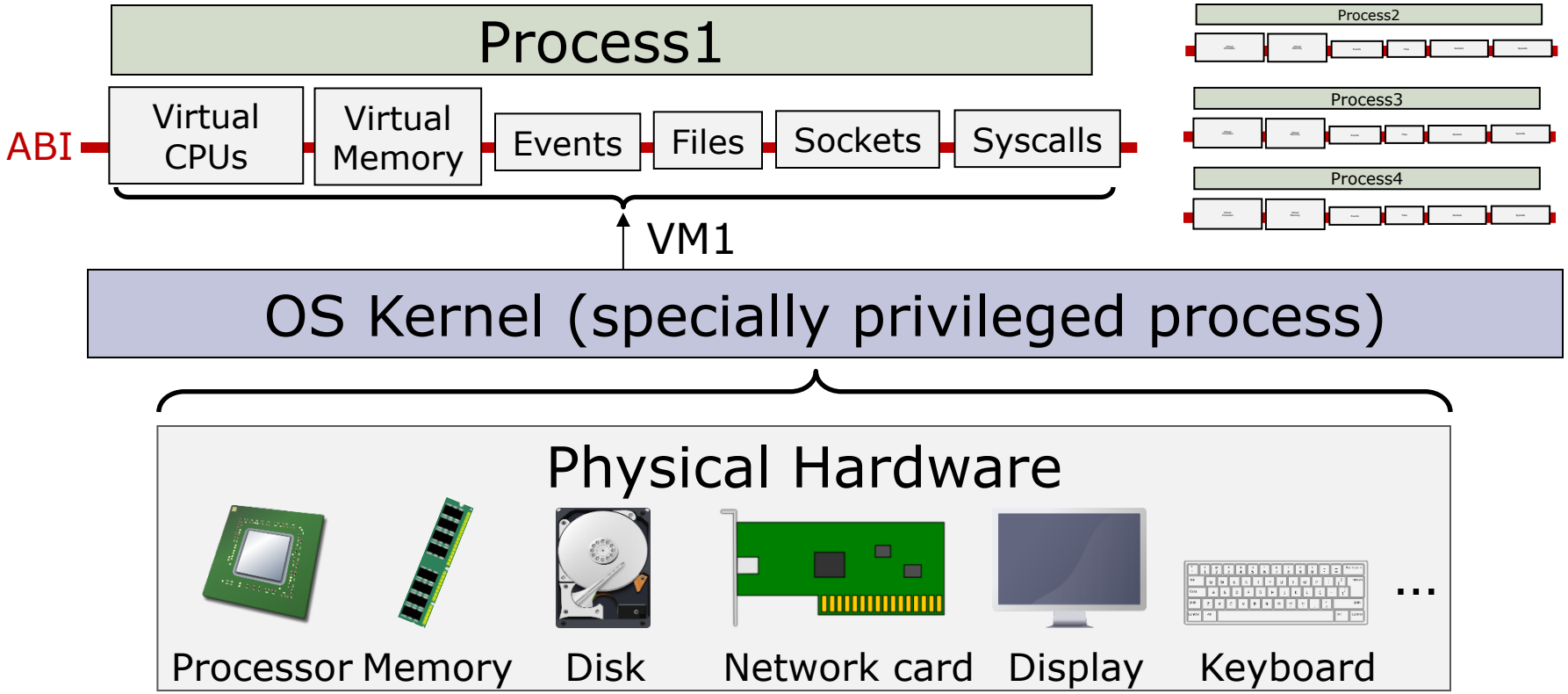
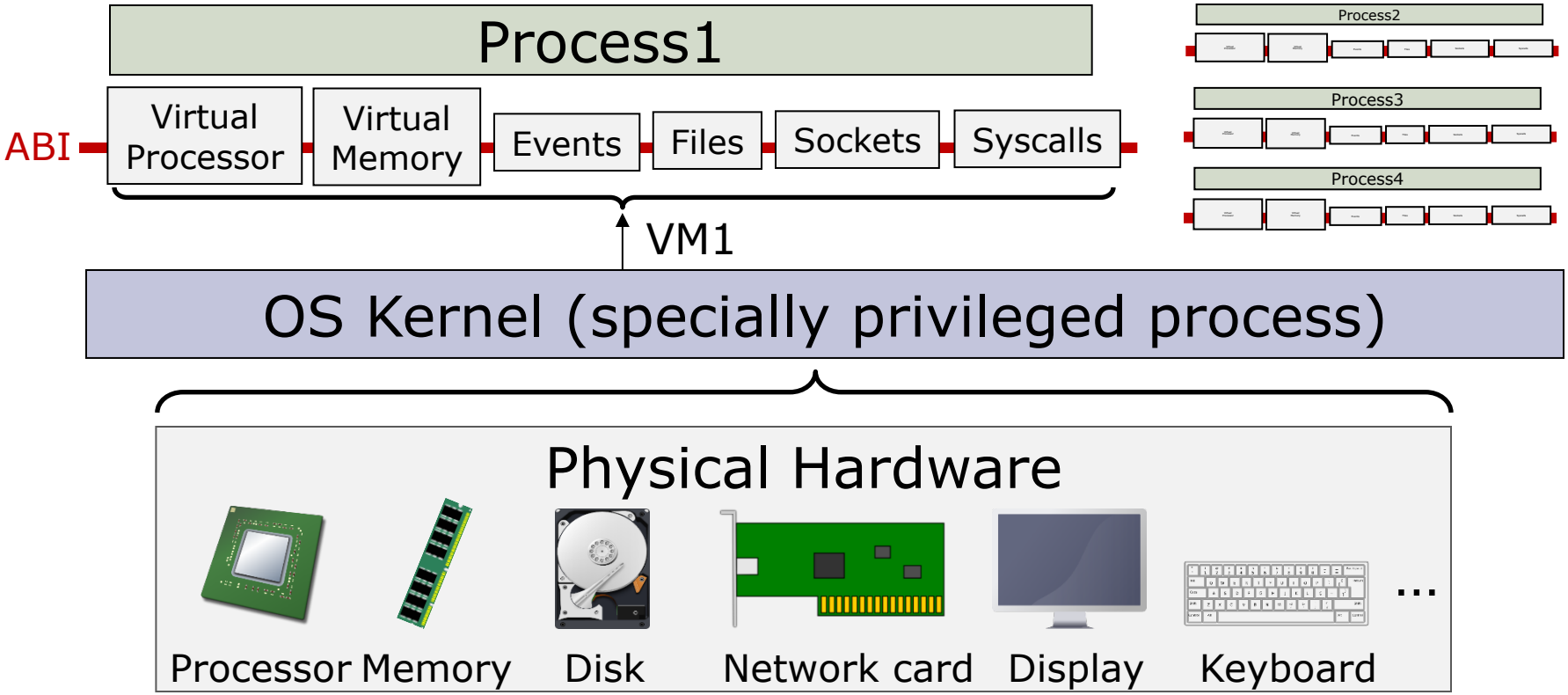


Virtual Machines

- A Virtual Machine (VM) is an emulation of a computer system
  - Very general concept, used beyond operating systems



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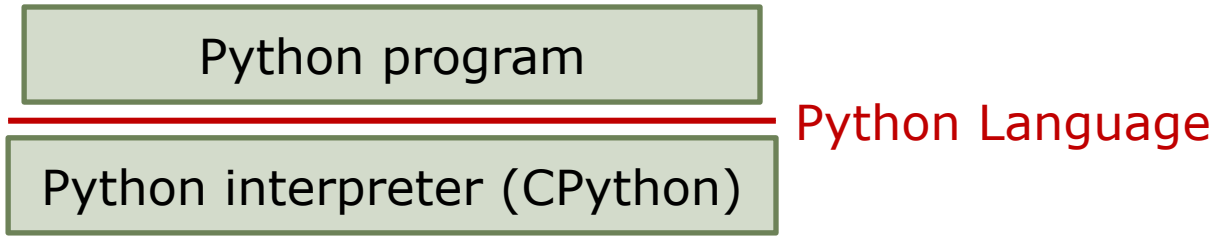

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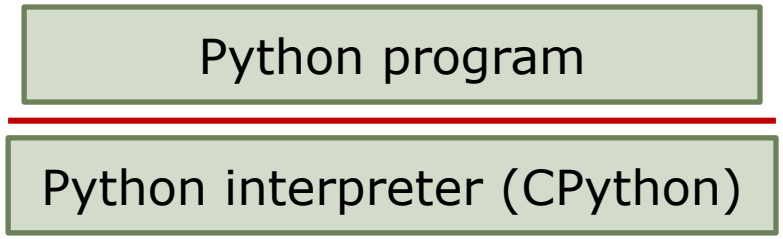

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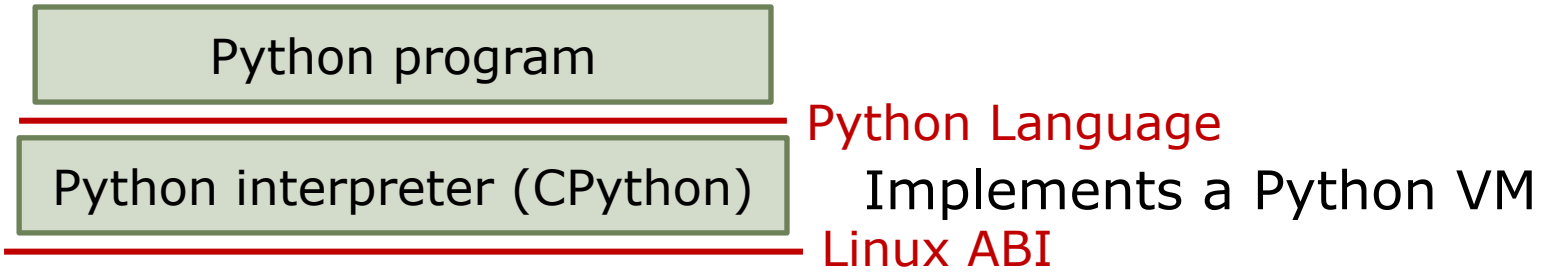

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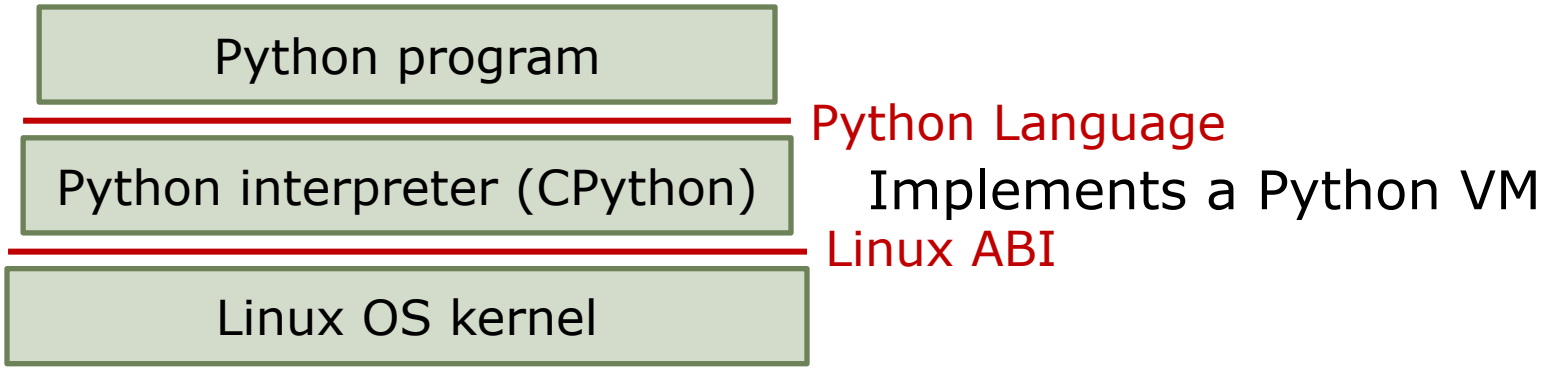

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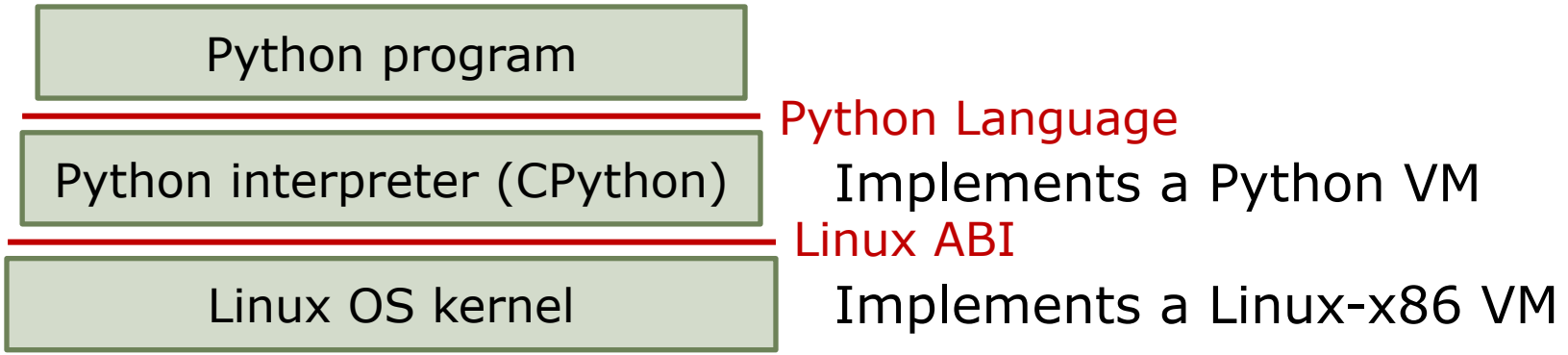

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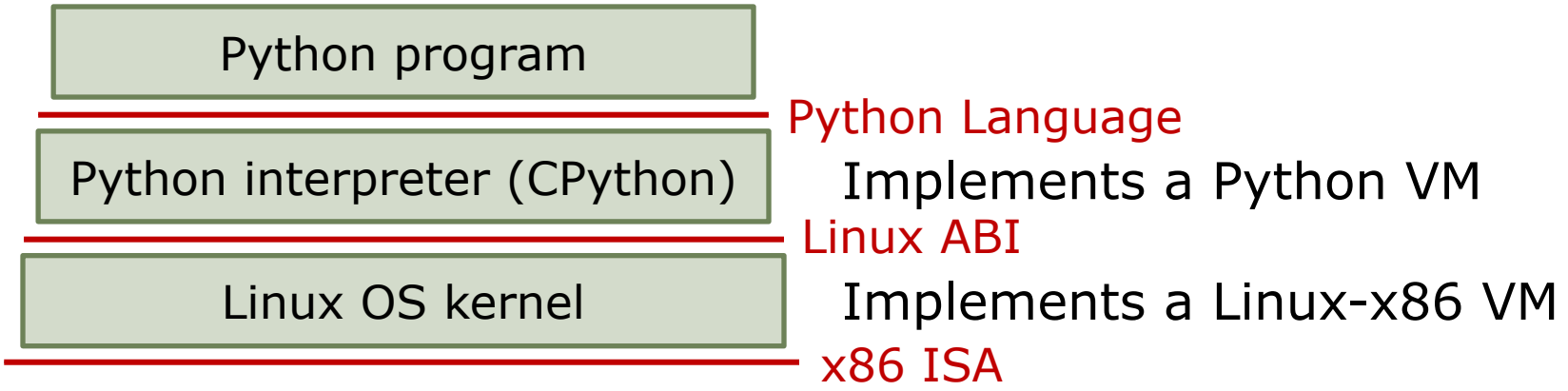

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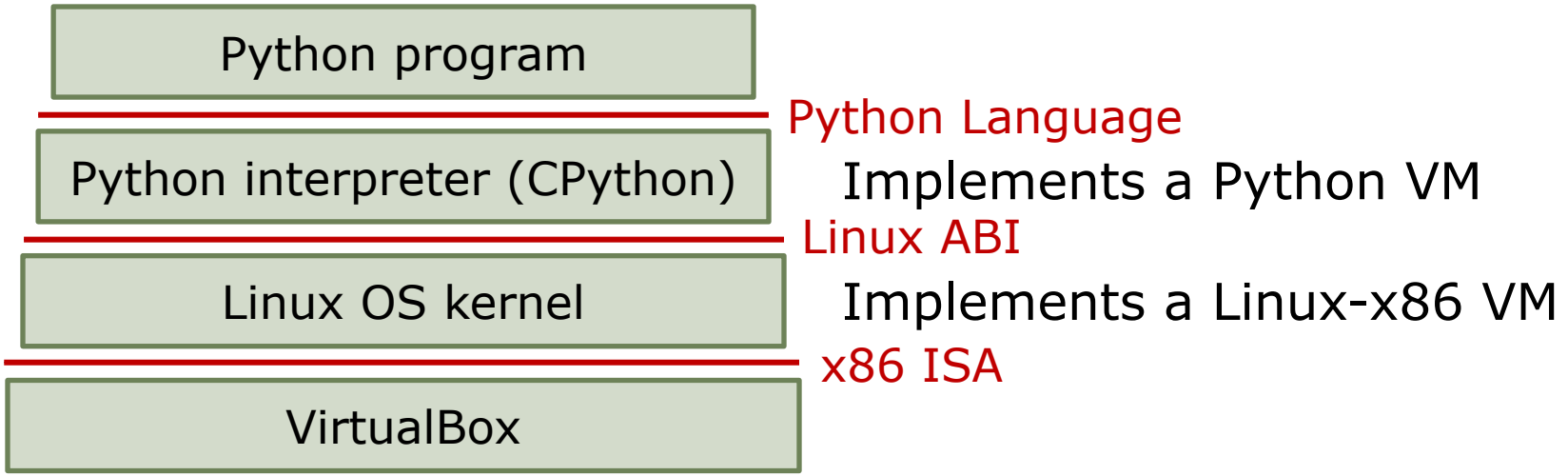

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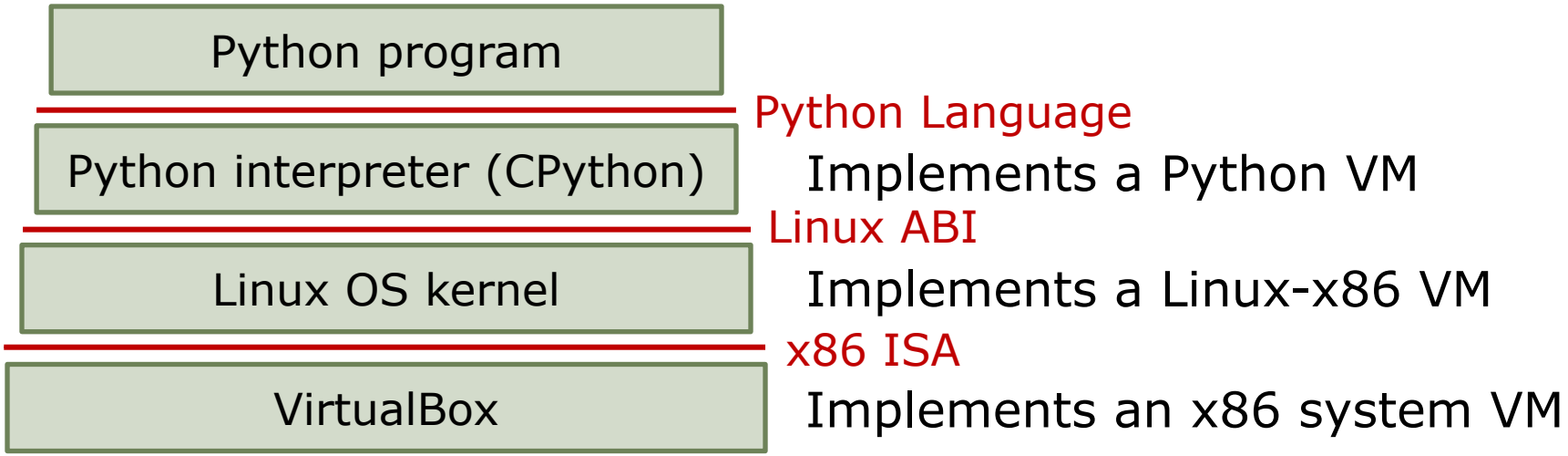

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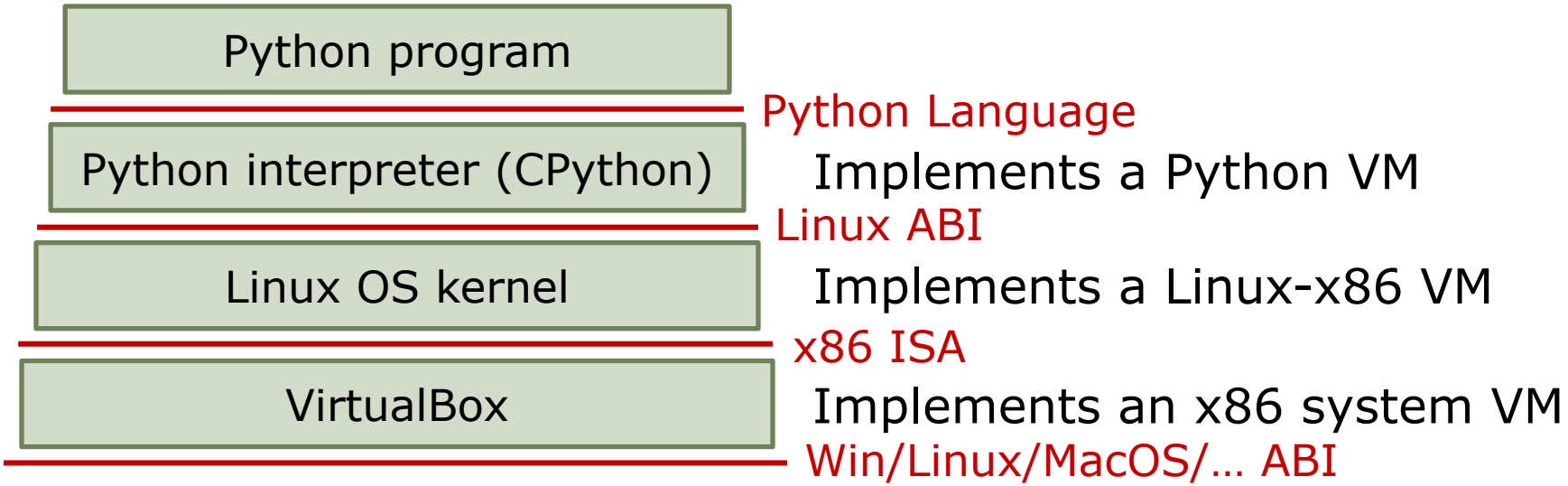

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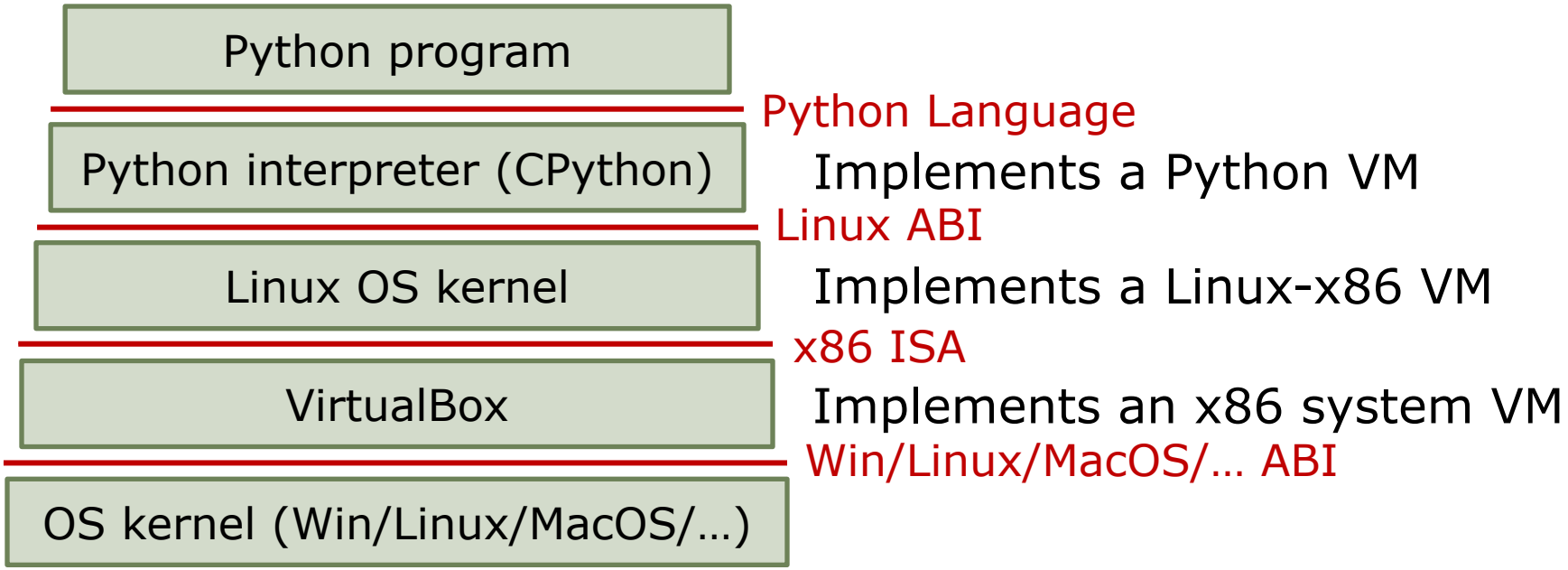

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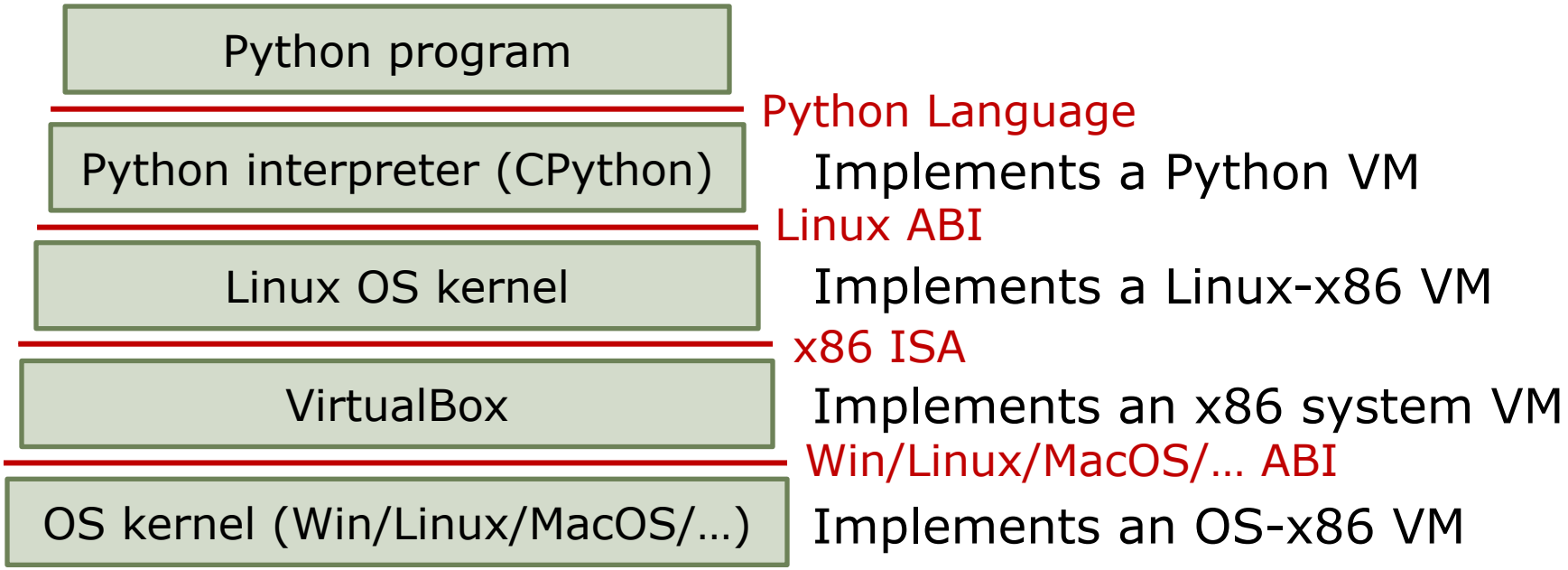

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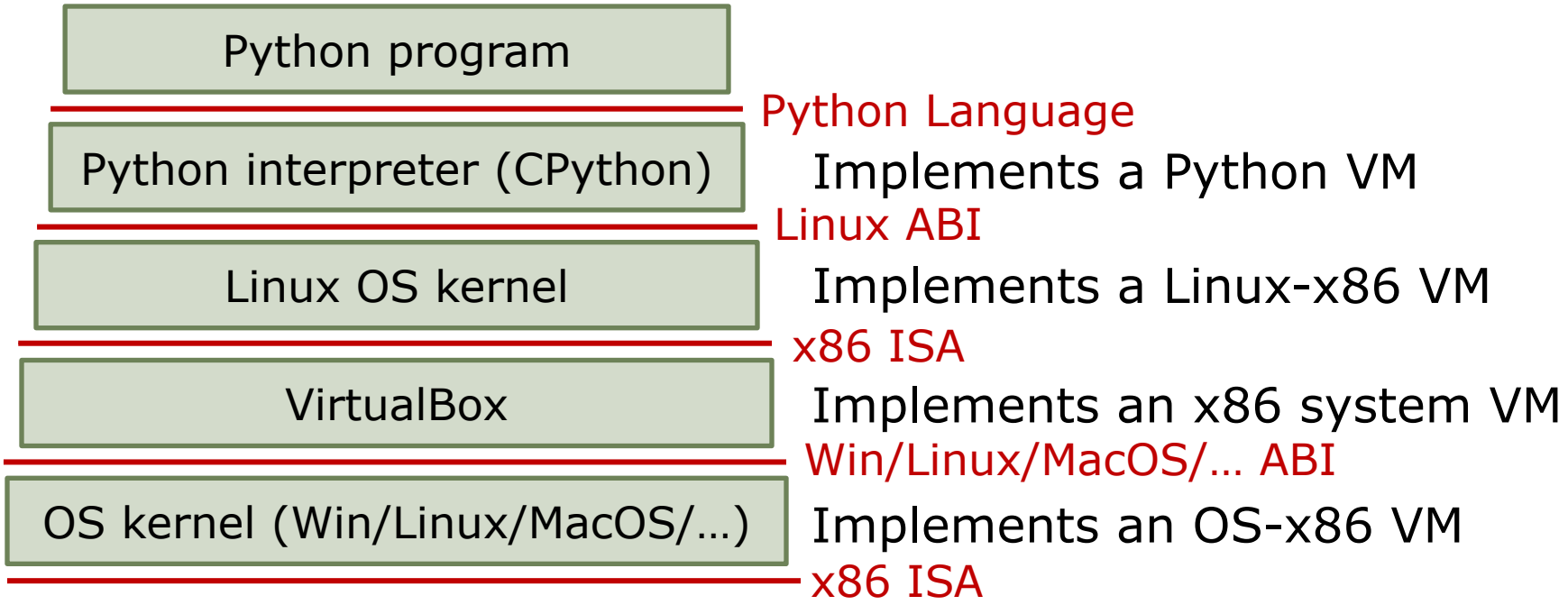

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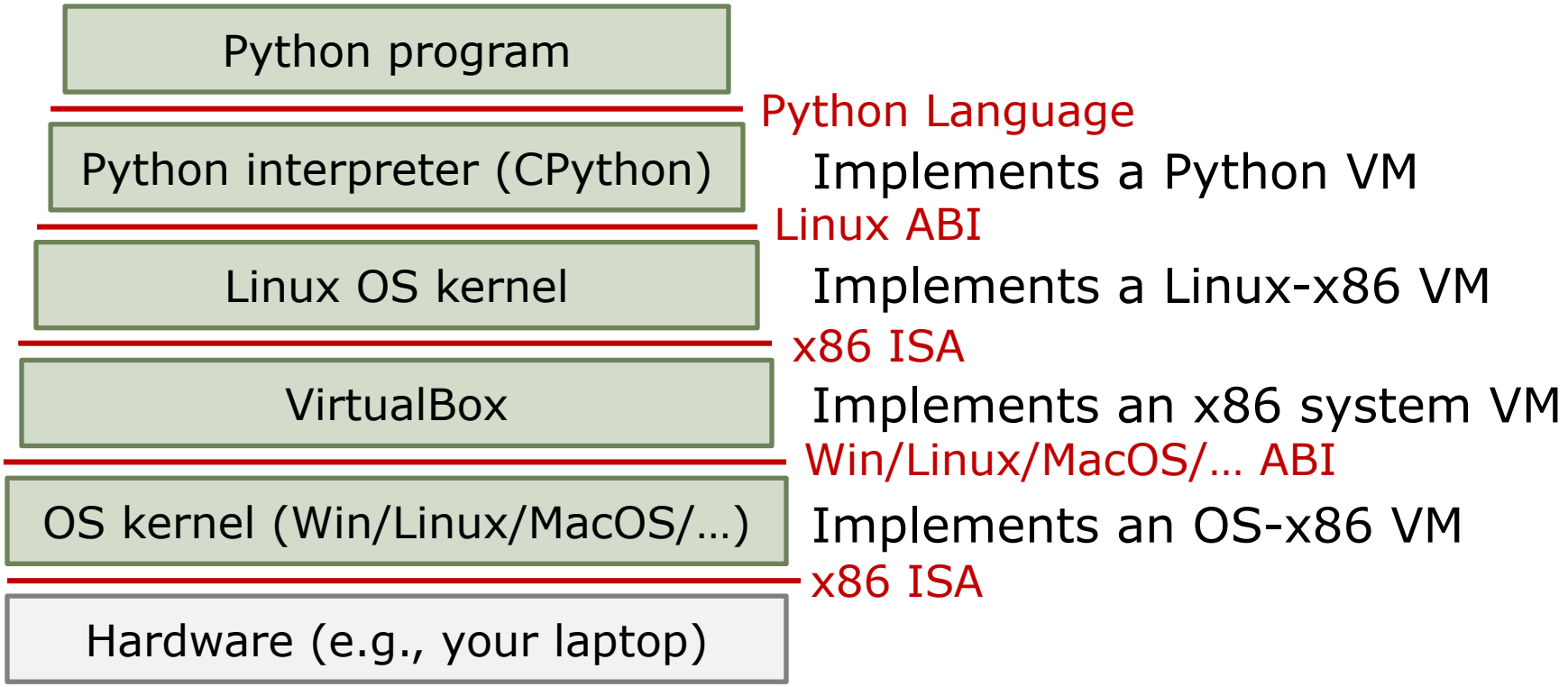

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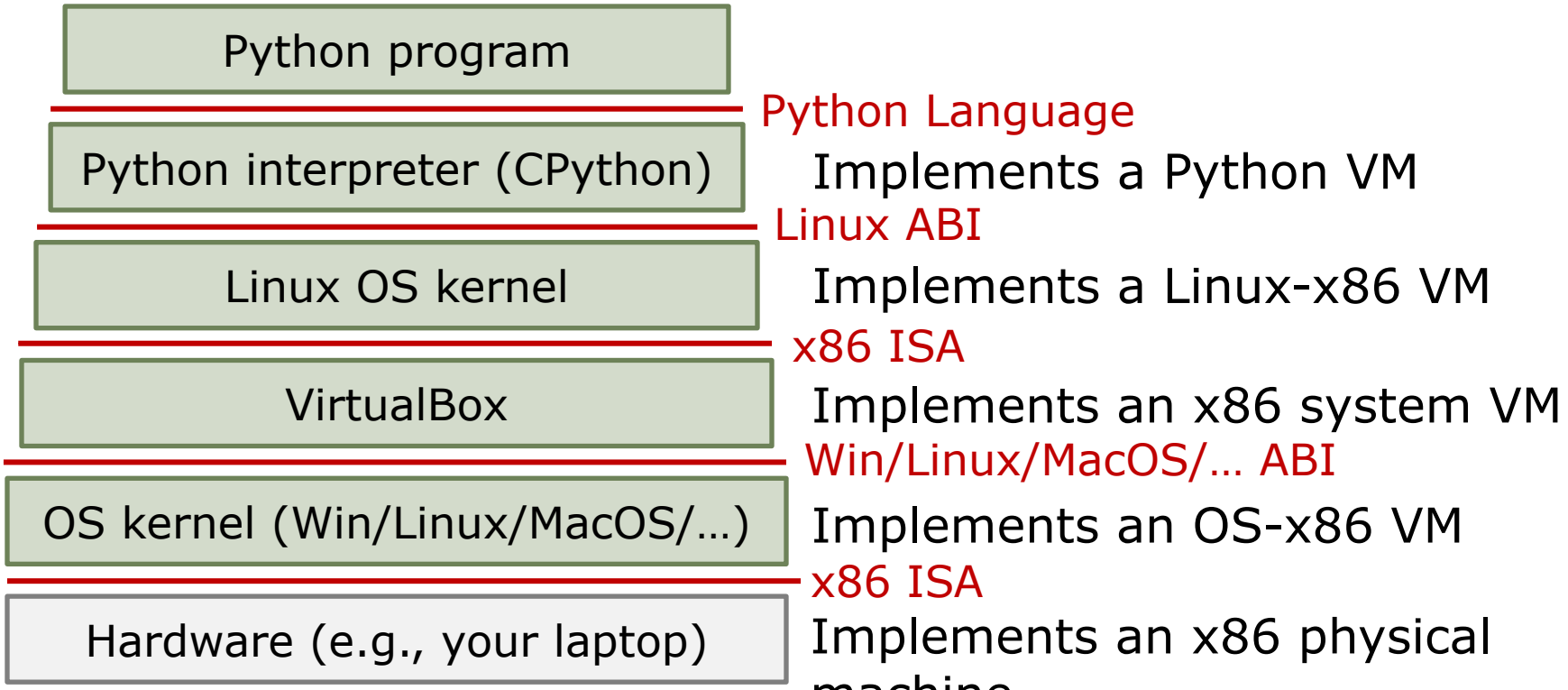

Implementing Virtual Machines

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- We want to support virtual machines with minimal overheads → need hardware support!

ISA Extensions to Support OS

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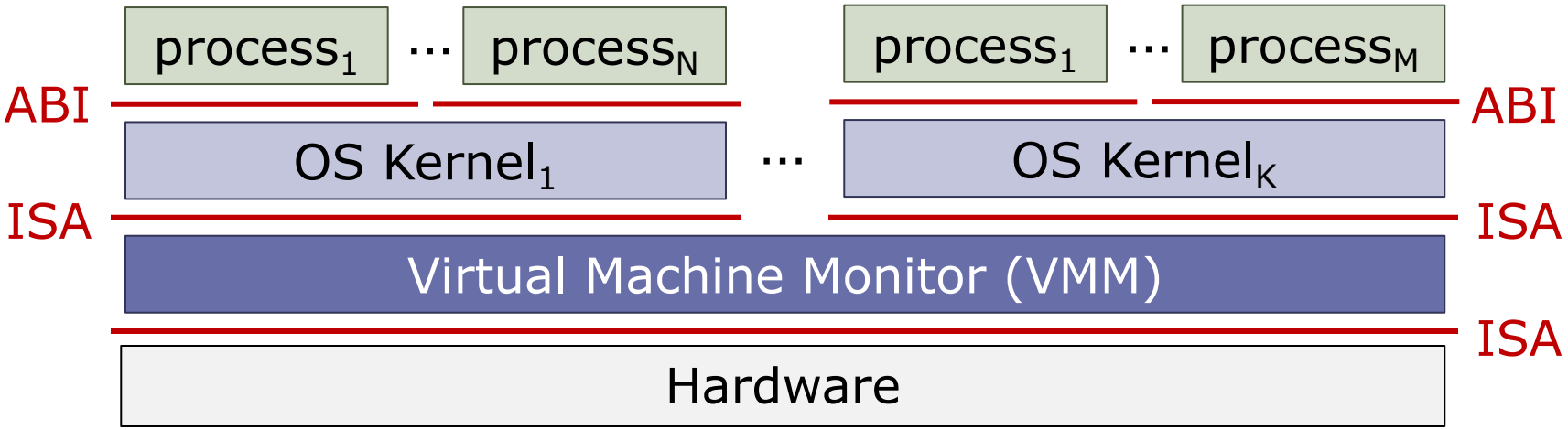
- Virtual memory to provide private address spaces and abstract the storage resources of the machine

Supporting Multiple OSs



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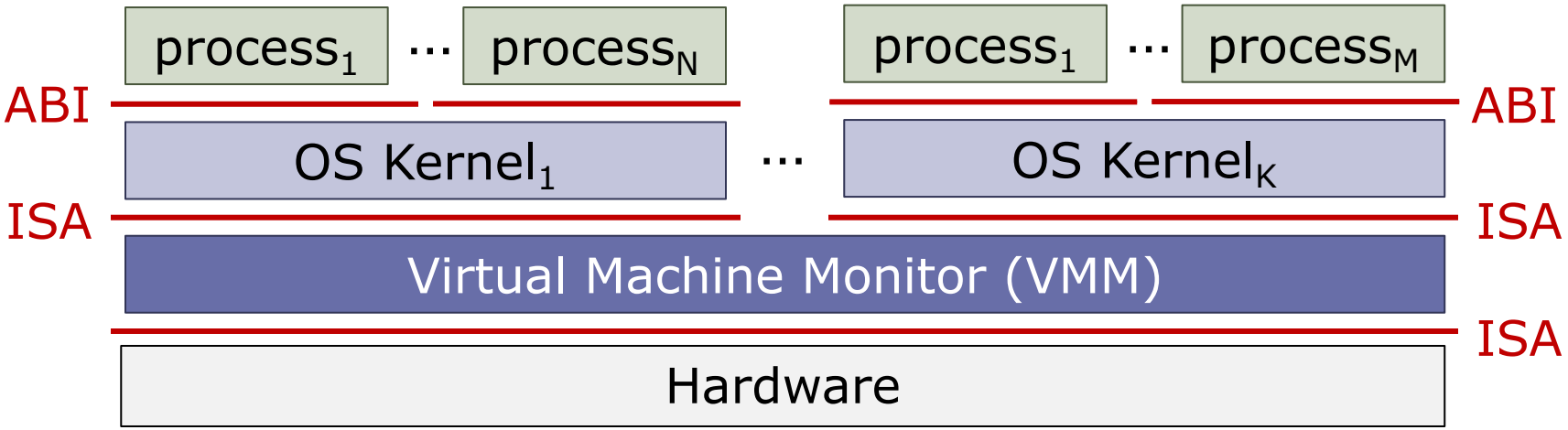

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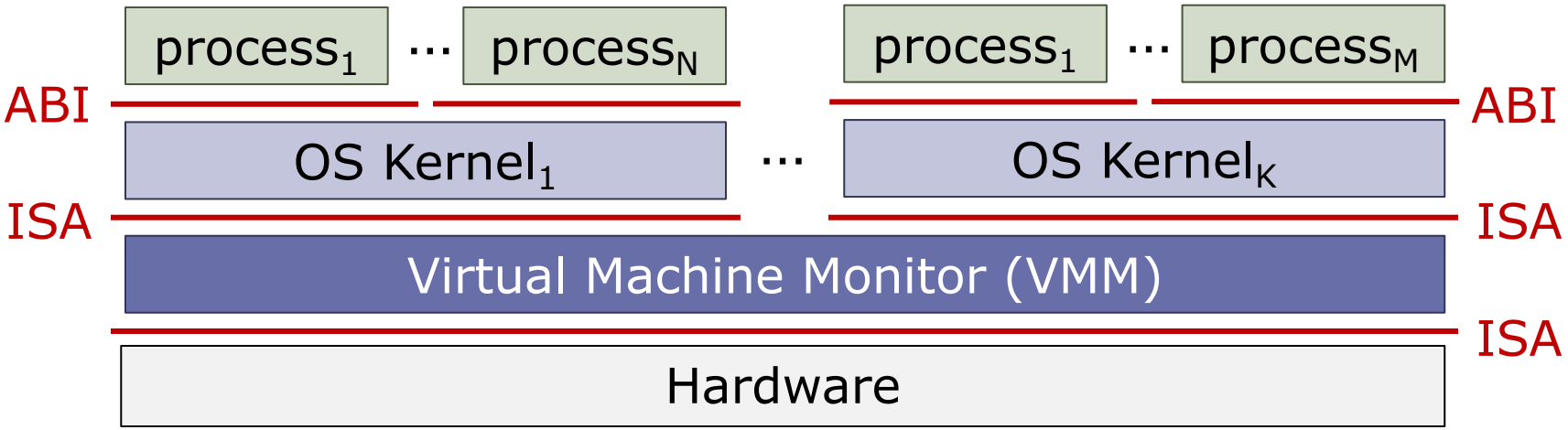

- A VMM (aka Hypervisor) provides a system virtual machine to each OS
- VMM can run directly on hardware (as above) or on another OS
  - Precisely, VMM can be implemented against an ISA (as above) or a process-level ABI. Who knows what lays below the interface…

Motivation for Multiple OSs

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- Allows for load balancing and migration across multiple machines.
- Allows operating system development without making entire machine unstable or unusable.

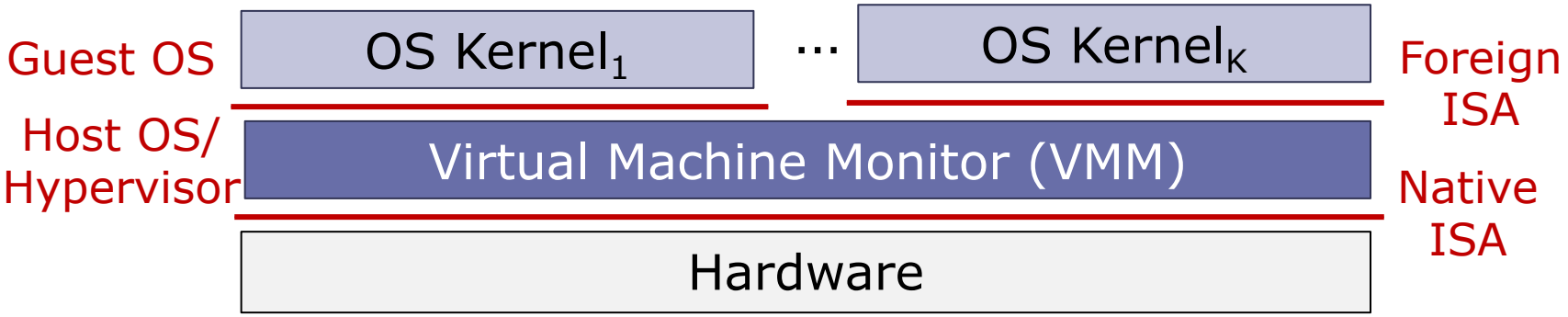
Virtualization Nomenclature

From (Machine we are attempting to execute)

- Guest
- Client
- Foreign ISA

To (Machine that is doing the real execution)

- Host
- Target
- Native ISA



Virtual Machine Requirements
[Popek and Goldberg, 1974]

- Equivalence/Fidelity: A program running on the VMM should exhibit a behavior essentially identical to that demonstrated when running on an equivalent machine directly.

- Resource control/Safety: The VMM must be in complete control of the virtualized resources.

- Efficiency/Performance: A statistically dominant fraction of machine instructions must be executed without VMM intervention.
  - Every instruction is intervened by VMM: Virtual machines implemented entirely in software using binary emulation
  - VMM only intervenes sensitive instructions: need hardware support

Virtual Machine Requirements
[Popek and Goldberg, 1974]

Classification of instructions into 3 groups:

- Privileged instructions: Instructions that trap if the processor is in user mode and do not trap if it is in a more privileged mode.
- Control-sensitive instructions: Instructions that attempt to change the configuration of resources in the system.
- Behavior-sensitive instructions: Those whose behavior depends on the configuration of resources, e.g., mode

Building an *effective* VMM for an architecture is possible if the set of sensitive instructions is a **subset** of the set of privileged instructions.

Security and Side Channels

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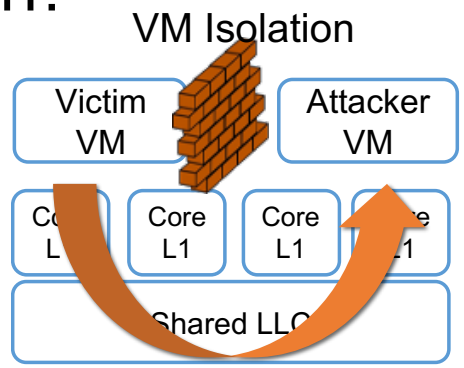
  - Specify *what* should happen, not *when*
- Hardware isolation mechanisms like virtual memory guarantee that architectural state will not be directly exposed to other processes…
- …but timing and other implementation details (e.g., microarchitectural state, power, etc.) may be used as side channels to leak information!



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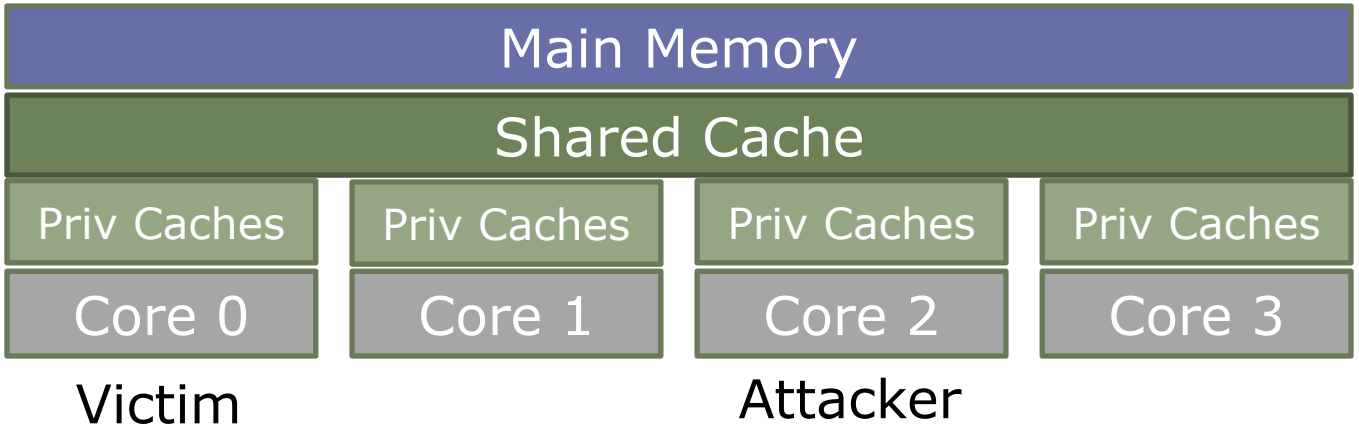
- Side channels leak information based on the implementation of a computer system
  - E.g. acoustic side channel
  - Timing information, power consumption, electromagnetic leaks etc.

Cache-Based Side Channels



- Attacker can infer shared cache behavior of victim
  - e.g., prime+probe attack, flush+reload attacks
  - Leaks address-dependent information, e.g., RSA [Percival 2005] and AES keys [Osvik et al. 2005]

Cache-based Side Channels

- RSA example:
  - Square-and-multiply based exponentiation

```
Input : base b, modulo m,
        exponent e = (e_{n-1} ...e_0 )_2
Output: b^e mod m
r = 1
for i = n−1 down to 0 do
        r = sqr(r)
        r = mod(r,m)
        if e_i == 1 then
            r = mul(r,b)
            r = mod(r,m)
        end
end
return r
```

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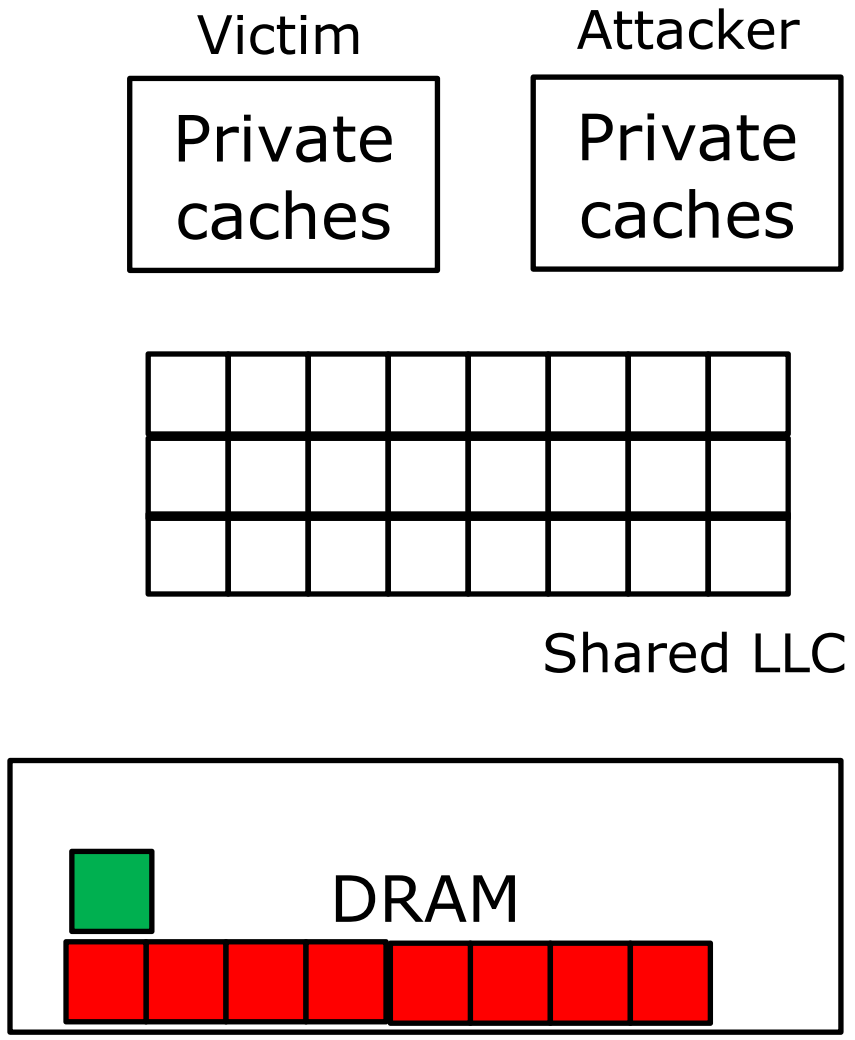
for i = n−1 down to 0 do
    r = sqr(r)
    r = mod(r,m)
    if e_i == 1 then
        r = mul(r,b)
        r = mod(r,m)
    end
end
return r
```

Secret-dependent memory accesses → transmitter

Cache-based Side Channels

- Prime+Probe



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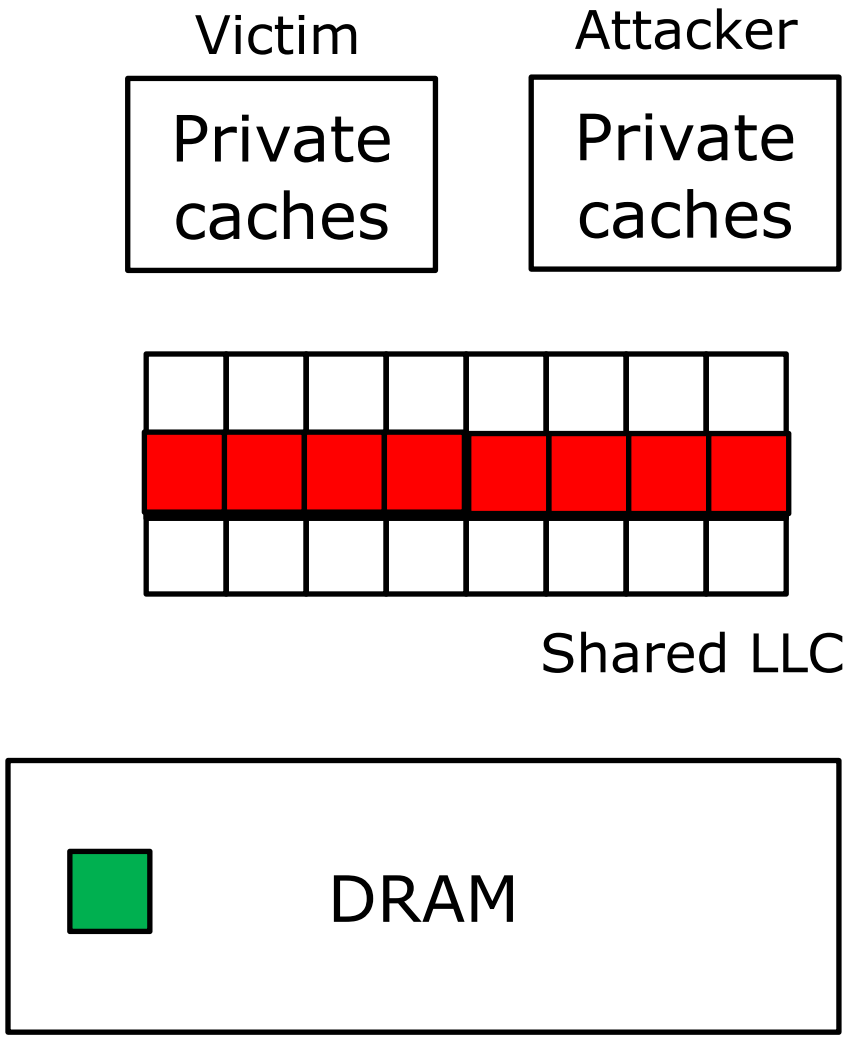

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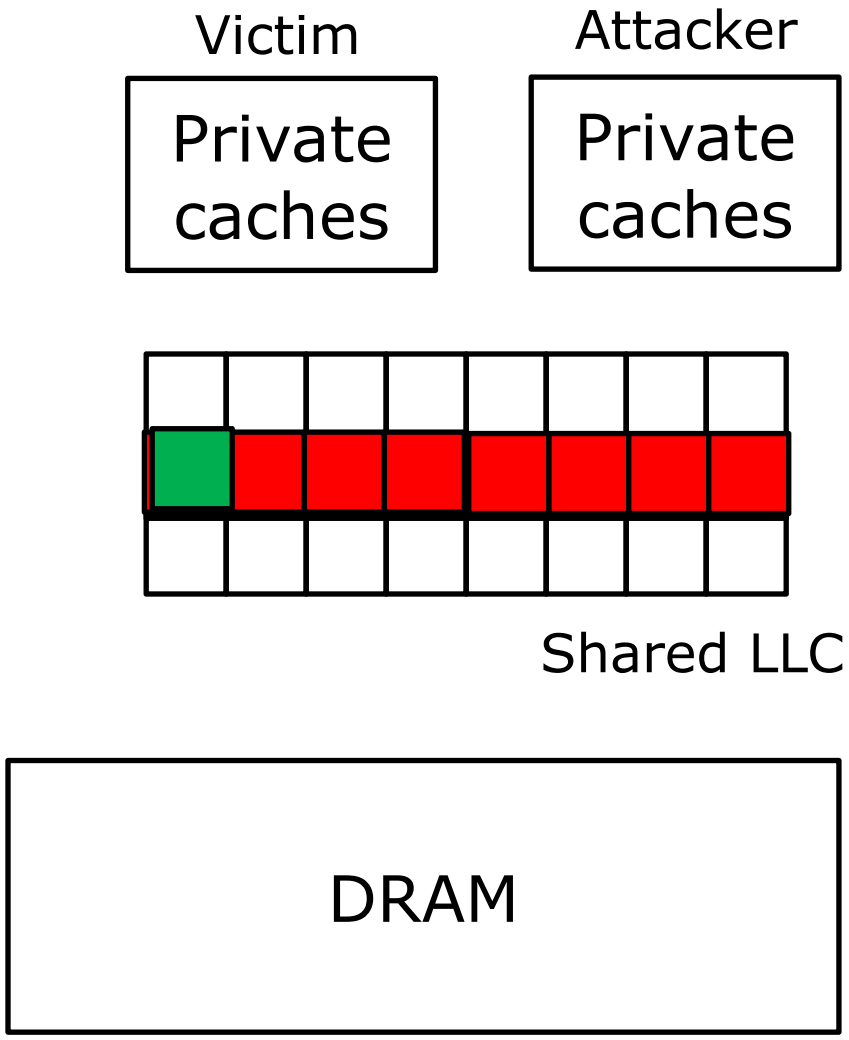

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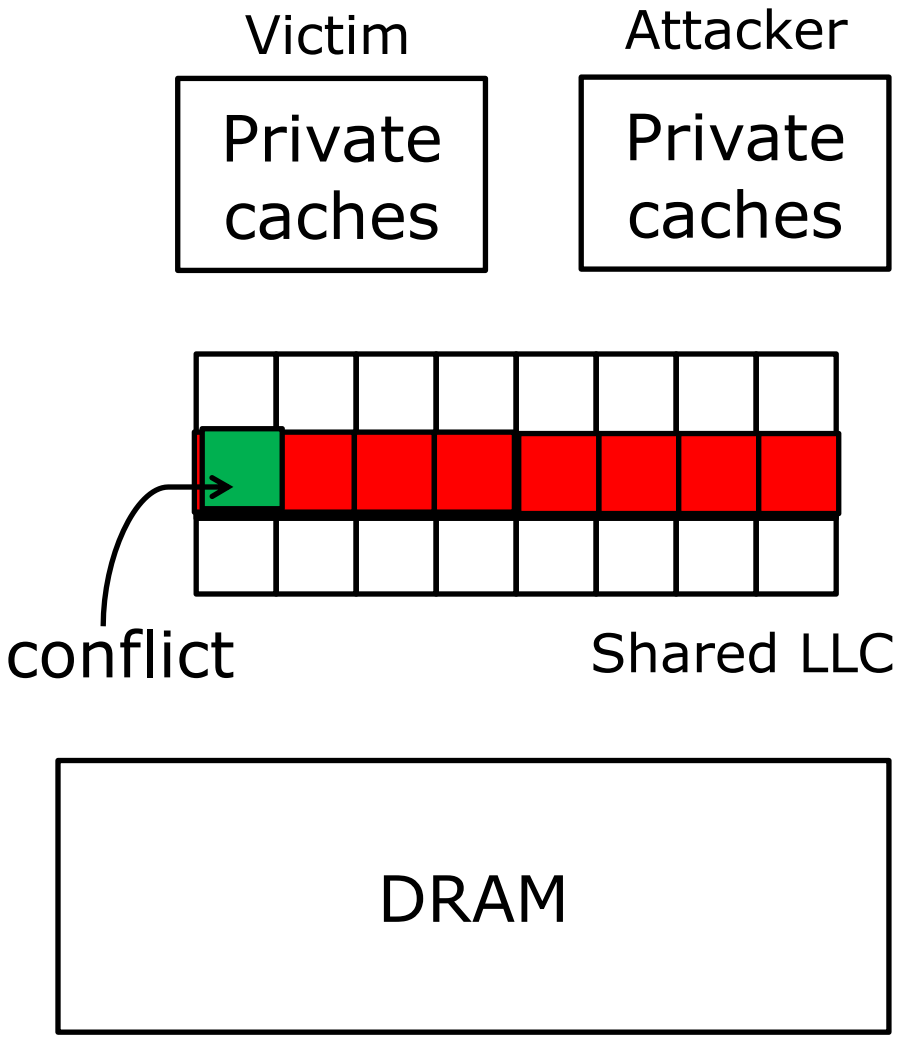

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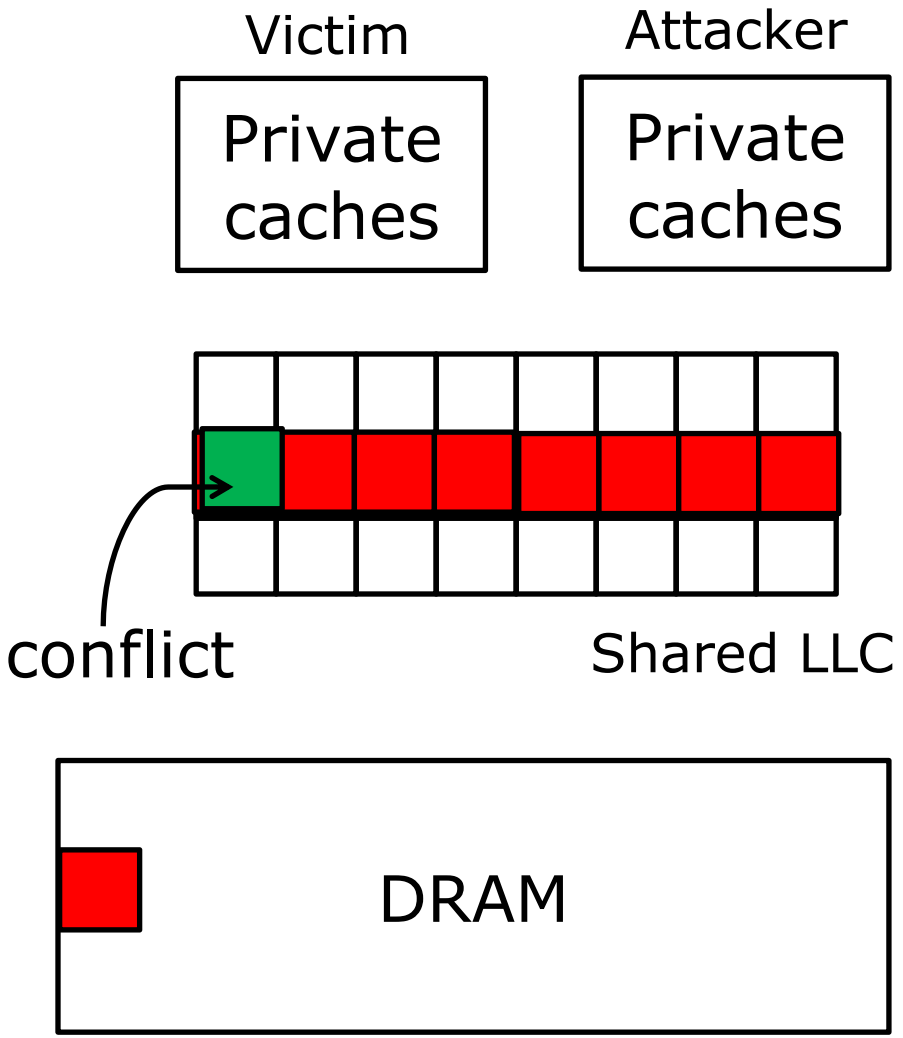

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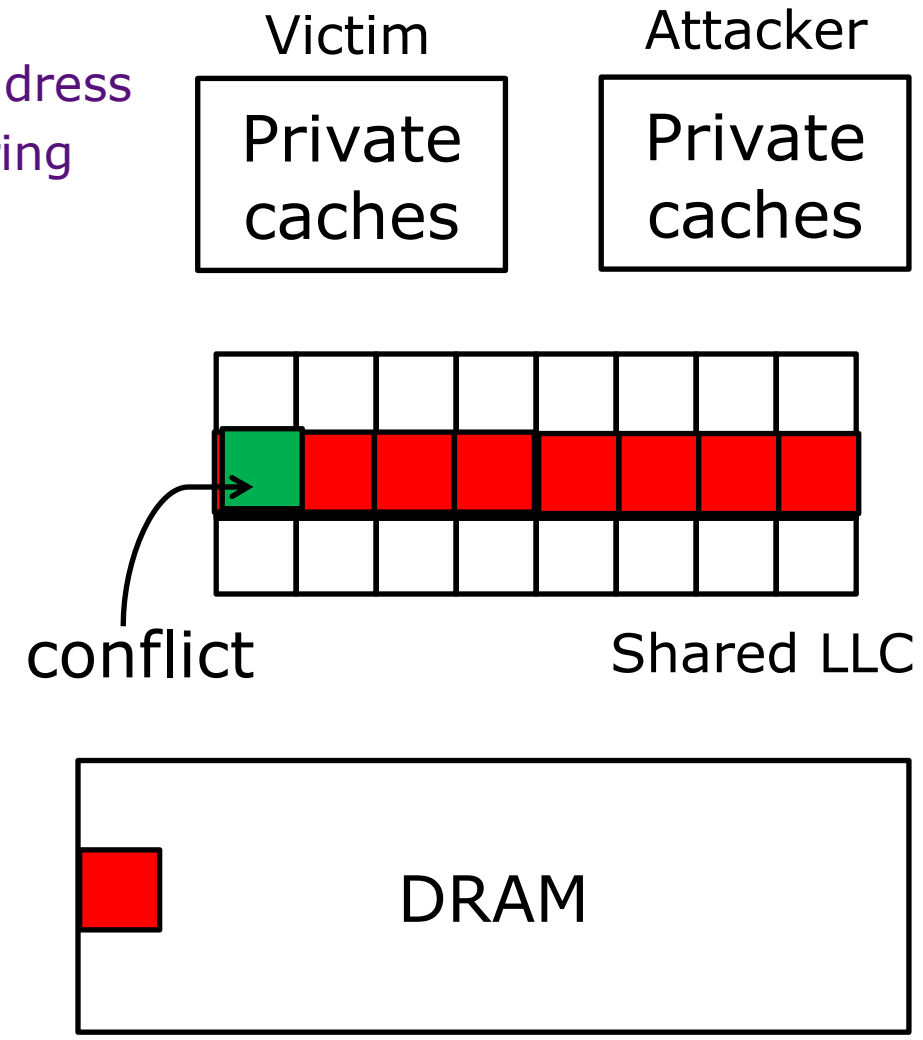

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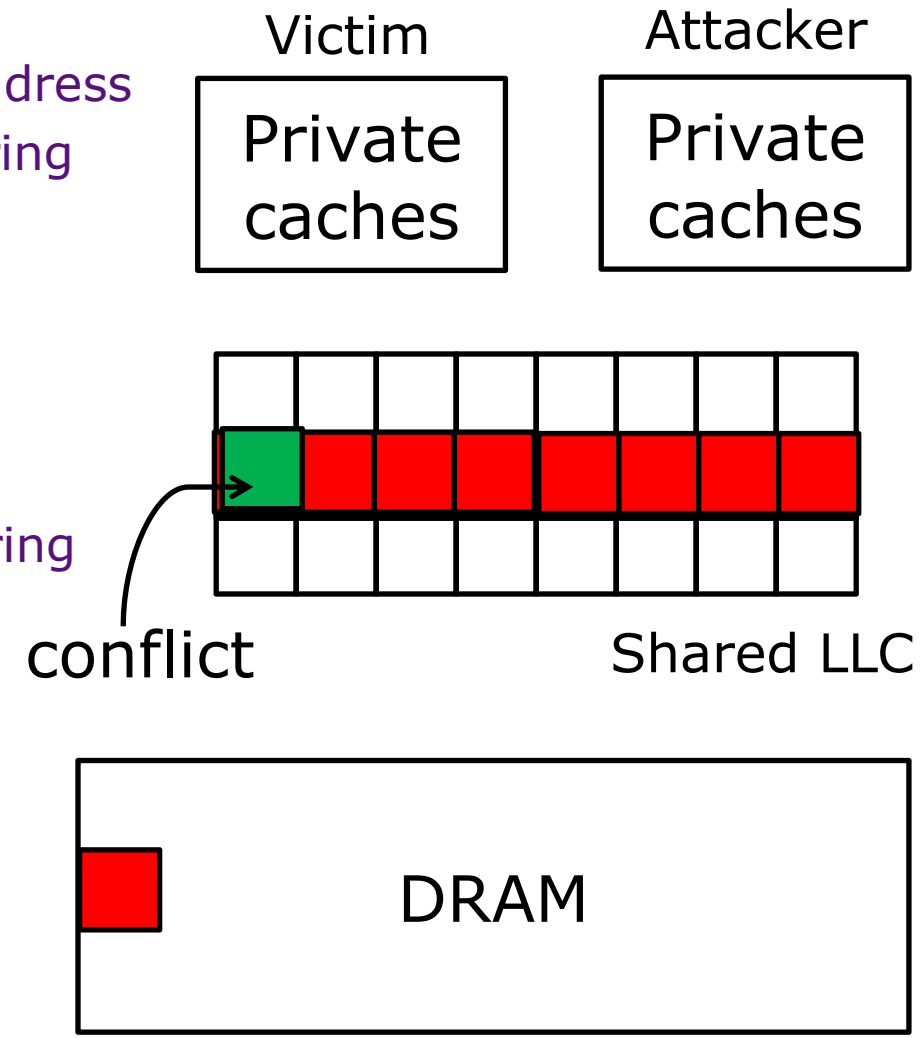

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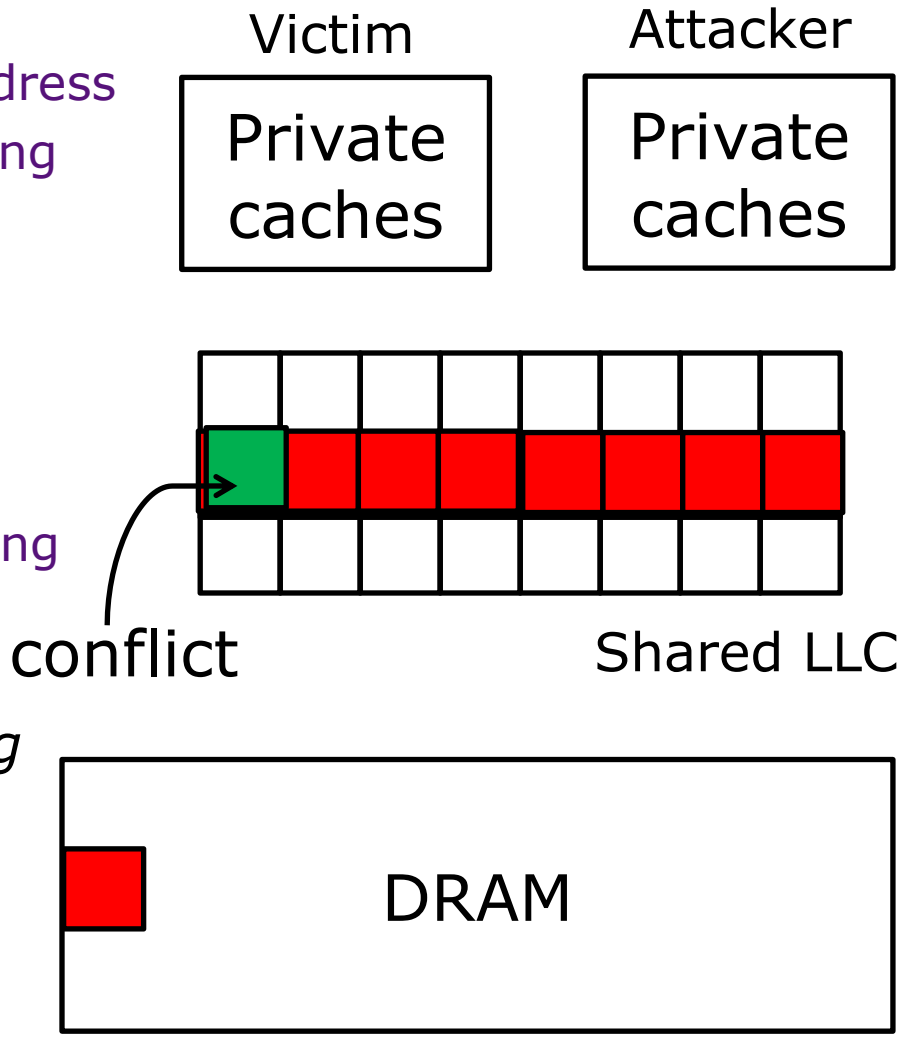

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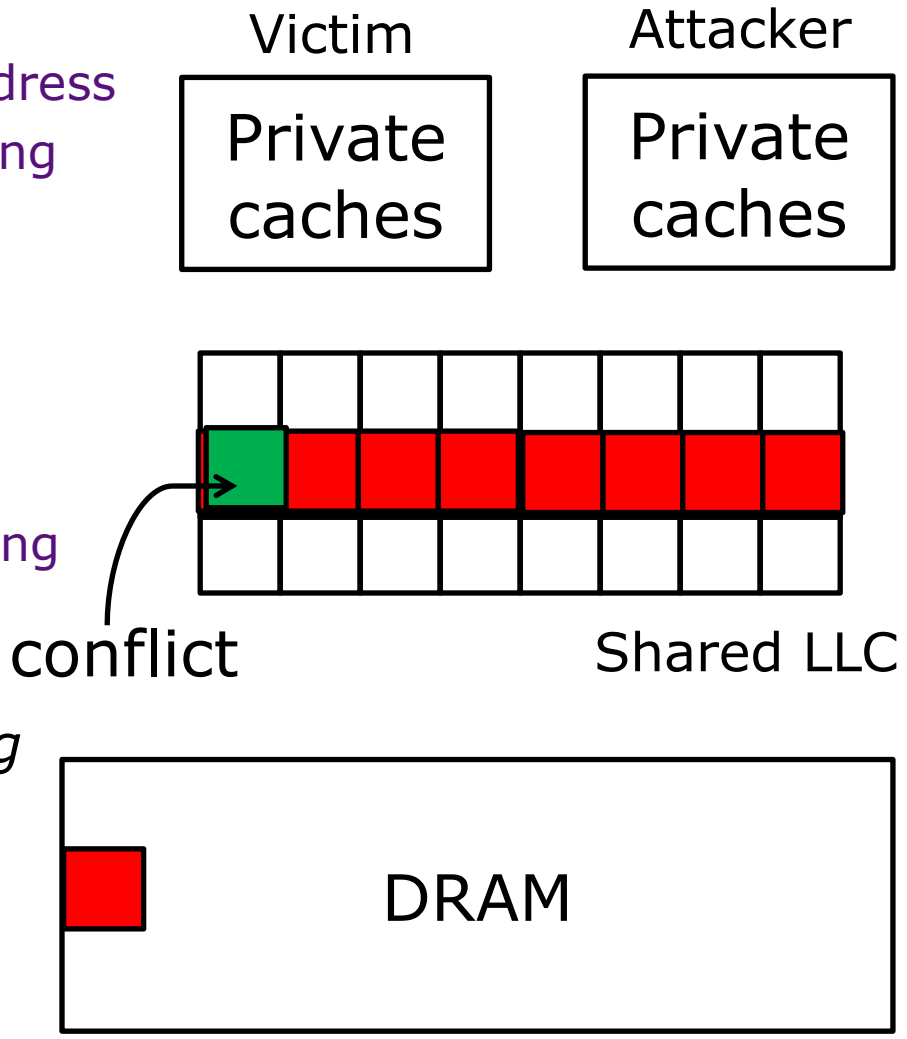

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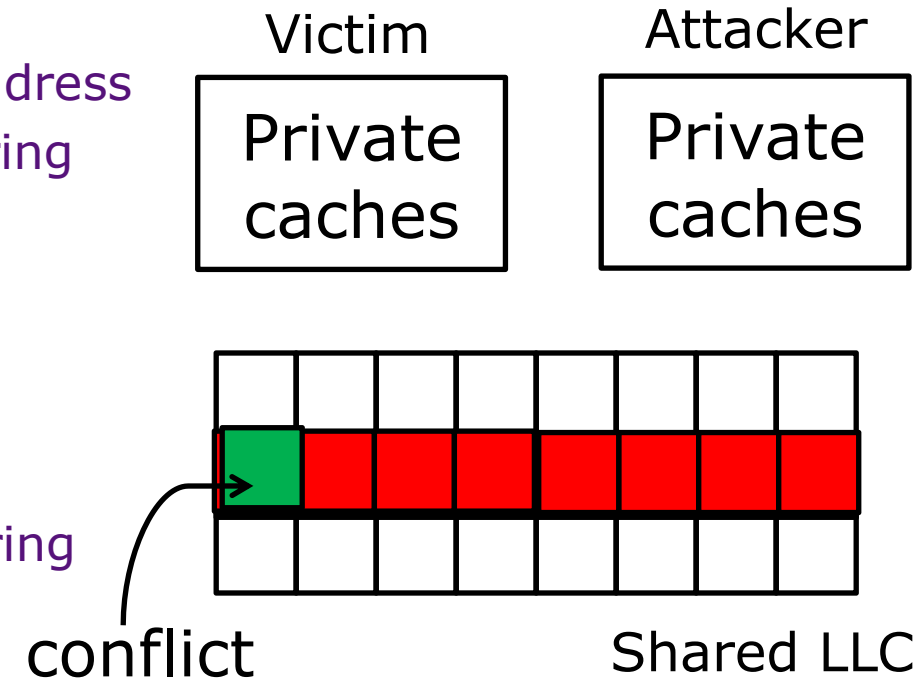

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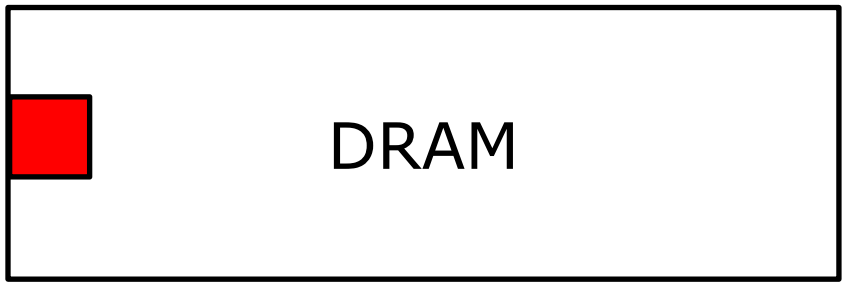

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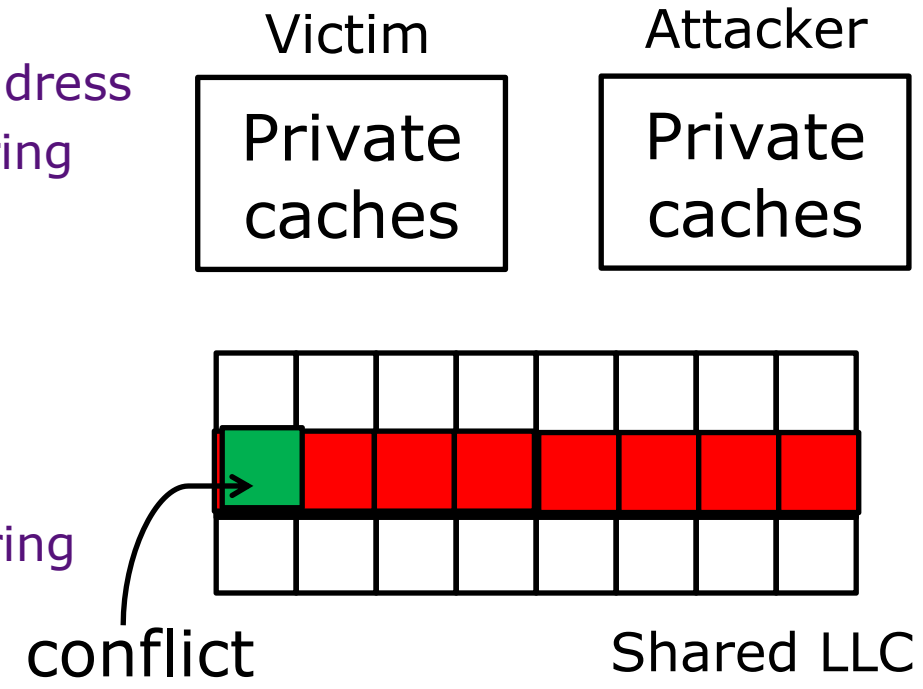

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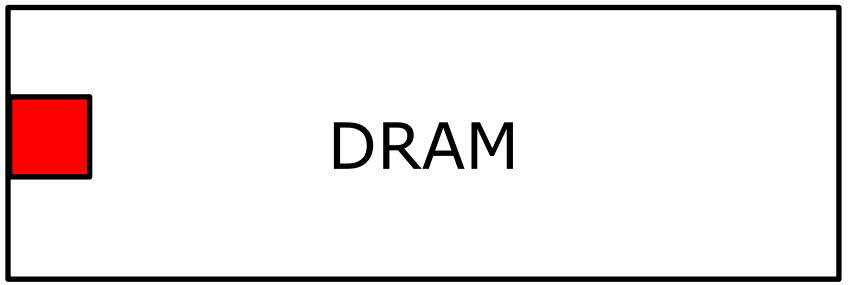

Microarchitecture Side Channels

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Attack Platforms

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Target Applications

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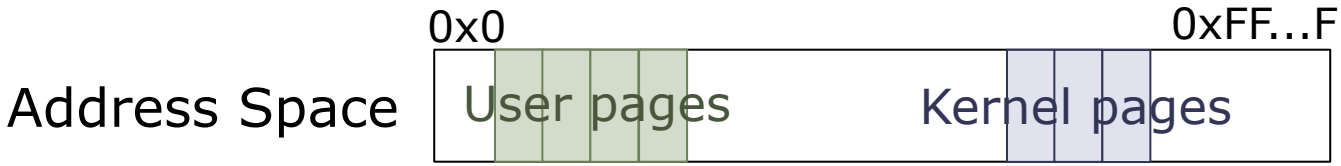

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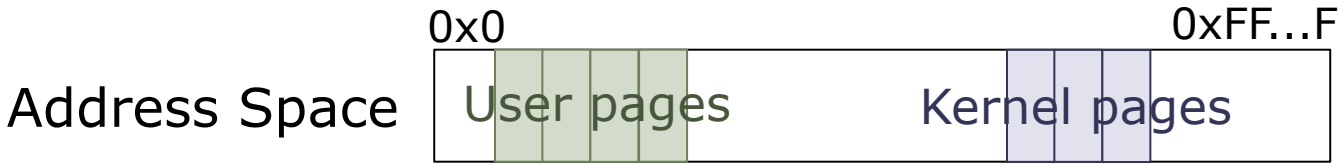

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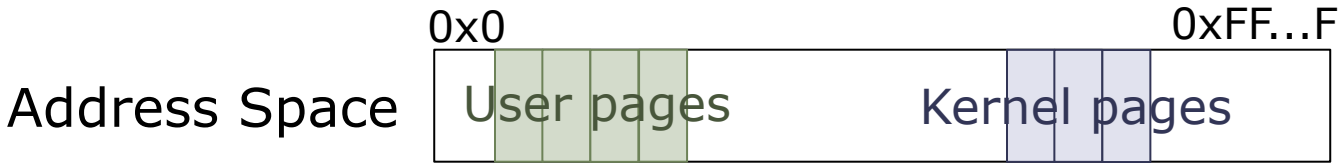

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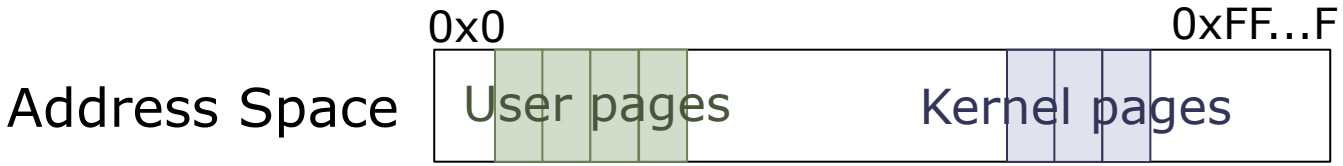

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Causes a protection fault

In Intel processors, protection fault is handled late
→ Kernel data speculatively loaded into val register!

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[Lipp et al. 2018]

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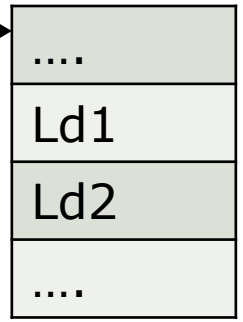

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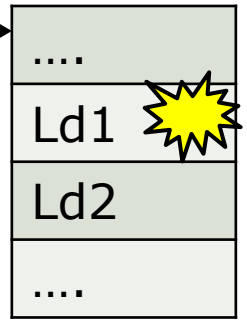

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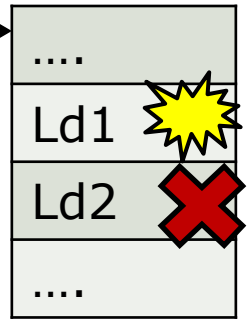

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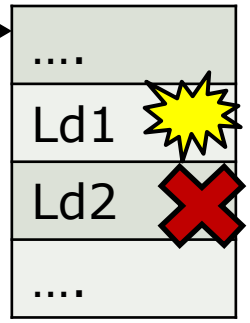

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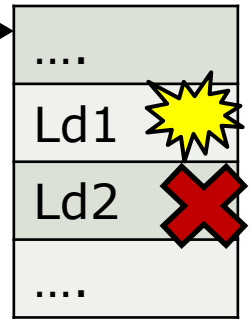

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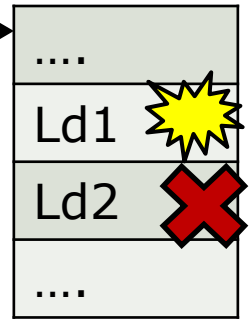

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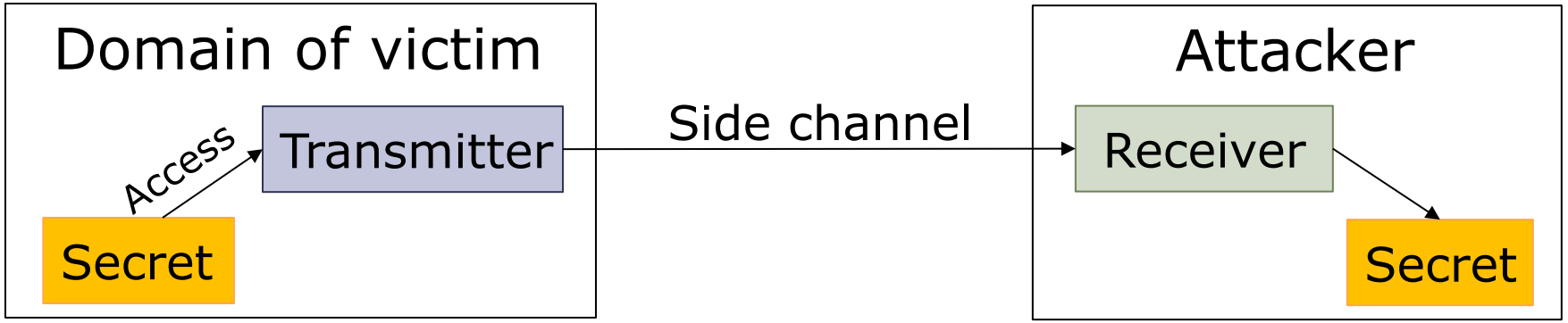
- Result: Attacker can read arbitrary kernel data!
  - For higher performance, use transactional memory
  - Mitigation: Do not map kernel data in user page tables; Register poisoning

General Attack Schema
[Belay, Devadas, Emer]



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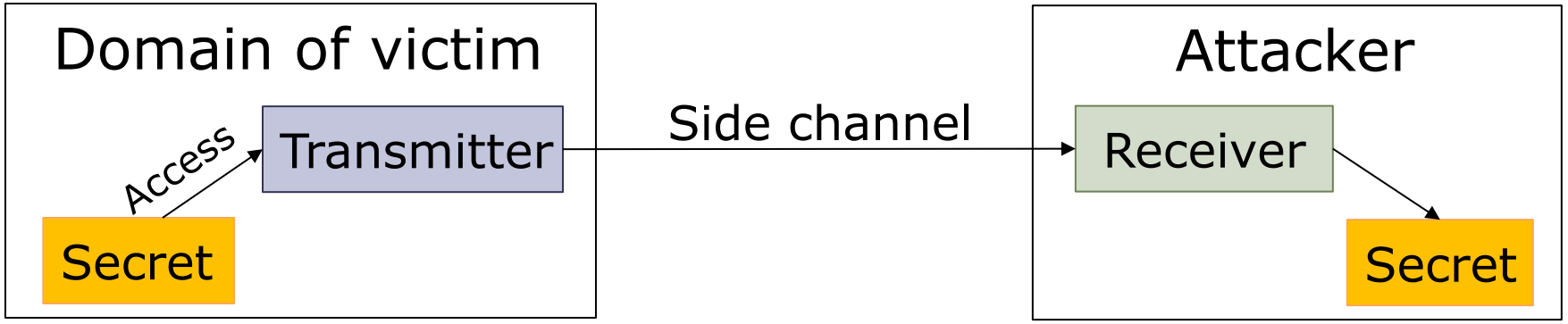

- Types of transmitter:
  1. Pre-existing (the victim itself leaks secret, e.g., RSA/AES keys)
  2. Programmed by attacker (e.g., Meltdown)
  3. Synthesized from existing victim code by attacker (e.g., Spectre)

Spectre variant 1 — Exploiting Conditional Branches [Kocher et al. 2018]

- Consider the following kernel code, e.g., in a system call

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Br:  if (x < size_array1) {
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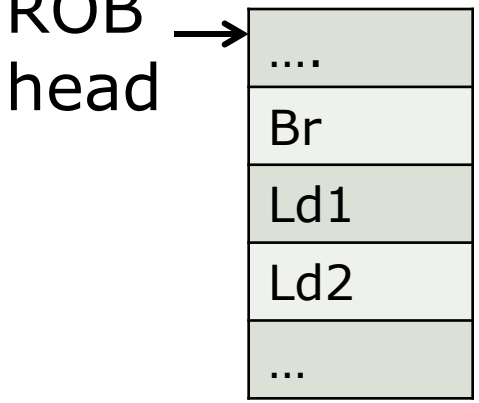

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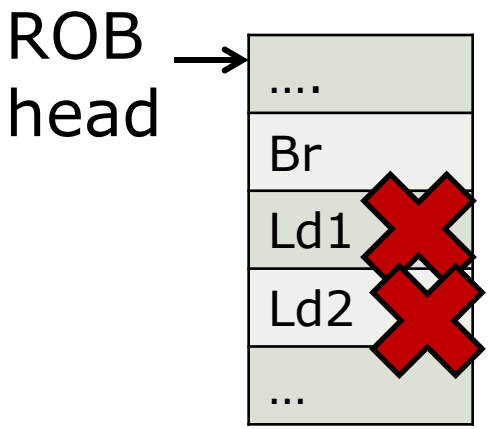

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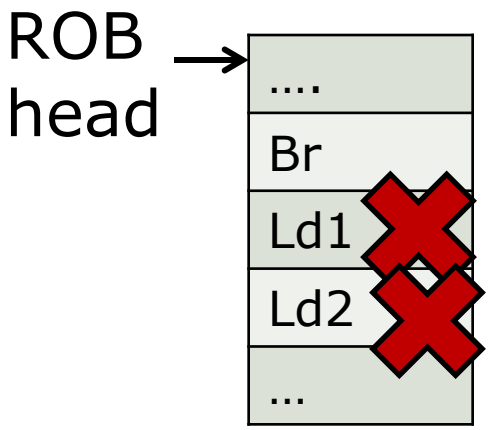

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- But most cores add an indirect branch predictor that stores full targets (e.g., to predict virtual function calls)
  - Spectre v2 exploits this predictor instead

Spectre variants and mitigations

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  - Disabling speculation?
  - Closing side channels?

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Spectre, Meltdown
Foreshadow,
Arithmetic timing

CacheOut, RIDL, Fallout
Port contention,
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RNG Unit Covert Chanel

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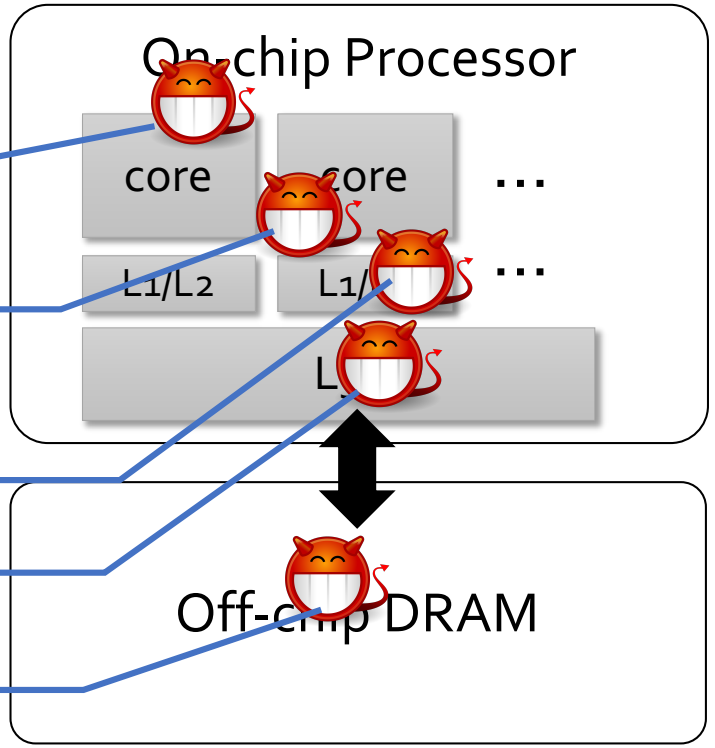

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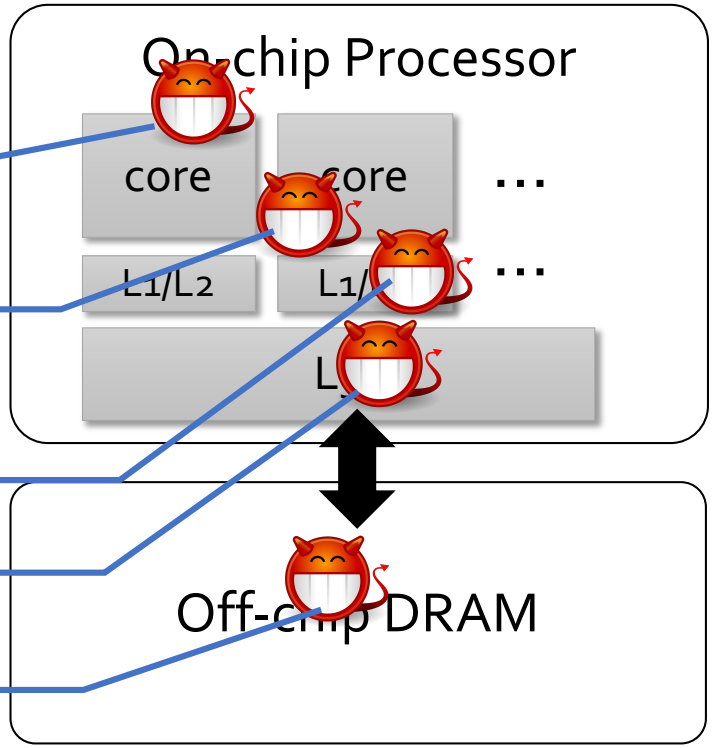
RowHammer, DRAMA
RAMBleed



New Special Topic course in Fall 2020
6.888 Secure Hardware Design

Thank you!