Cache Coherence

Daniel Sanchez
Computer Science & Artificial Intelligence Lab
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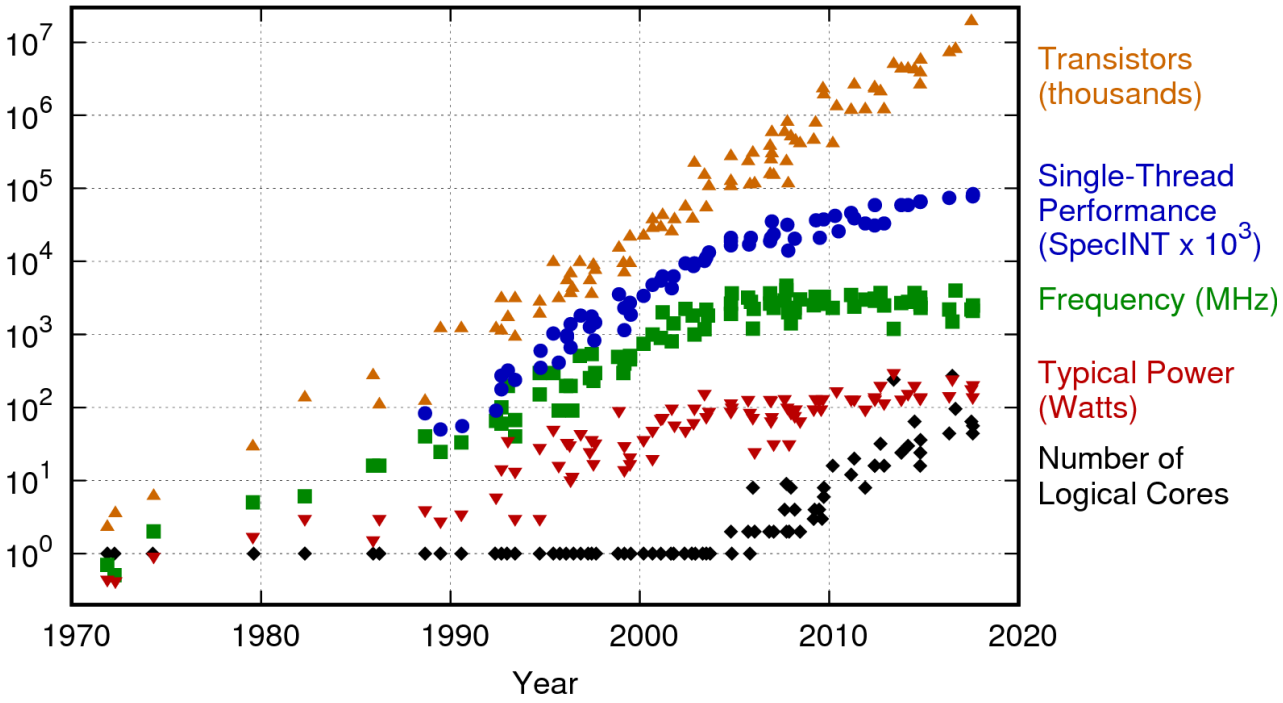
The Shift to Multicore



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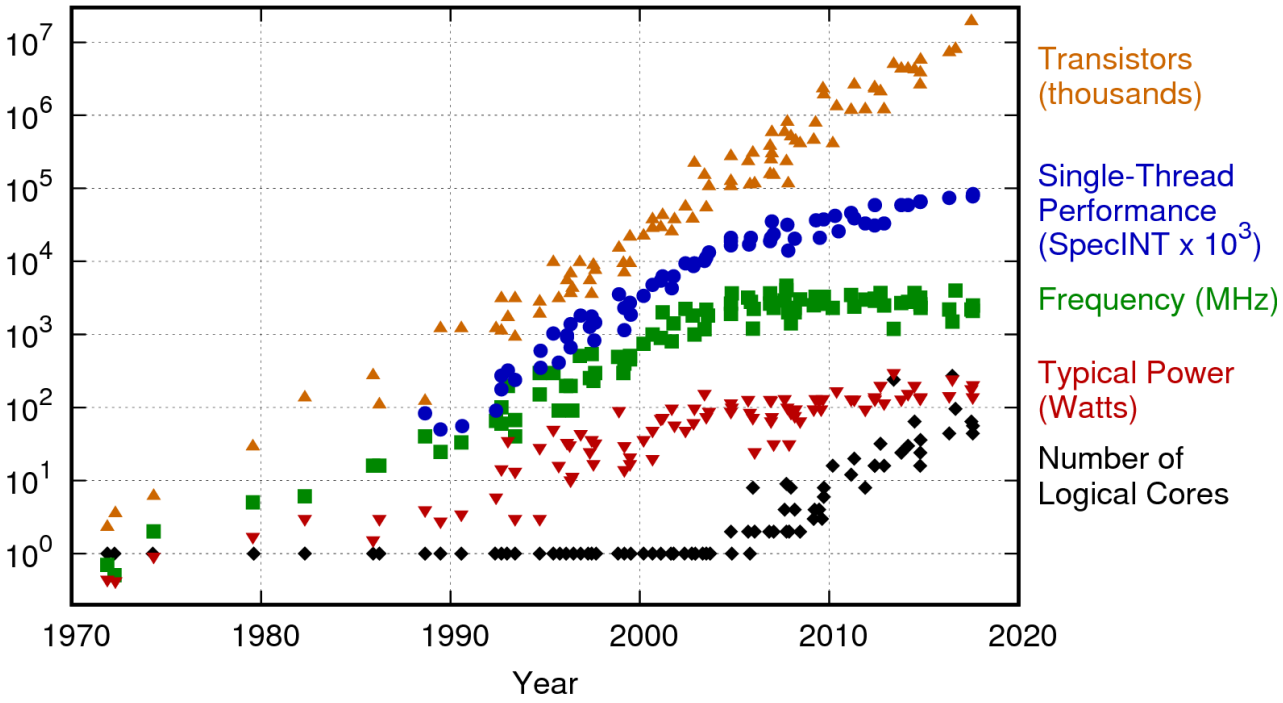

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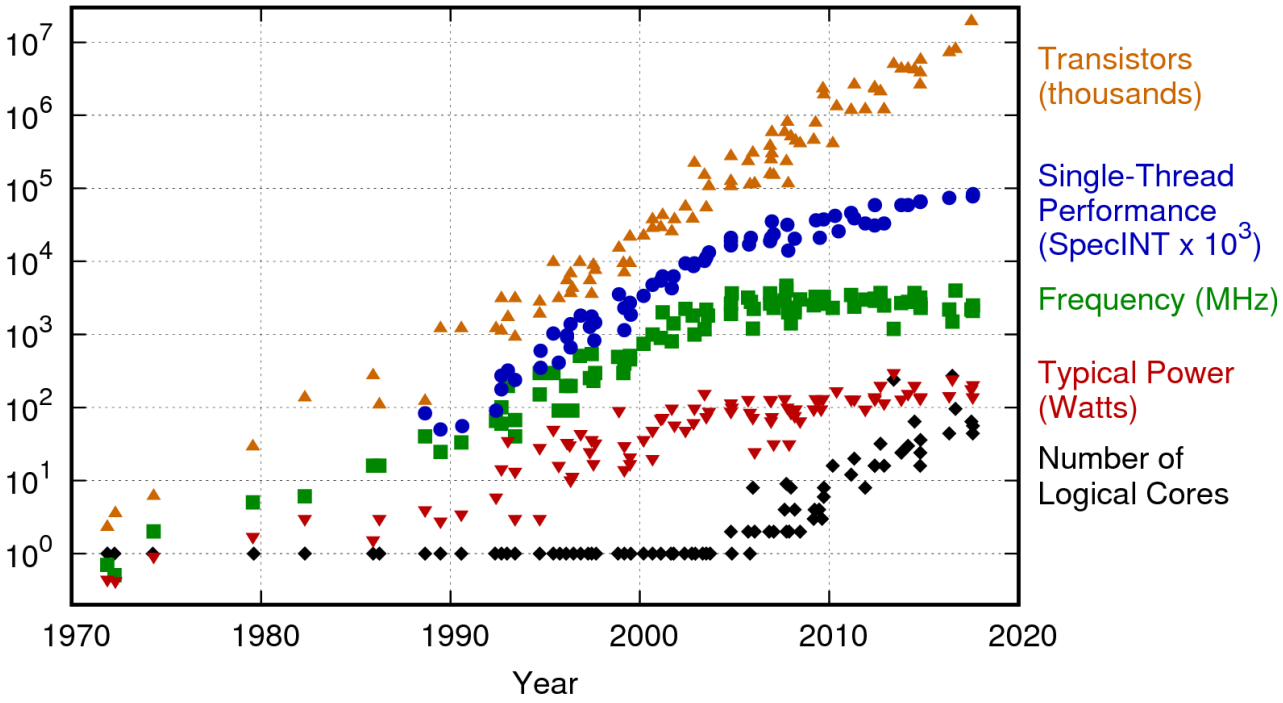

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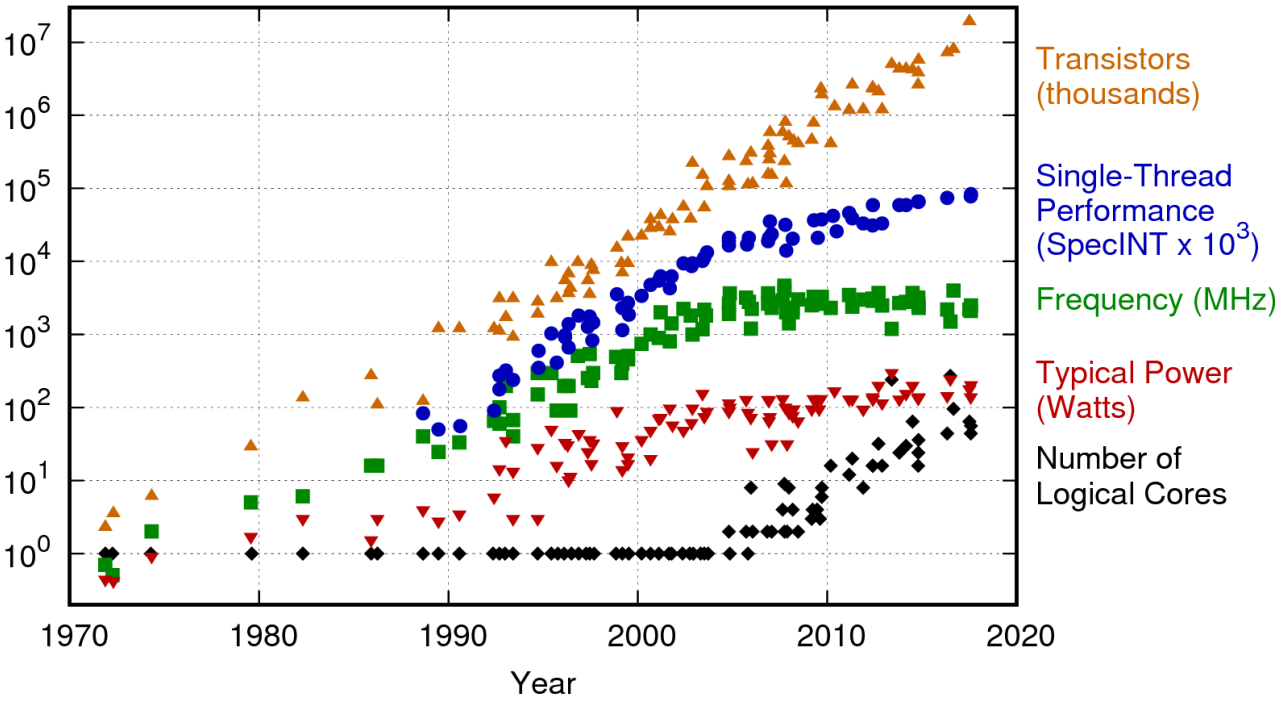

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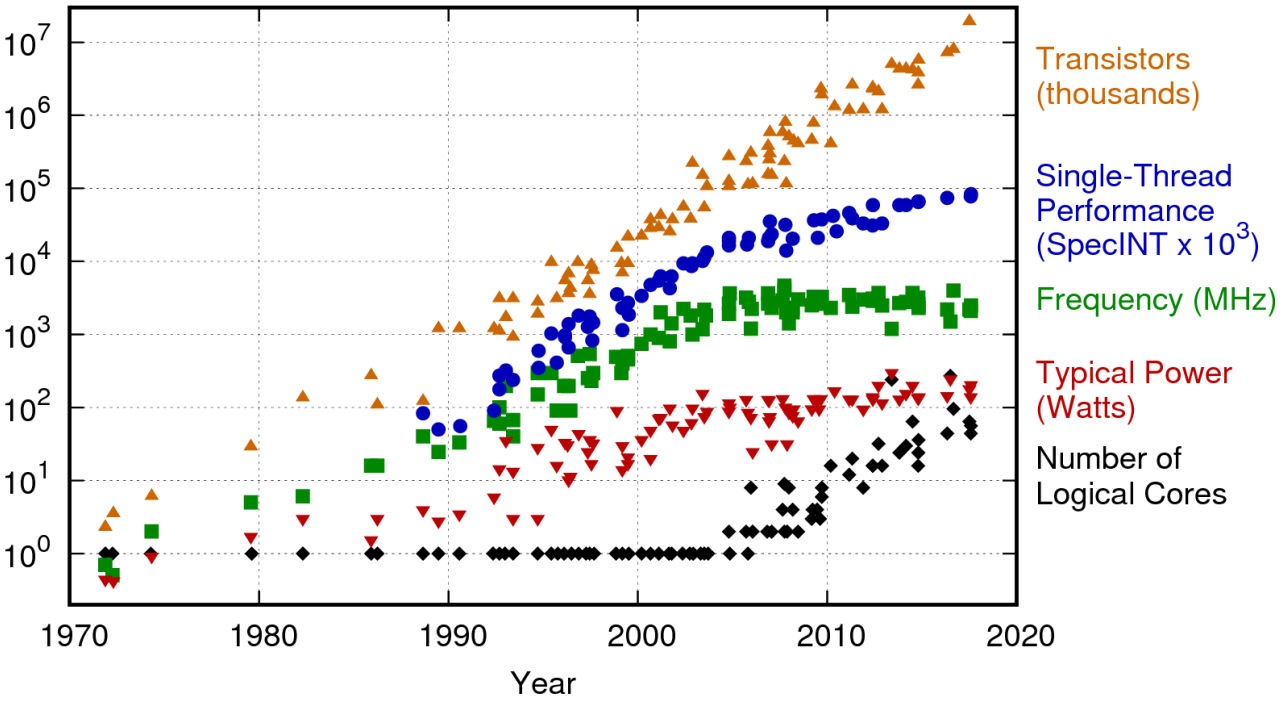

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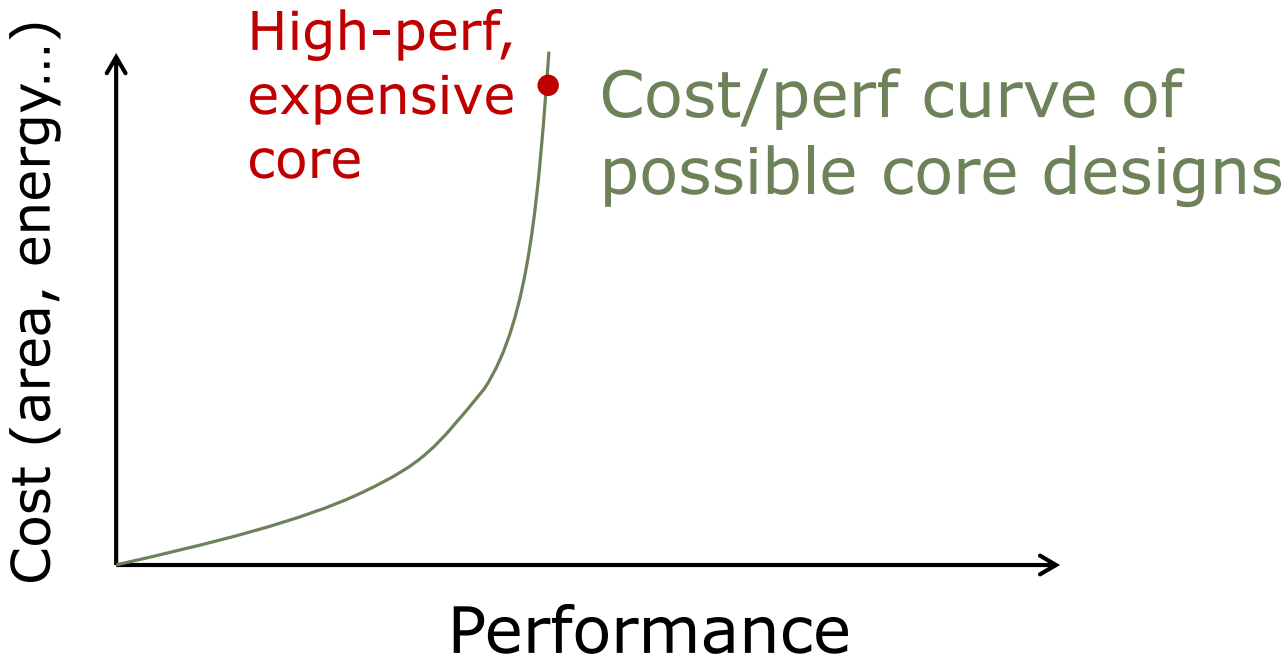
  Limited instruction-level parallelism

Multicore Performance



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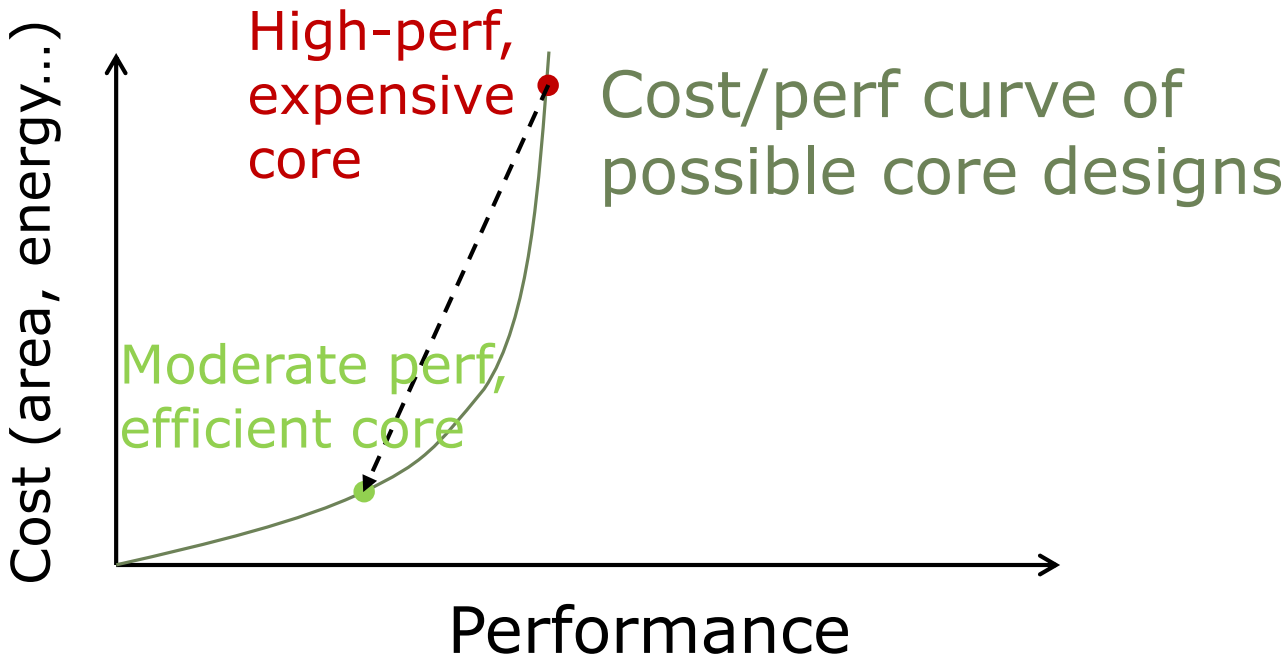

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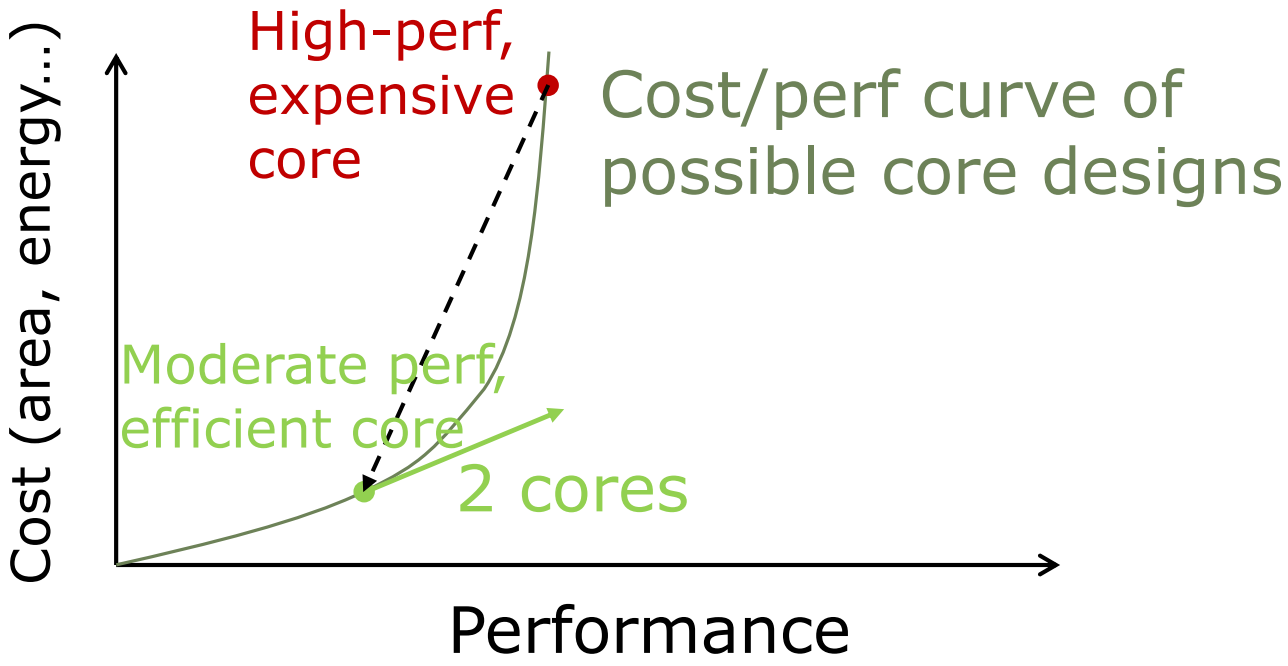

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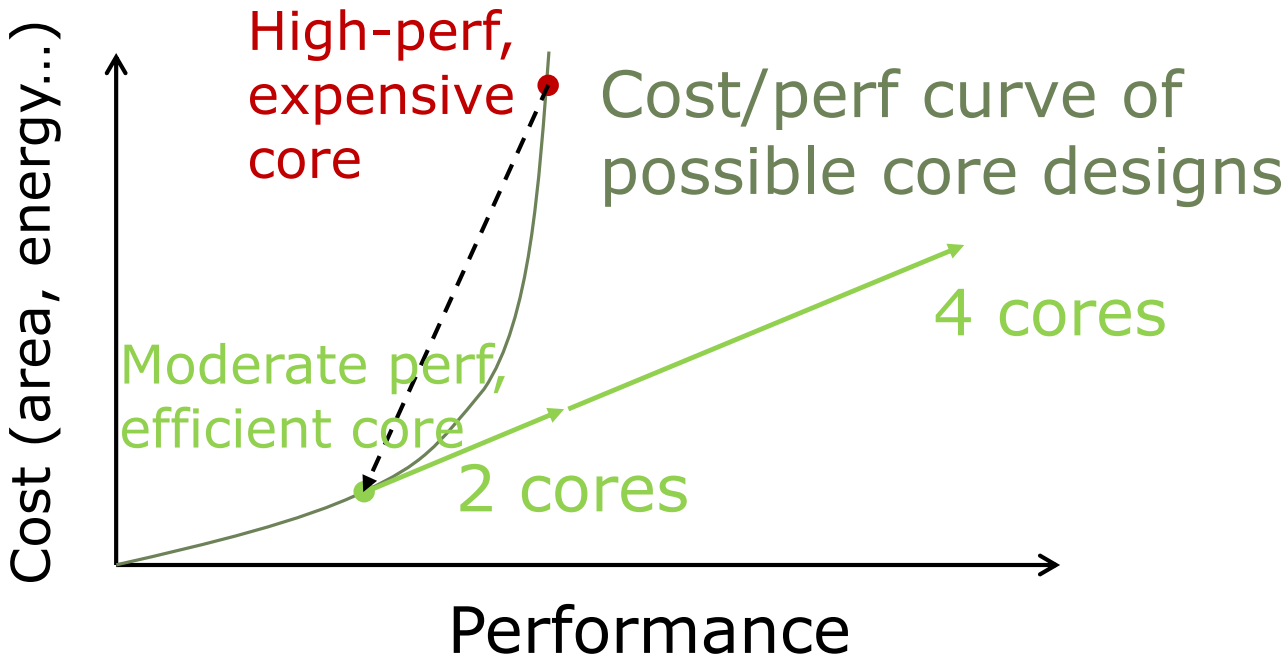

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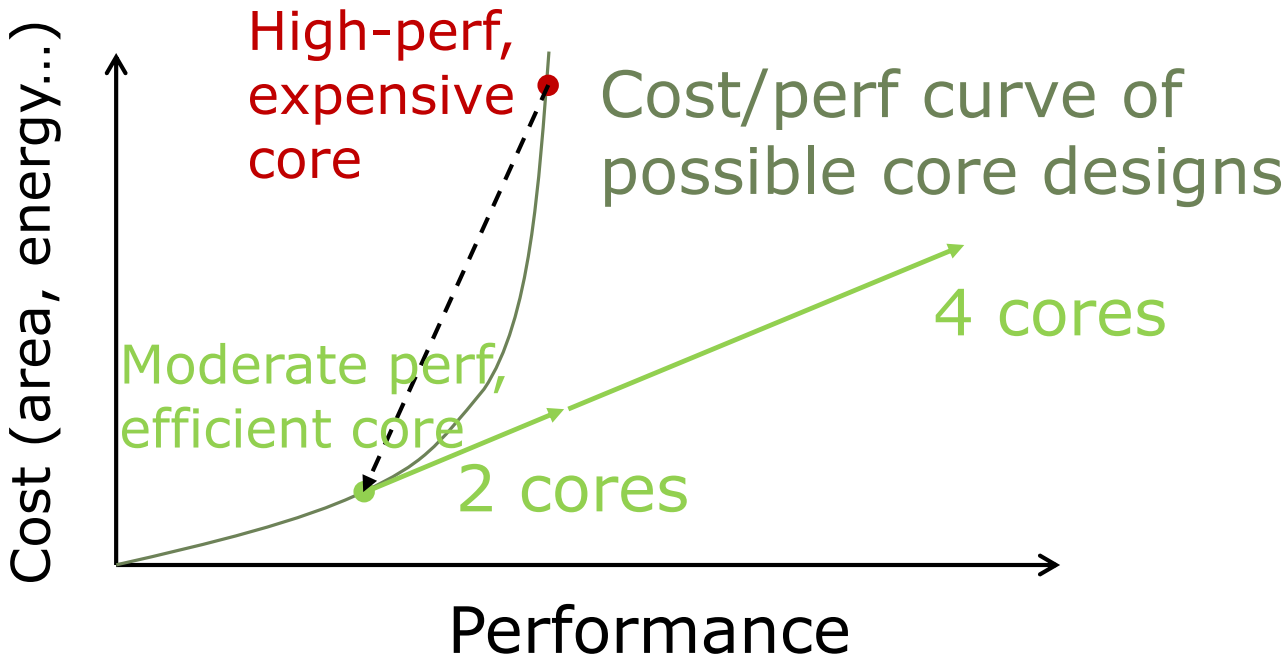

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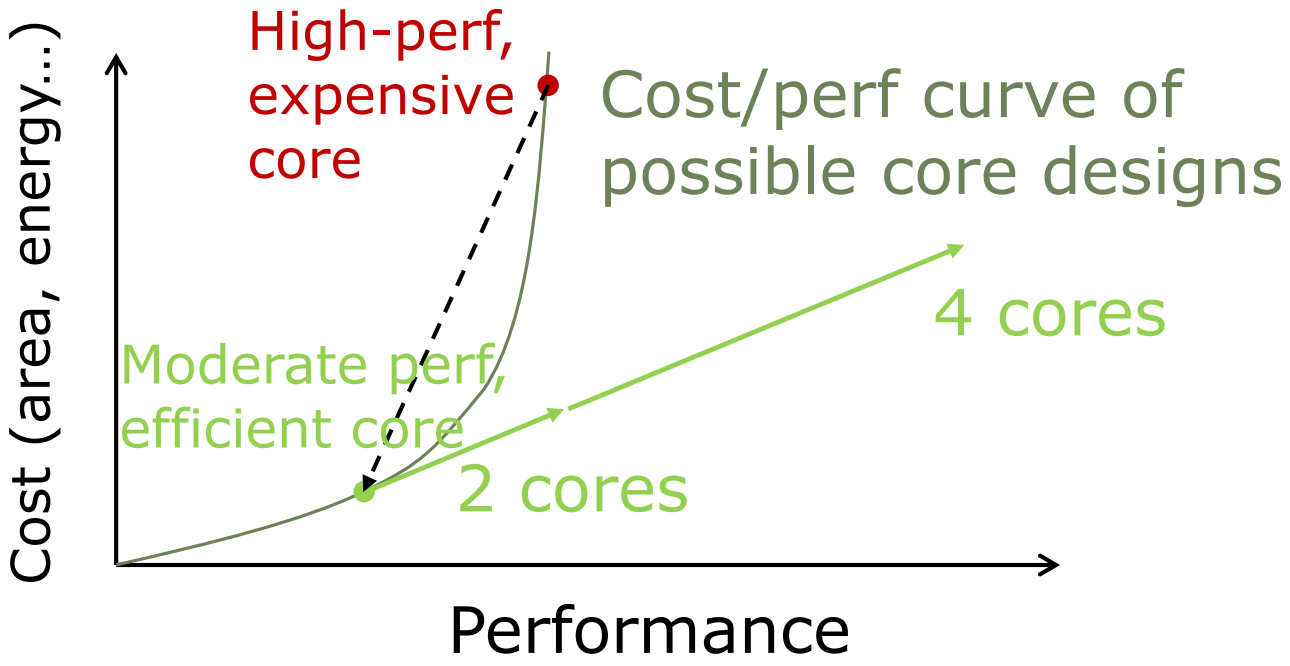

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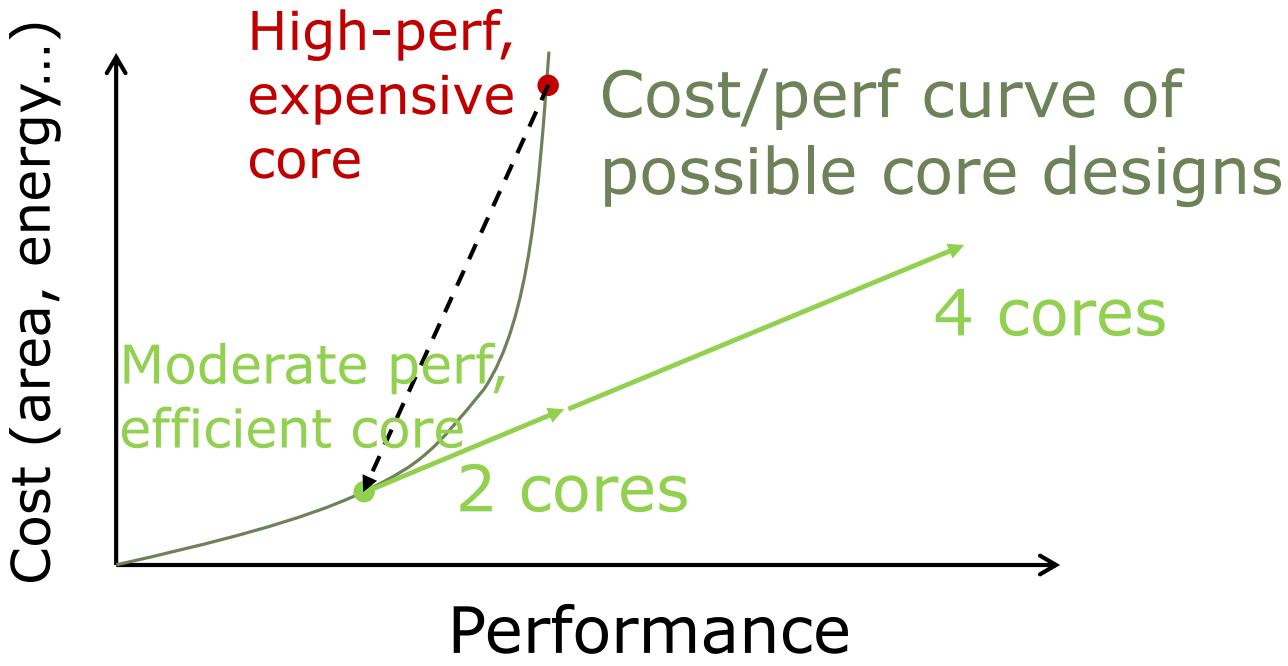

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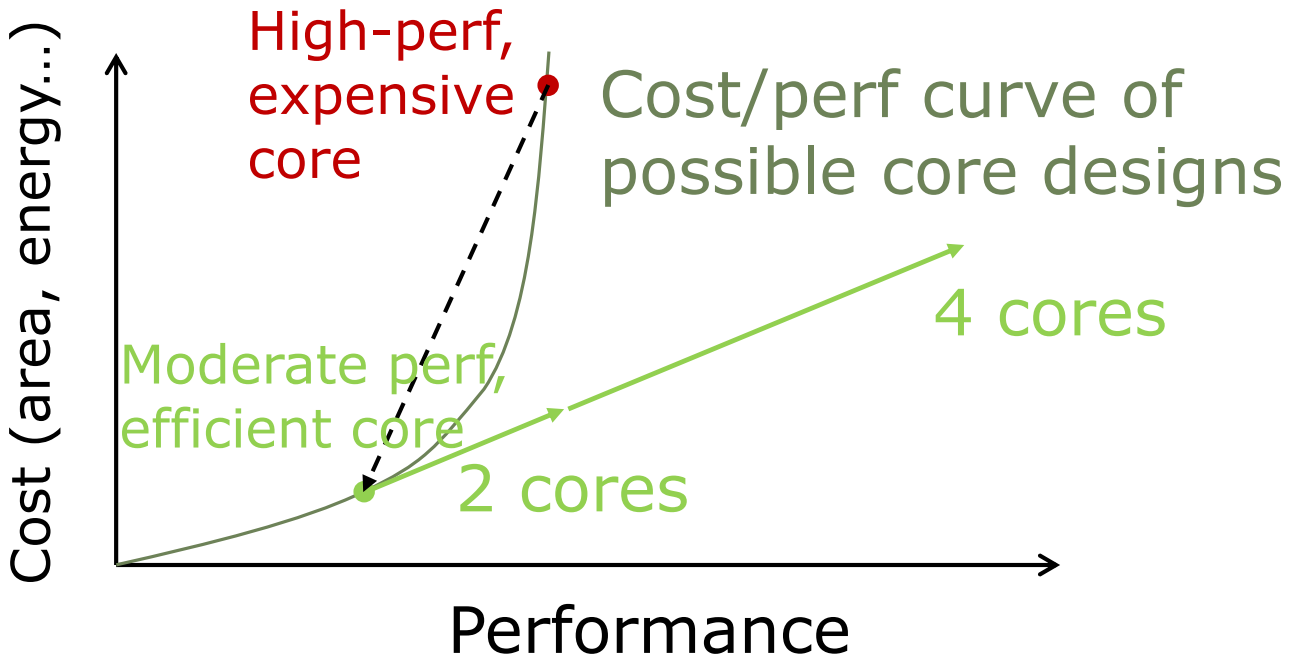

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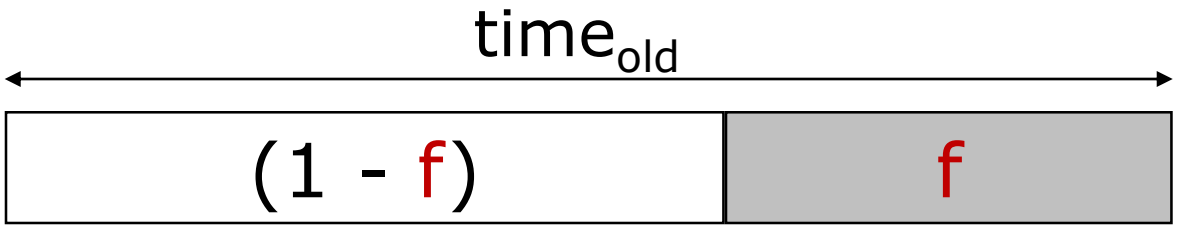
- Programming complexity

Amdahl's Law

- Speedup= $\text{time}_{\text{without enhancement}}$ / $\text{time}_{\text{with enhancement}}$
- Suppose an enhancement speeds up a fraction f of a task by a factor of S



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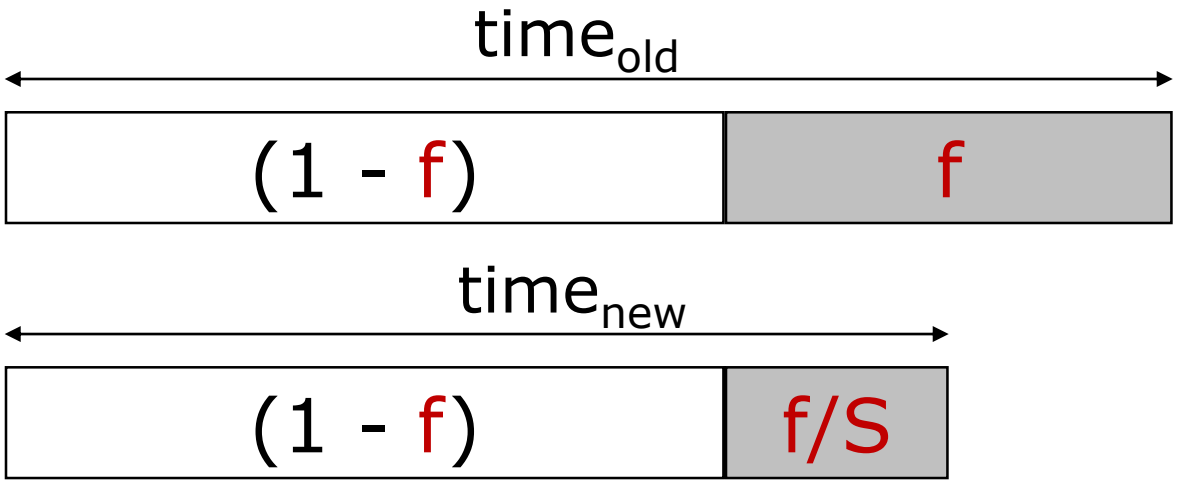

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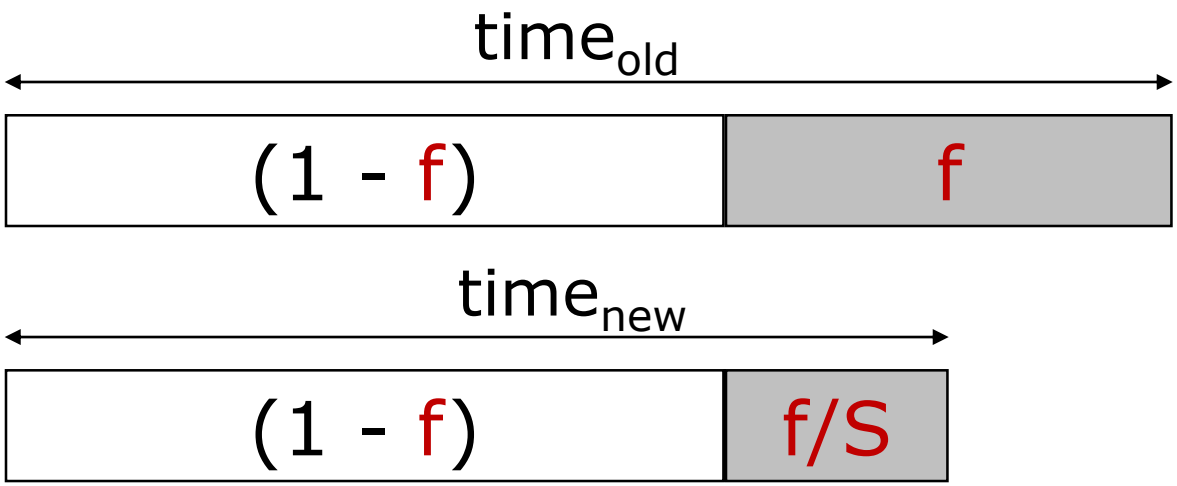

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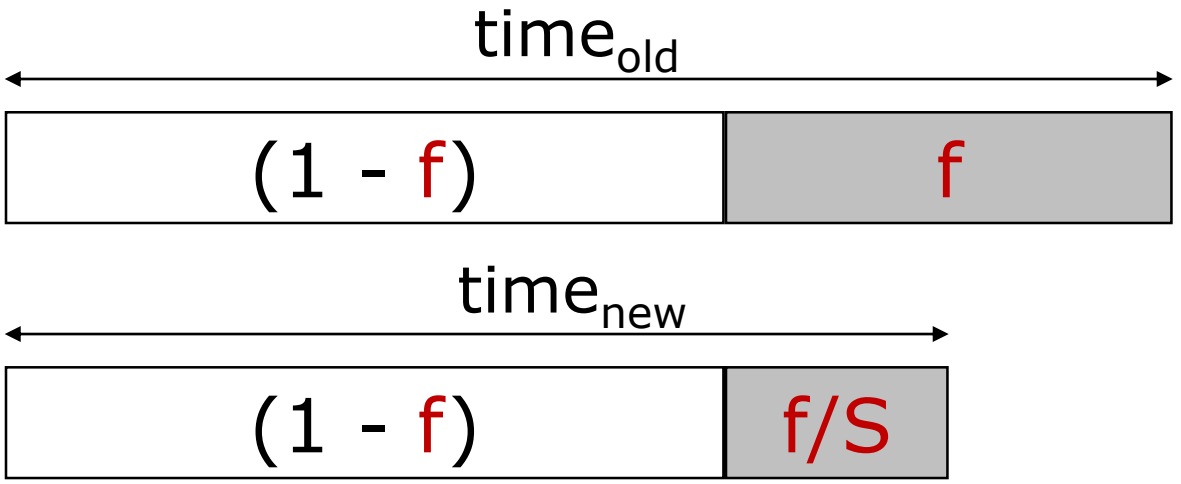

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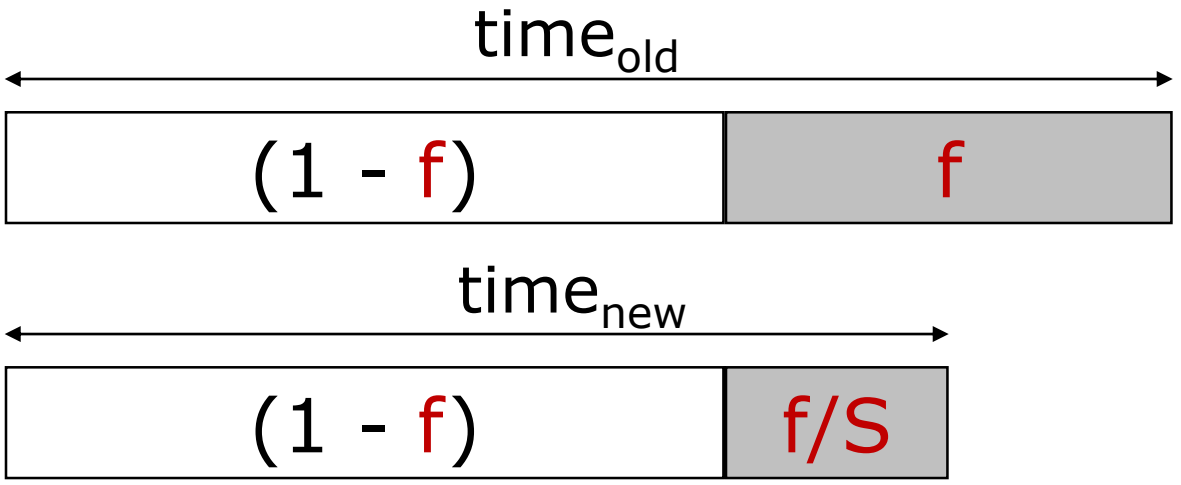

Corollary: Make the common case fast

Amdahl's Law and Parallelism

- Say you write a program that can do 90% of the work in parallel, but the other 10% is sequential
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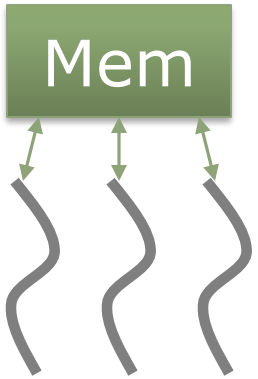
What f do you need to use a 1000-core machine well?

Communication Models

- Shared memory:
  - Single address space
  - Implicit communication by reading/writing memory
    - Data
    - Control (semaphores, locks, barriers, …)
  - Low-level programming model: threads



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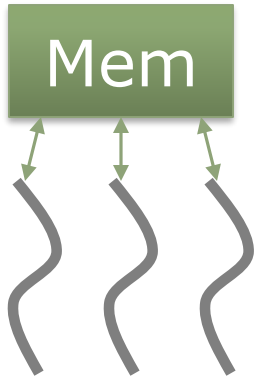

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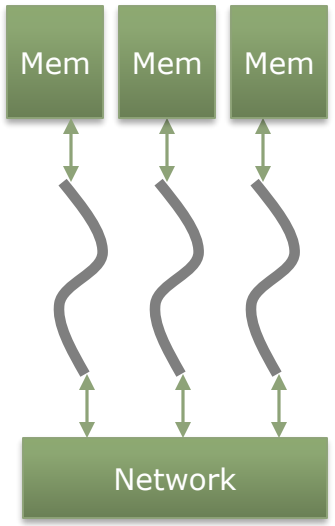

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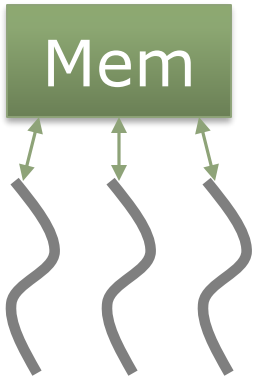

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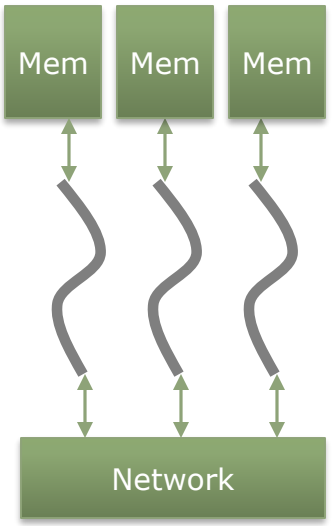

- Pros/cons of each model?

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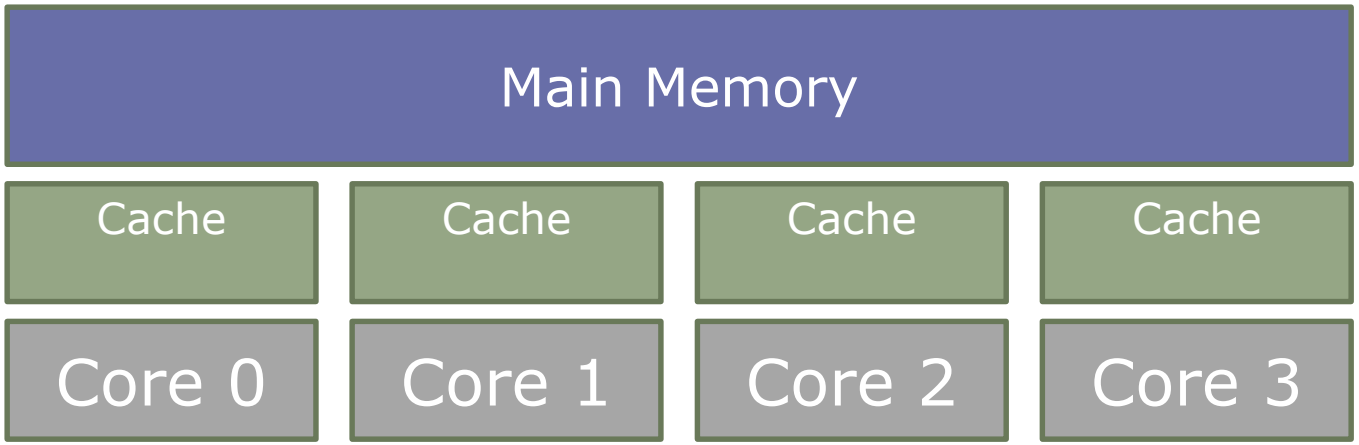

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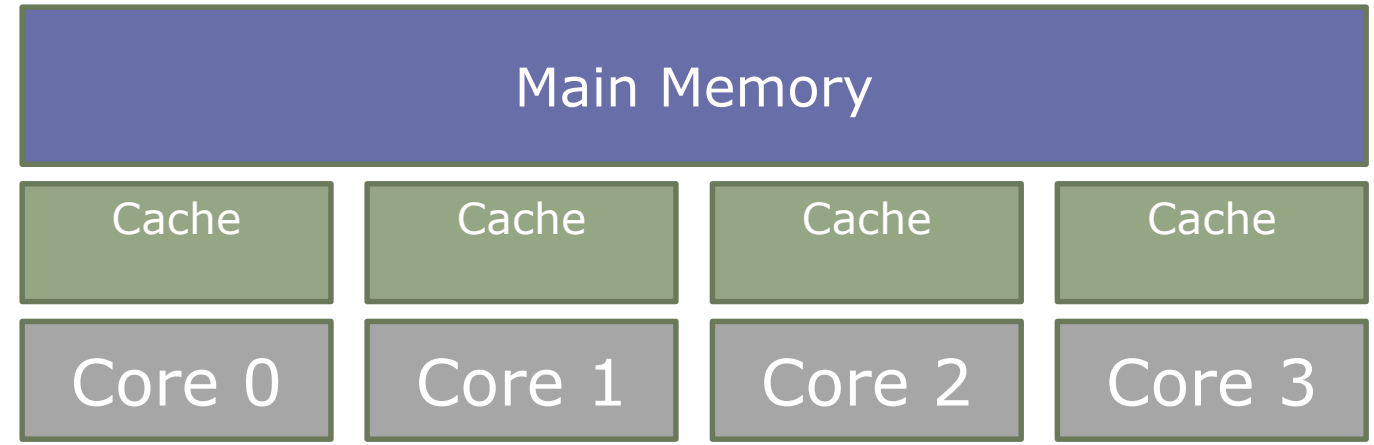

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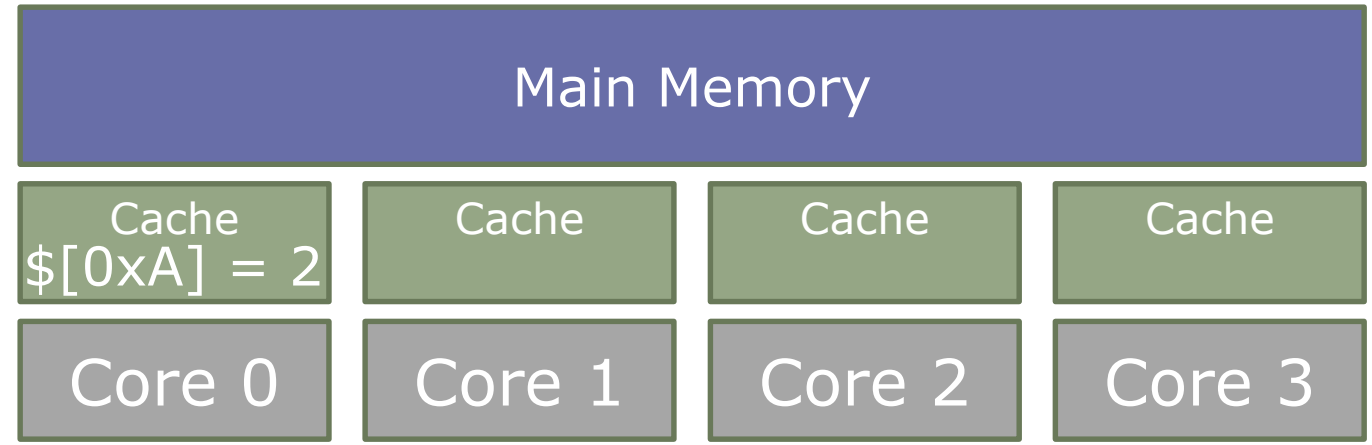

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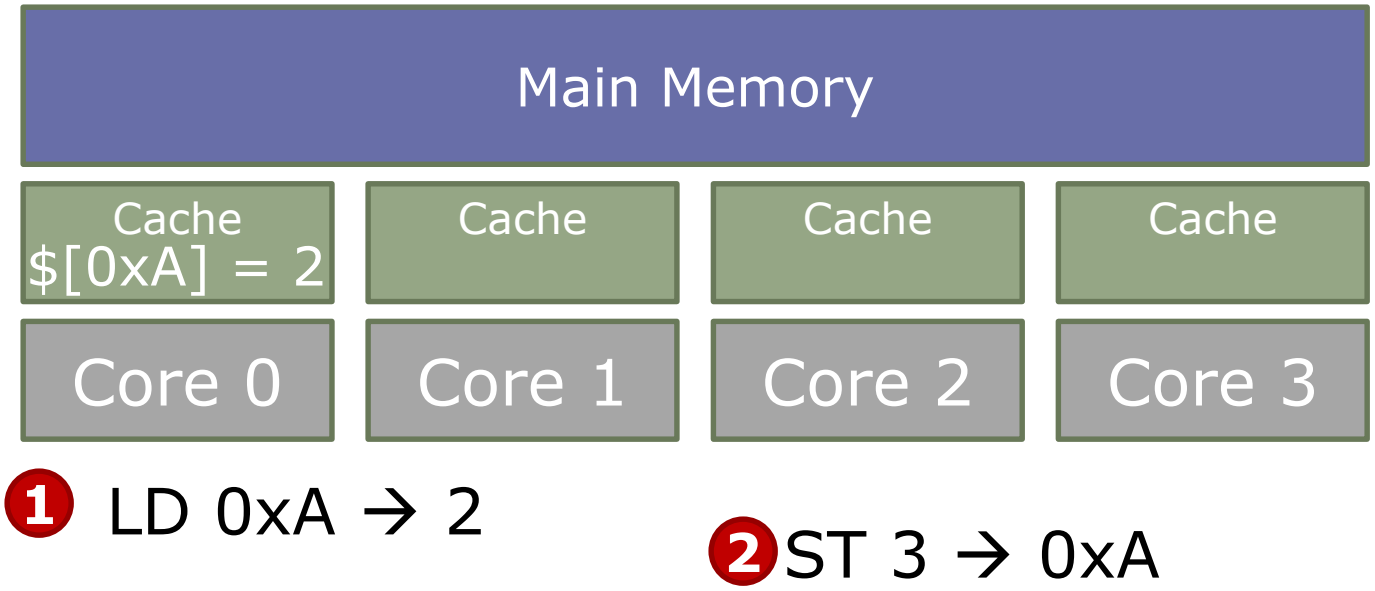

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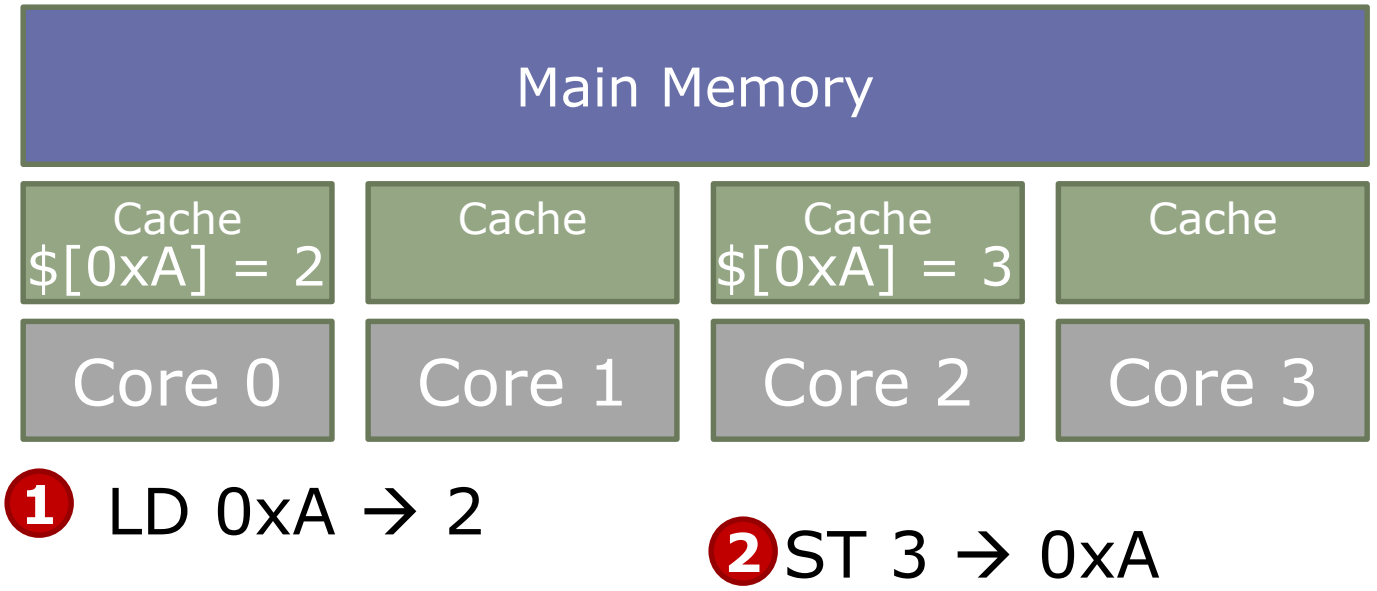

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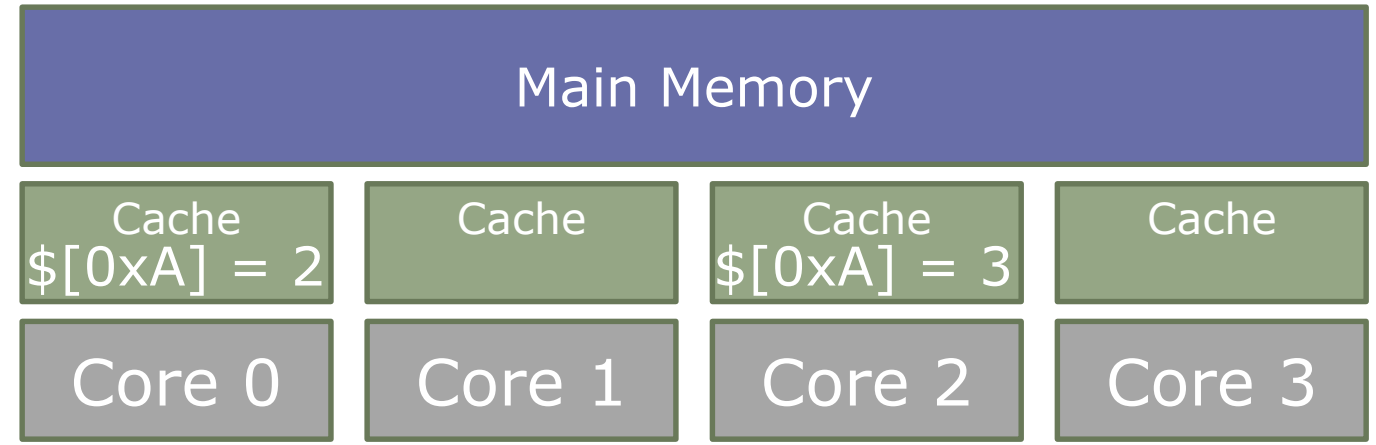

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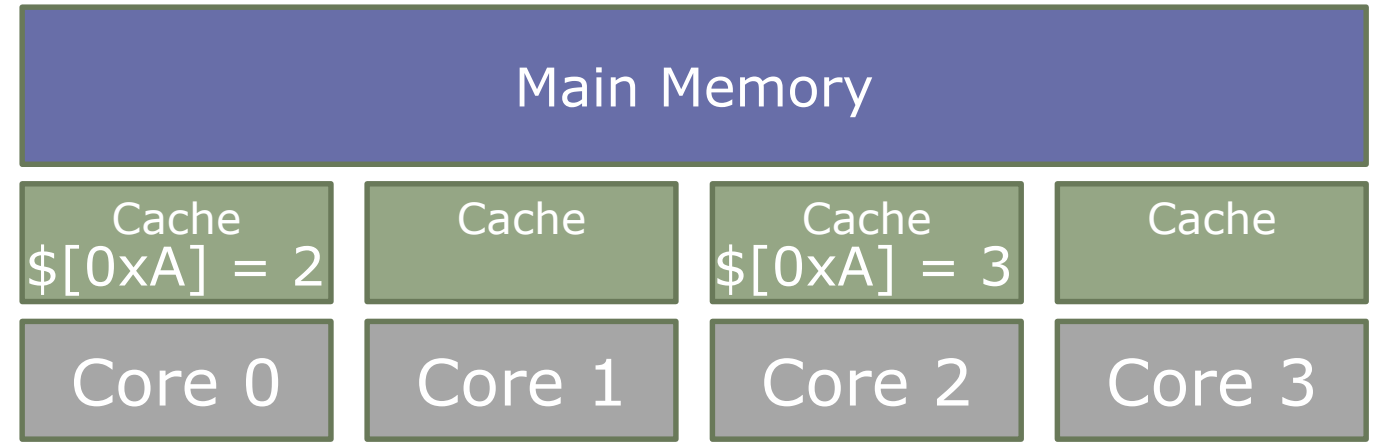

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- A cache coherence protocol controls cache contents to avoid stale cache lines

Implementing Cache Coherence

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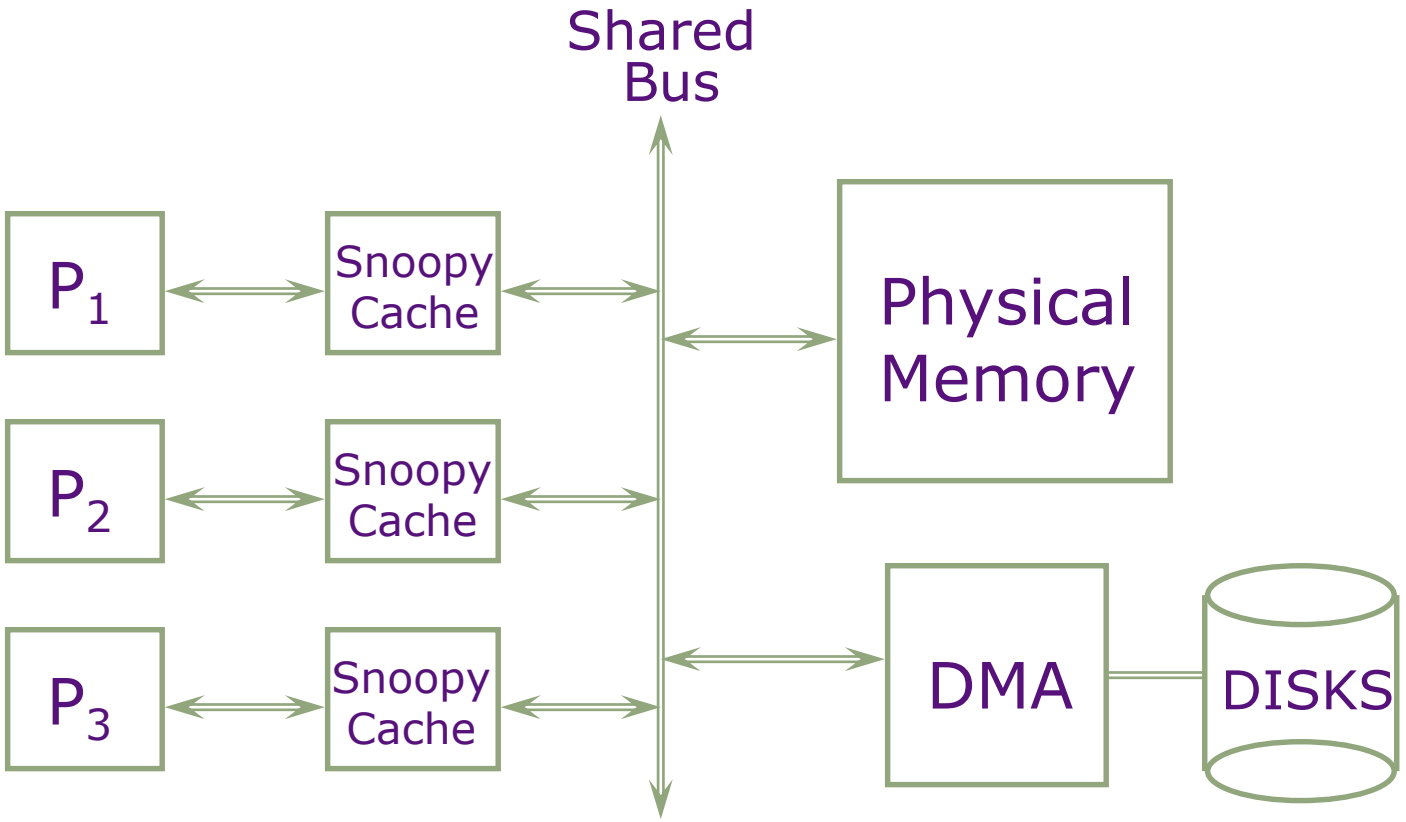
- How to track sharing state of cached data and serialize requests to the same address?
  - *Snooping-based protocols*: All caches observe each other's actions through a shared bus (bus is the serialization point)
  - *Directory-based protocols*: A coherence directory tracks contents of private caches and serializes requests (directory is the serialization point)

Snooping-Based Coherence
(Goodman, 1983)



Caches watch (snoop on) bus to keep all processors' view of memory coherent

Snooping-Based Coherence

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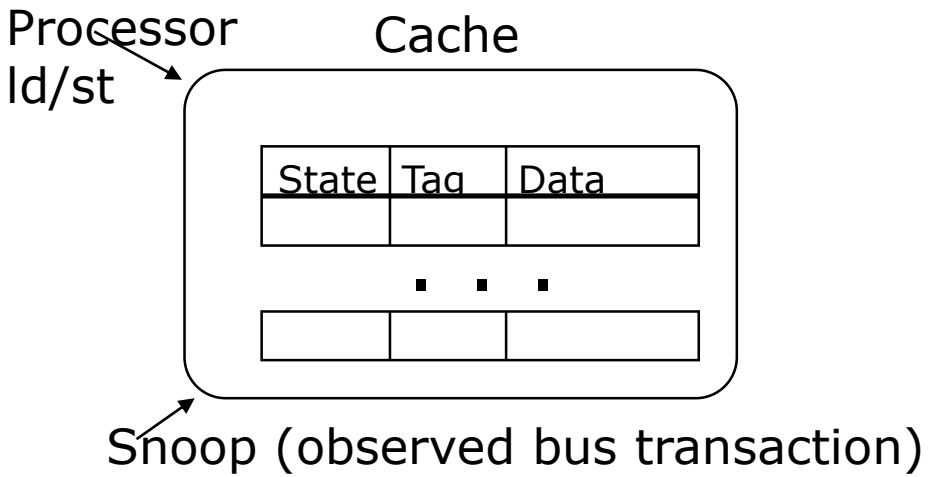

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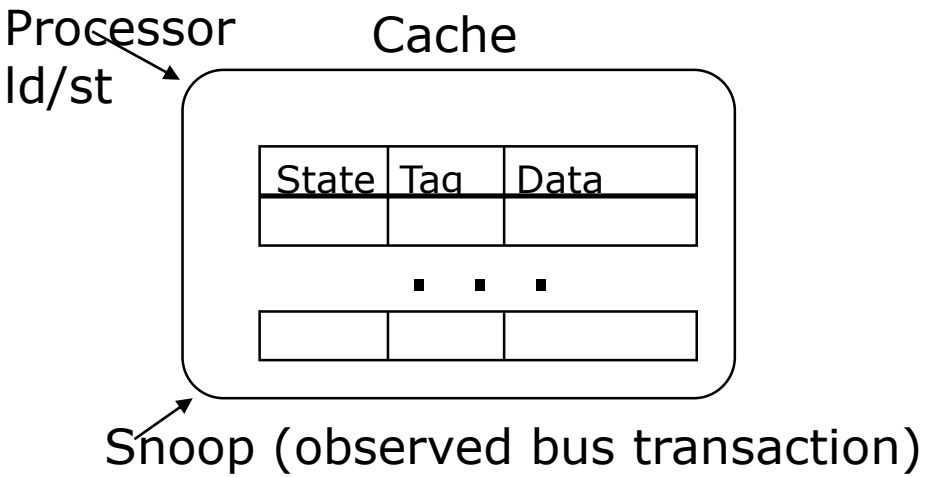

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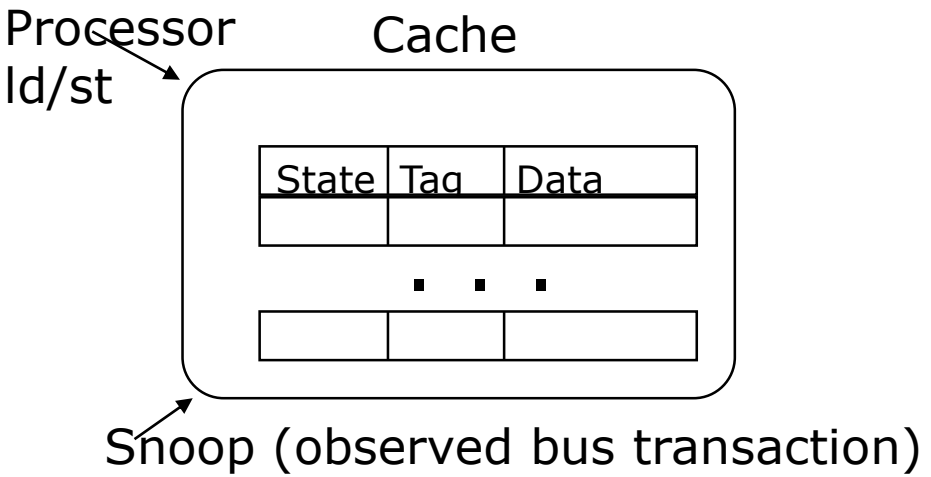
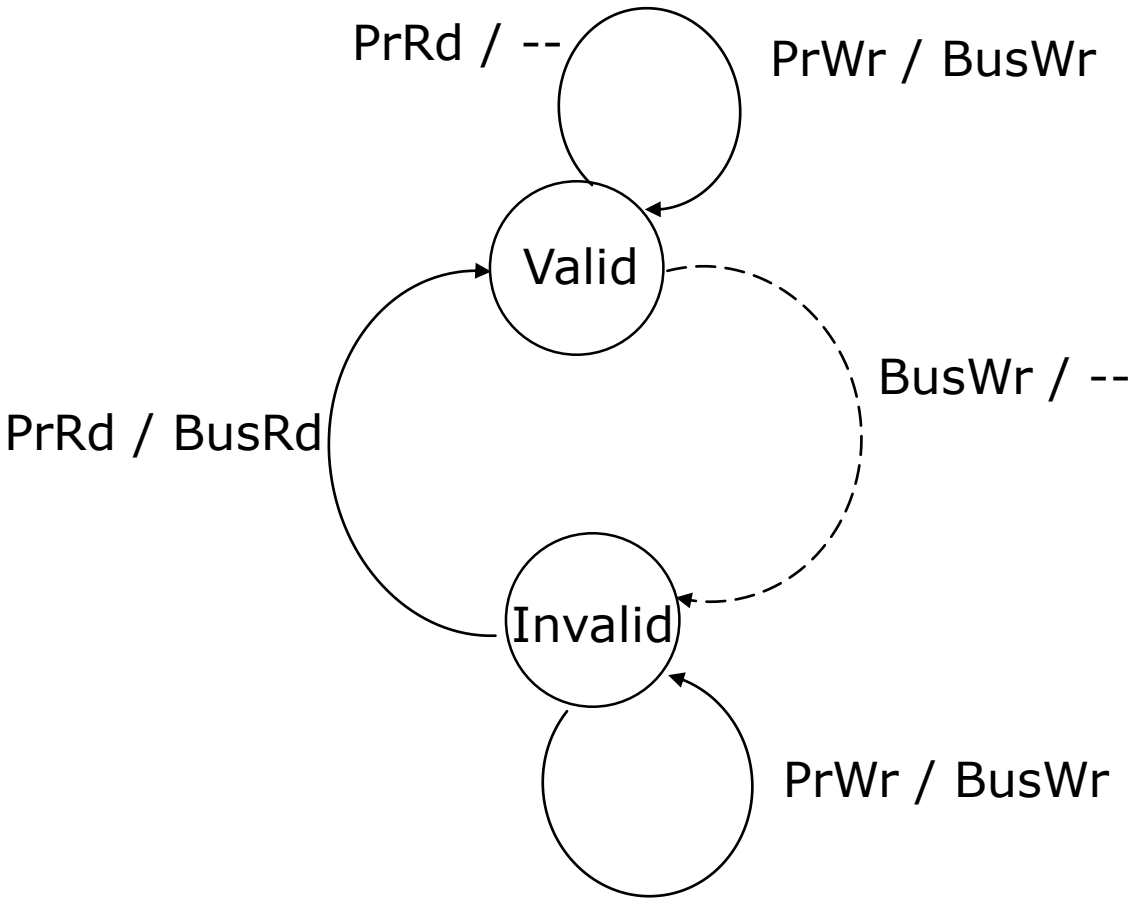
- Handling writes:
  - Write-invalidate
  - Write-update



A Simple Protocol: Valid/Invalid (VI)

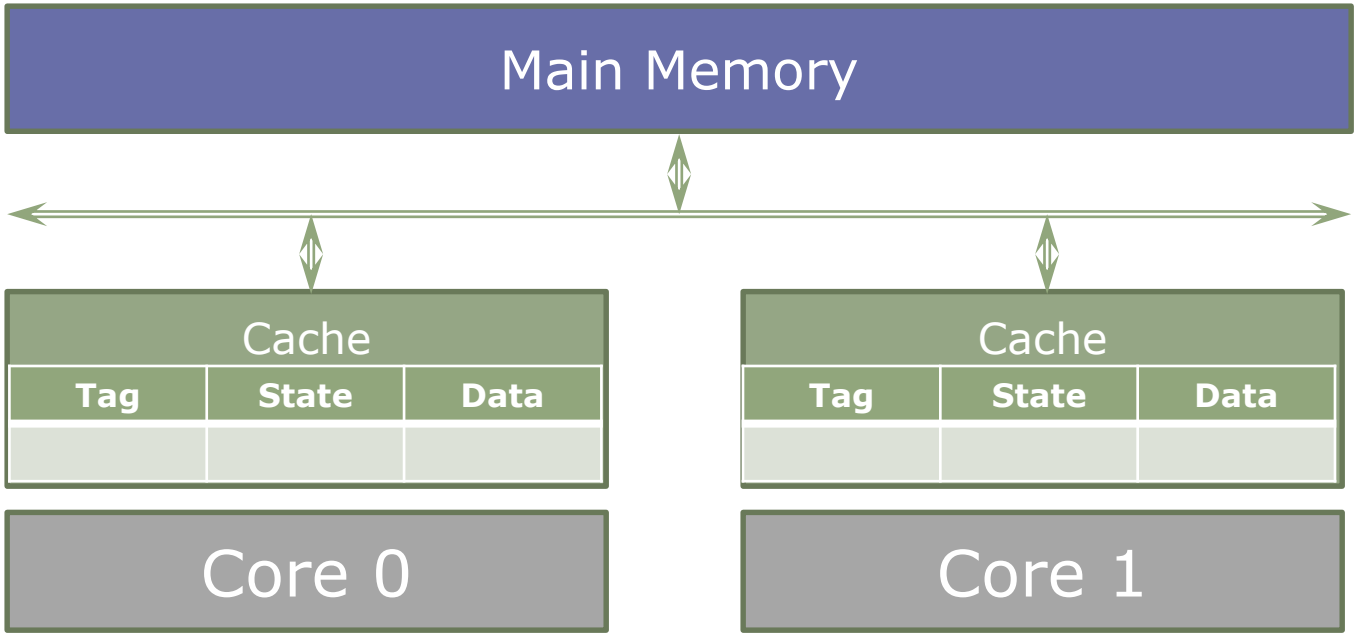


- Assume write-through caches
- Transition nomenclature:

triggering action / taken action(s)

Actions
Processor Read (PrRd)
Processor Write (PrWr)
Bus Read (BusRd)
Bus Write (BusWr)

Valid/Invalid Example



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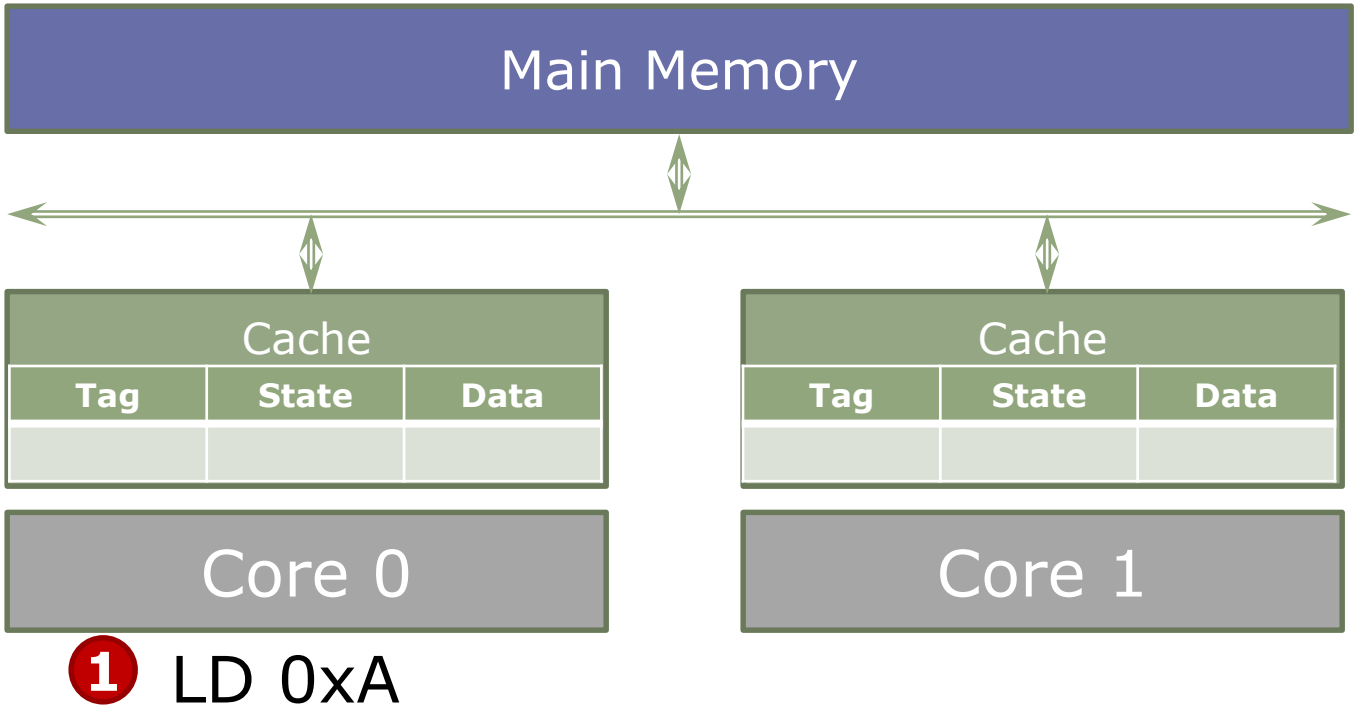
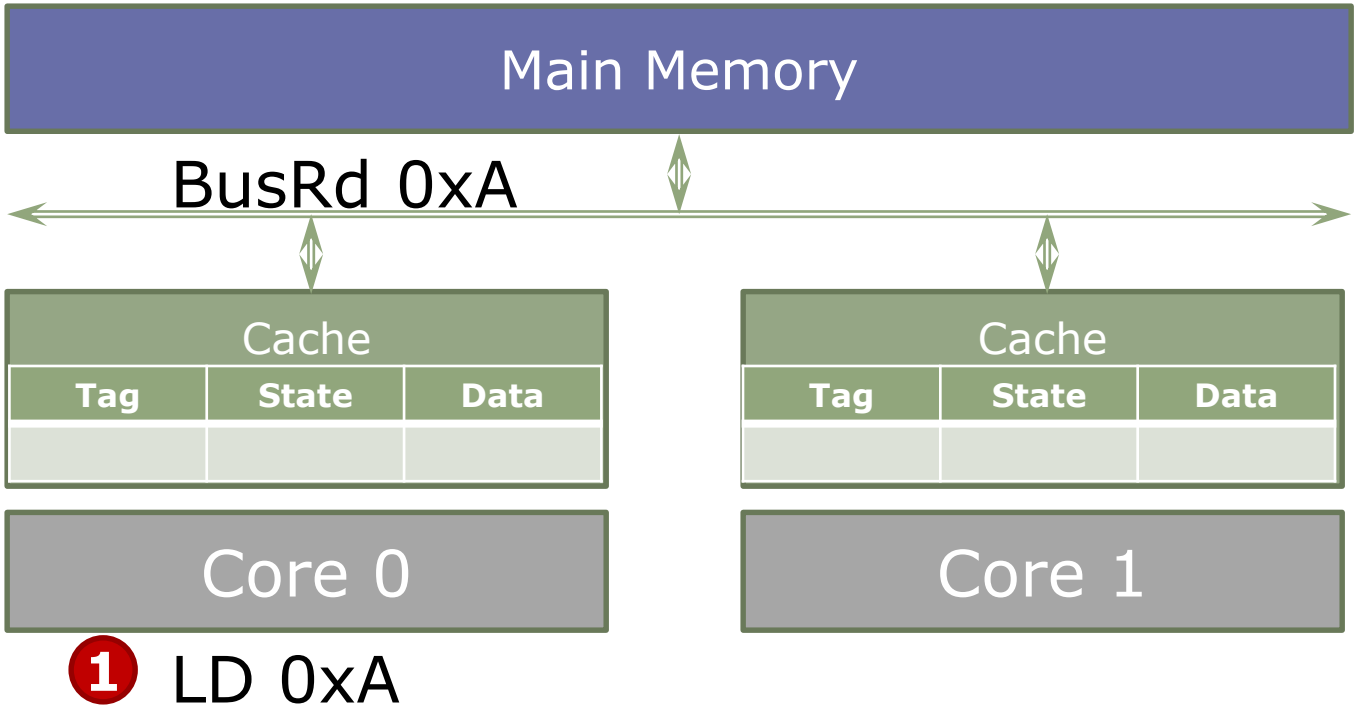
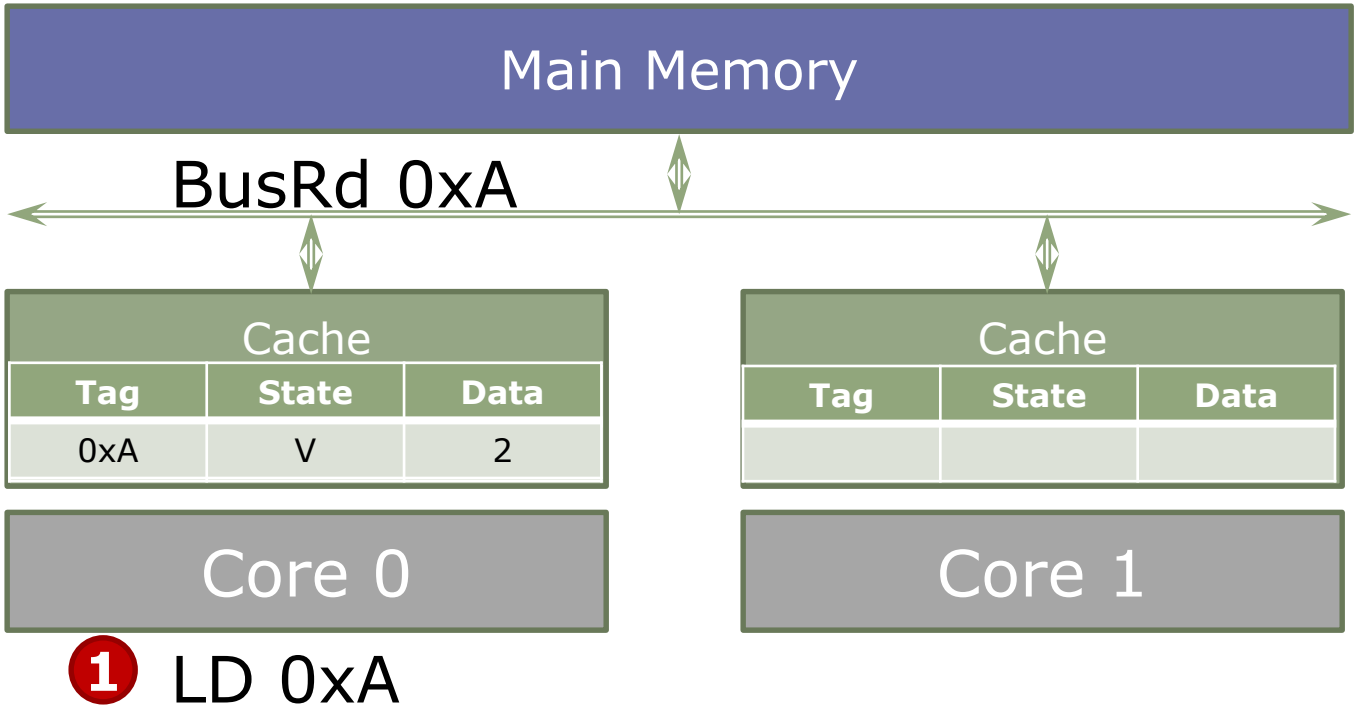


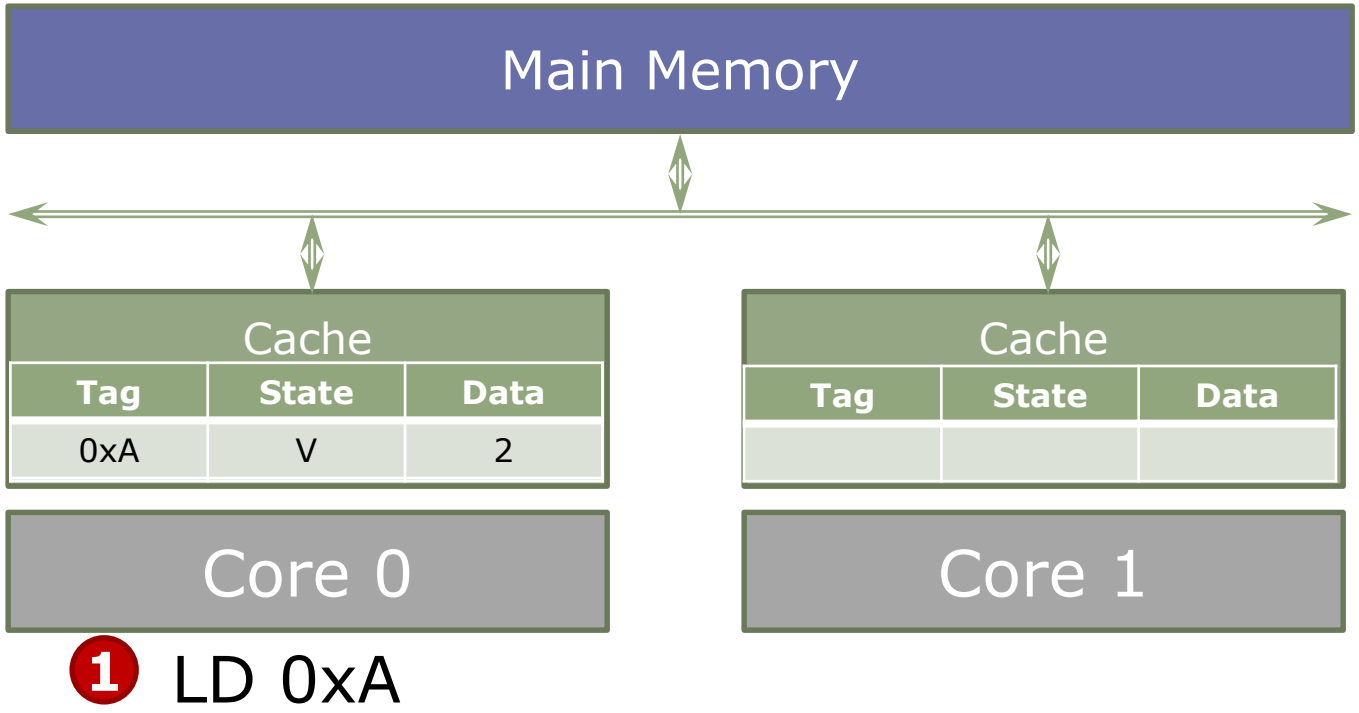
Valid/Invalid Example



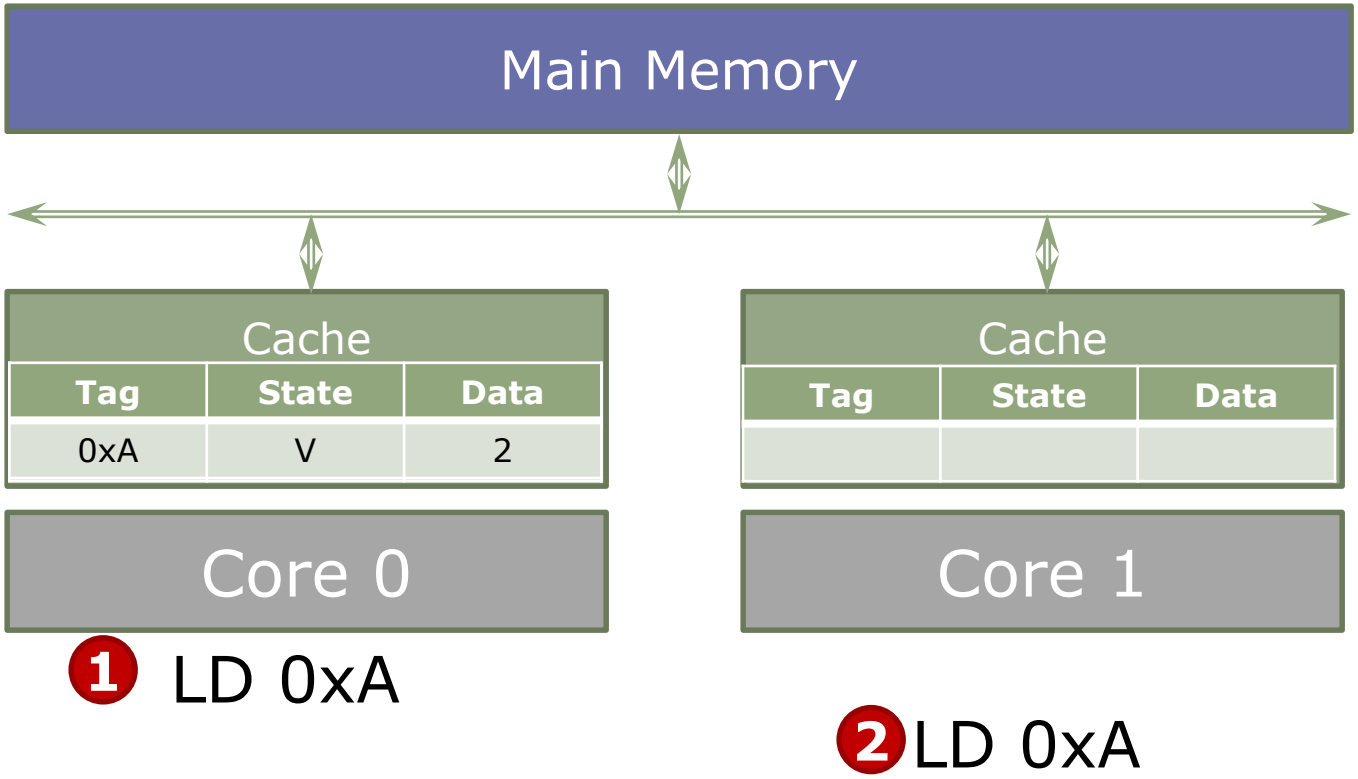
Valid/Invalid Example



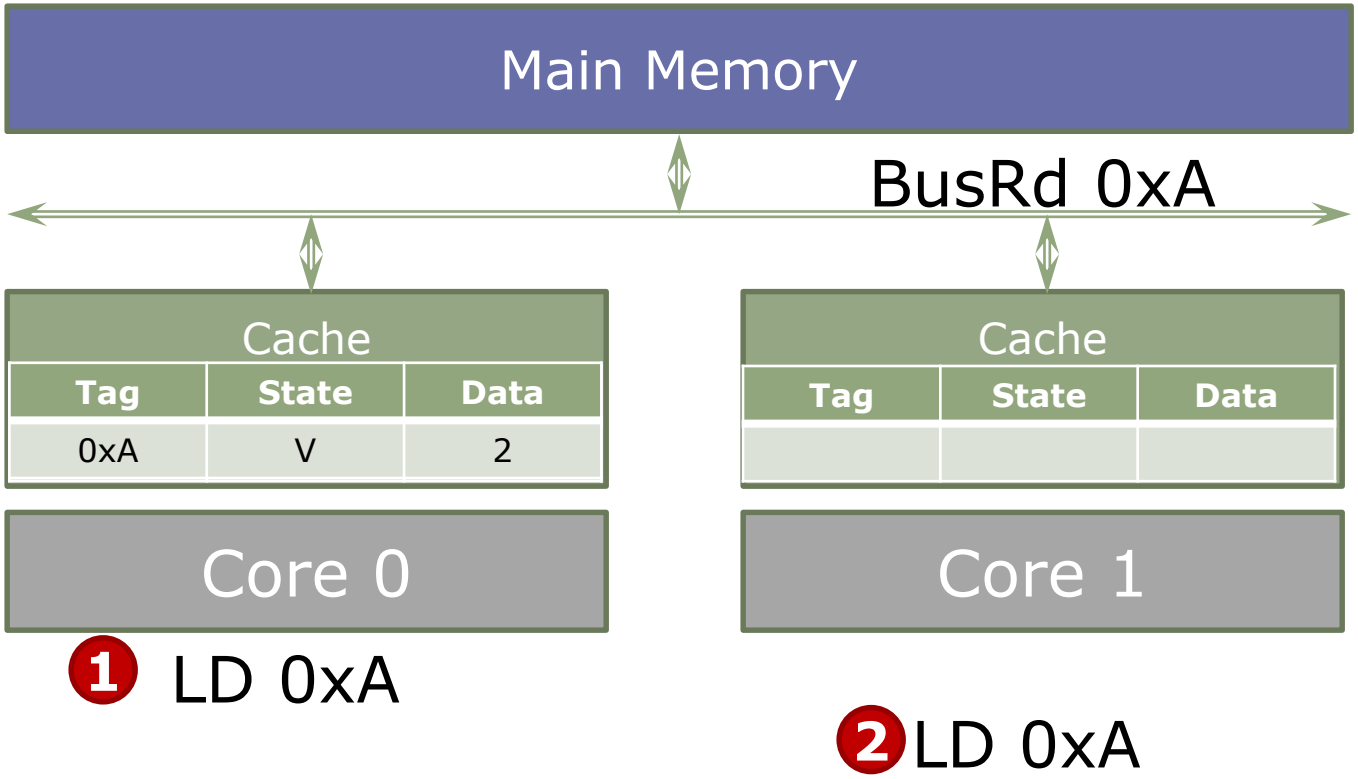
Valid/Invalid Example



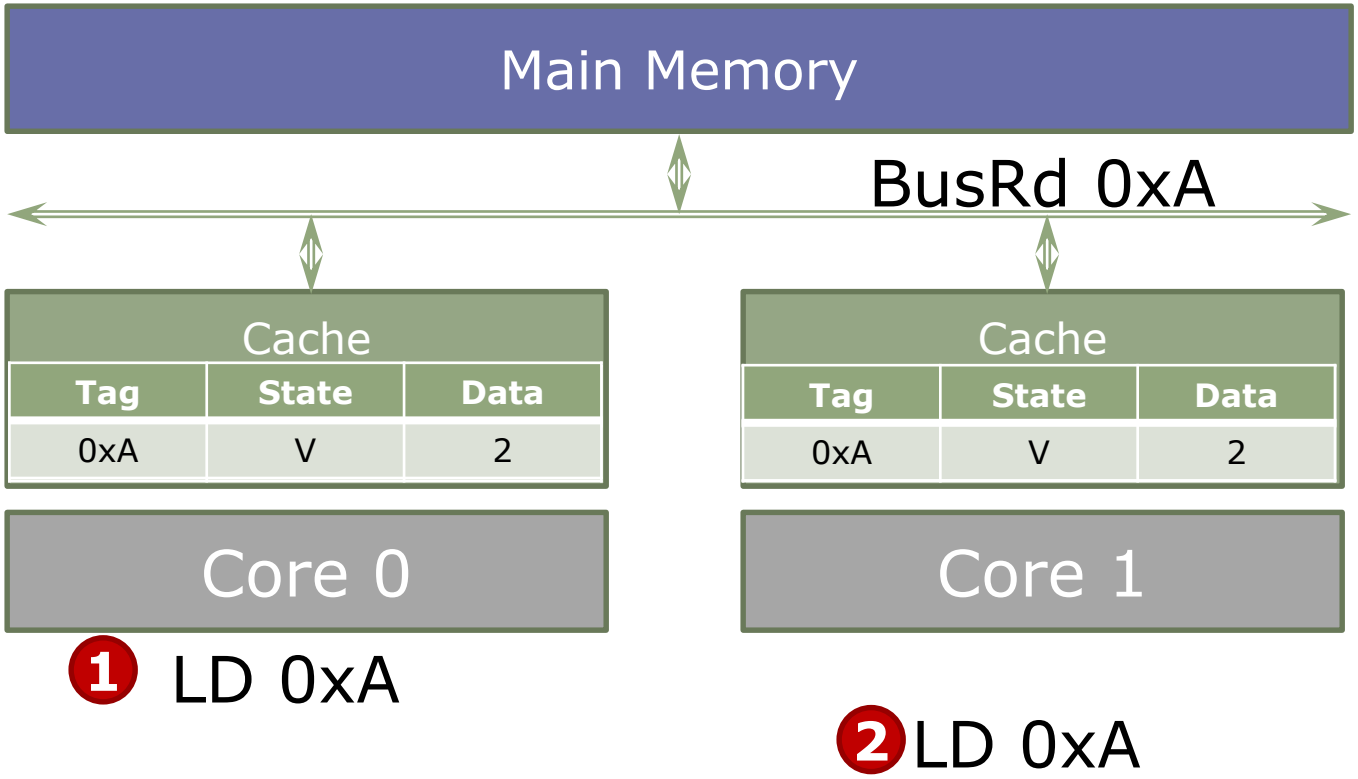
Valid/Invalid Example



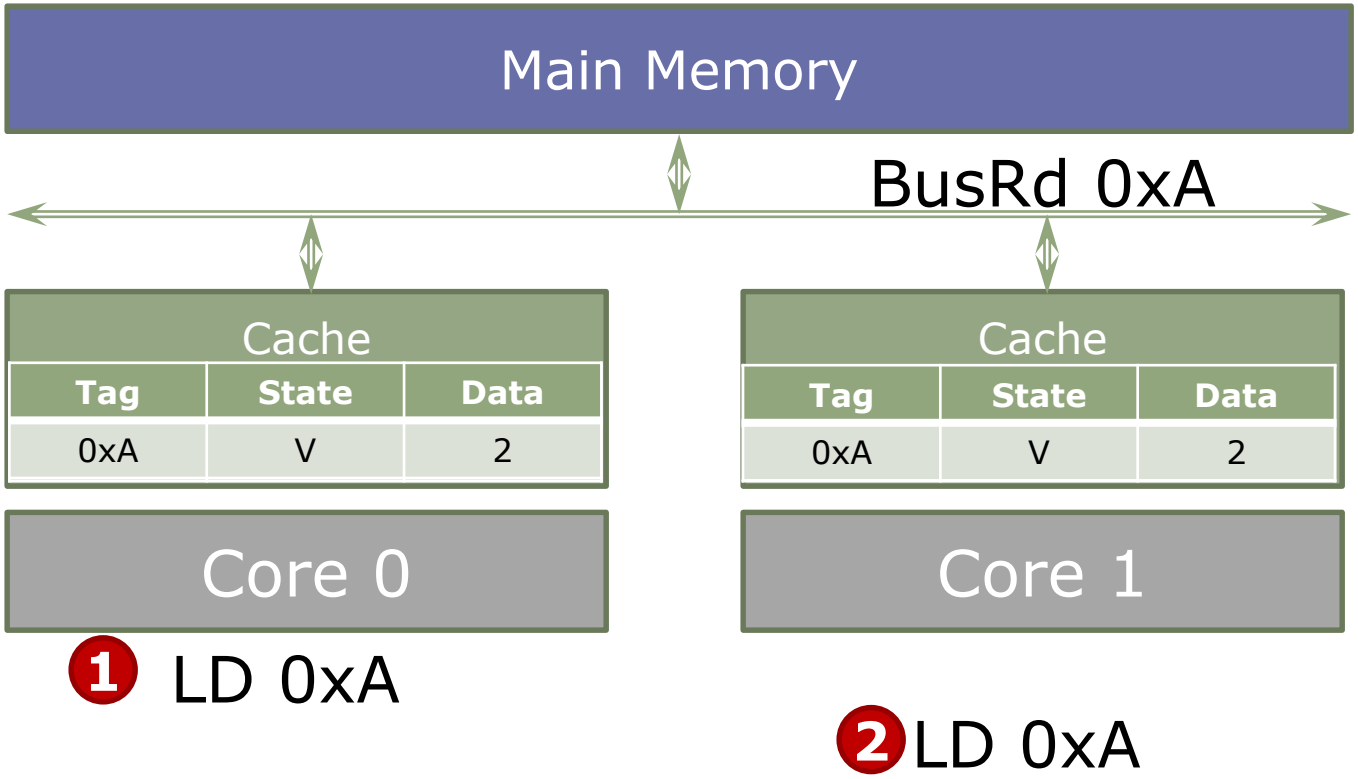
Valid/Invalid Example



Valid/Invalid Example

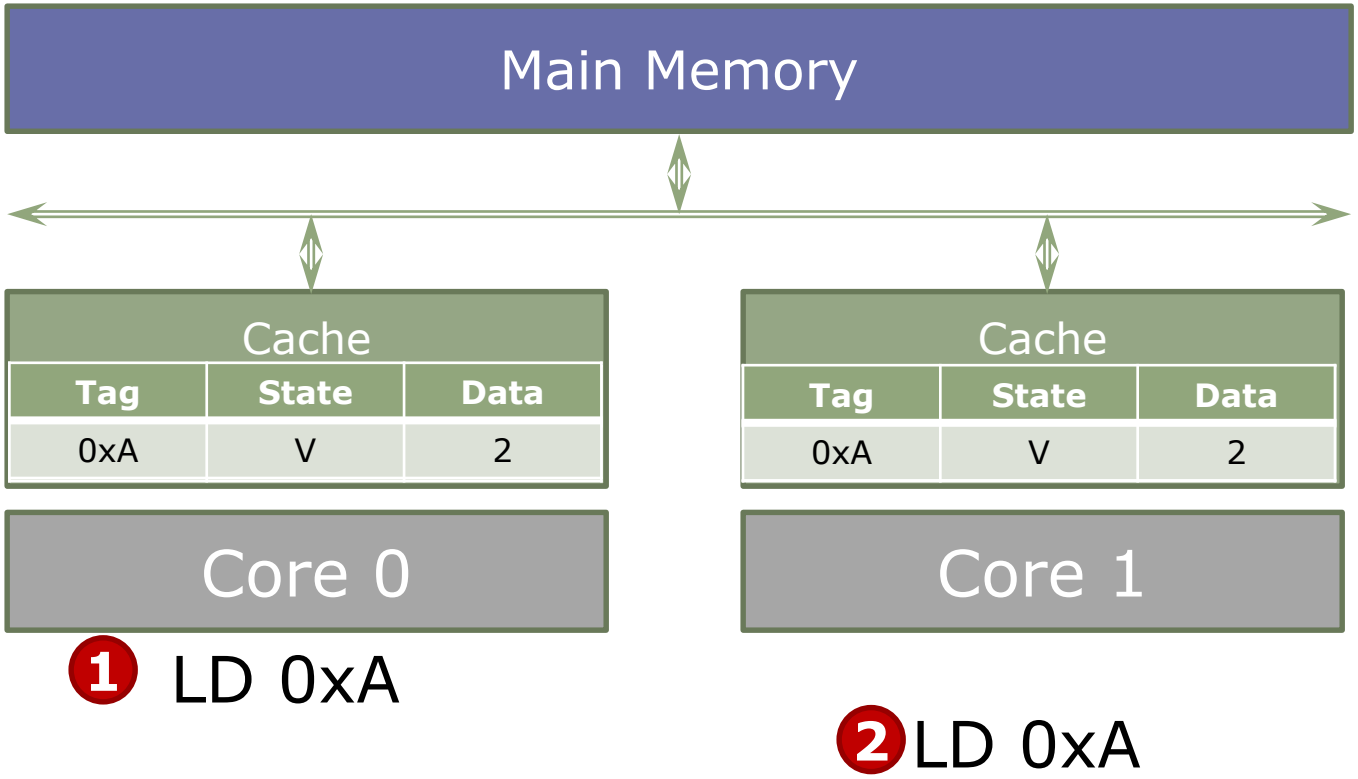


Valid/Invalid Example

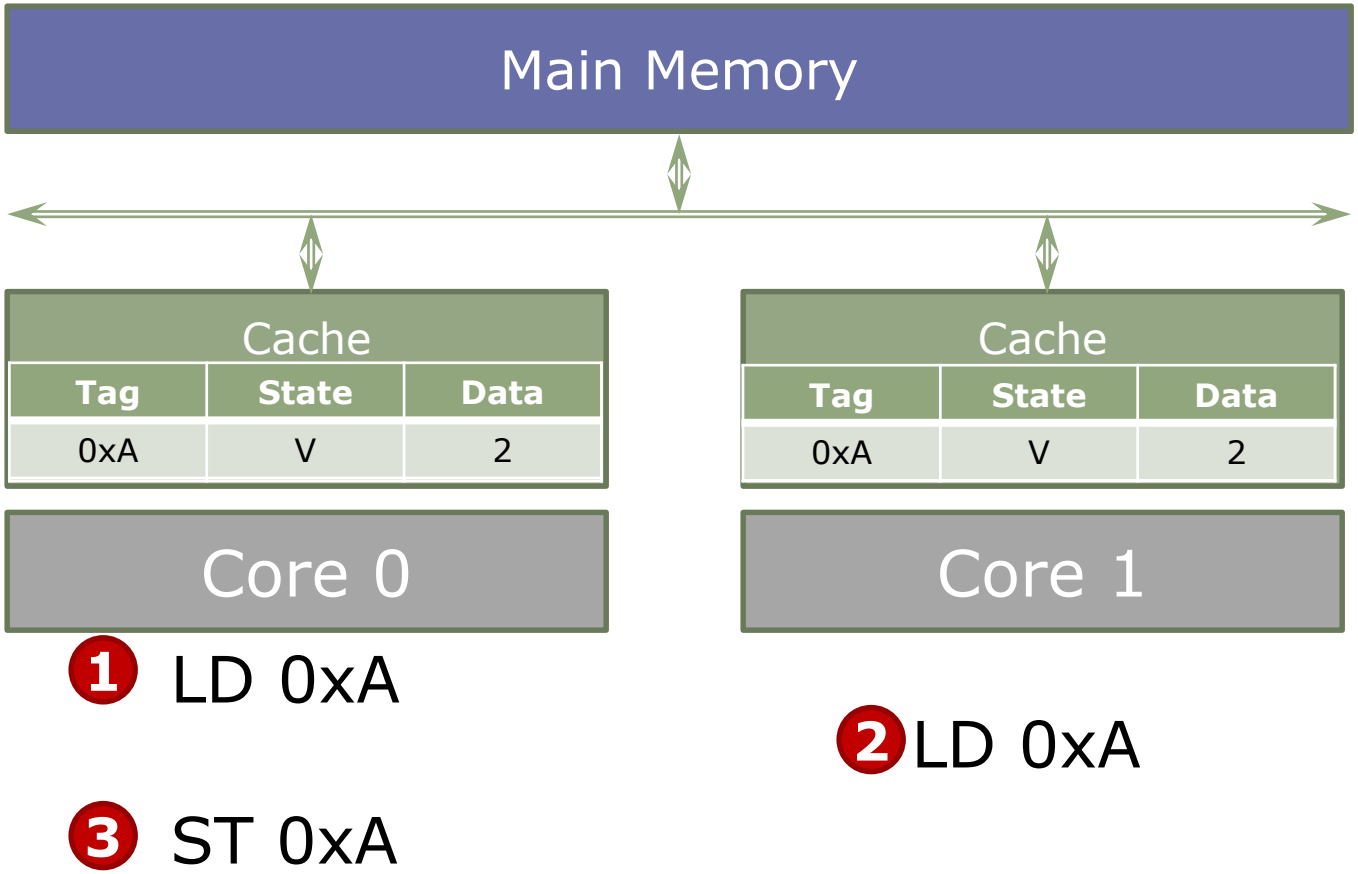


Additional loads satisfied locally, without BusRd

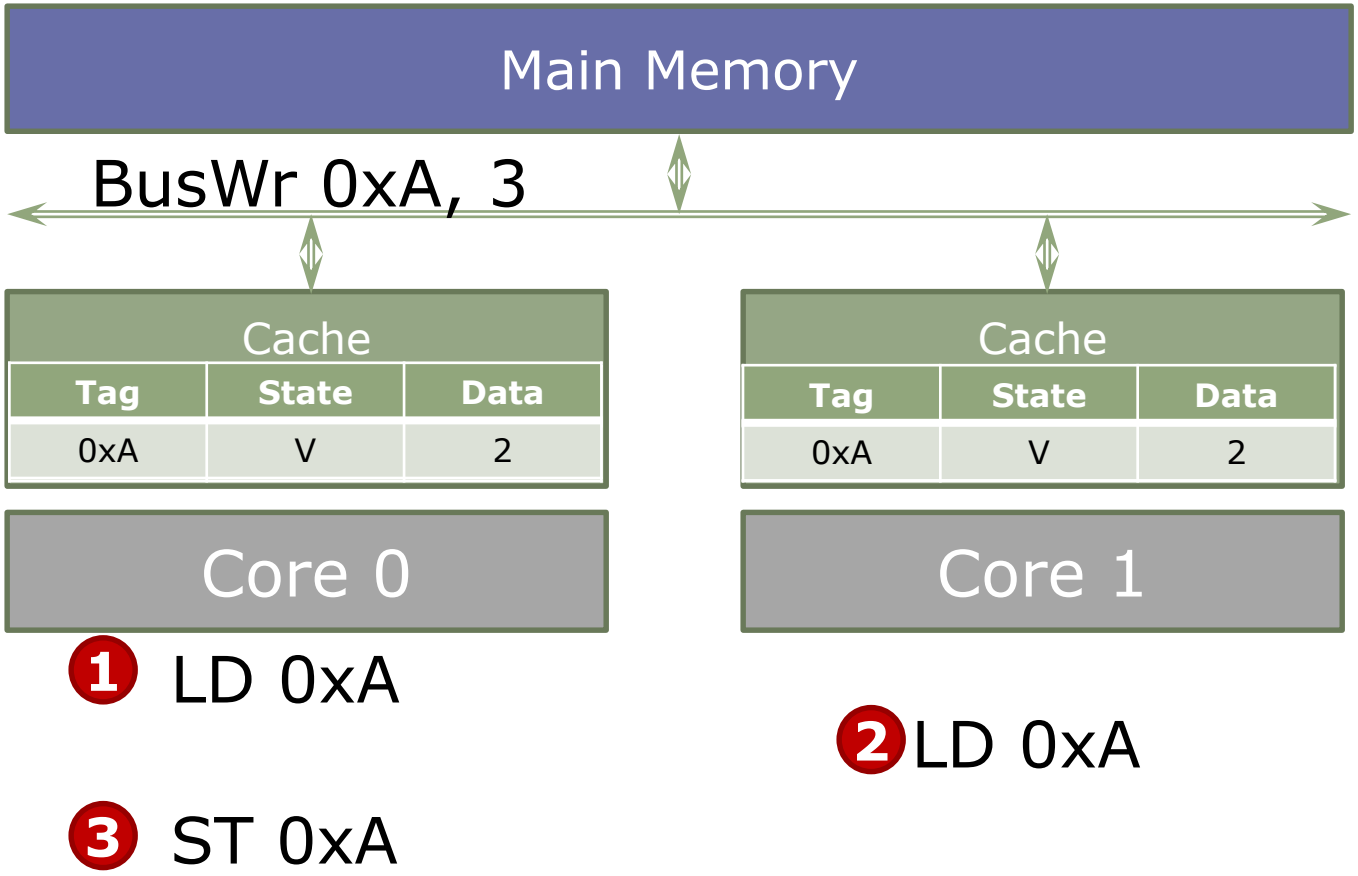
Valid/Invalid Example



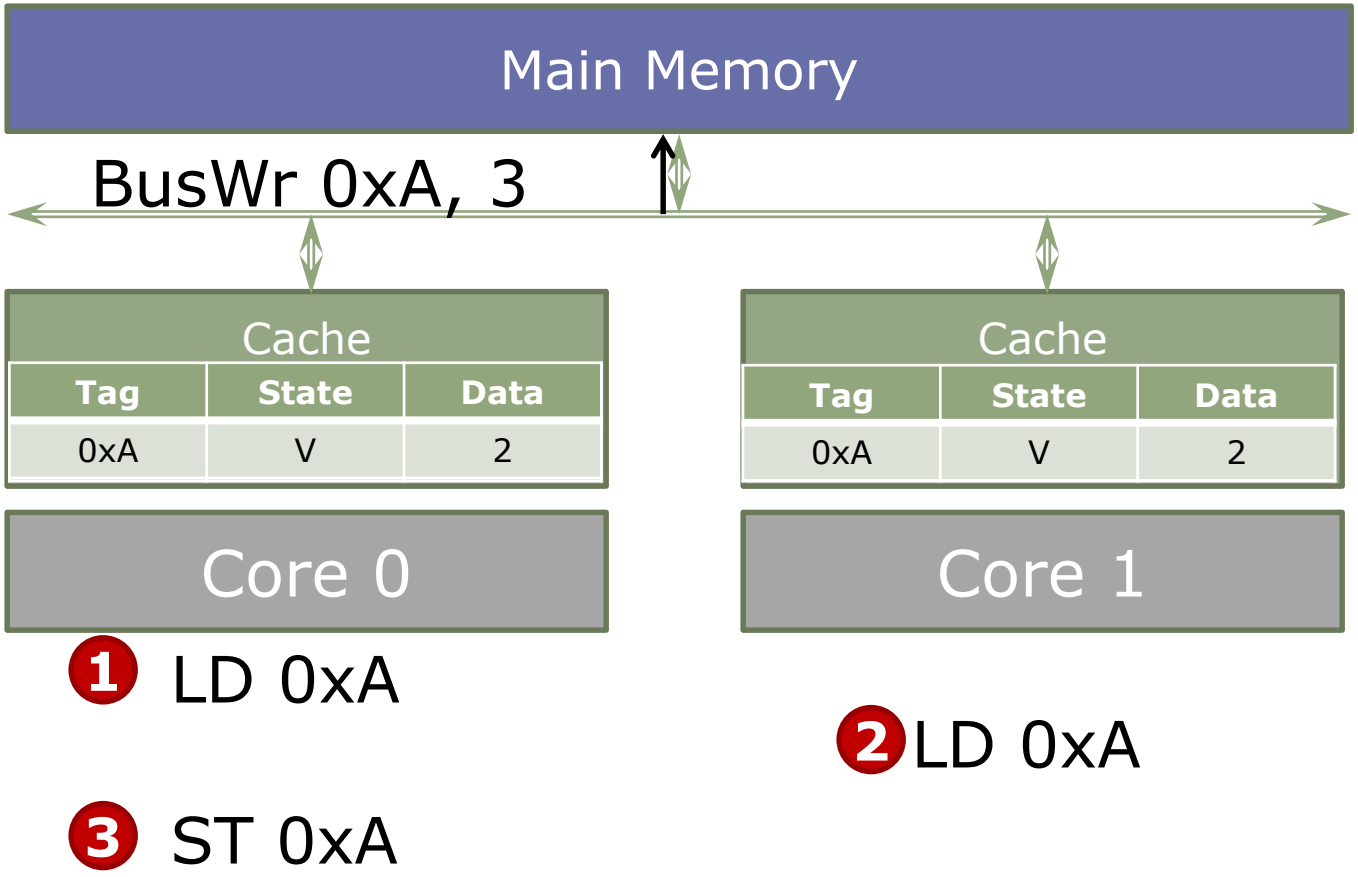
Valid/Invalid Example



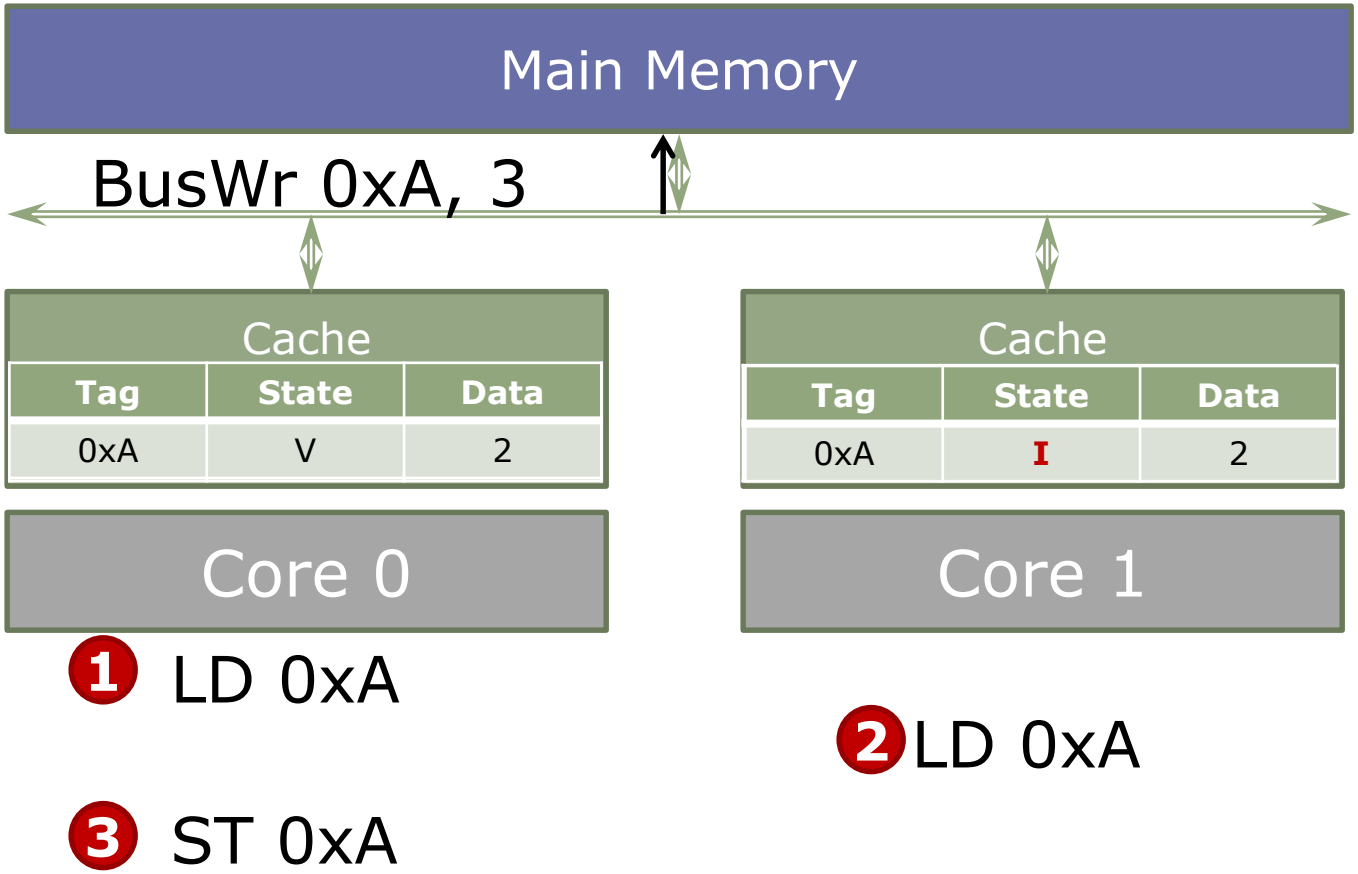
Valid/Invalid Example



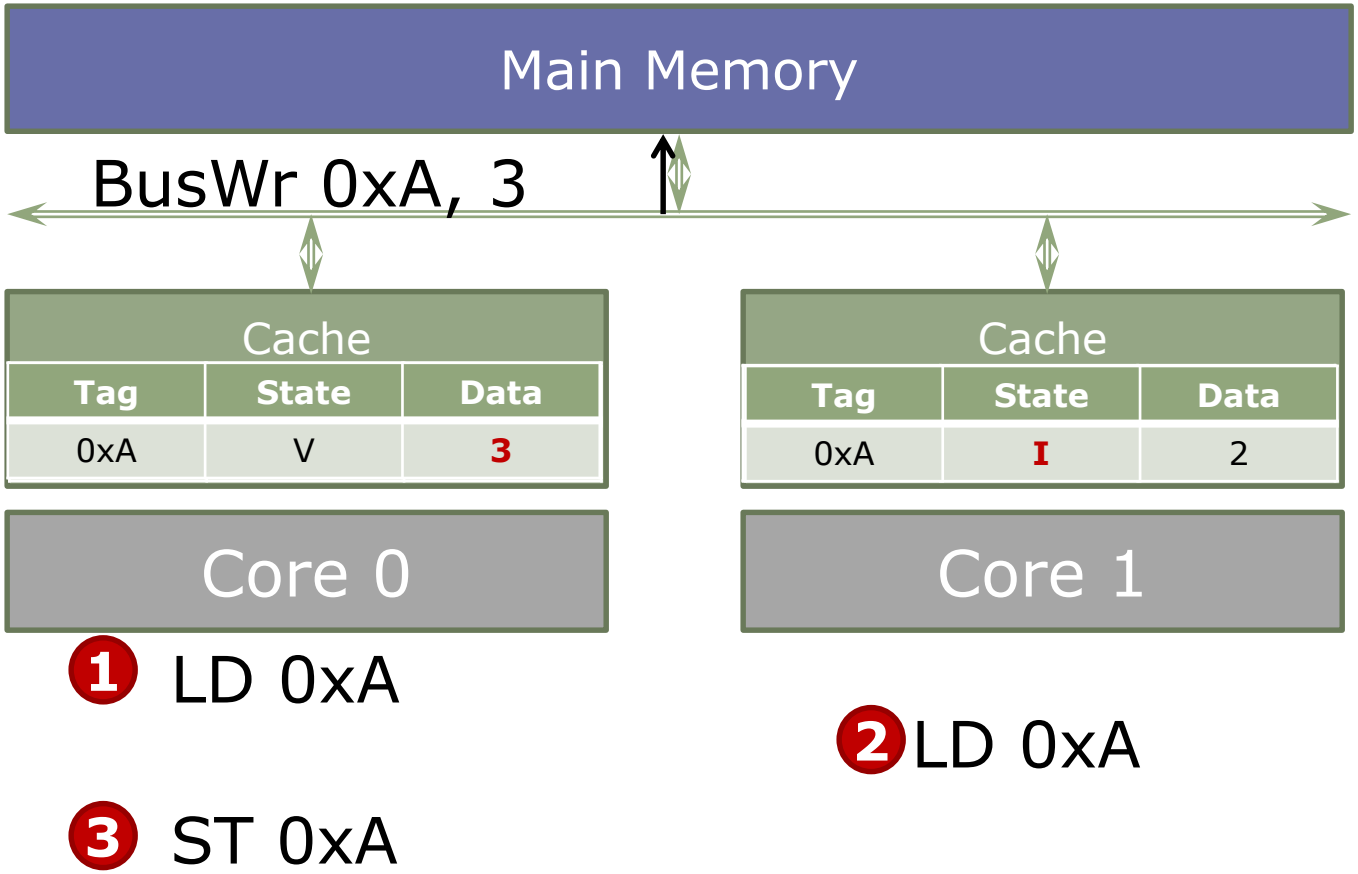
Valid/Invalid Example



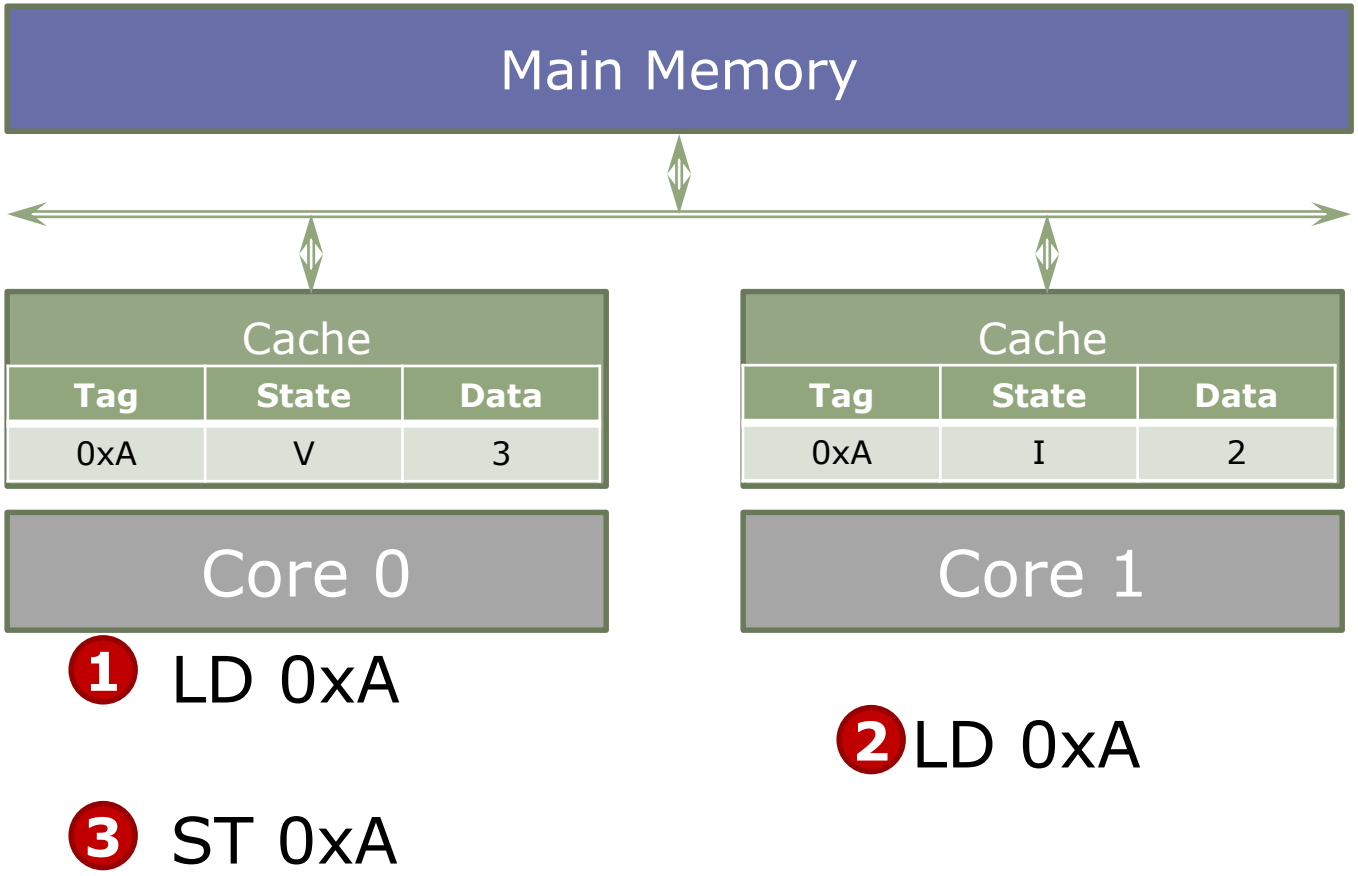
Valid/Invalid Example



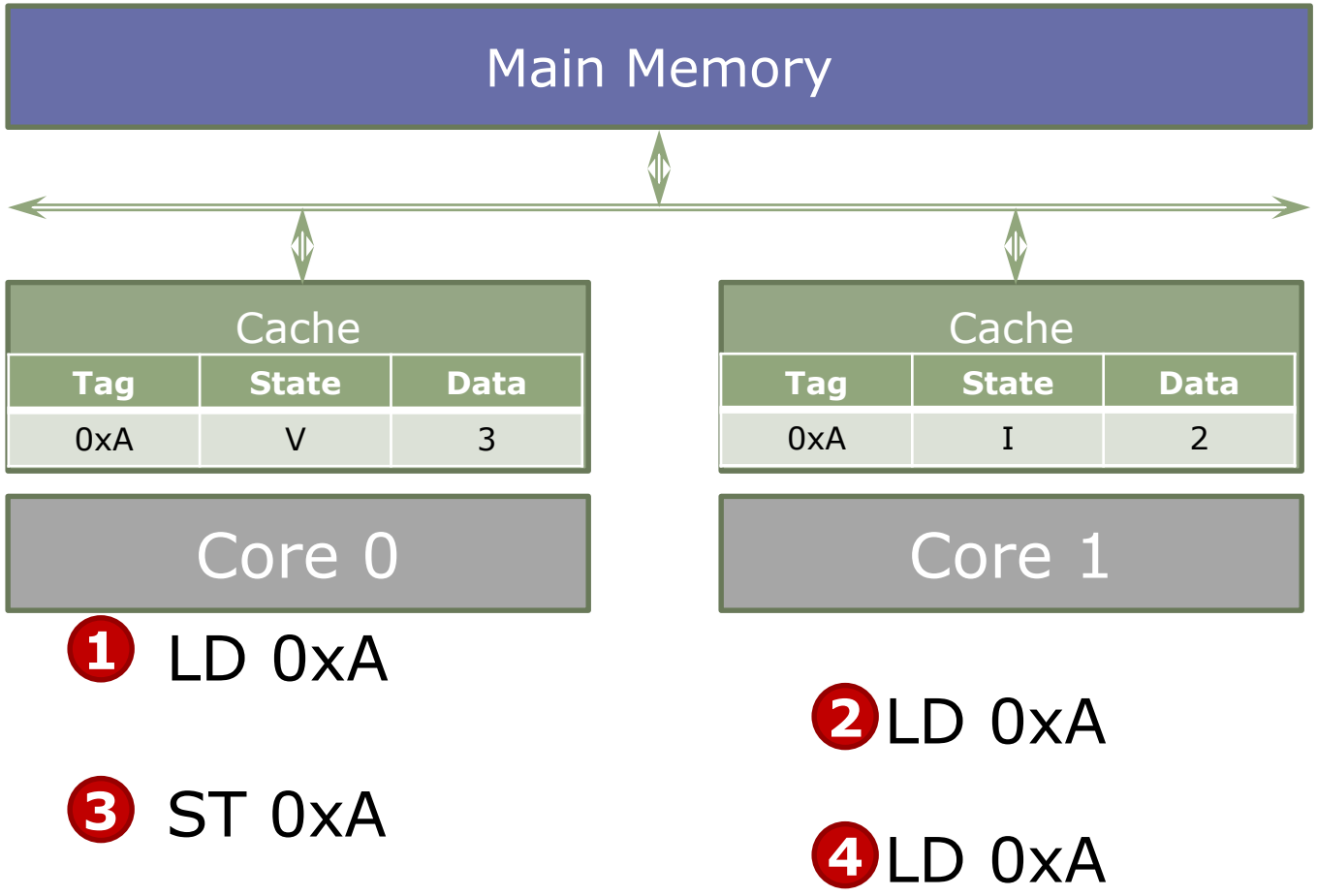
Valid/Invalid Example



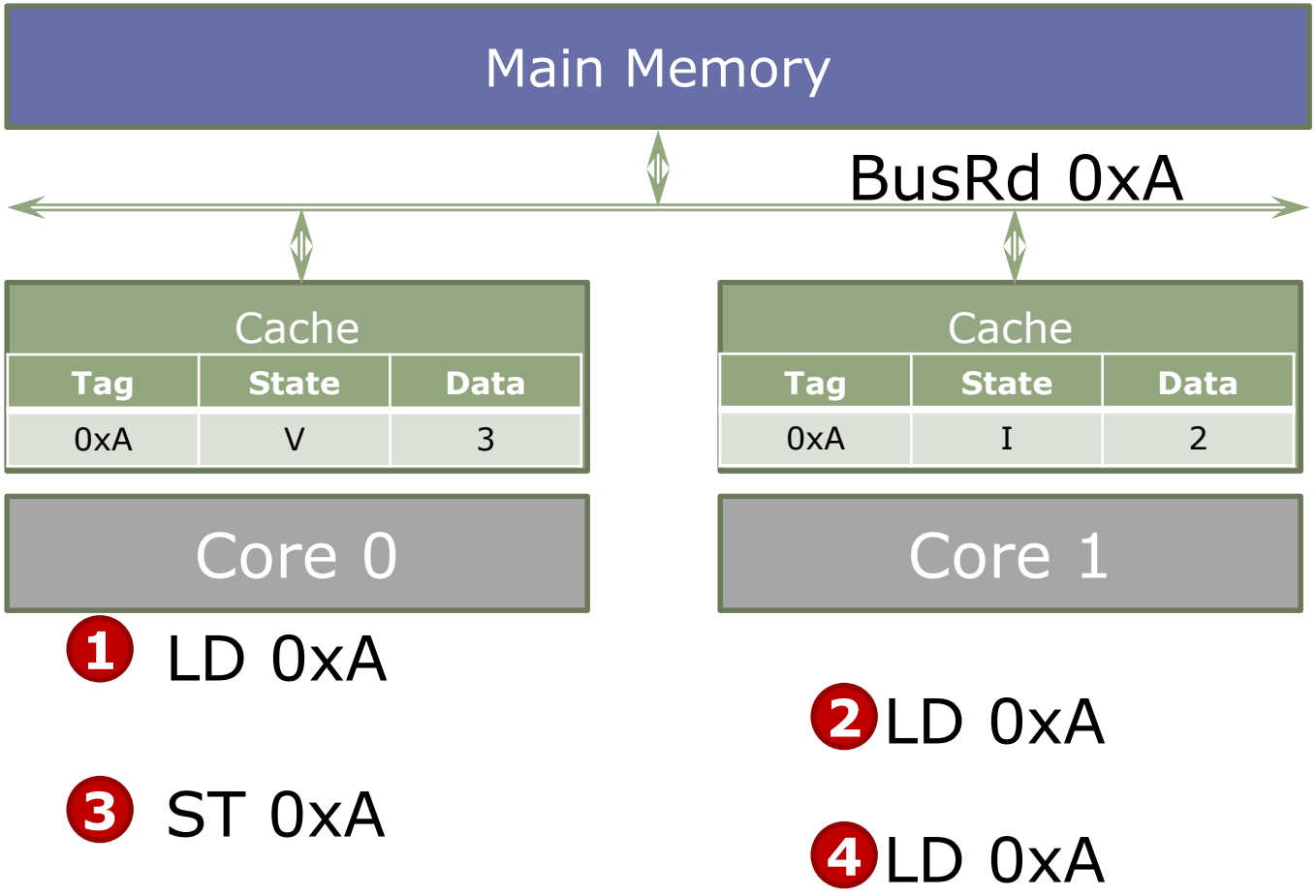
Valid/Invalid Example



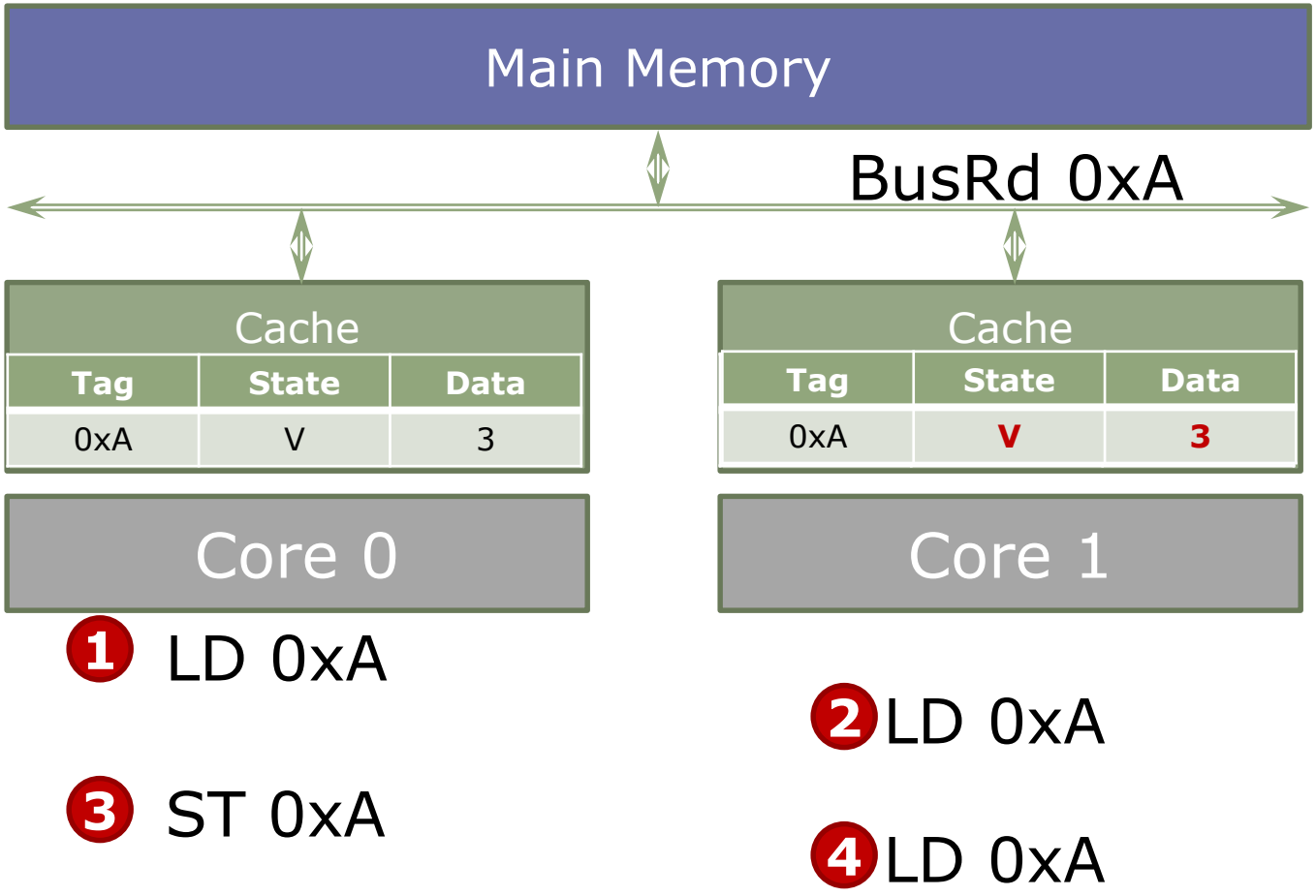
Valid/Invalid Example



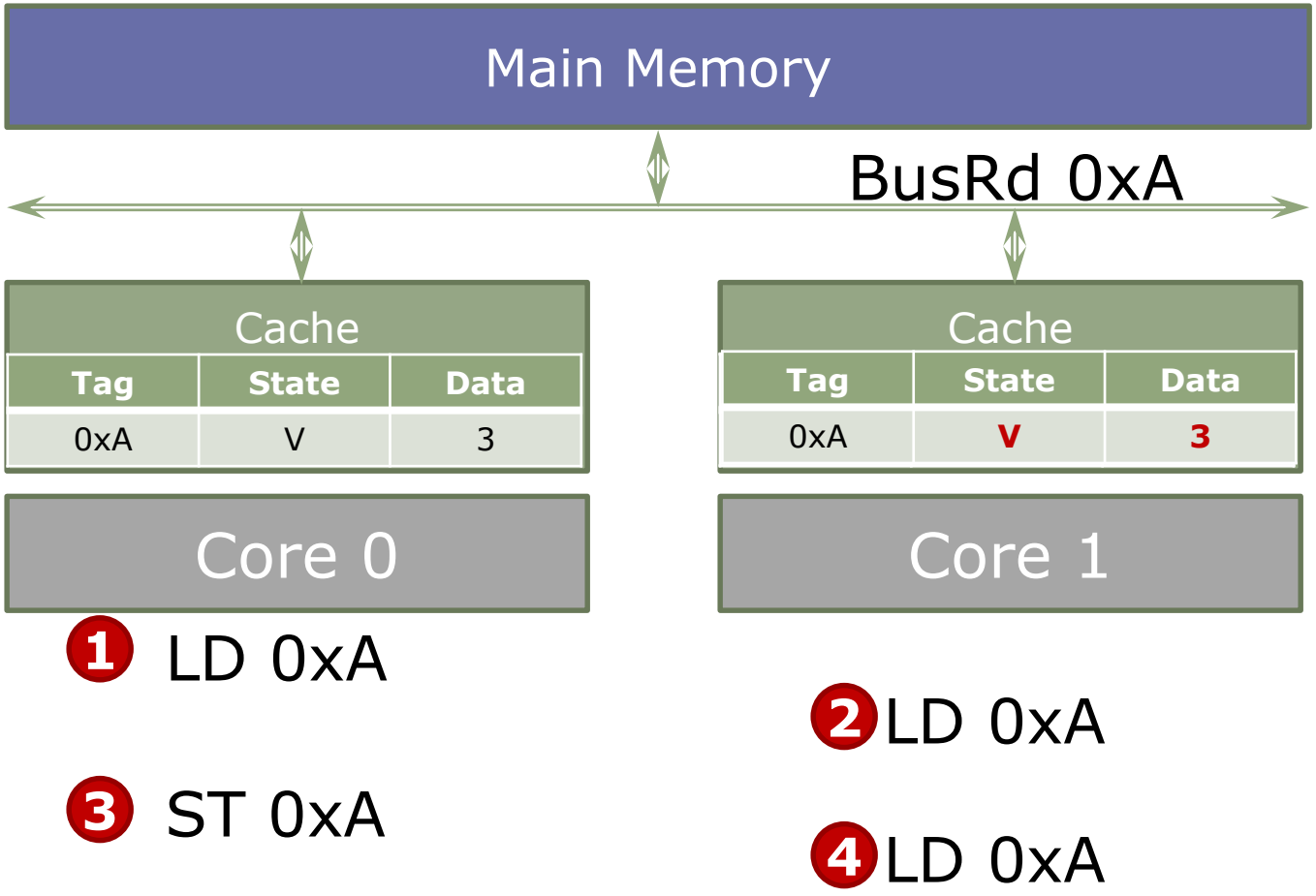
Valid/Invalid Example



Valid/Invalid Example

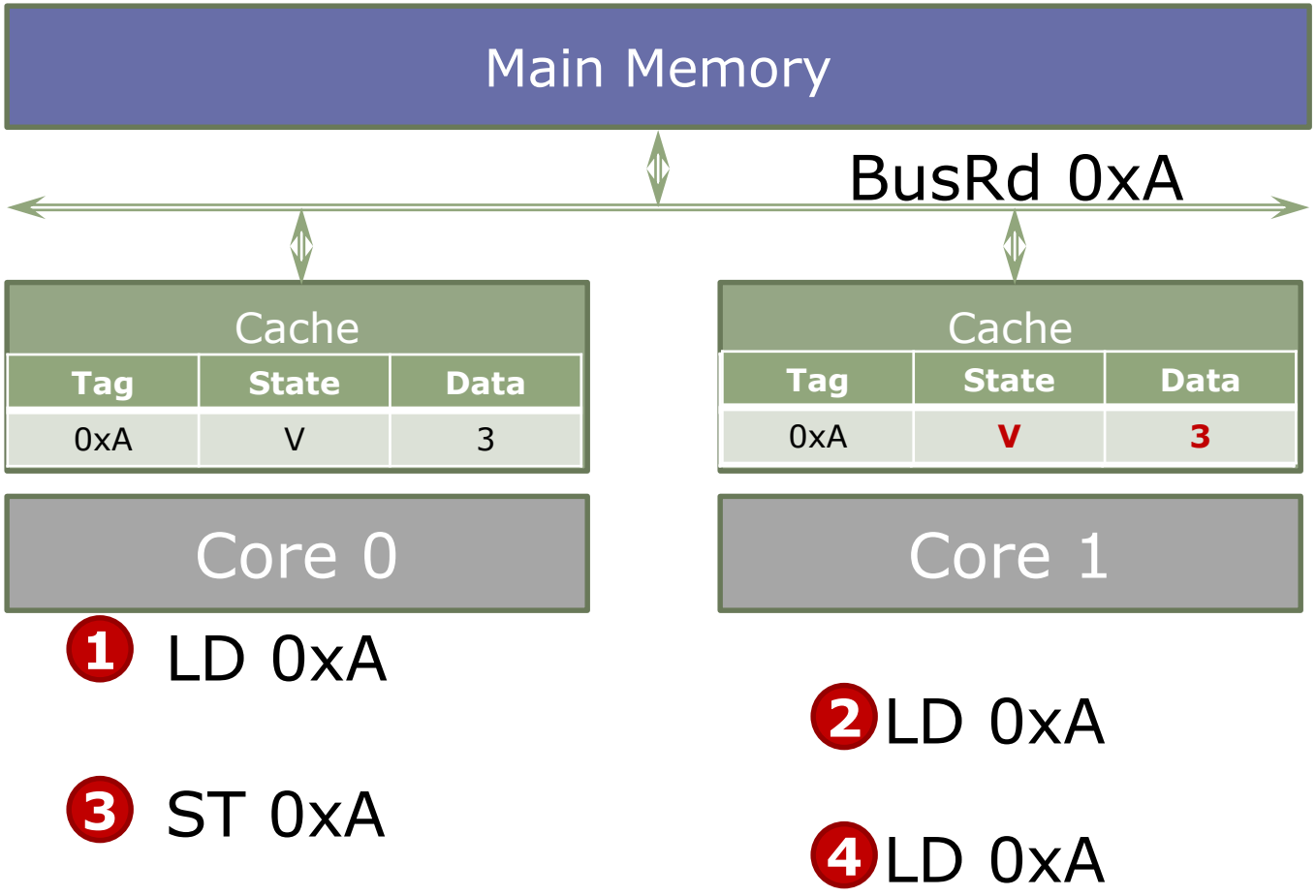


Valid/Invalid Example



VI Problems?

Valid/Invalid Example



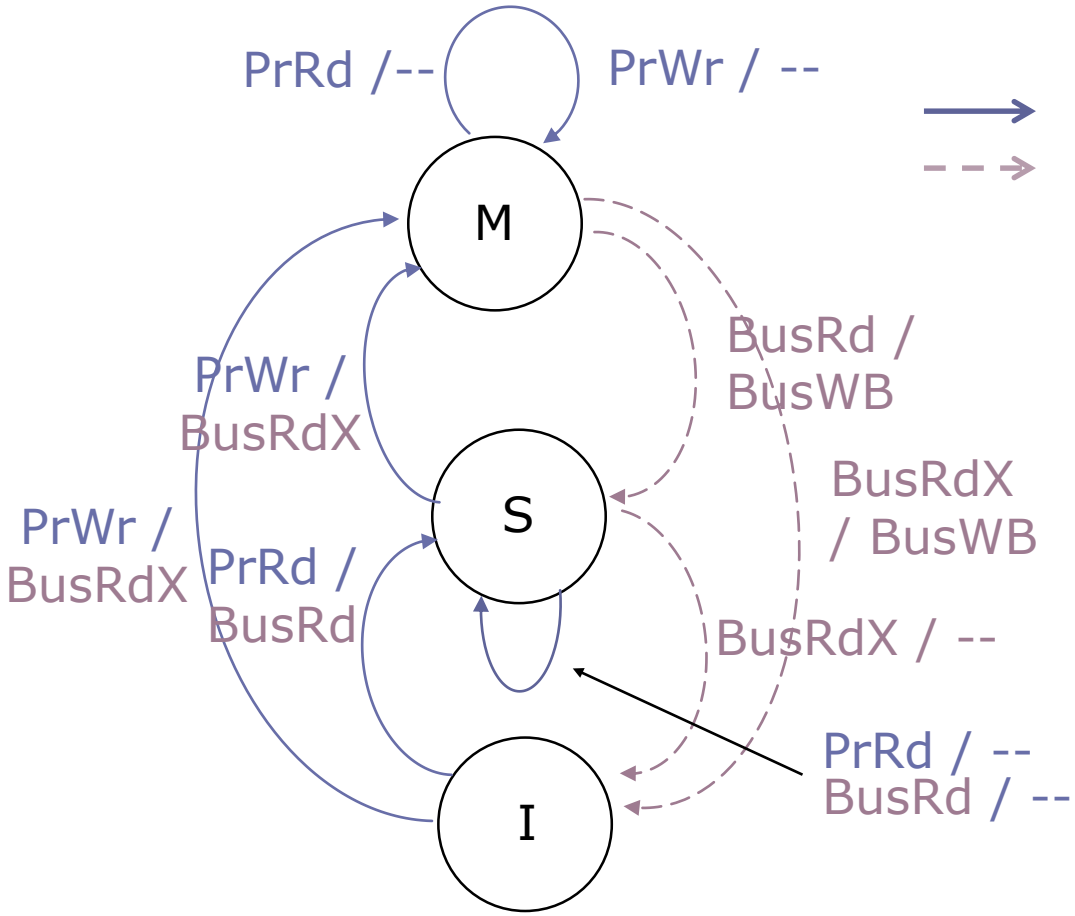
VI Problems?

Every write updates main memory

Every write requires broadcast & snoop

Modified/Shared/Invalid (MSI) Protocol

- Allows writeback caches + satisfying writes locally

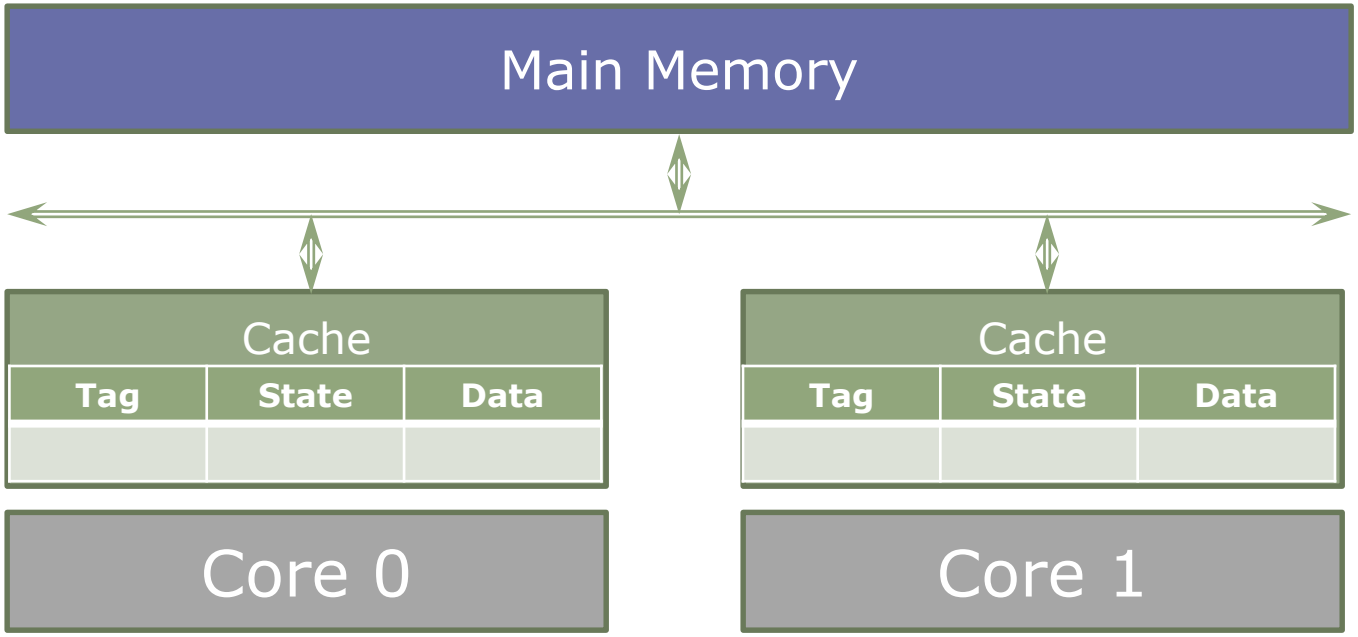


Processor-initiated transitions

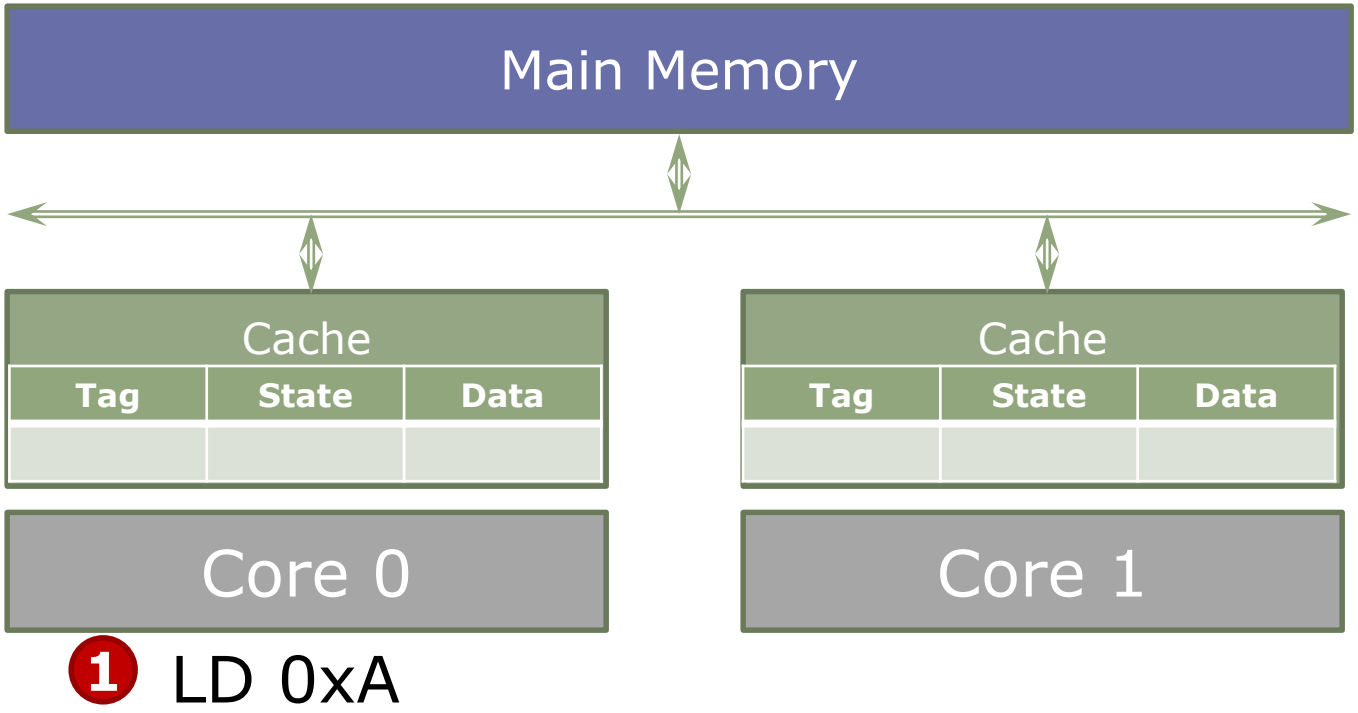
Bus-initiated transitions

Actions
Processor Read (PrRd)
Processor Write (PrWr)
Bus Read (BusRd)
Bus Read Exclusive (BusRdX)
Bus Writeback (BusWB)

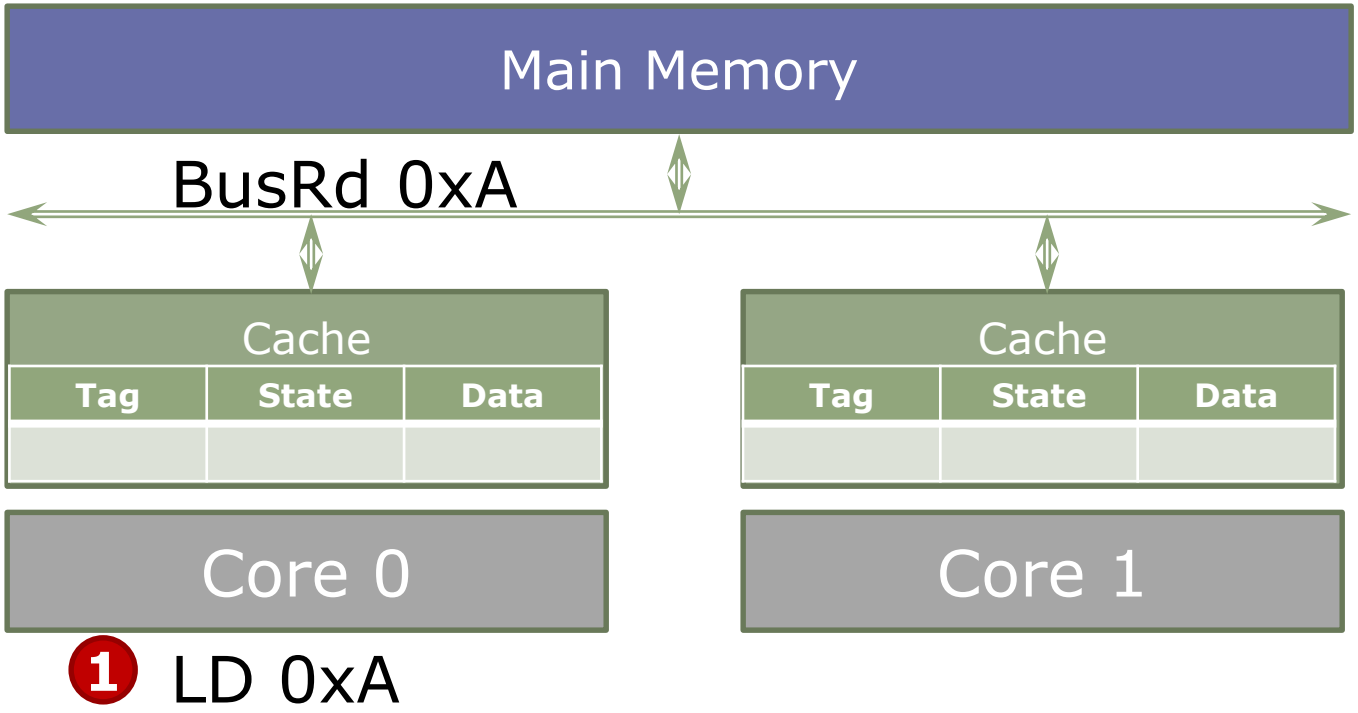
MSI Example


Main Memory
Cache
Tag
State
Data
Cache
Tag
State
Data
Core 0
Core 1

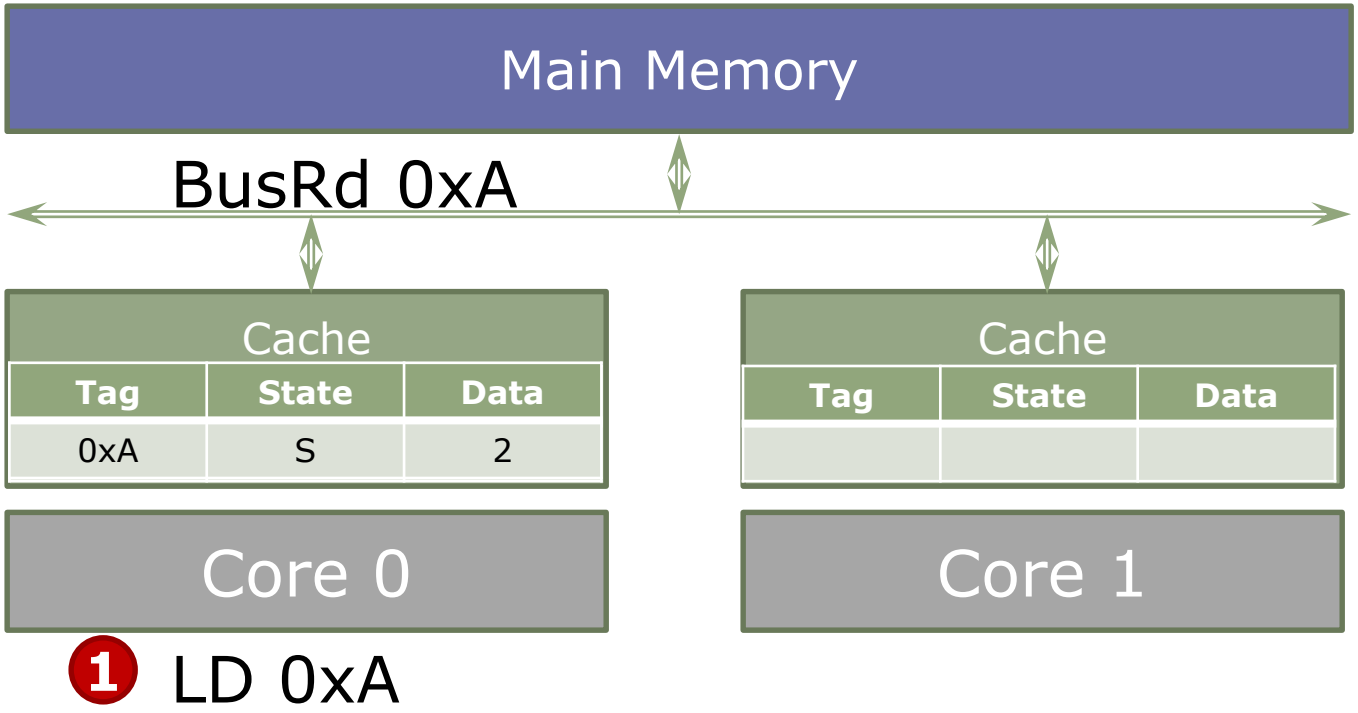
MSI Example


Main Memory
Cache
Tag
State
Data
Cache
Tag
State
Data
Core 0
Core 1
1
LD 0xA

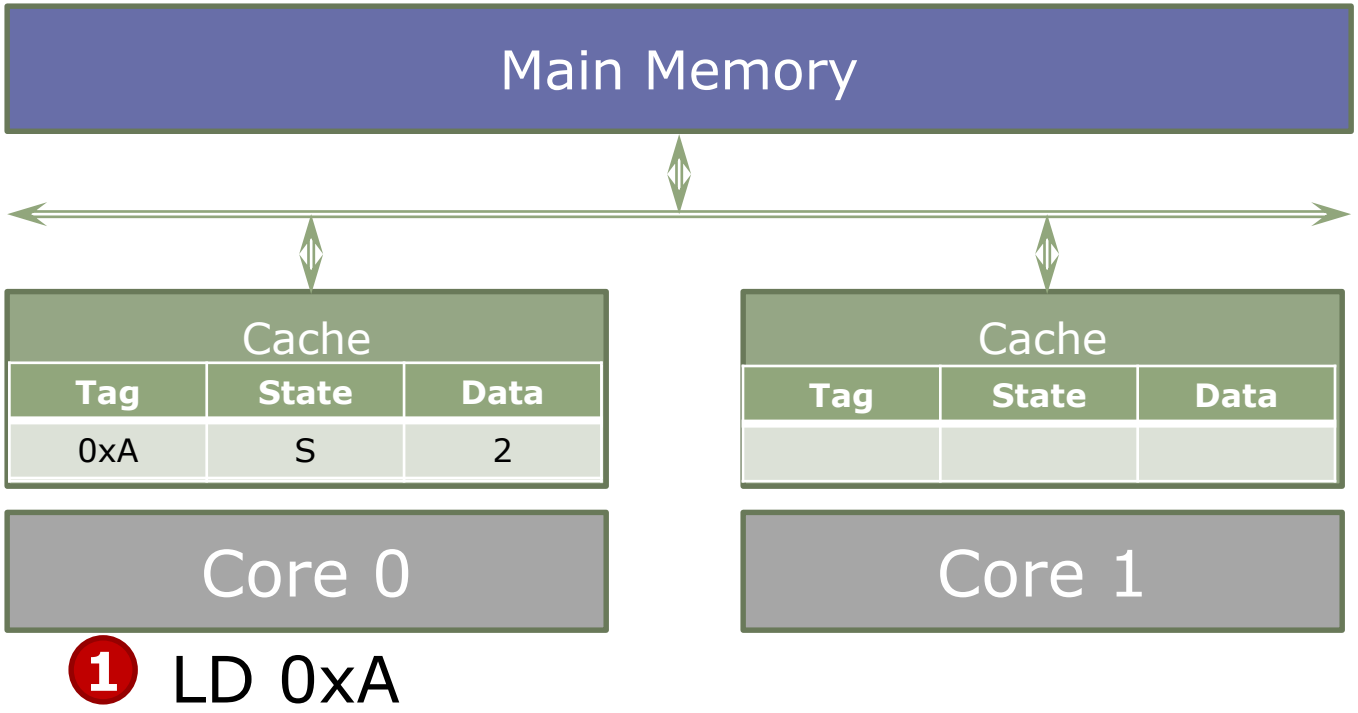
MSI Example


Main Memory
BusRd 0xA
Cache
Tag
State
Data
Cache
Tag
State
Data
Core 0
Core 1
1
LD 0xA

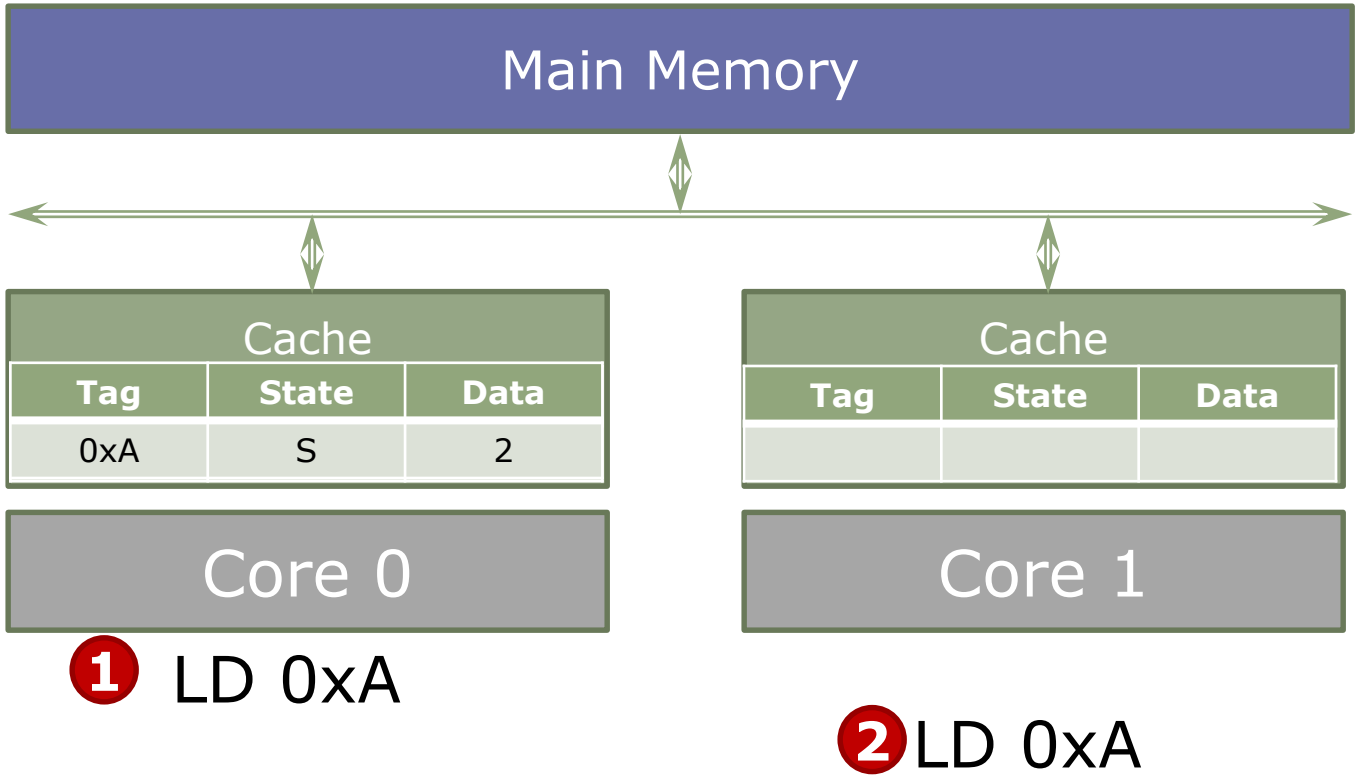
MSI Example


Main Memory
BusRd 0xA
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
Core 0
Core 1
1
LD 0xA

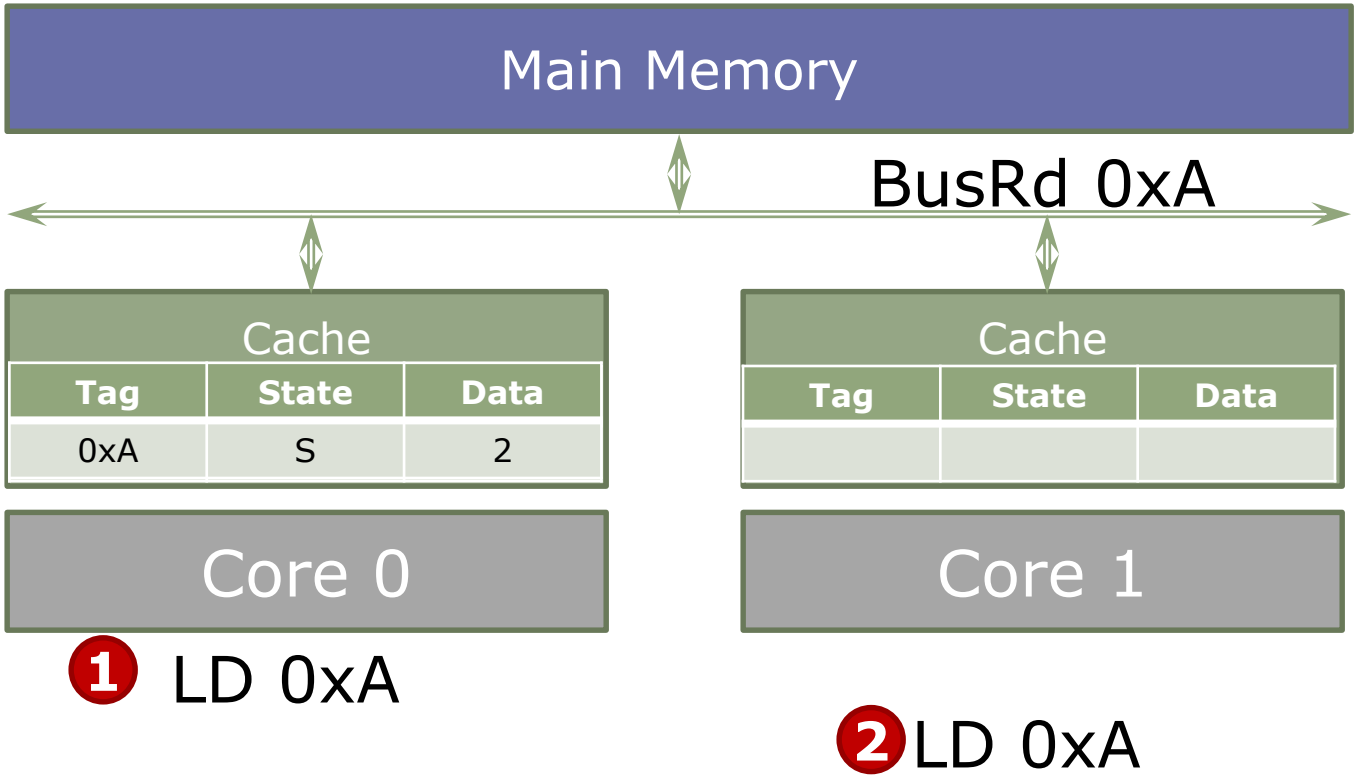
MSI Example


Main Memory
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
Core 0
Core 1
1
LD 0xA

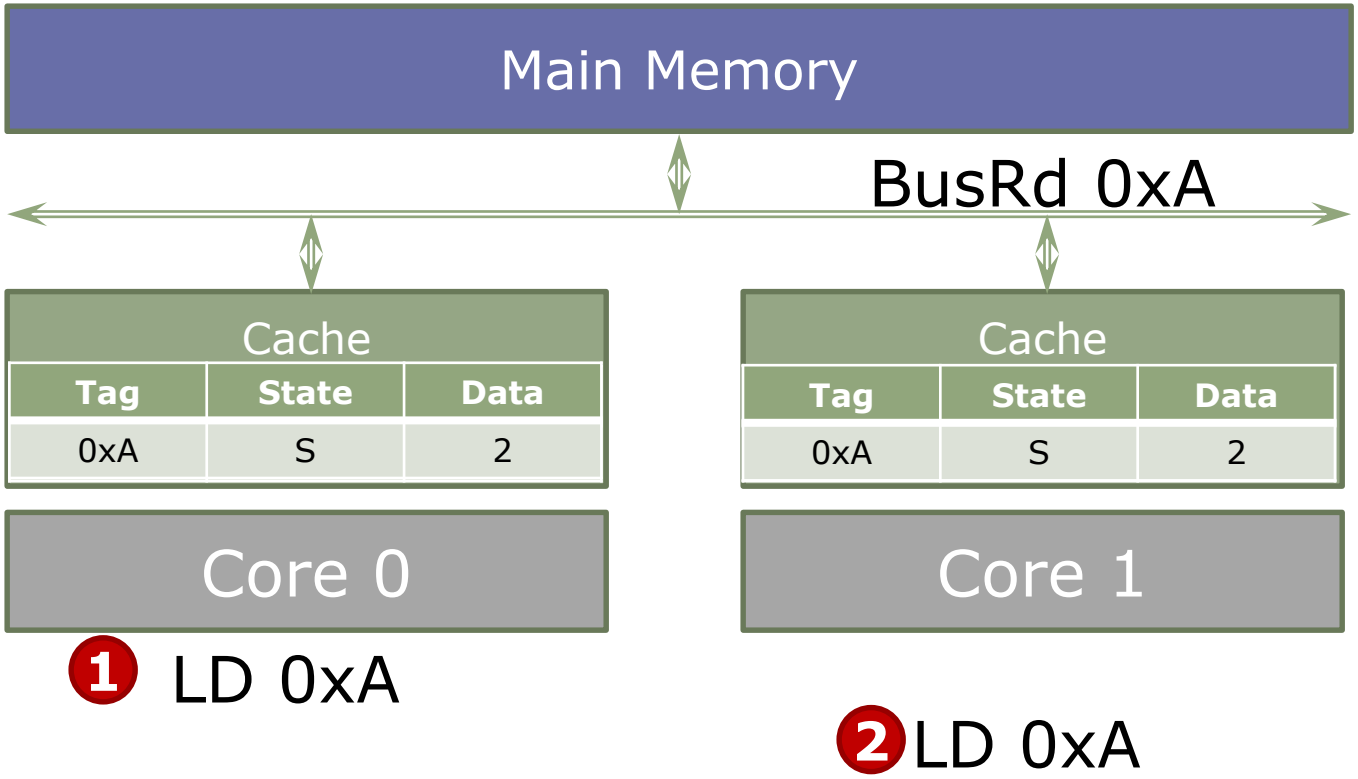
MSI Example


Main Memory
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
Core 0
Core 1
1
LD 0xA
2
LD 0xA

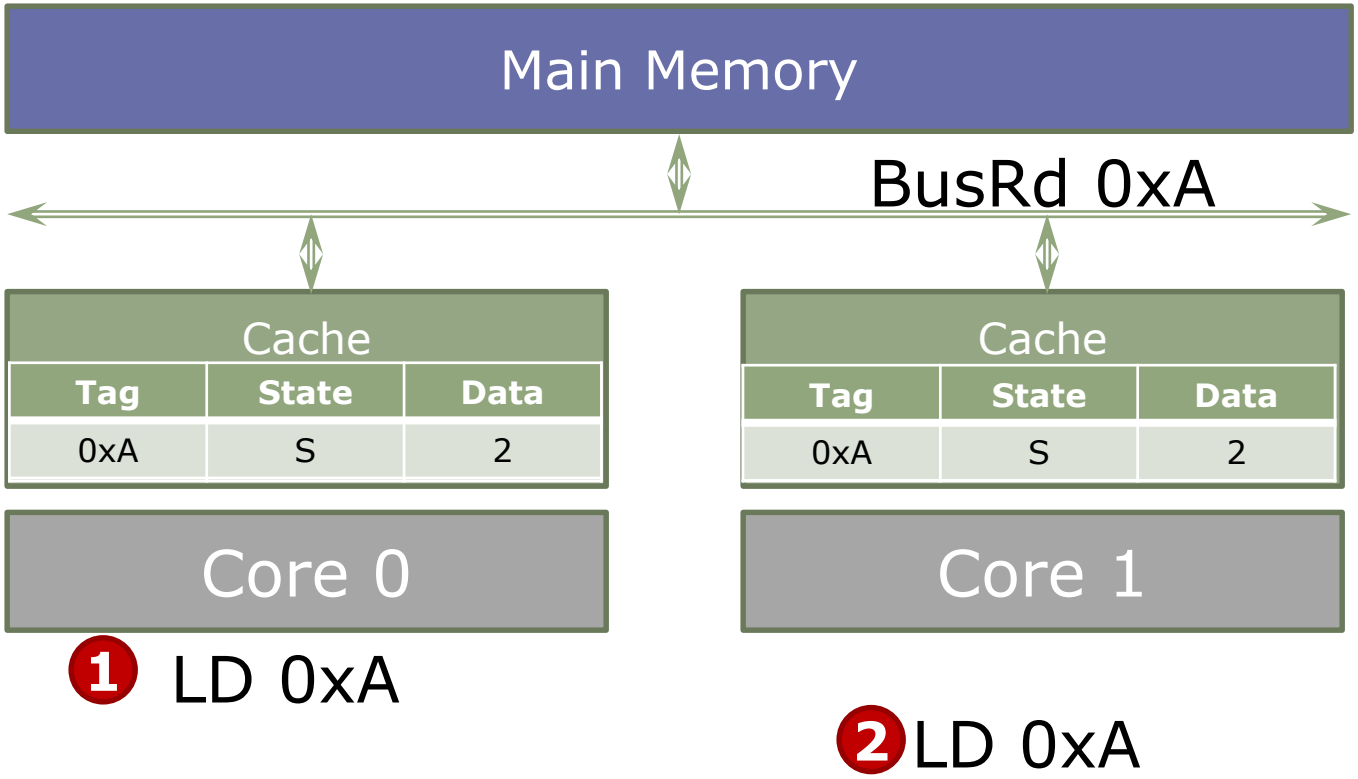
MSI Example


Main Memory
BusRd 0xA
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
Core 0
Core 1
1
LD 0xA
2
LD 0xA

MSI Example

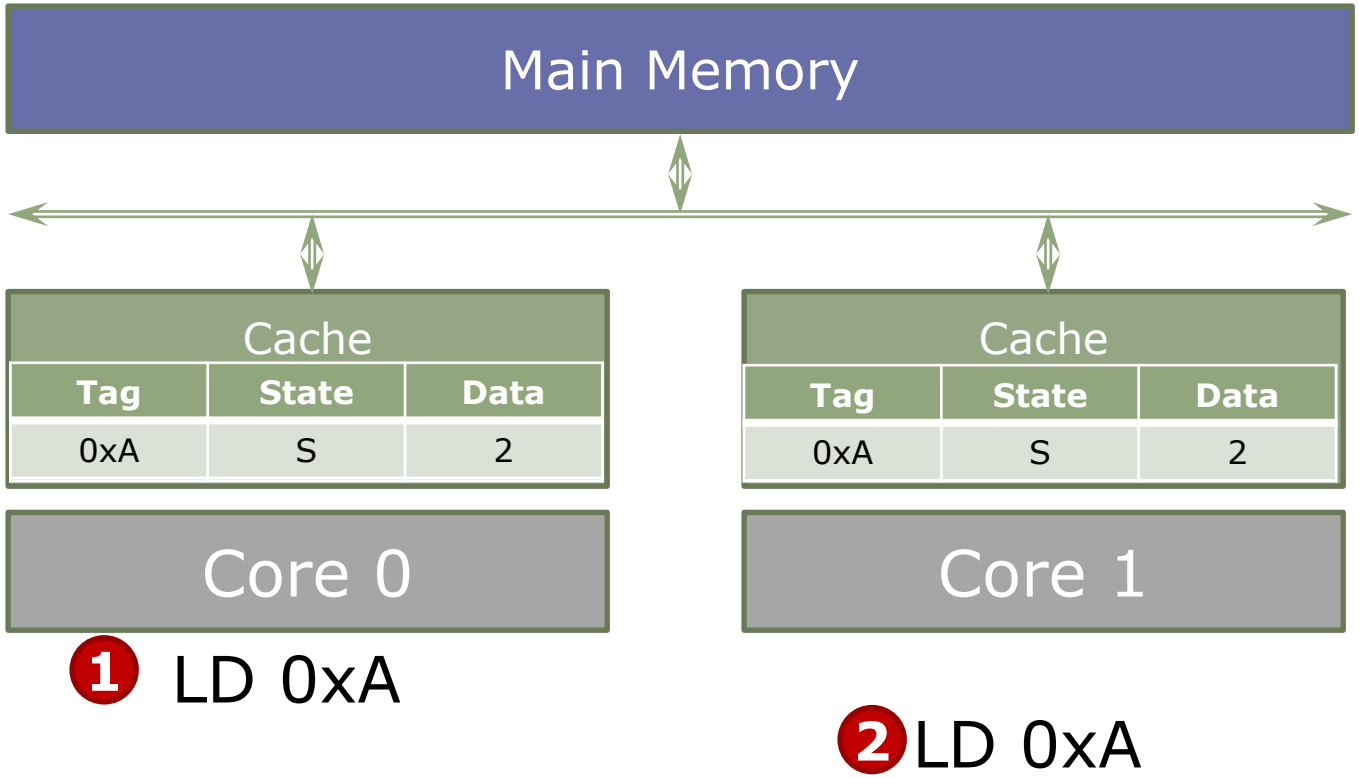

Main Memory
BusRd 0xA
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
0xA
S
2
Core 0
Core 1
1
LD 0xA
2
LD 0xA

MSI Example

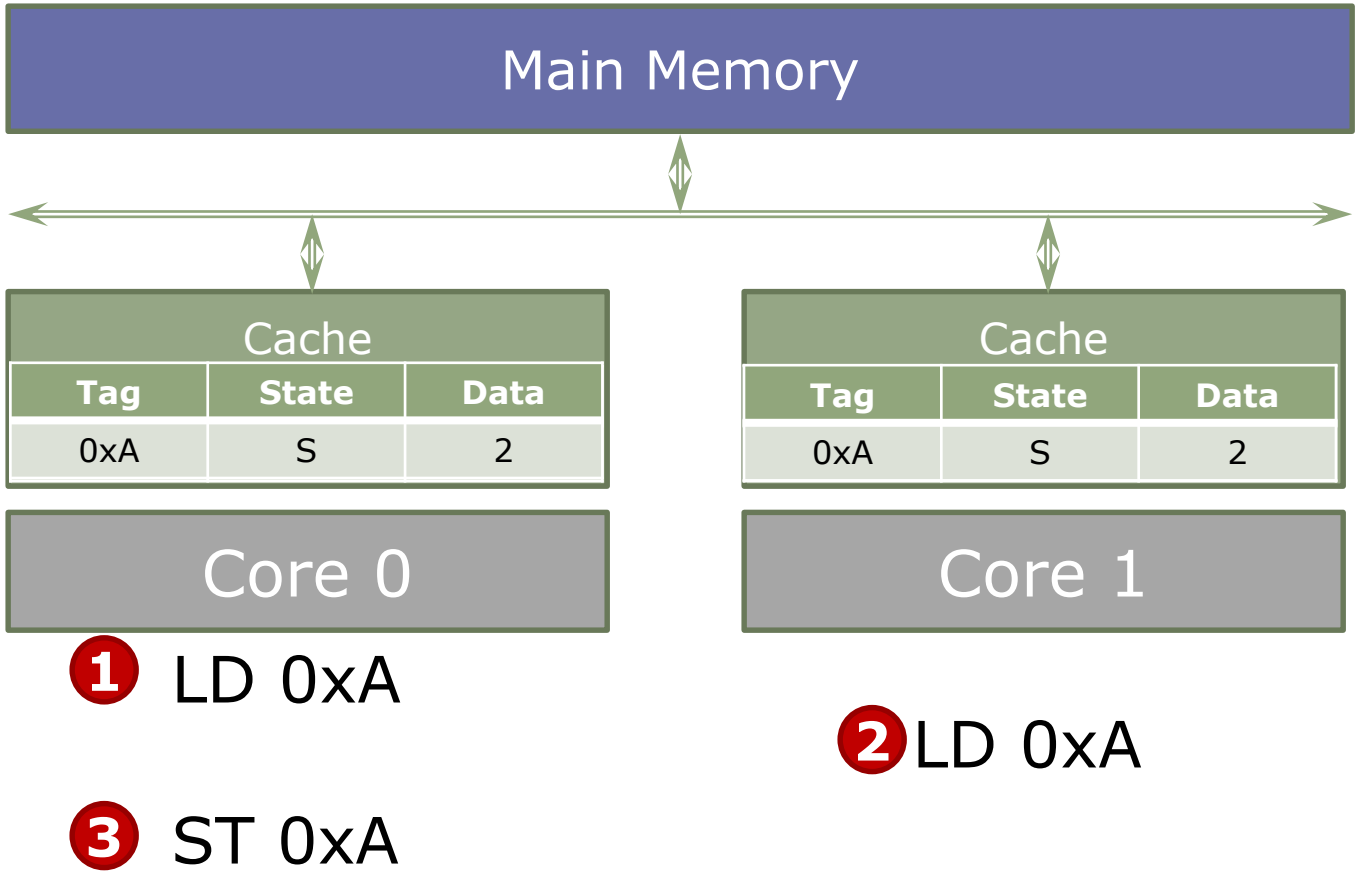


Additional loads satisfied locally, without BusRd (like in VI)

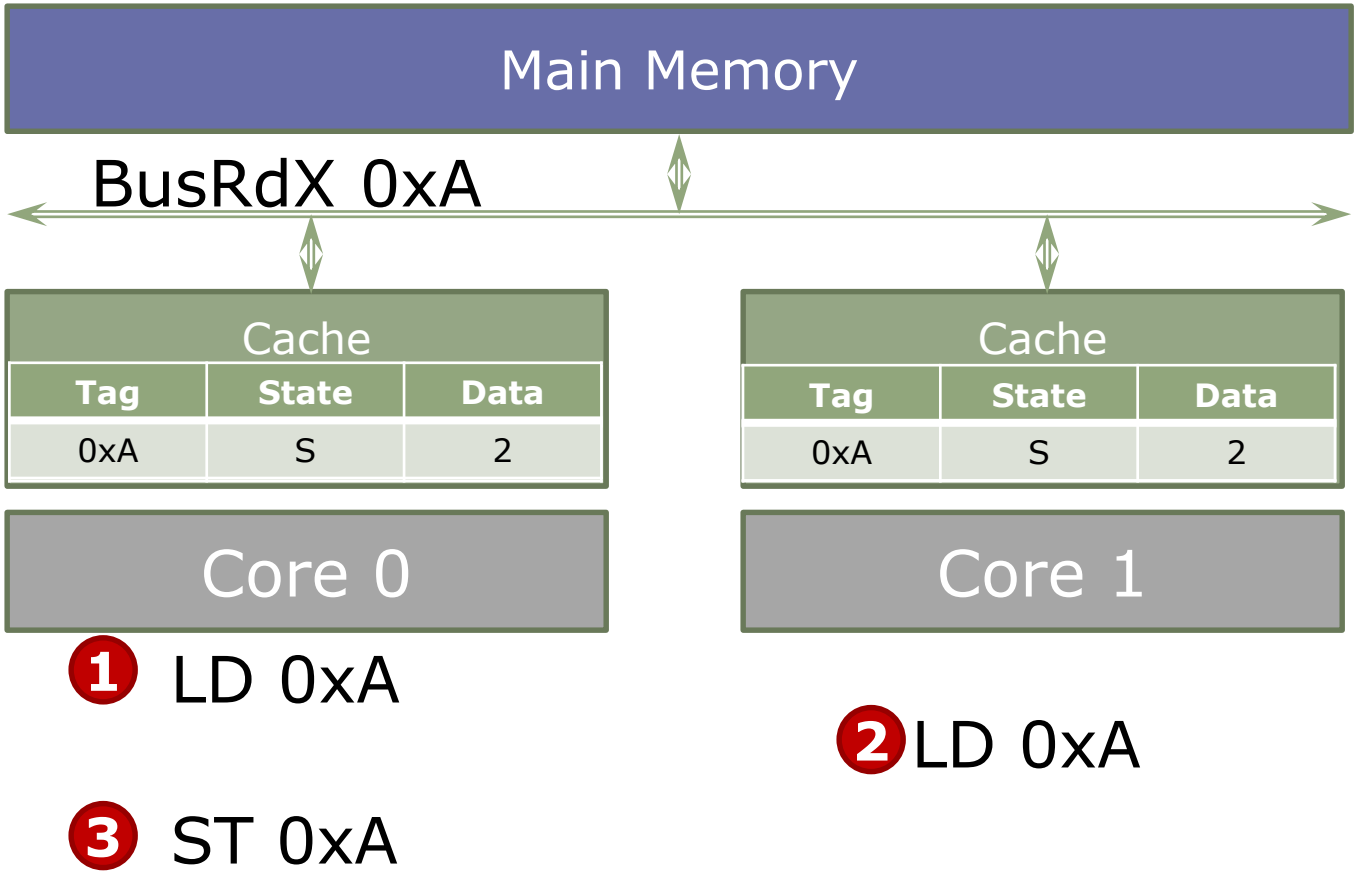
MSI Example


Main Memory
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
0xA
S
2
Core 0
Core 1
1
LD 0xA
2
LD 0xA

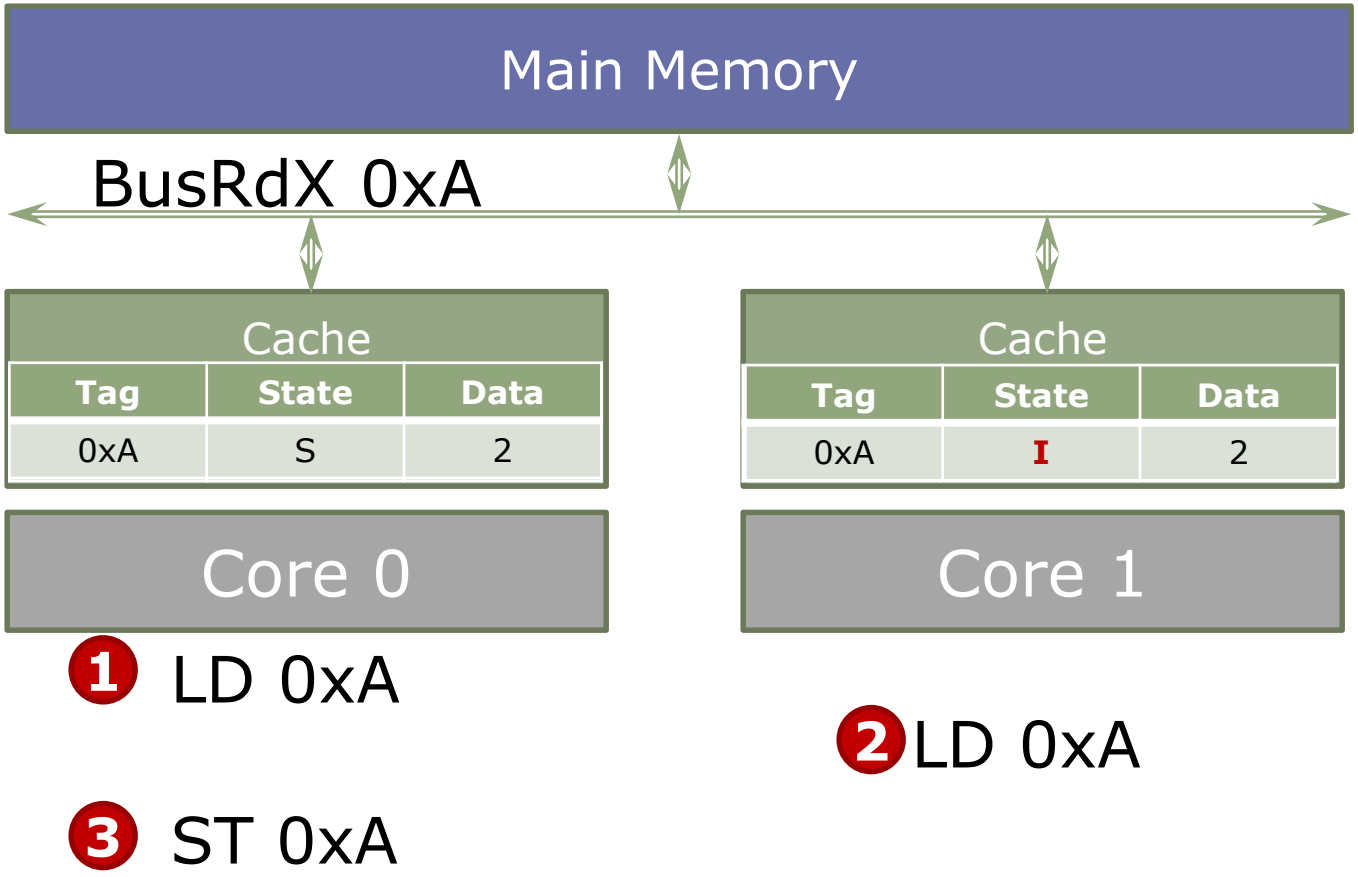
MSI Example


Main Memory
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
0xA
S
2
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA

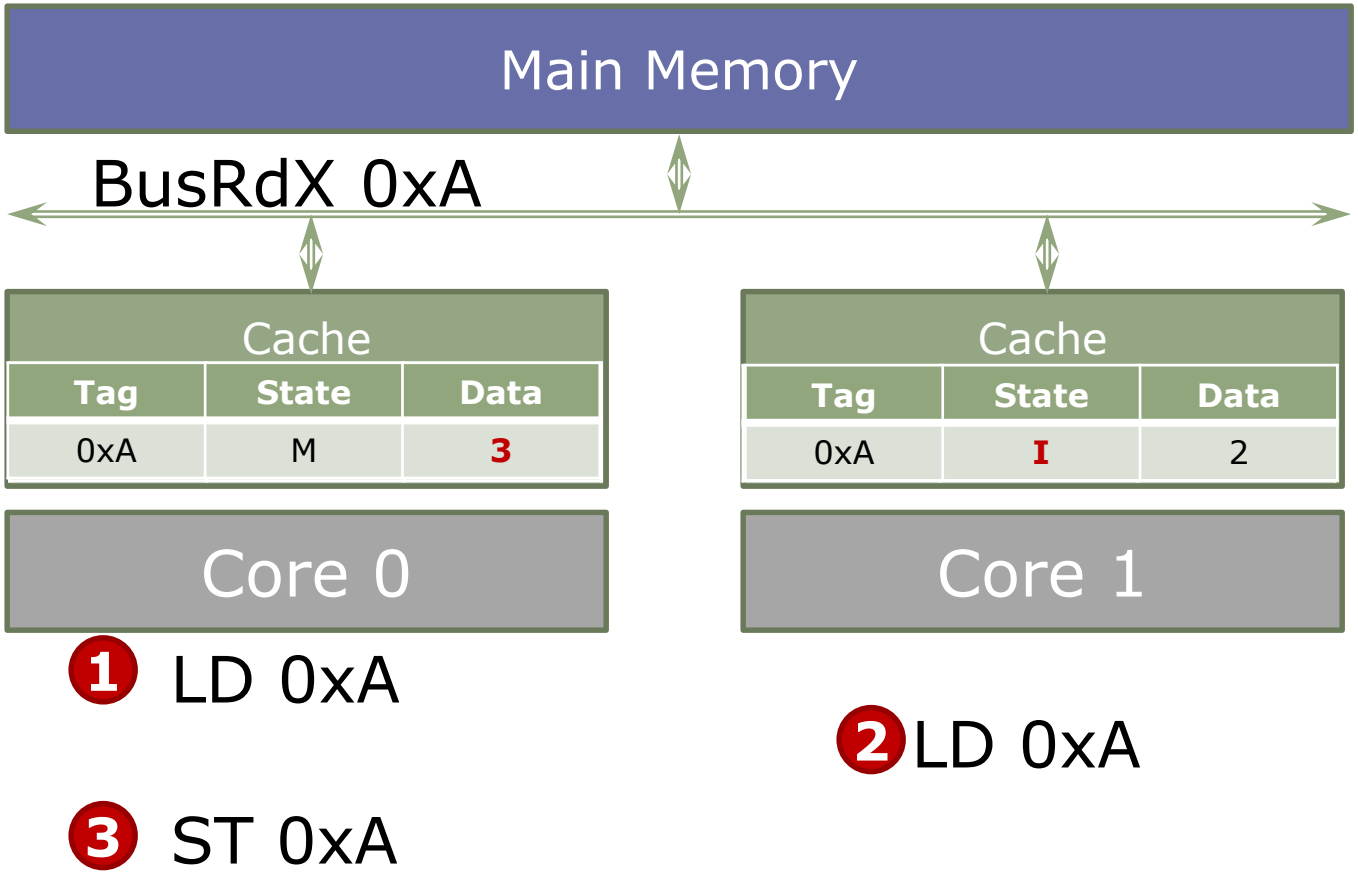
MSI Example


Main Memory
BusRdX 0xA
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
0xA
S
2
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA

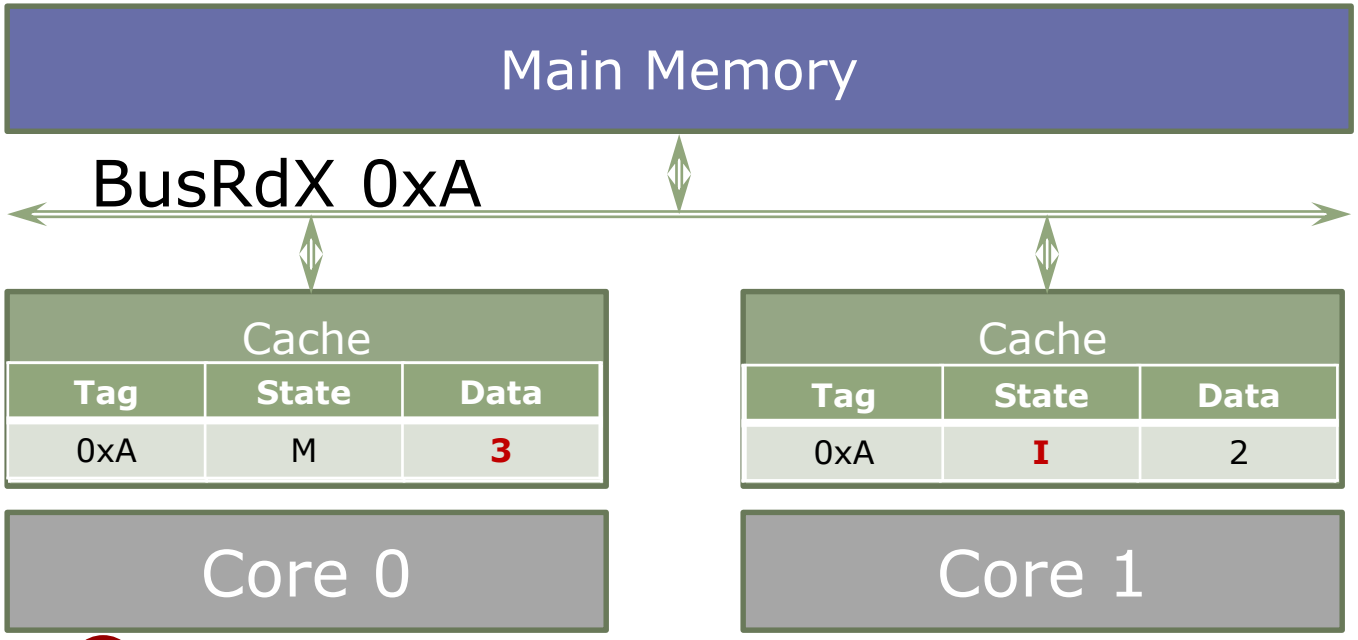
MSI Example


Main Memory
BusRdX 0xA
Cache
Tag
State
Data
0xA
S
2
Cache
Tag
State
Data
0xA
I
2
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA

MSI Example

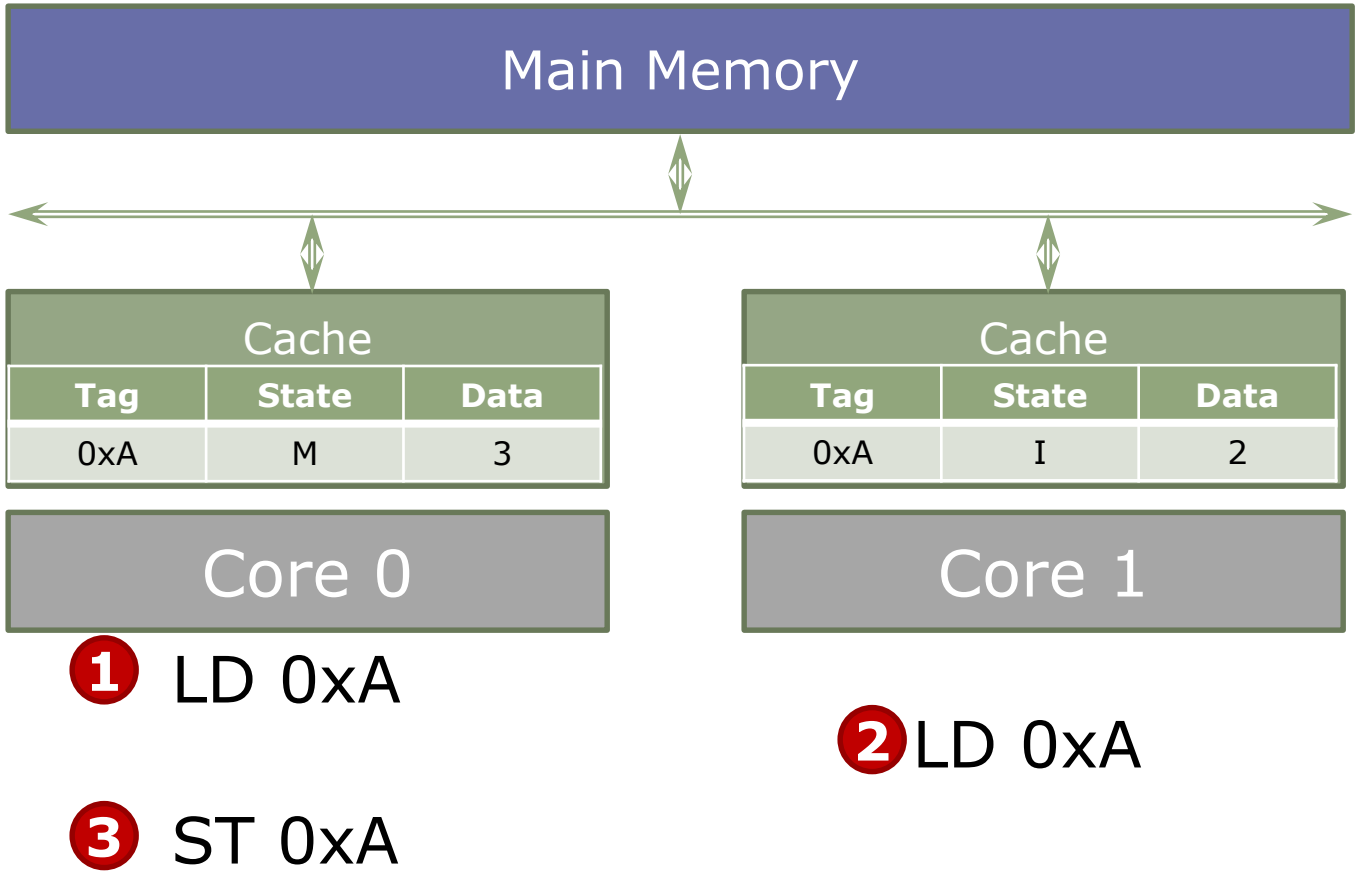

Main Memory
BusRdX 0xA
Cache
Tag
State
Data
0xA
M
3
Cache
Tag
State
Data
0xA
I
2
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA

MSI Example

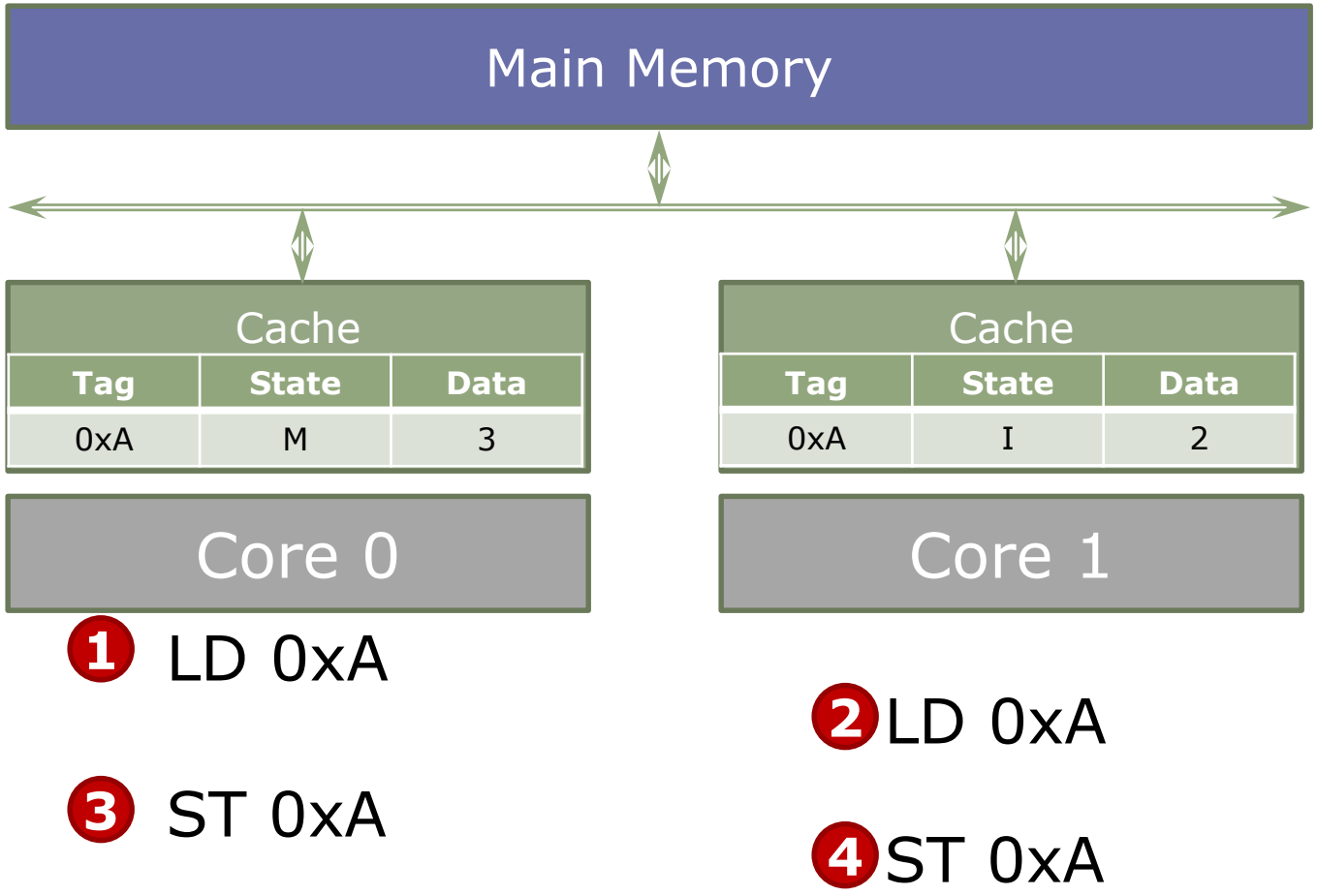


Additional loads *and stores* from core 0 satisfied locally, without bus transactions (unlike in VI)

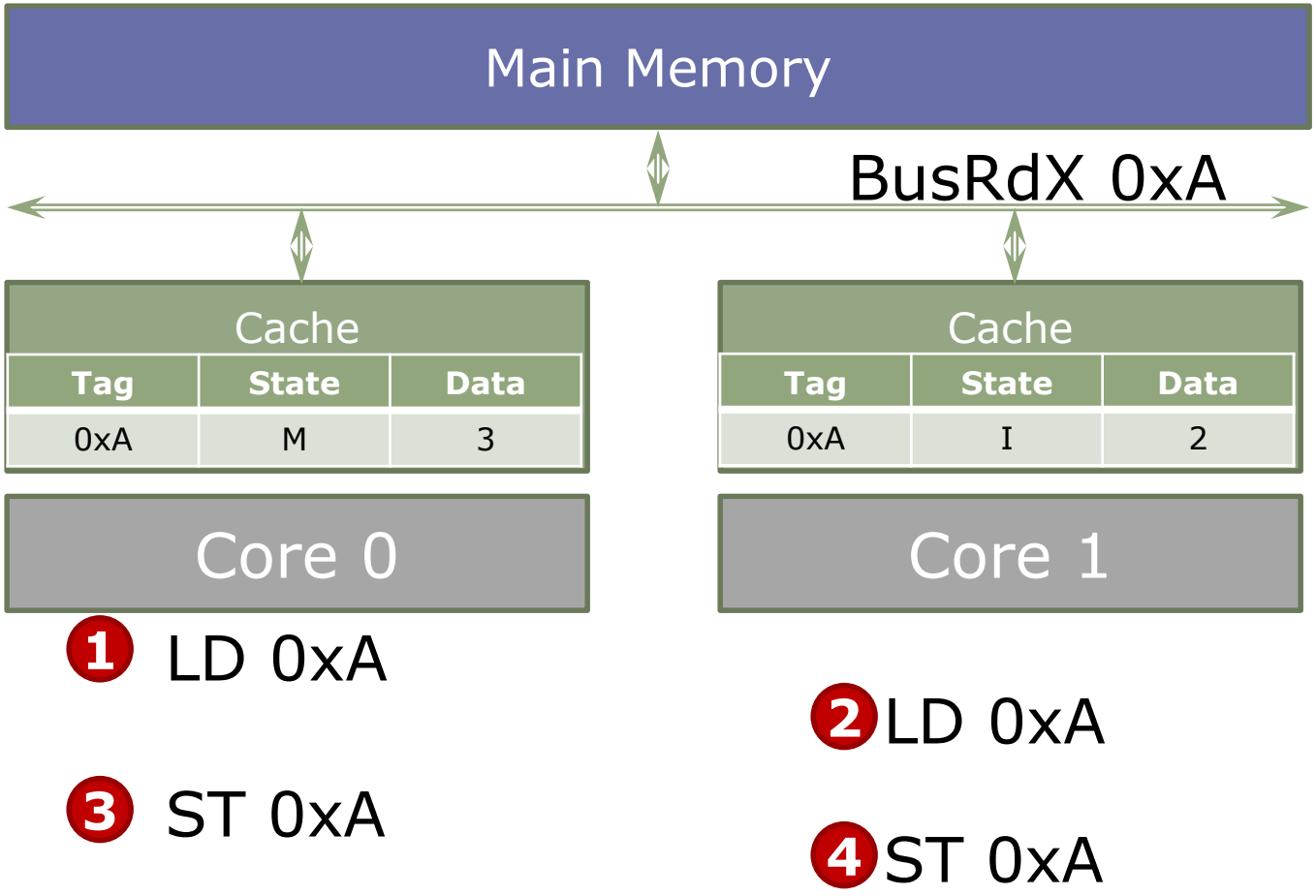
MSI Example


Main Memory
Cache
Tag
State
Data
0xA
M
3
Cache
Tag
State
Data
0xA
I
2
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA

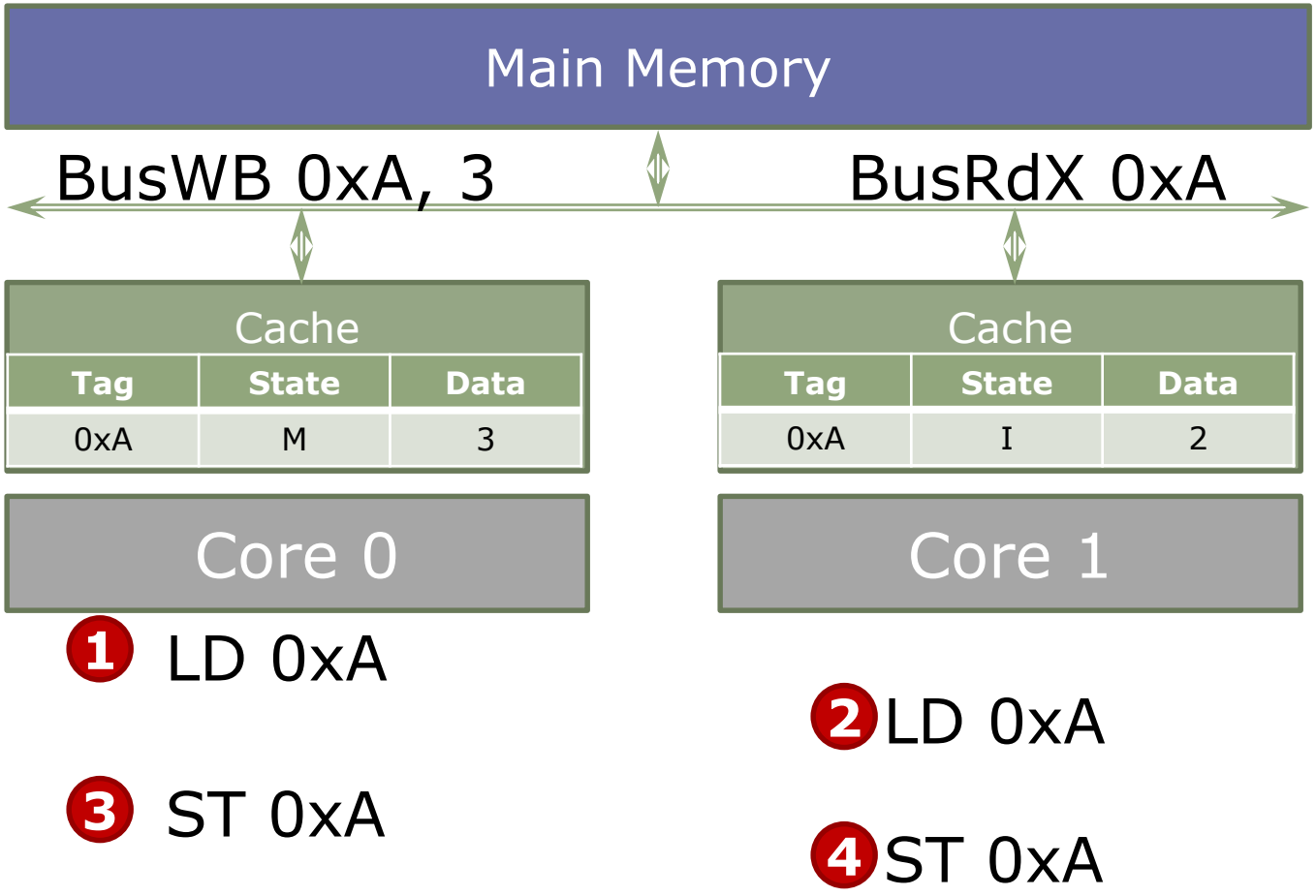
MSI Example


Main Memory
Cache
Tag
State
Data
0xA
M
3
Cache
Tag
State
Data
0xA
I
2
Core 0
Core 1
1 LD 0xA
3 ST 0xA
2 LD 0xA
4 ST 0xA

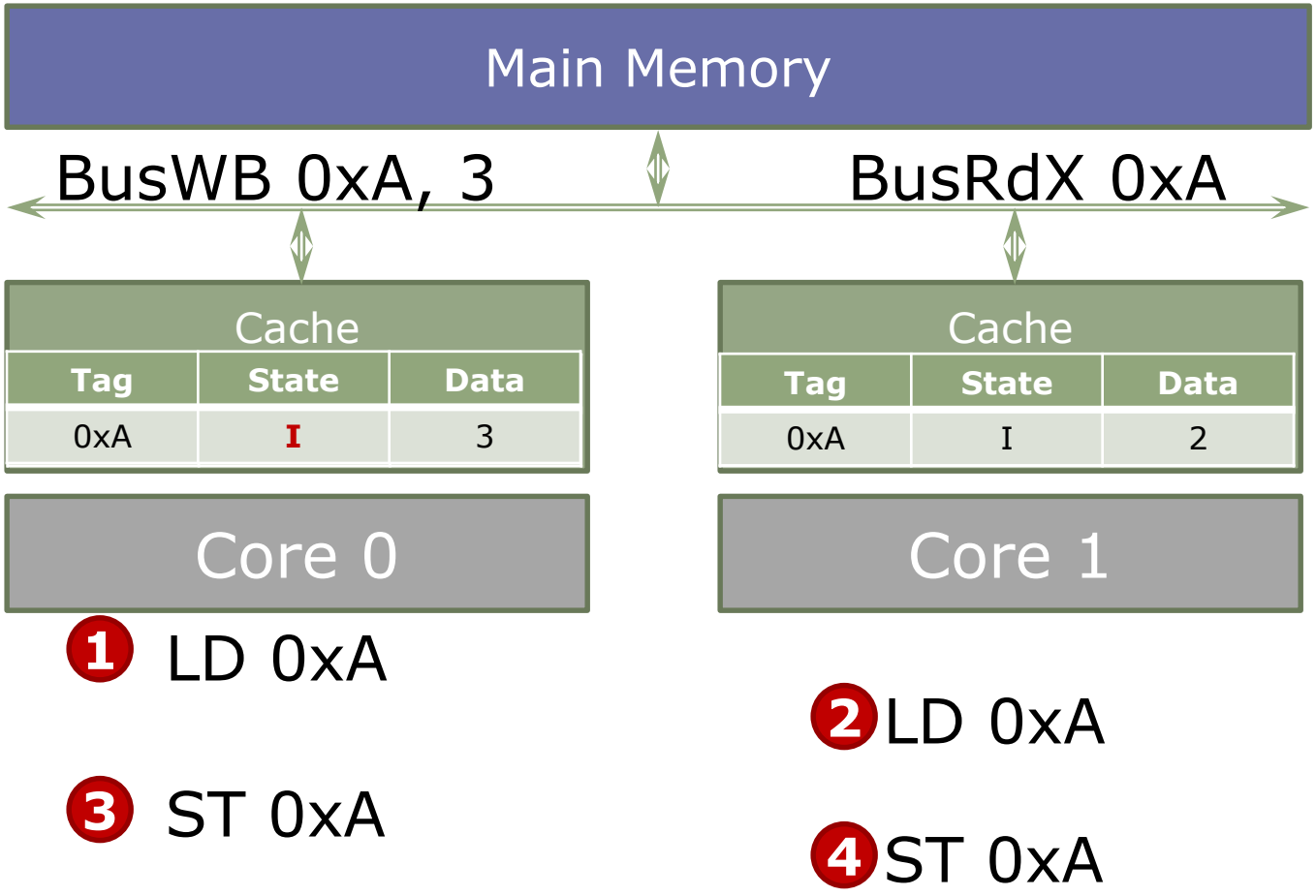
MSI Example


Main Memory
BusRdX 0xA
Cache
Tag
State
Data
0xA
M
3
Cache
Tag
State
Data
0xA
I
2
Core 0
Core 1
1 LD 0xA
3 ST 0xA
2 LD 0xA
4 ST 0xA

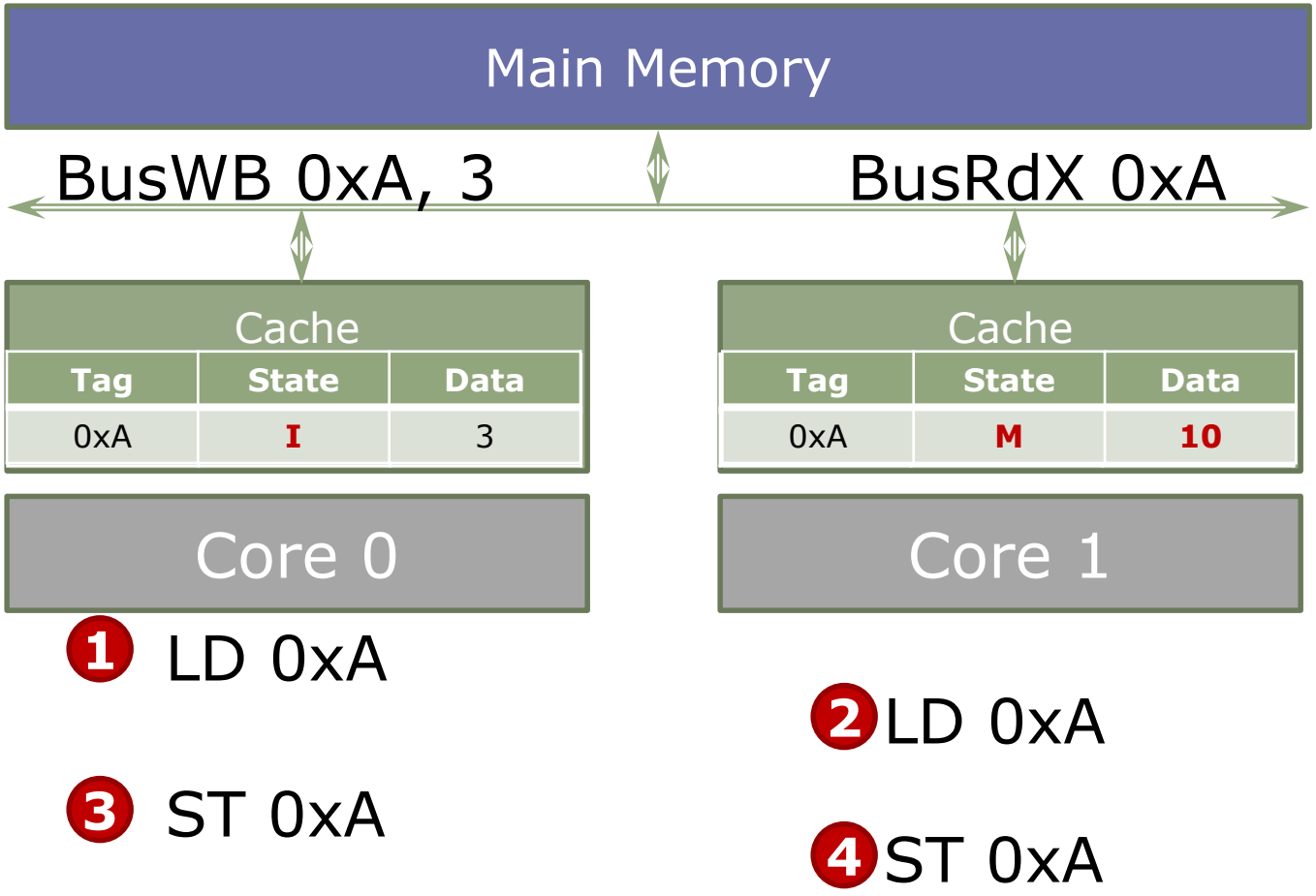
MSI Example


Main Memory
BusWB 0xA, 3
BusRdX 0xA
Cache
Tag
State
Data
0xA
M
3
Cache
Tag
State
Data
0xA
I
2
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA
4 ST 0xA

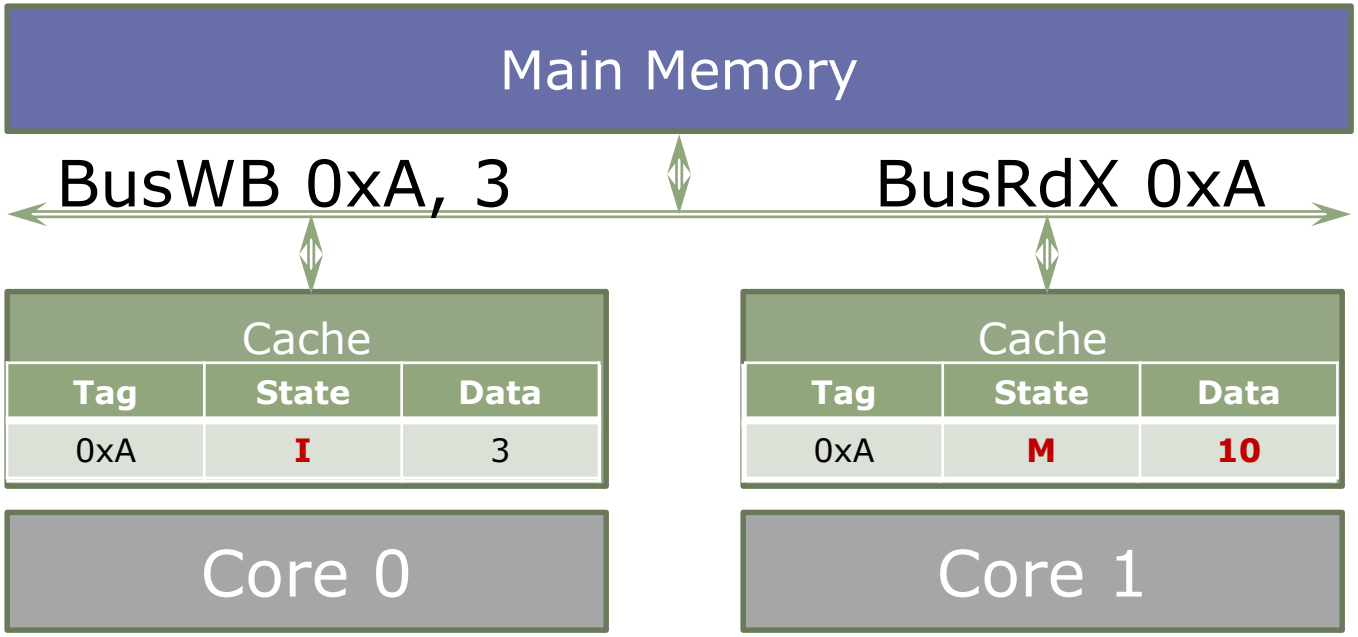
MSI Example


Main Memory
BusWB 0xA, 3
BusRdX 0xA
Cache
Tag
State
Data
0xA
I
3
Cache
Tag
State
Data
0xA
I
2
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA
4 ST 0xA

MSI Example

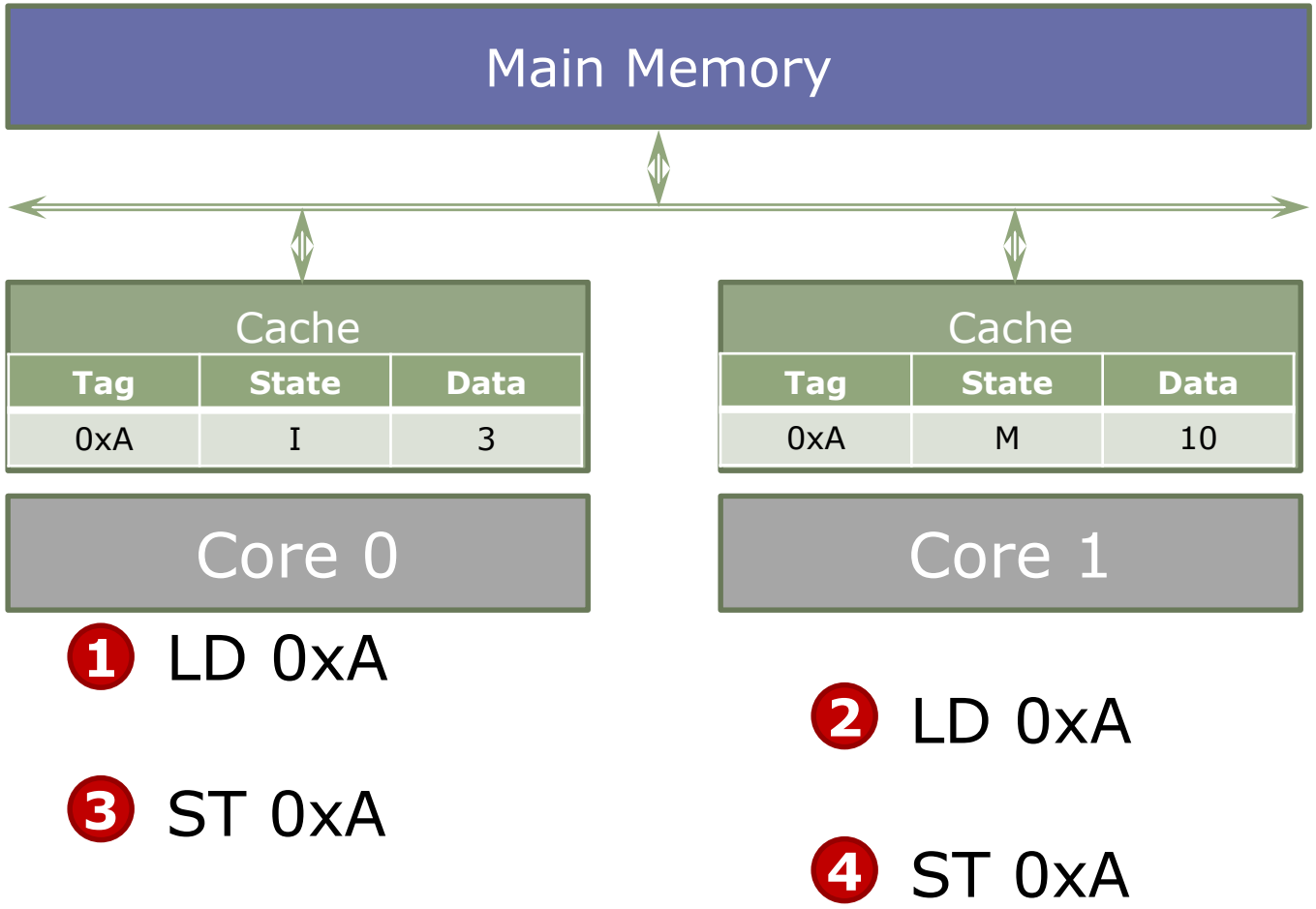

Main Memory
BusWB 0xA, 3
BusRdX 0xA
Cache
Tag
State
Data
0xA
I
3
Cache
Tag
State
Data
0xA
M
10
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA
4 ST 0xA

Cache interventions

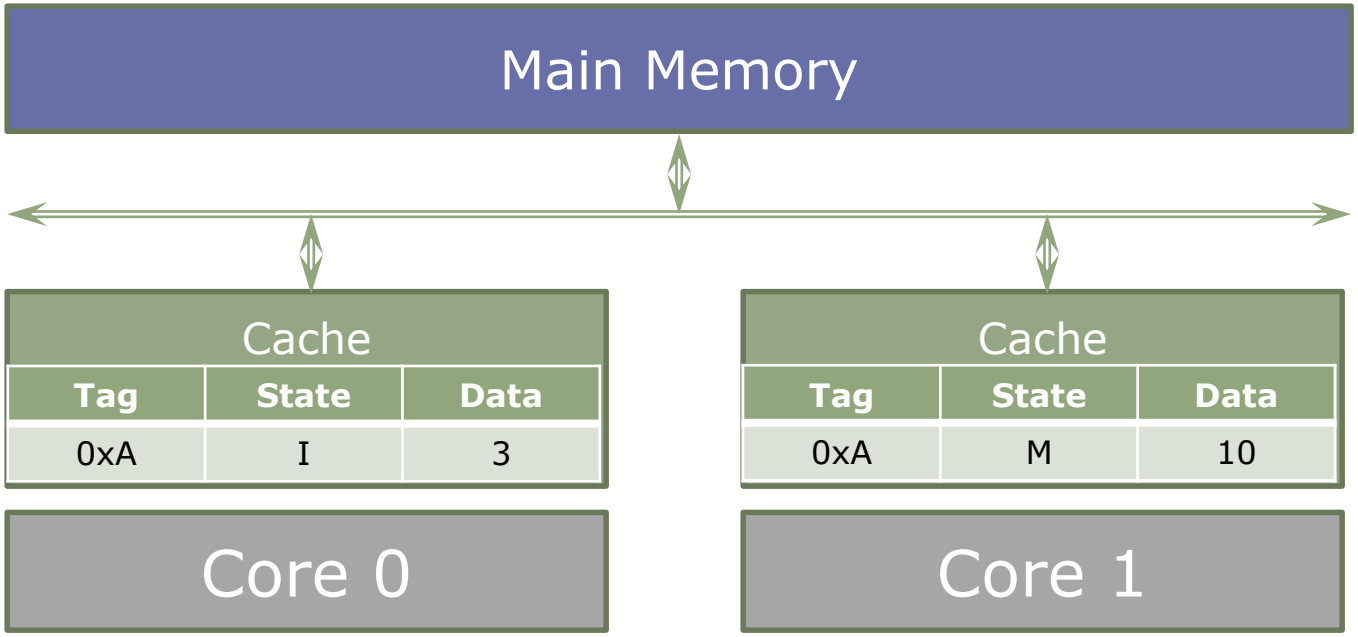


- MSI allows caches to serve writes without updating memory, so main memory can have stale data
  - Core 0's cache needs to supply data
  - But main memory may also respond!
- Cache must override response from main memory

MSI Example

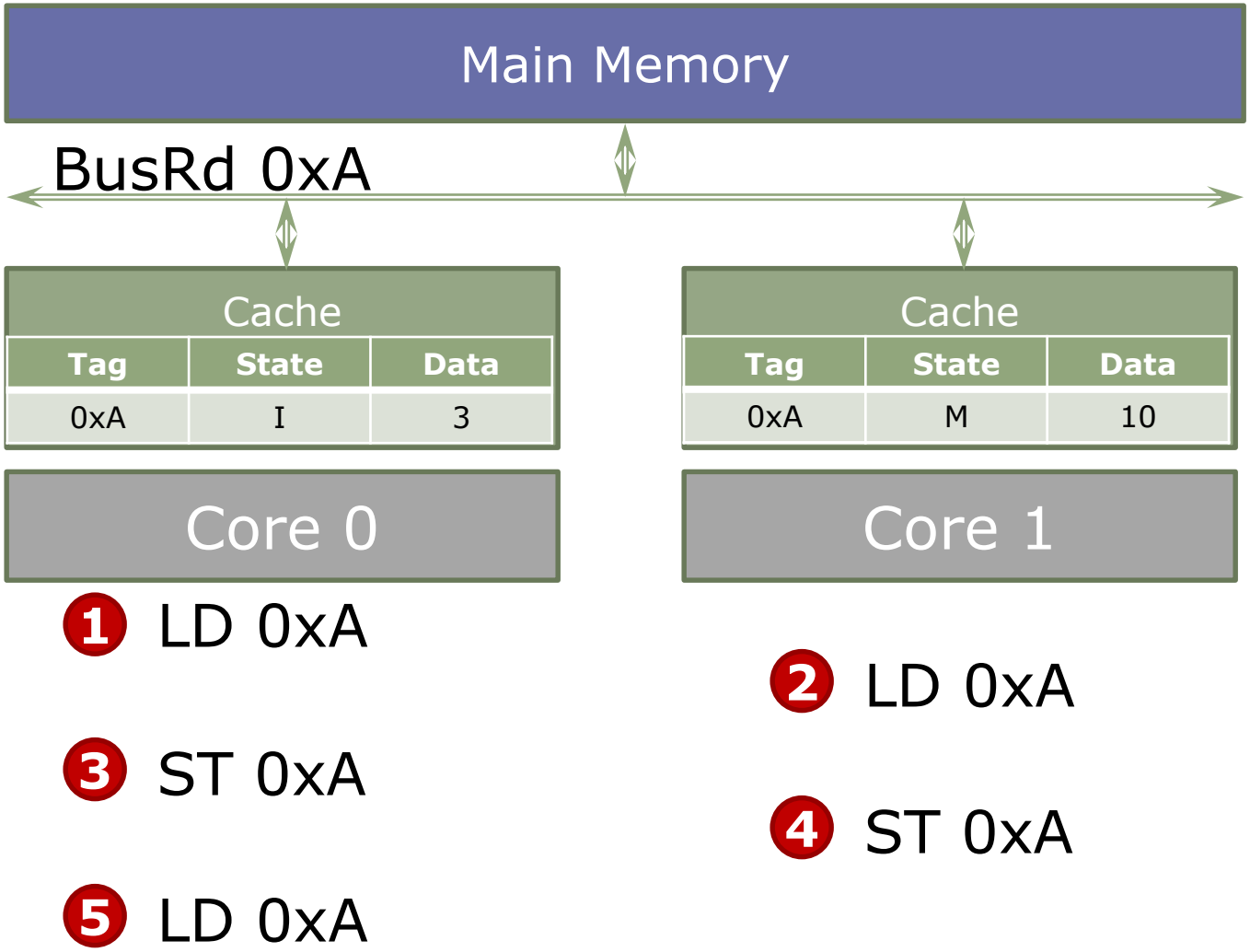

Main Memory
Cache
Tag
State
Data
0xA
I
3
Cache
Tag
State
Data
0xA
M
10
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA
4 ST 0xA

MSI Example

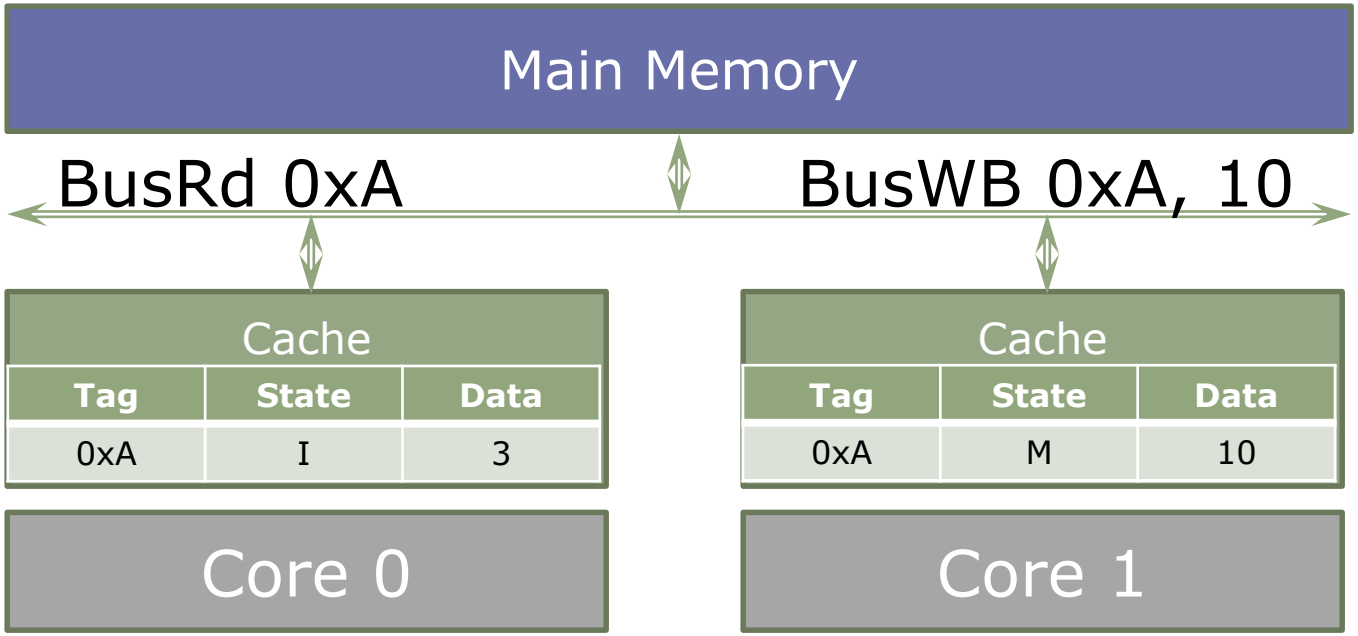


1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA

MSI Example

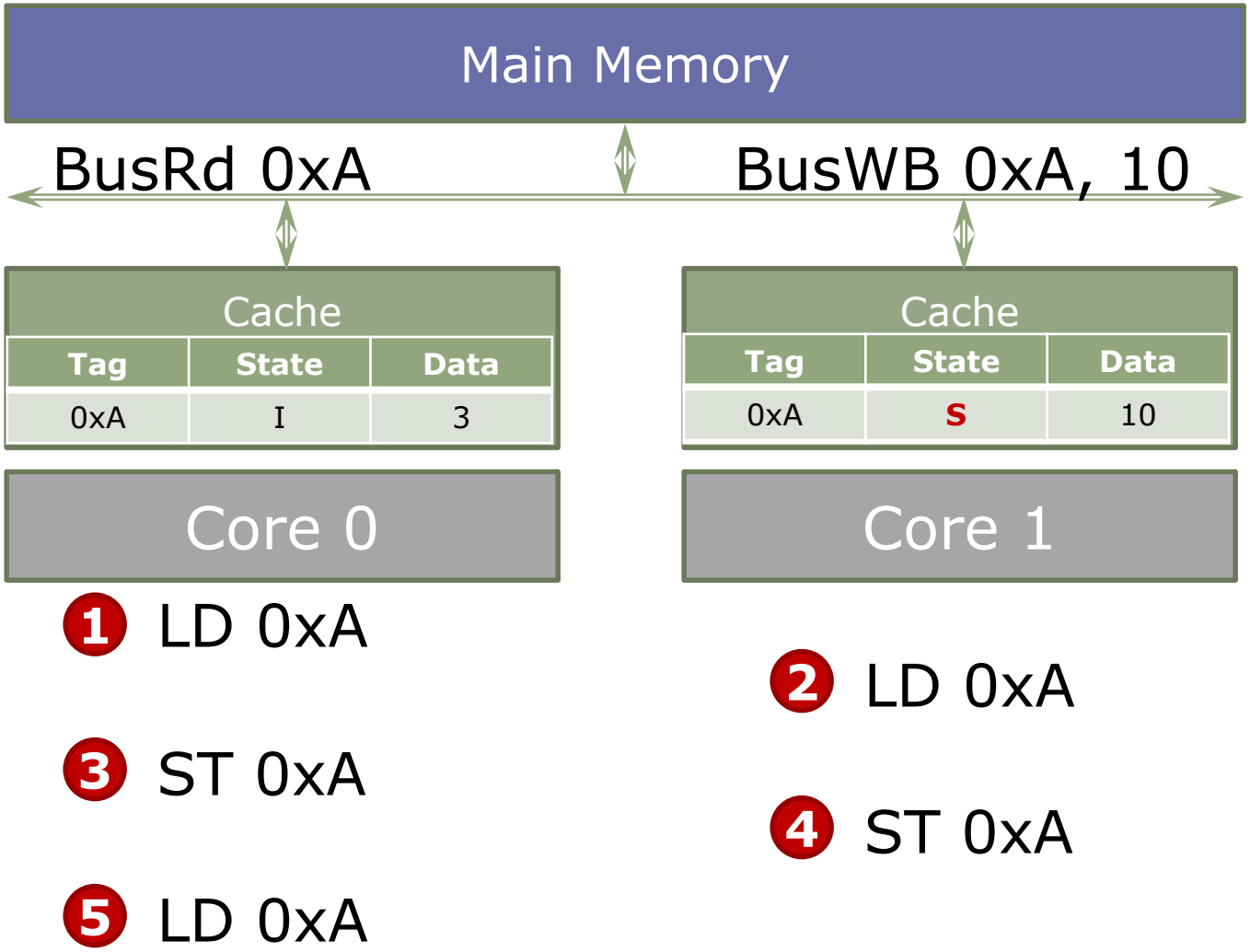

Main Memory
BusRd 0xA
Cache
Tag
State
Data
0xA
I
3
Cache
Tag
State
Data
0xA
M
10
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA
4 ST 0xA
5 LD 0xA

MSI Example



1. LD 0xA
2. LD 0xA
3. ST 0xA
4. ST 0xA
5. LD 0xA

MSI Example


Main Memory
BusRd 0xA
BusWB 0xA, 10
Cache
Tag
State
Data
0xA
I
3
Cache
Tag
State
Data
0xA
S
10
Core 0
Core 1
1 LD 0xA
2 LD 0xA
3 ST 0xA
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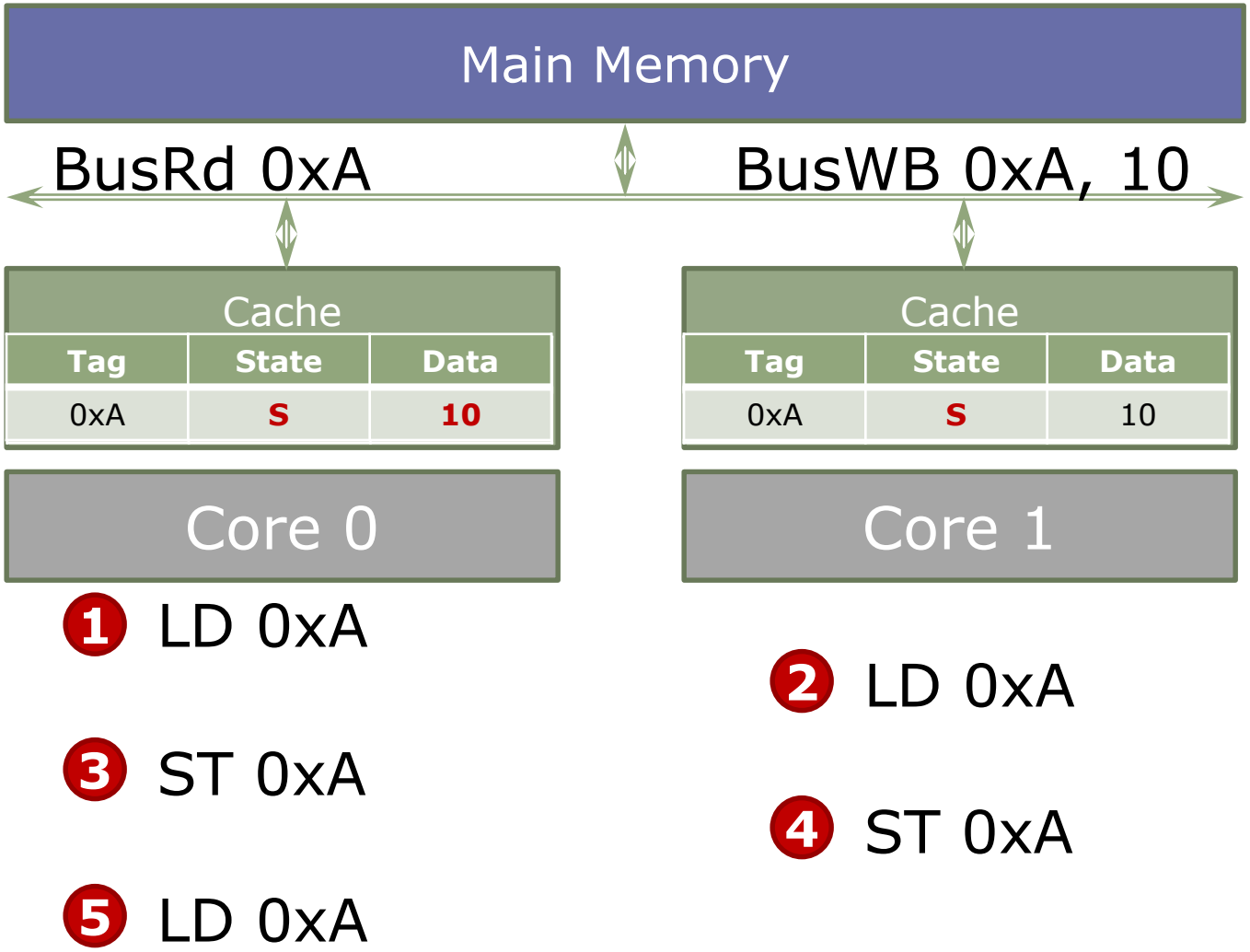
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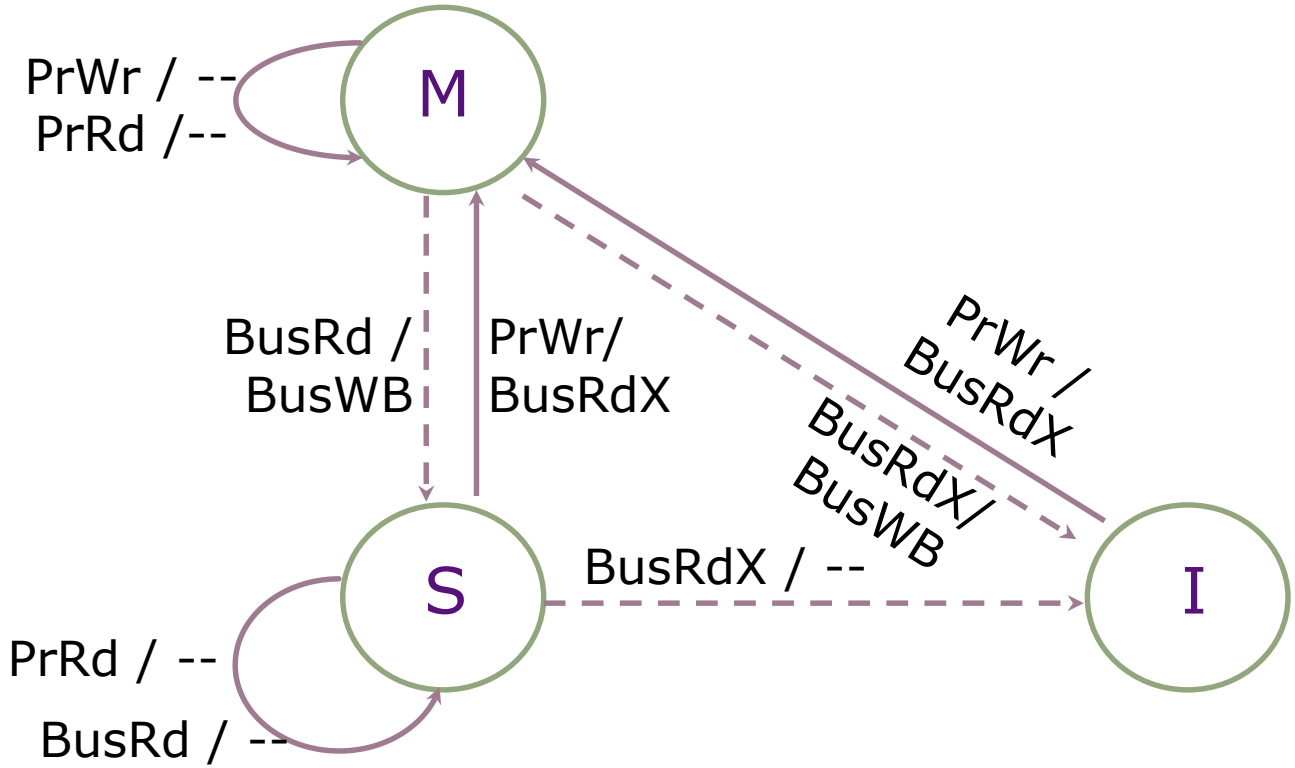
  - What's the problem with MSI?

- Solution: E state (exclusive, clean)
  - If no other sharers, a read acquires line in E instead of S
  - Writes silently cause E→M (exclusive, dirty)

MESI: An Enhanced MSI protocol
increased performance for private read-write data

M: Modified Exclusive
E: Exclusive, unmodified
S: Shared
I: Invalid



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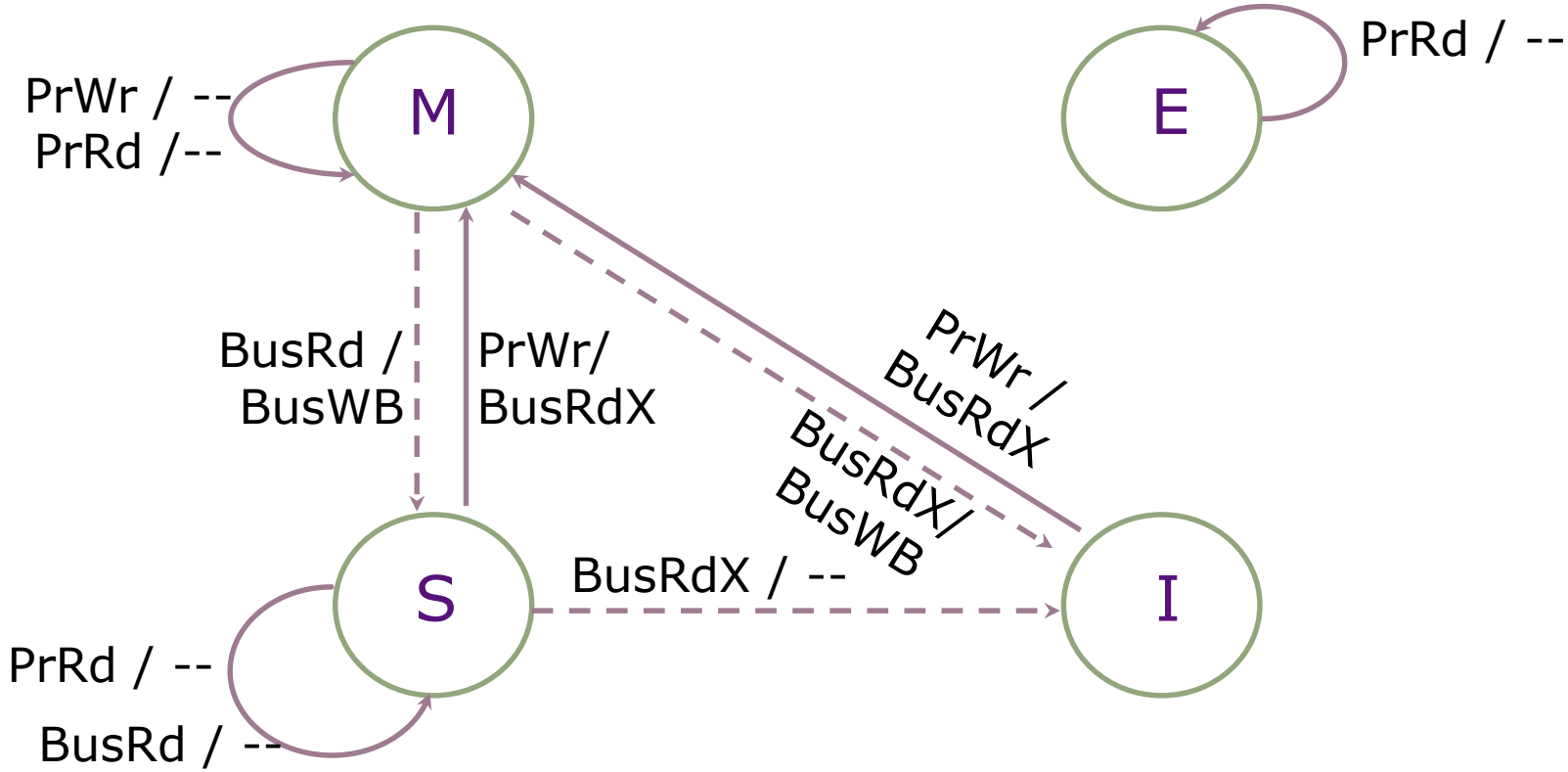

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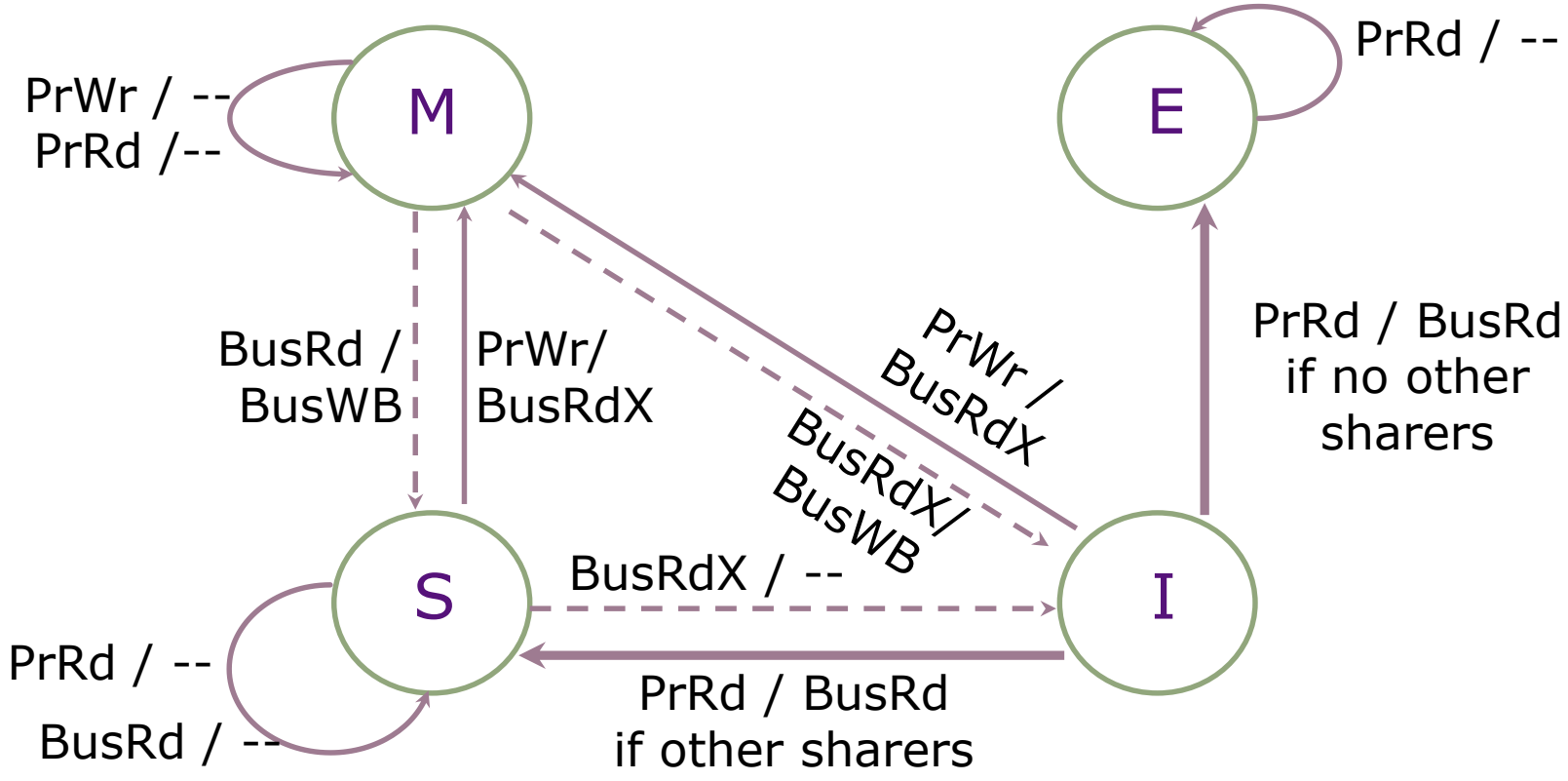

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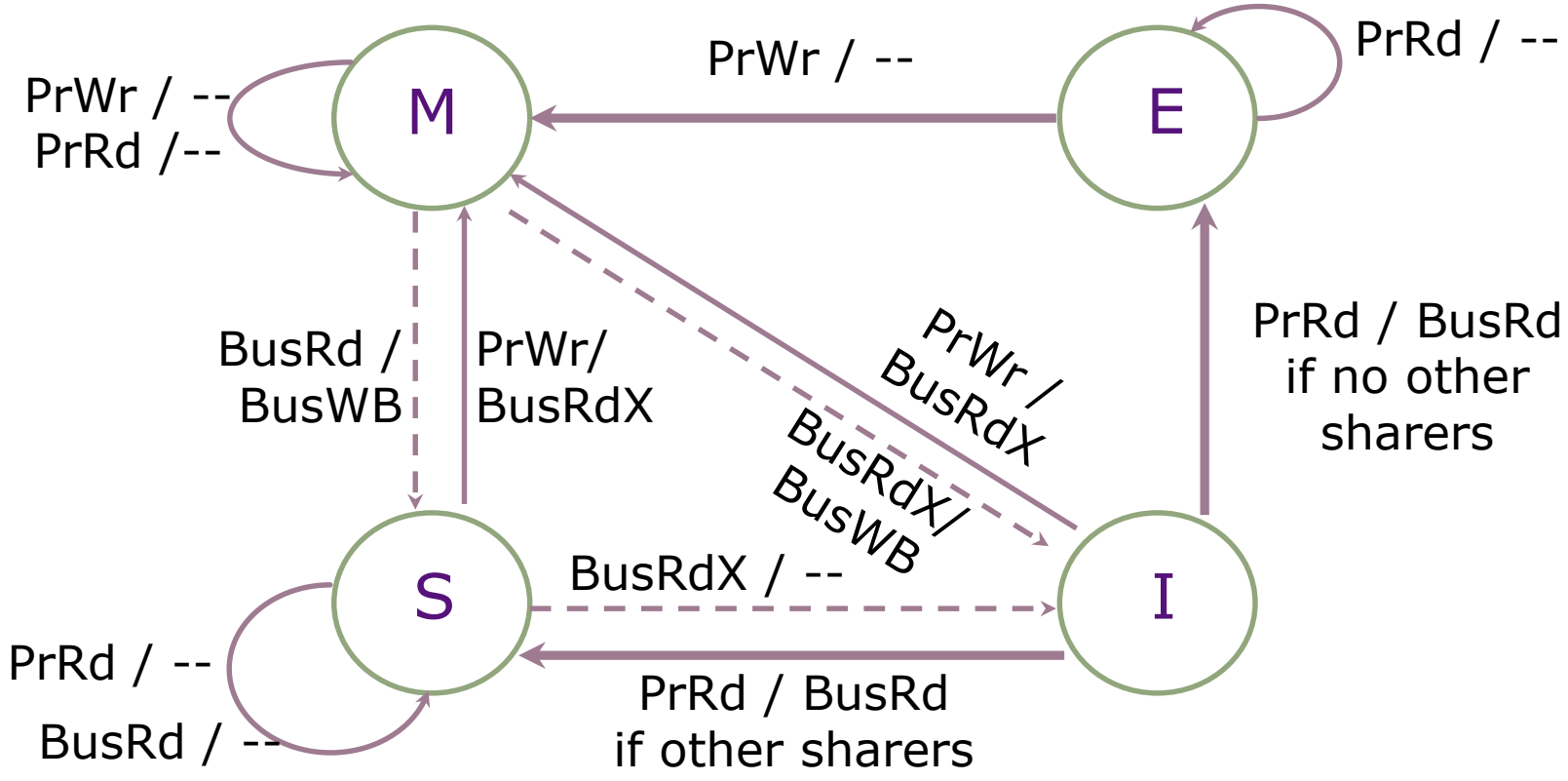

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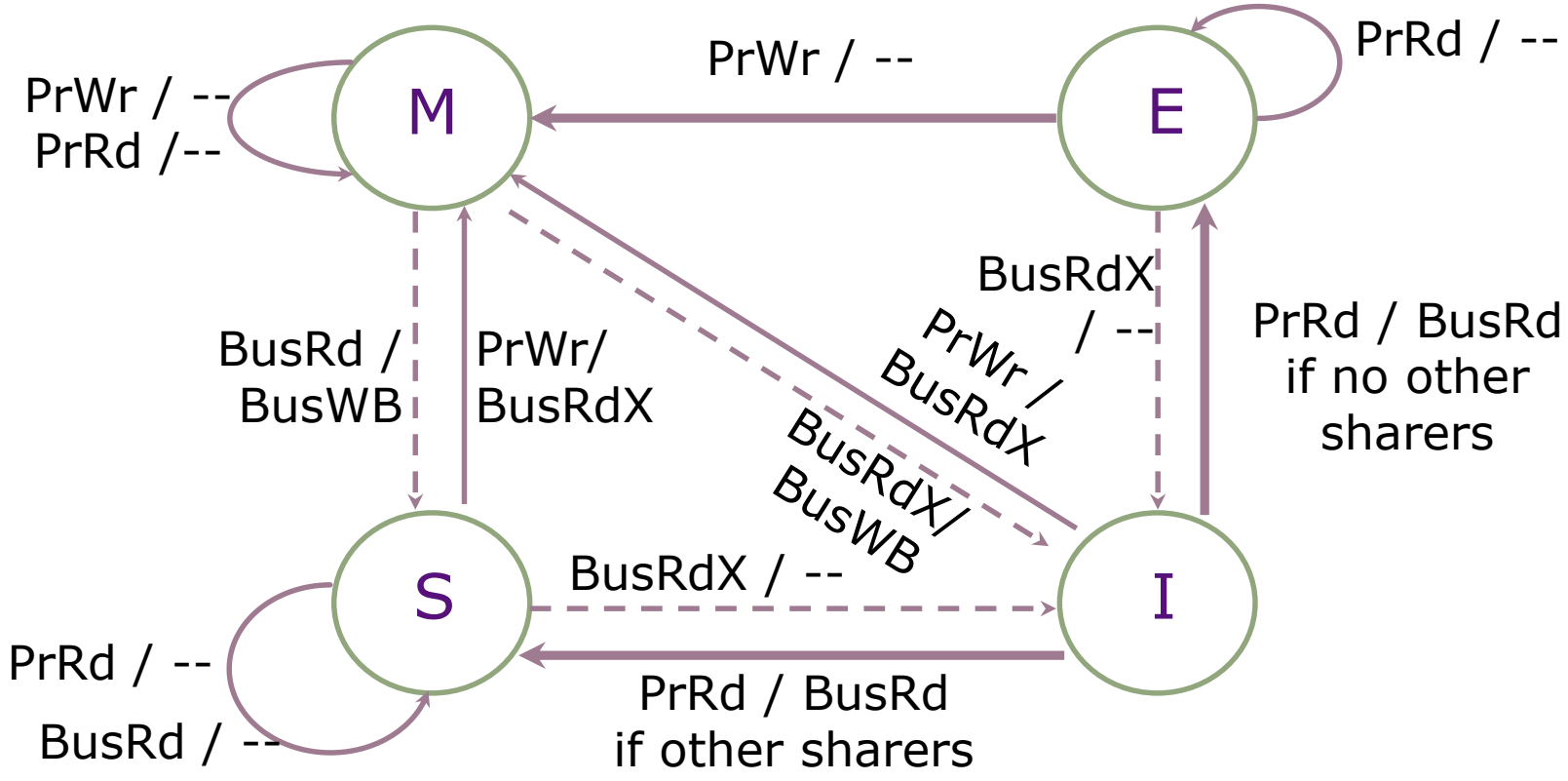

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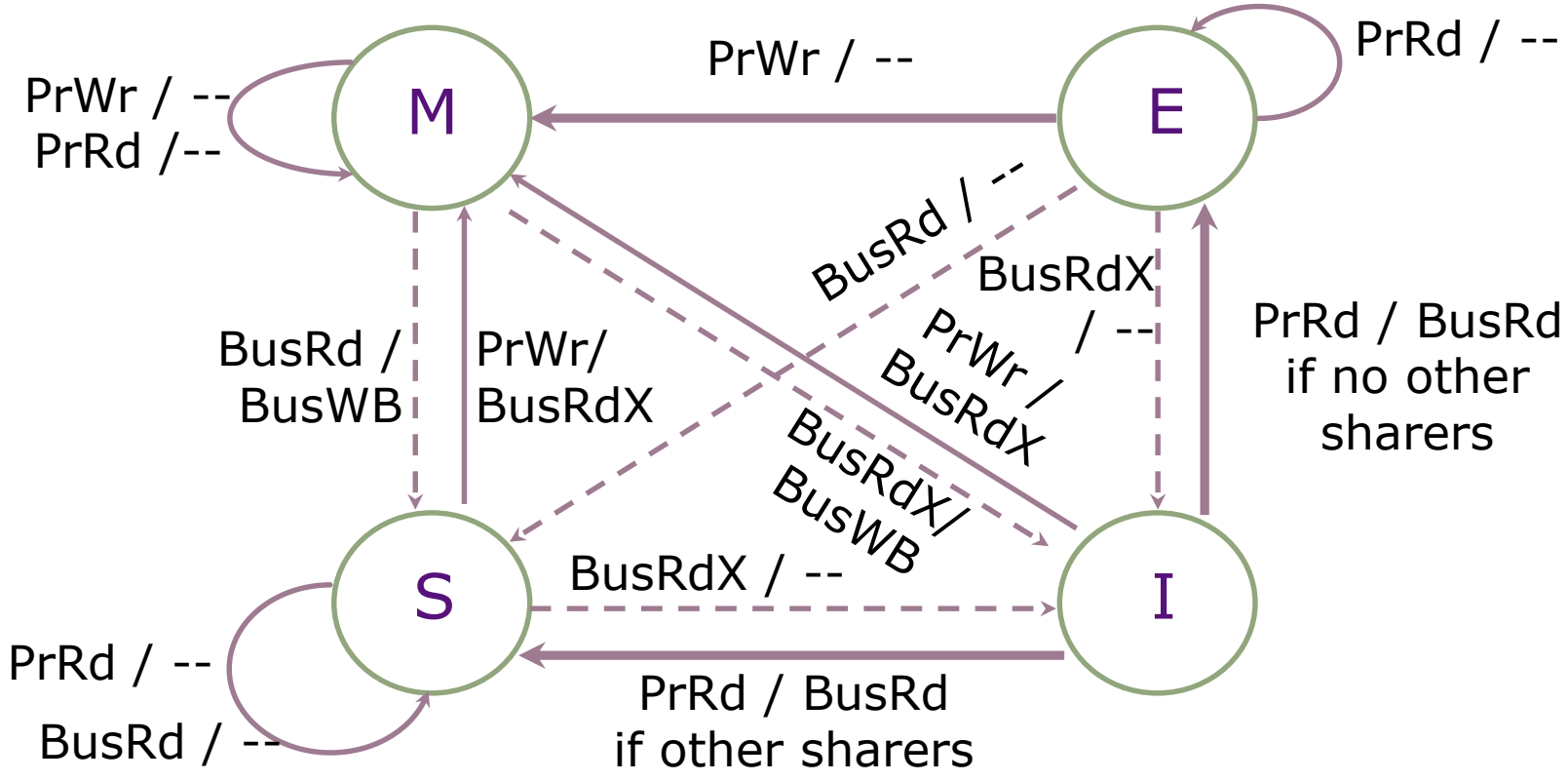

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Each cache line has a tag

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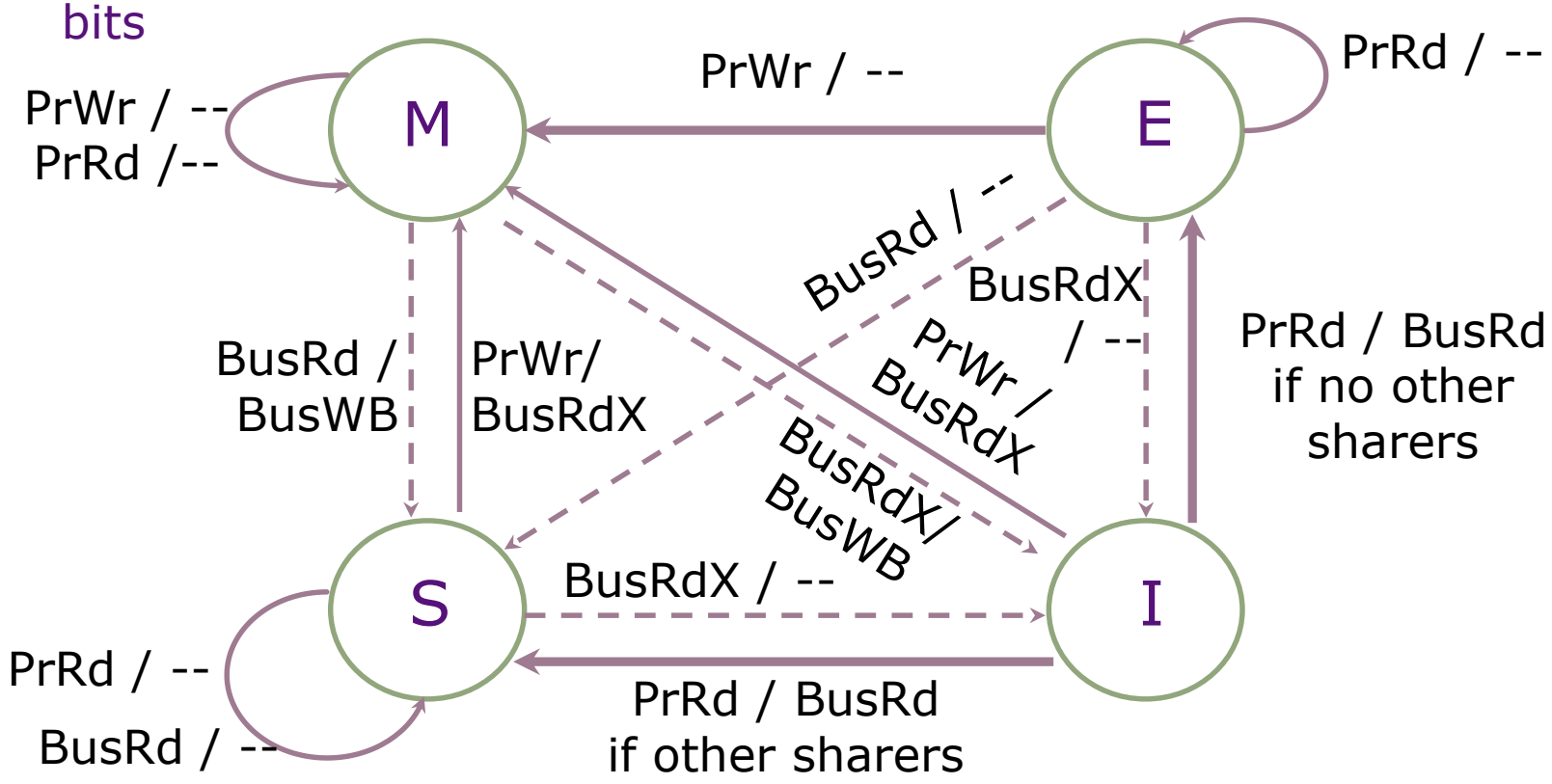

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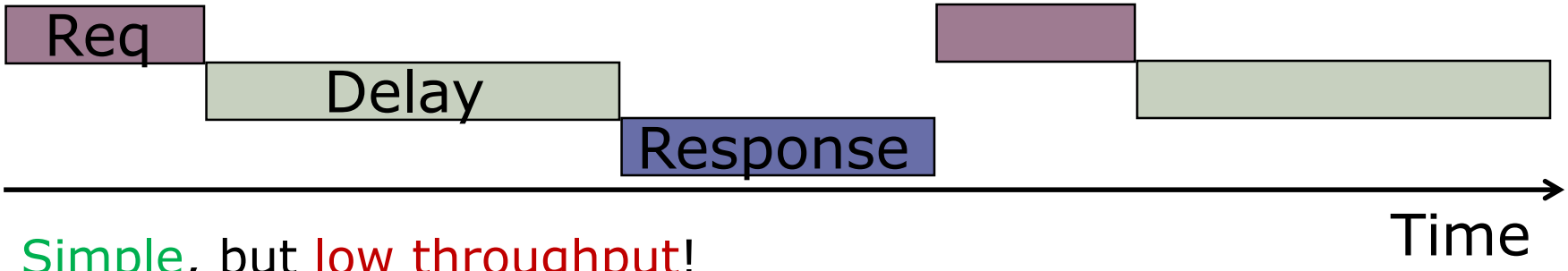
- MSI, MESI, MOSI, MOESI…
  - Typically E if private read-write >> shared read-only (common)
  - Typically O only if writebacks are expensive (main mem vs L3)

Split-Transaction and Pipelined Buses

Atomic Transaction Bus



Simple, but low throughput!

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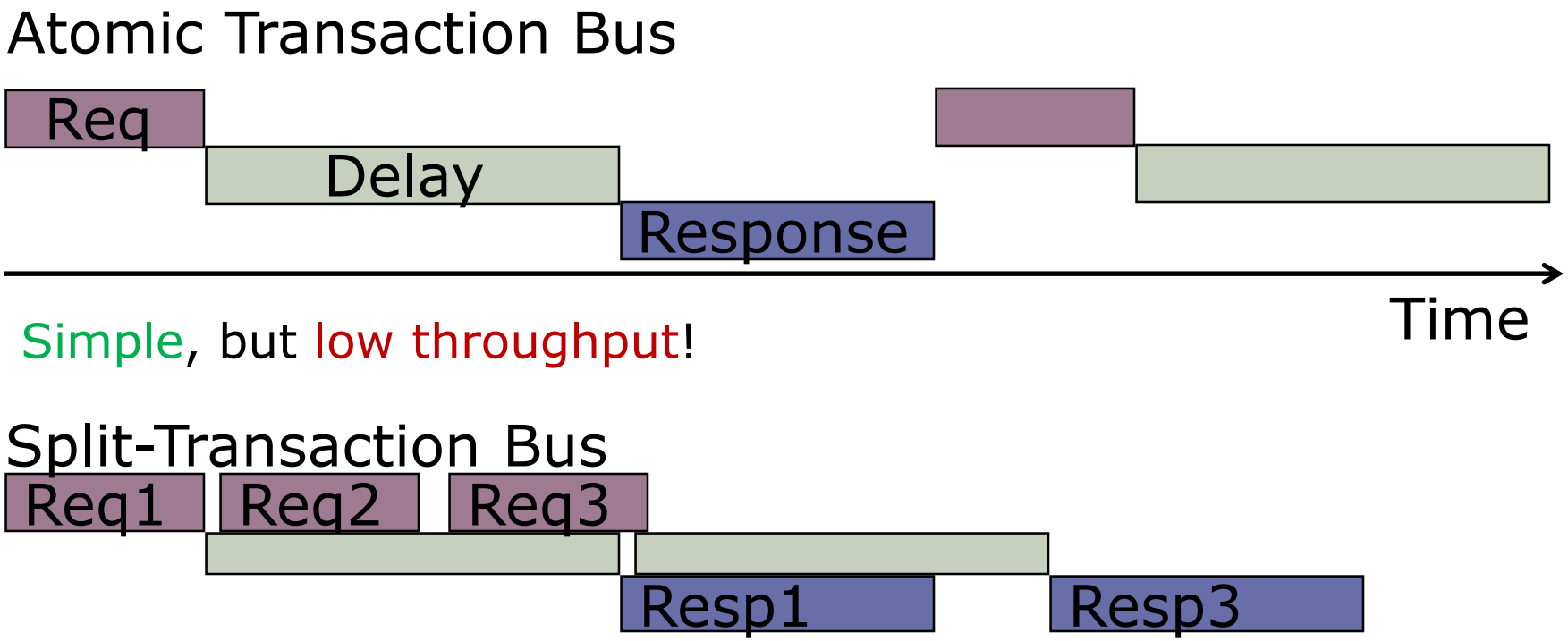

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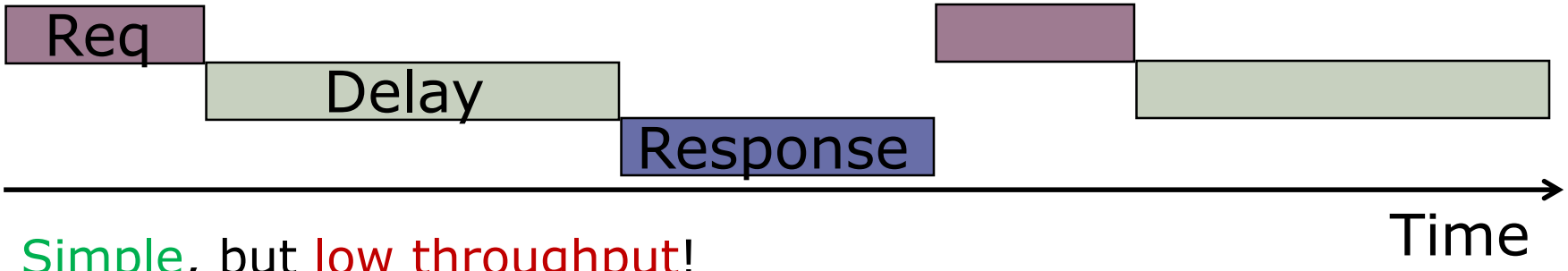

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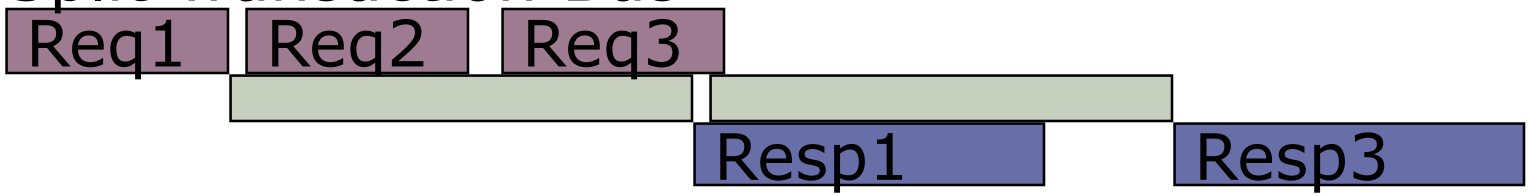

- Supports multiple simultaneous transactions

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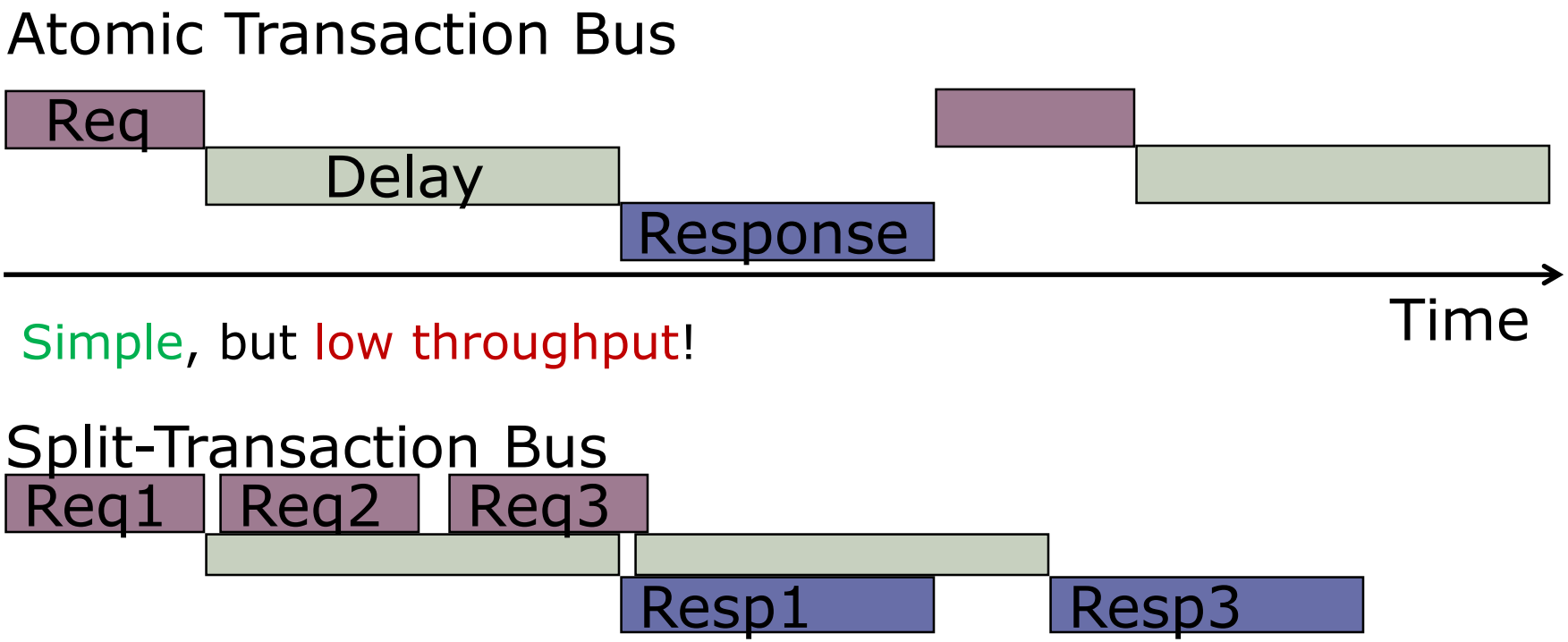

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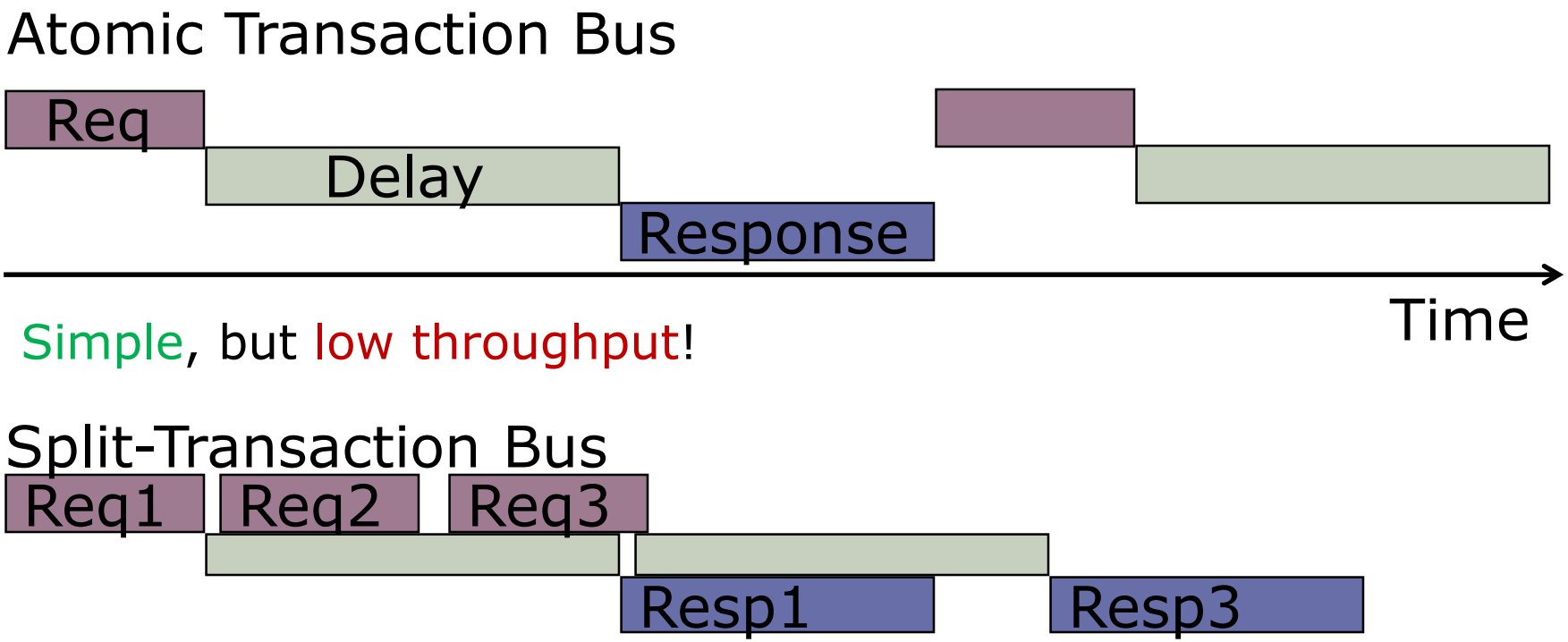
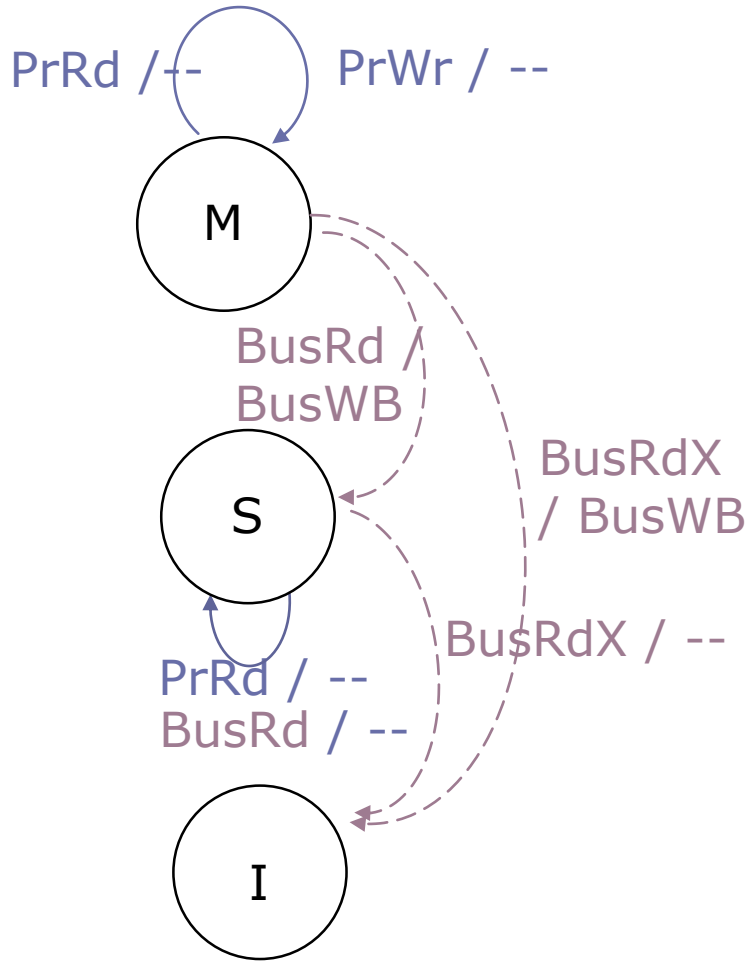


- Supports multiple simultaneous transactions
  - Higher throughput
  - Responses may arrive out of order
- Often implemented as multiple buses (req+resp)

Non-Atomicity → Transient States

- Protocol must handle lack of atomicity
- Two types of states
  - Stable (e.g. MSI)
  - Transient
- Split + race transitions
- More complex



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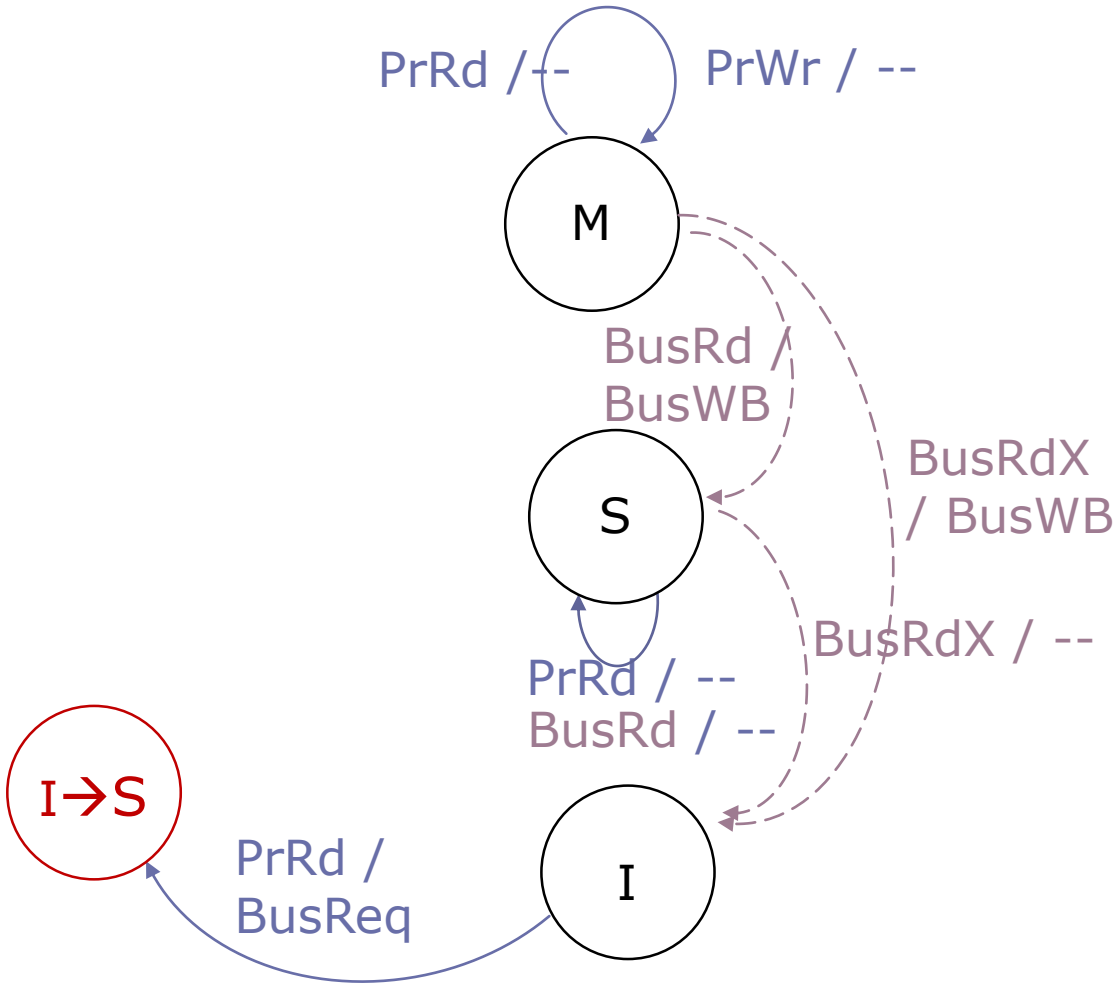

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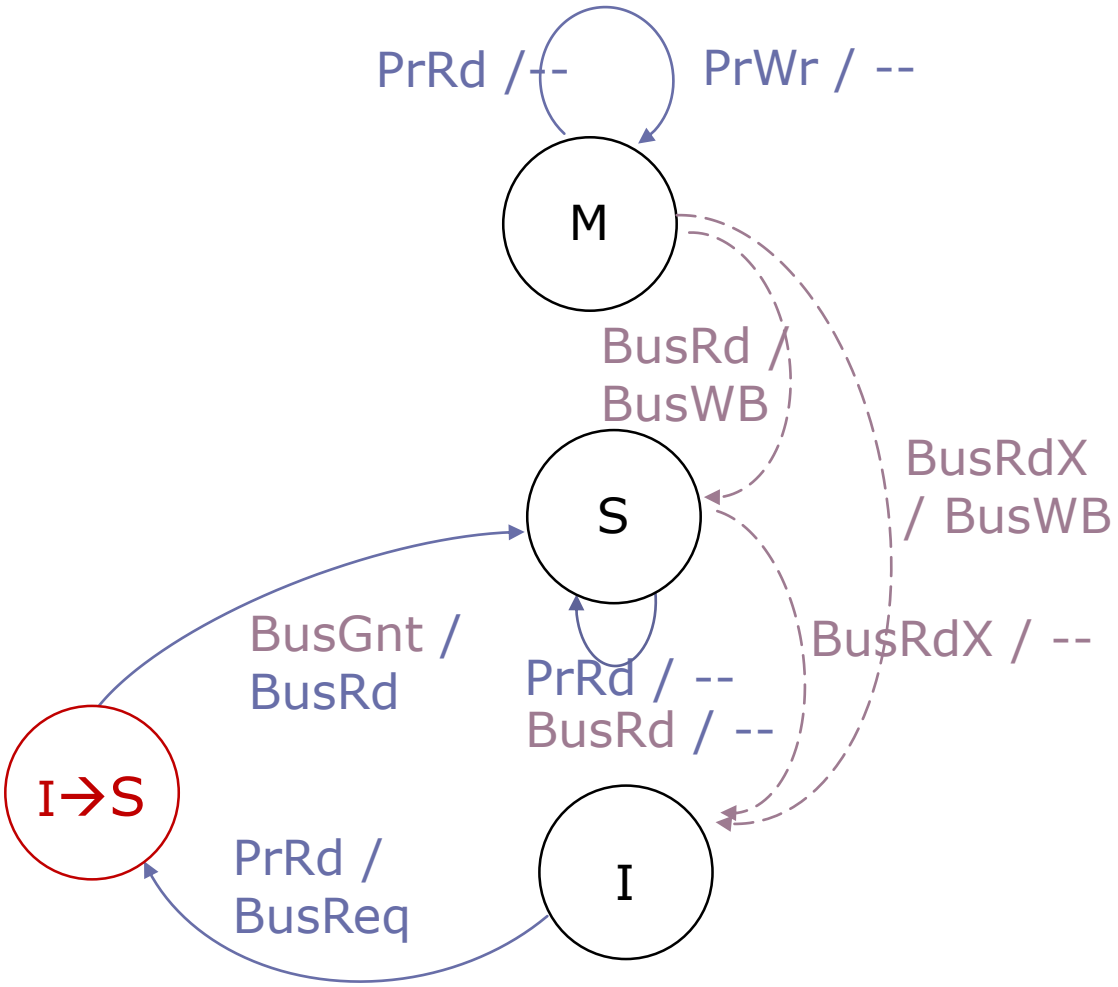

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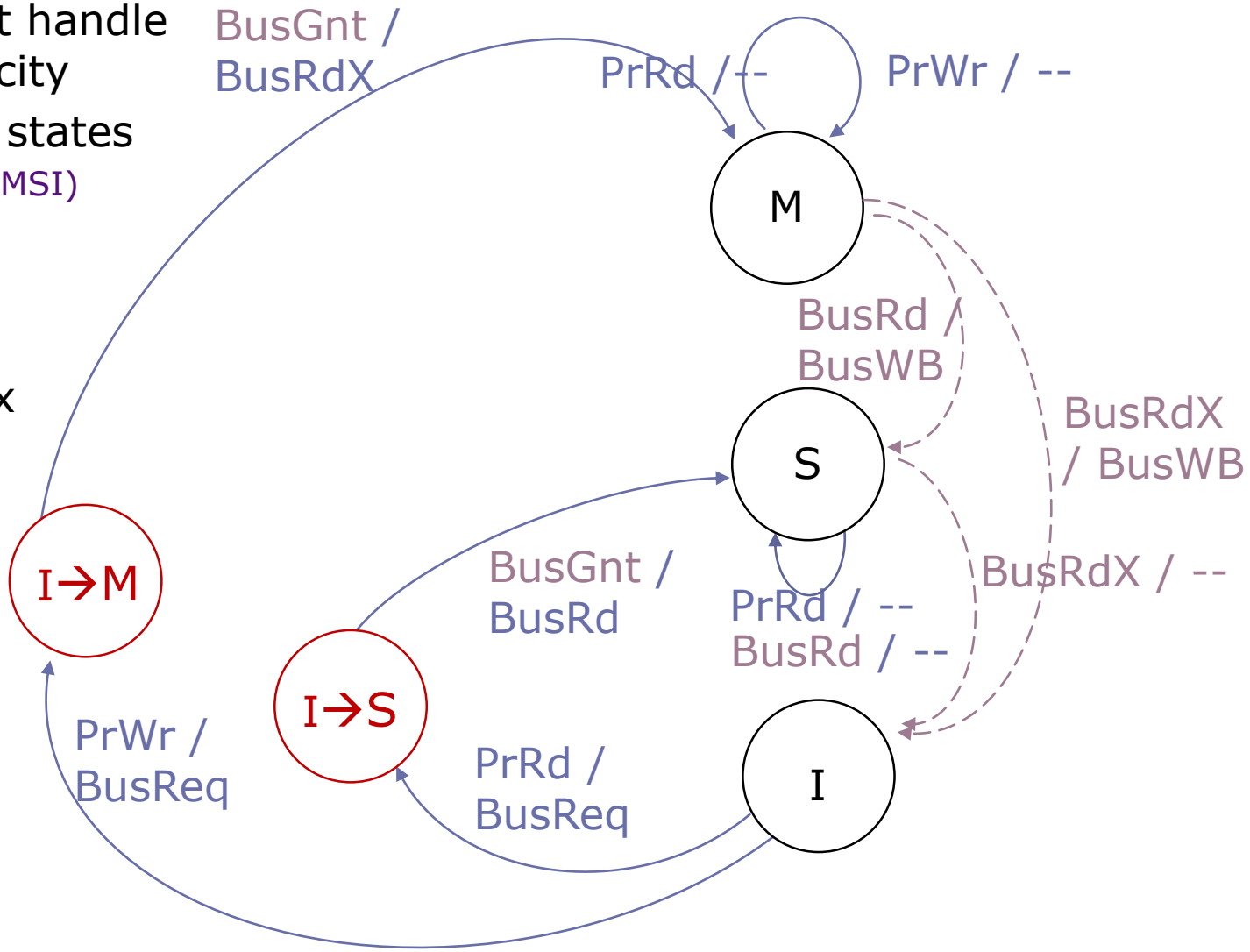

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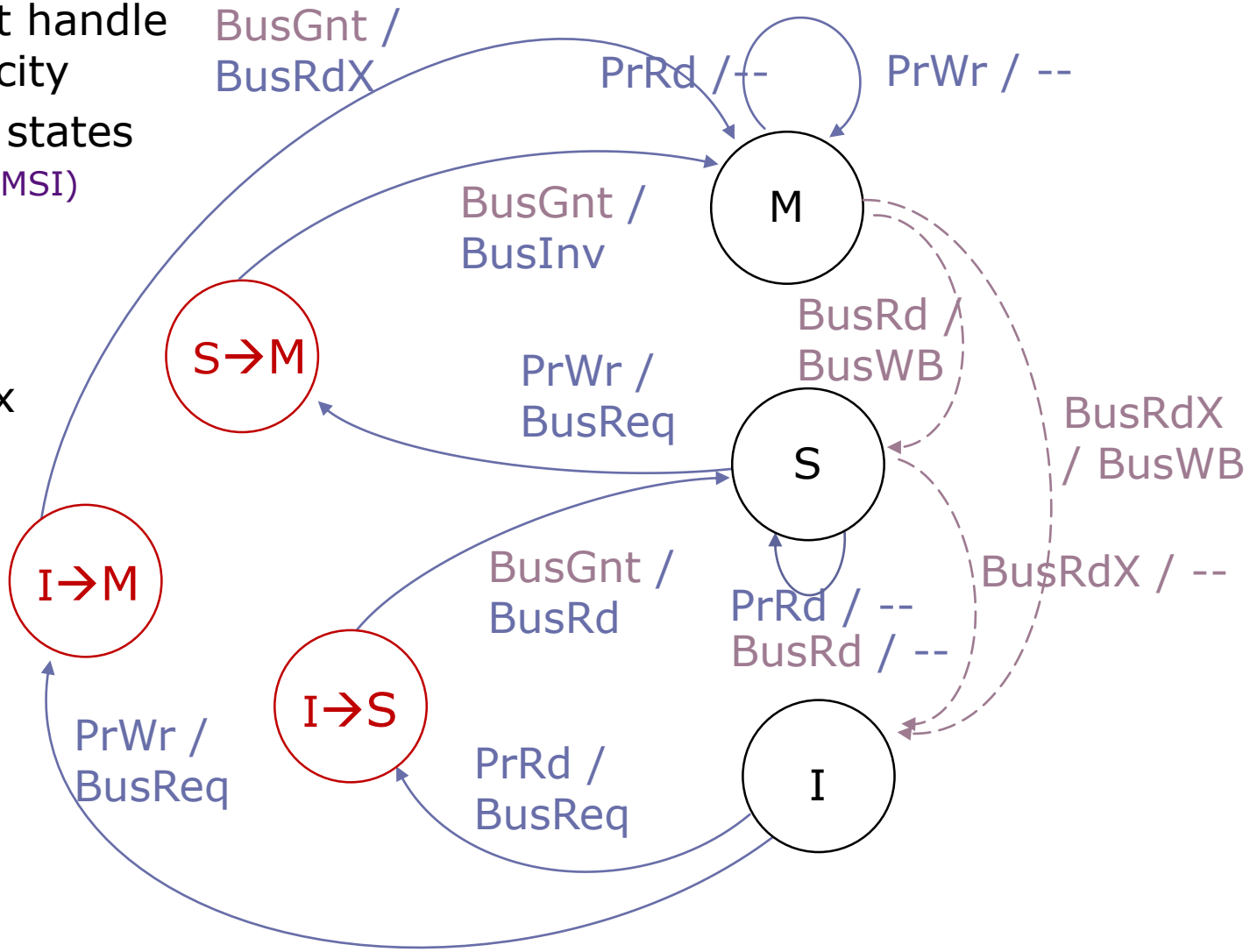

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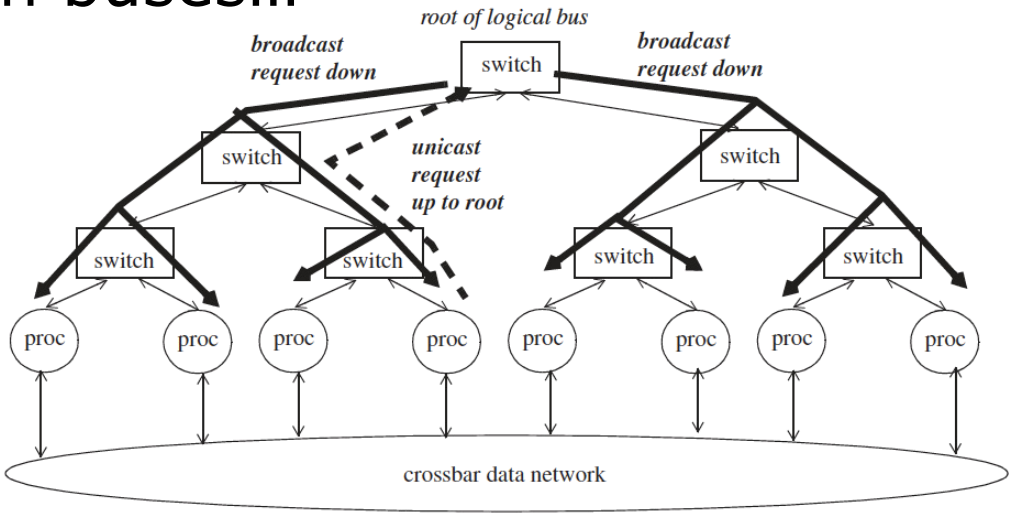
Scaling Cache Coherence

- Can implement ordered interconnects that scale better than buses…



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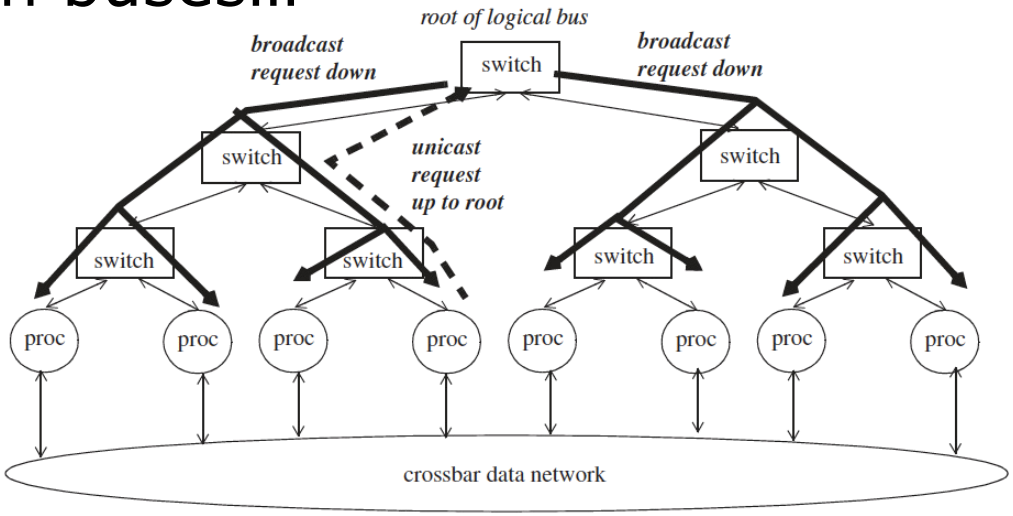
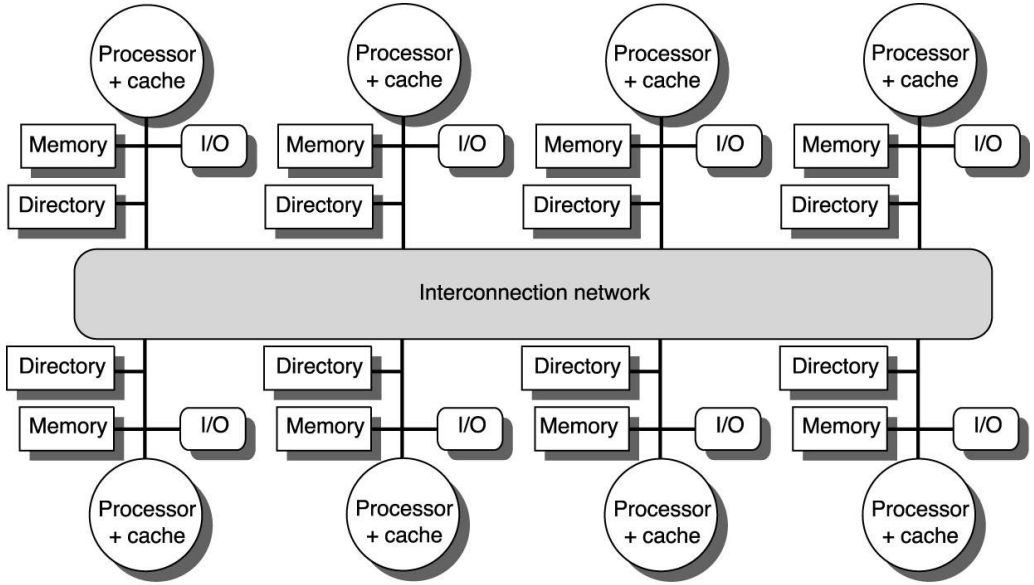


Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors

- … but broadcast is fundamentally unscalable
  - Bandwidth, energy of transactions with 100s of cache snoops?

Directory-Based Coherence



- Route all coherence transactions through a directory
  - Tracks contents of private caches → No broadcasts
  - Serves as ordering point for conflicting requests → Unordered networks

(more on next lecture)

Coherence and False Sharing
Performance Issue #1

A cache block contains more than one word and cache coherence is done at the block-level and not word-level

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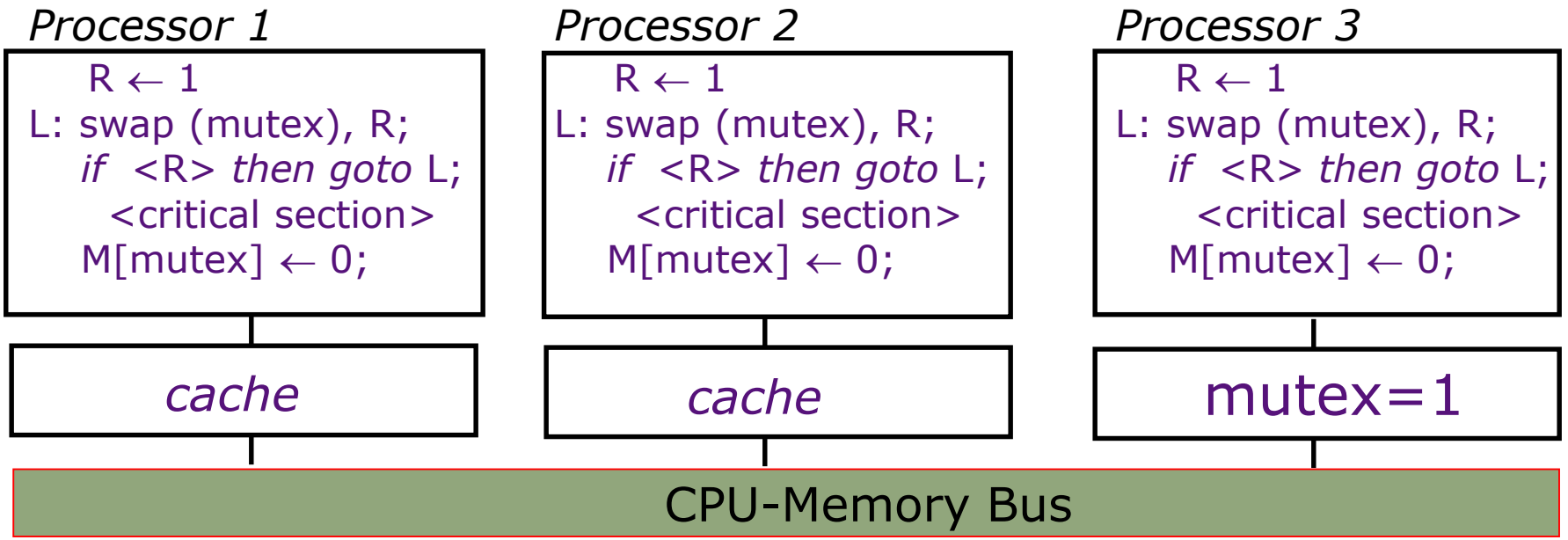
How to address this problem?

Coherence and Synchronization
Performance Issue #2



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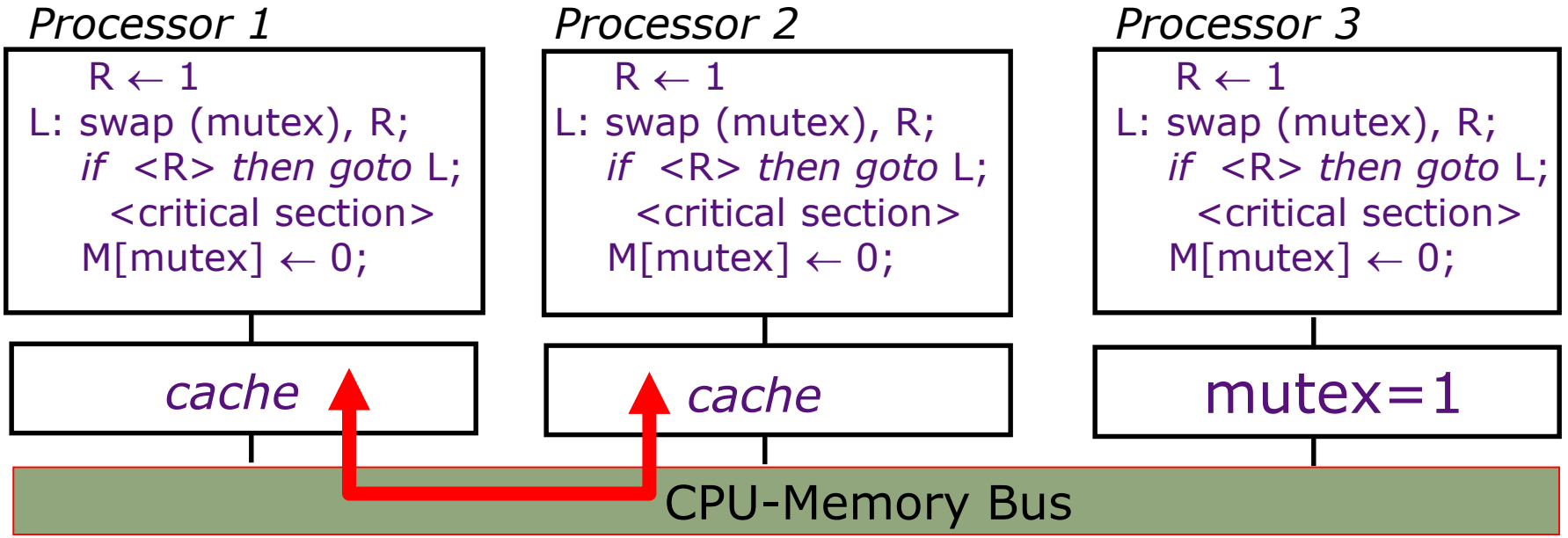

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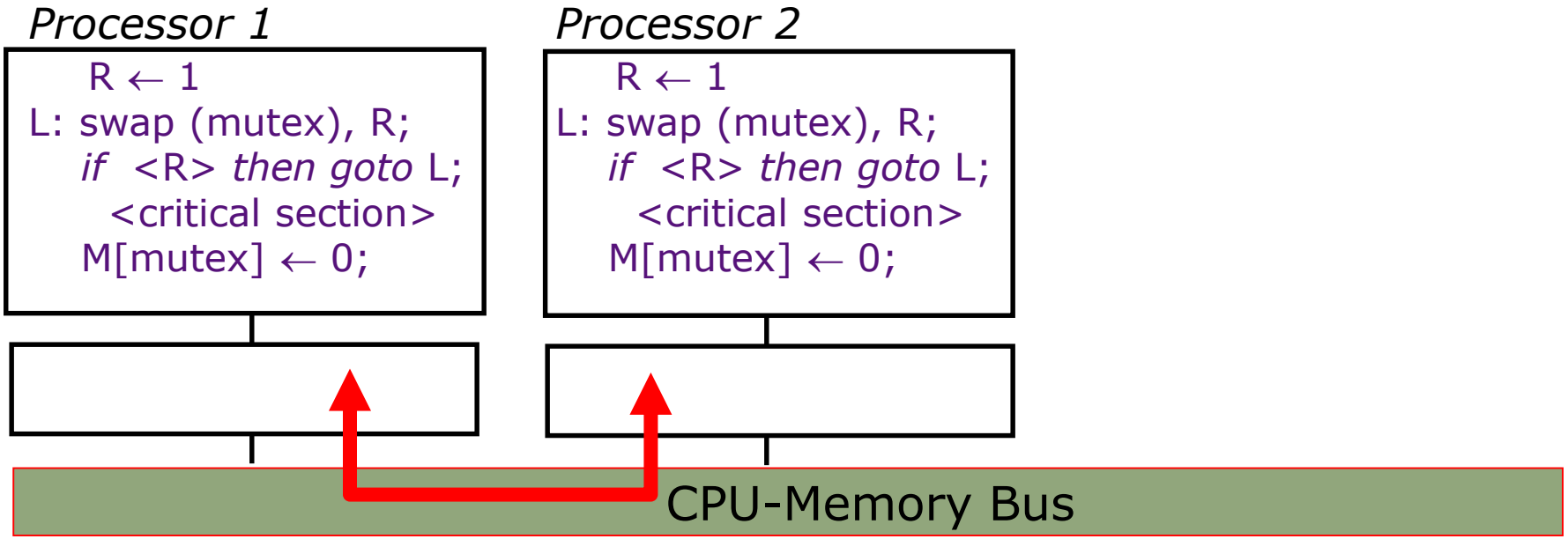

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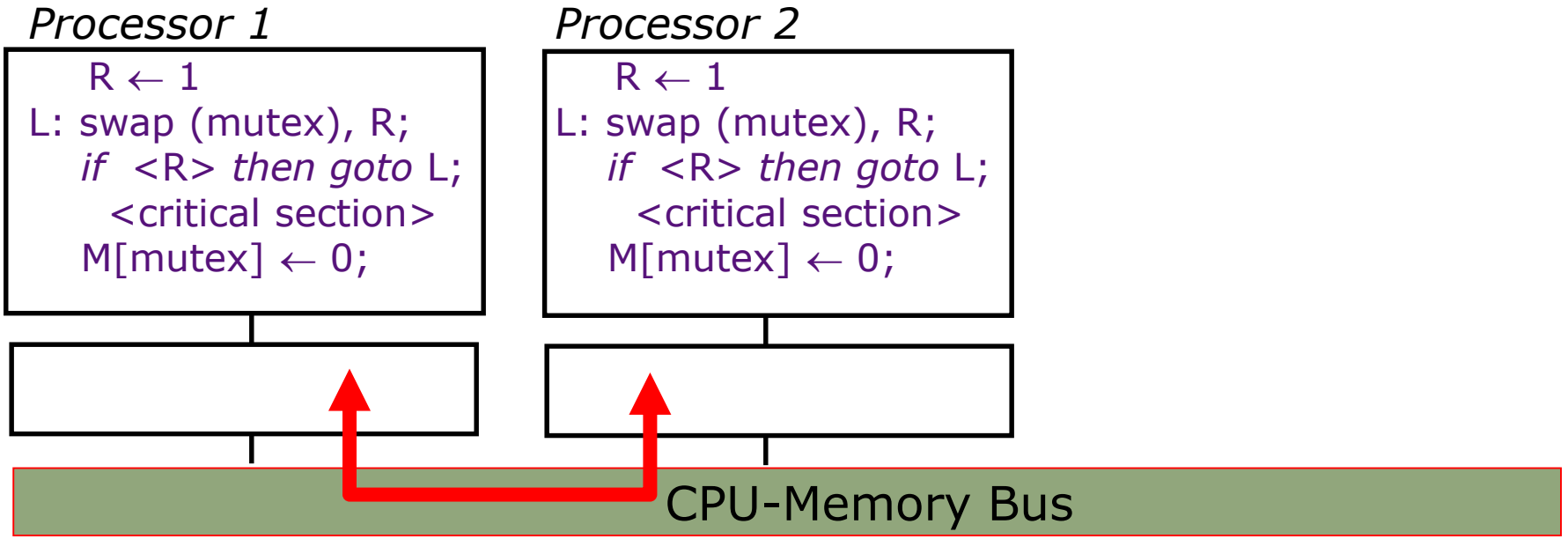

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Ping-ponging can be reduced by first reading the mutex location *(non-atomically)* and executing a swap only if it is found to be zero (test&test&set).

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- modern processors use
  load-reserve
  store-conditional

Load-reserve & Store-conditional

Special register(s) to hold reservation flag and address, and the outcome of store-conditional

```
Load-reserve R, (a):
    <flag, adr> ← <1, a>;
    R ← M[a];
```

```
Store-conditional (a), R:
    if <flag, adr> == <1, a>
    then  cancel other procs'
          reservation on a;
          M[a] ← <R>;
          status ← succeed;
    else  status ← fail;
```

If the snooper sees a store transaction to the address in the reserve register, the reserve bit is set to 0

- Several processors may reserve 'a' simultaneously
- These instructions are like ordinary loads and stores with respect to the bus traffic

Performance:
Load-reserve & Store-conditional

The total number of memory (bus) transactions is not necessarily reduced, but splitting an atomic instruction into load-reserve & store-conditional:

- *increases bus utilization* (and reduces processor stall time), especially in split-transaction buses

- *reduces cache ping-pong effect* because processors trying to acquire a mutex do not have to perform stores each time

Thank you!

Next lecture: Directory-based Cache Coherence