Hardware Implementation of an 802.11a Transmitter

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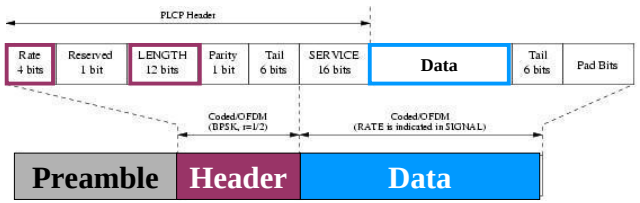
802.11a

- IEEE Standard for wireless communication
- Frequency of Operation: 5Ghz band
- Modulation: Orthogonal Frequency Division Multiplexing
  - OFDM symbol - unit of data transmission
    - One symbol consists of 48 data-encoded complex pairs and 4 pilot complex pairs which protect against noise

Transmitter Overview

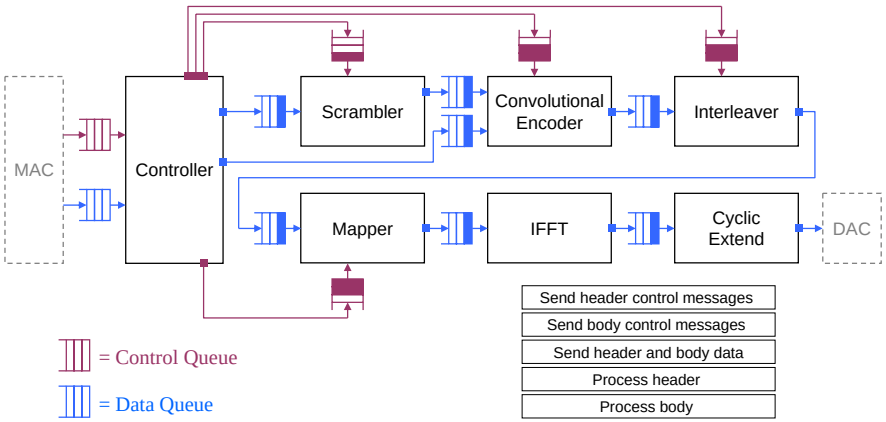
- Tasks:
  - Encodes data for forward error correction
  - Maps data into complex pairs & distributes them among the different frequency indices
  - Transform frequency data into time domain
- Packet Format:



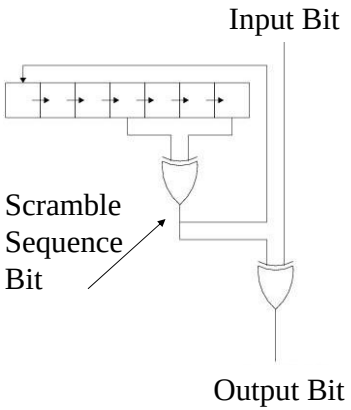
Design Specifications

- Transmit at 3 datarates:
  - 6Mb/s – 1 24-bit input data frame per OFDM symbol
  - 12Mb/s – 2 24-bit input data frames per OFDM symbol
  - 24Mb/s – 4 24-bit input data frames per OFDM symbol
- Design Goals:
  - Minimize Area
  - Minimize Power by reducing frequency and lowering V_{DD}
  - Just-in-time performance to meet the required datarates

Top Level Model



Basic Serial Scrambler Design



- Processes 1 input bit per cycle
- Simultaneously generates 1 scramble sequence bit and computes 1 output bit
- Repeatedly generates a 127-bit scramble sequence

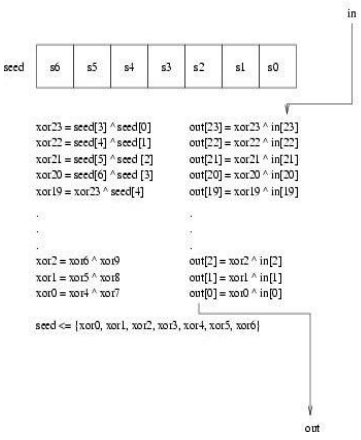
Initial Scrambler Design

For Each Message:
- Generates the entire 127-bit scramble sequence – 127 cycles
- Stores the scrambler sequence to be used throughout the message

Advantage:
- Processes 1 24-bit input frame per cycle

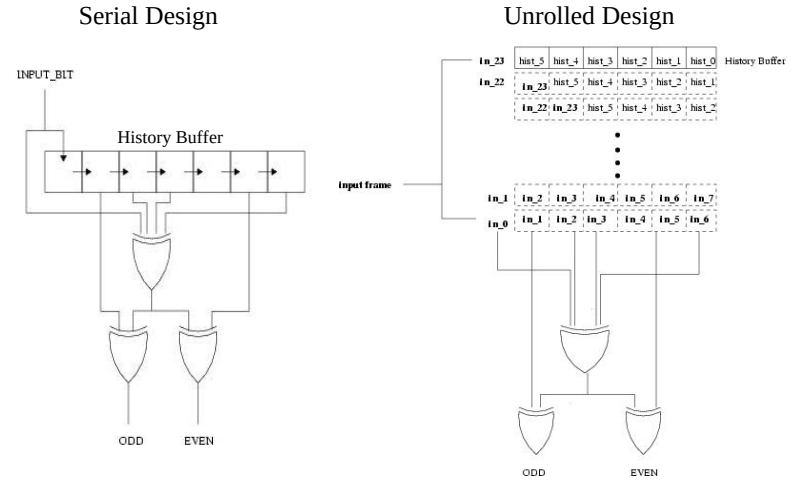
Disadvantage:
- Large initialization overhead is especially apparent for a series of very short messages

Unrolled Scrambler Design

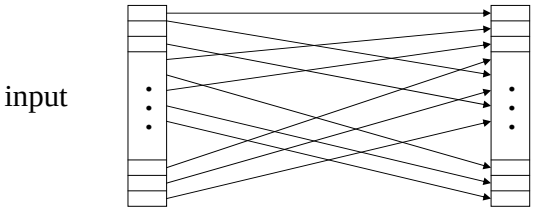


- Simultaneously generates 1 frame of the scrambler sequence and processes 1 frame of input data per cycle
- Updates the state of the seed register at end of each cycle
- Advantages:
  - 1 cycle initialization
  - Processes 1 24-bit frame per cycle

Convolutional Encoder Design

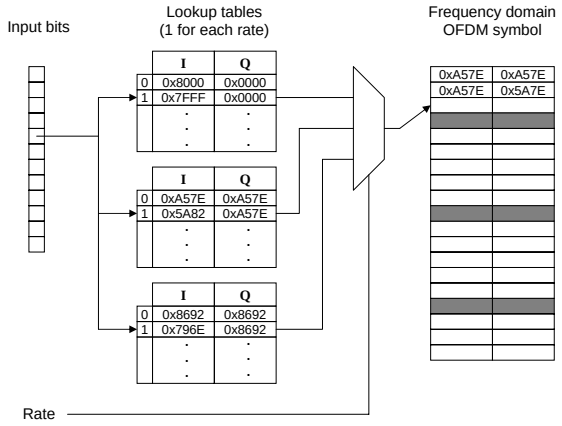


Interleaver Algorithm

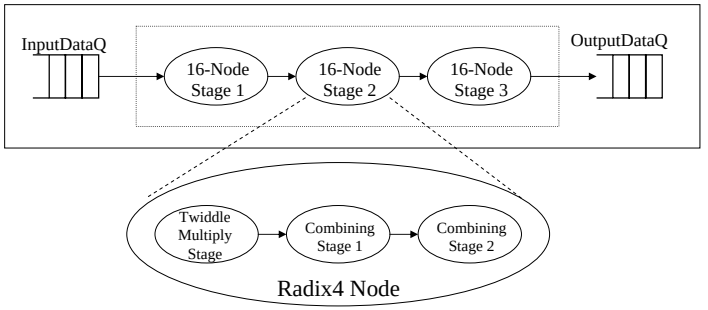


- Reorders input data bits
- Datarate dependent:
  - Interleaving Pattern
  - # of bits interleaved together

Mapper Algorithm



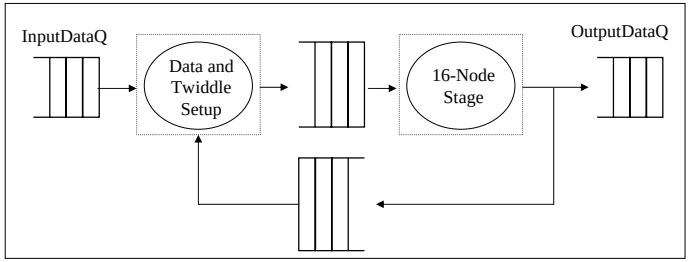
IFFT Initial Design



- Area = 29.12mm^2
- Cycle Time = 63.18ns

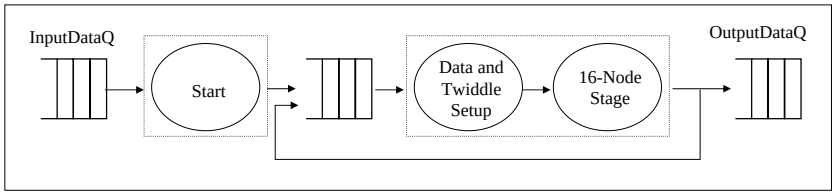
Radix4 Nodes	*	+
1	16	24
48	768	1152

IFFT Design Exploration 1



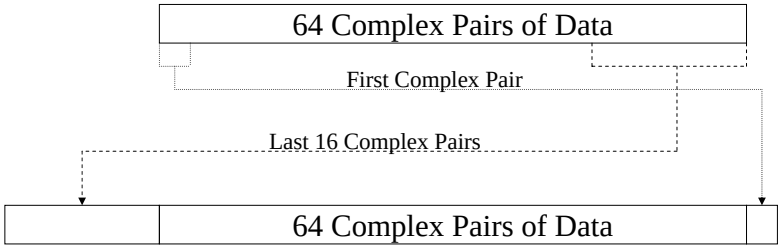
- Area = 5.19mm^2
- Cycle Time = 30.50ns

IFFT Design Exploration 2



- Area = 4.57mm^2
- Cycle Time = 32.89ns

Cyclic Extender



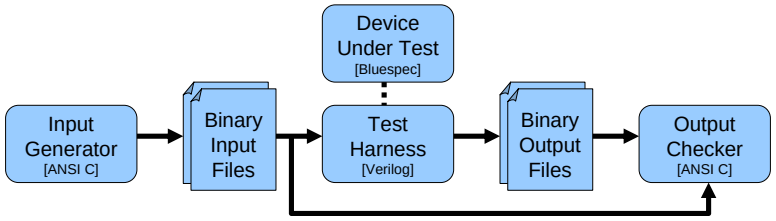
Test Strategy

- Our test structure must enable us to:
  - Debug each module separately
  - Quickly verify new version of modules
  - Verify correctness of entire system
  - Measure throughput of individual modules and system as a whole
- To do this, we leveraged the framework of the Extreme Benchmark Suite (XBS)

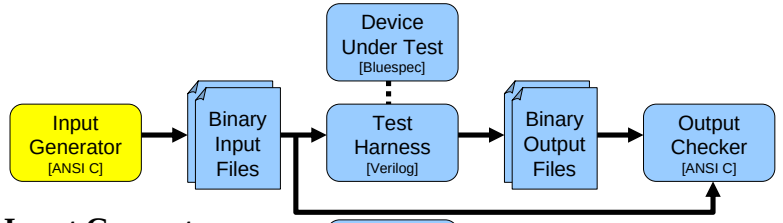
XBS Overview

XBS is a benchmark suite designed to measure the performance of highly parallel processors and custom hardware implementations.

All XBS benchmarks have the following structure:

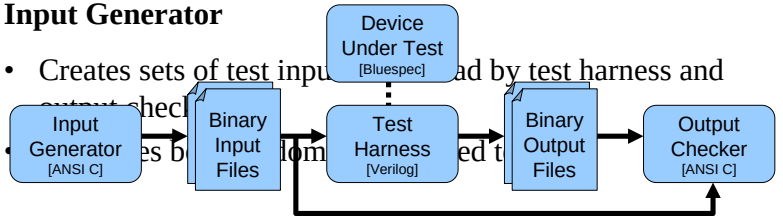


XBS Overview

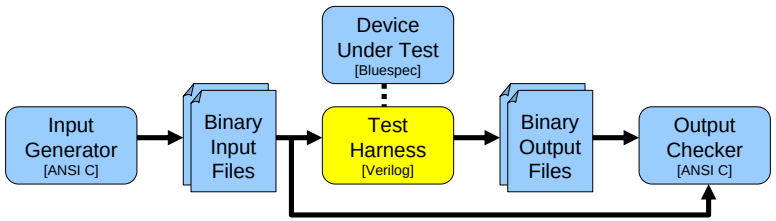


Input Generator

- Creates sets of test inpu ad by test harness and
- es b om ed t



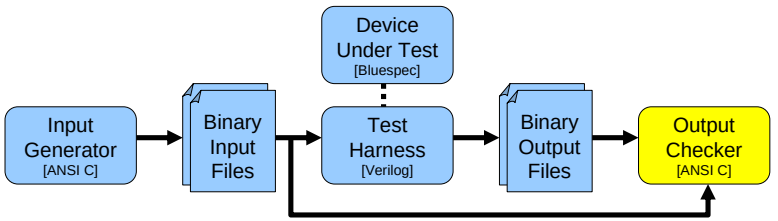
XBS Overview



Test Harness

- Encapsulates device under test
- Reads in input files and generates output files
- Measures performance [throughput in bits per cycle] of device under test

XBS Overview



Output Checker

- Reads in input and output files and determines if output files are correct
- Usually contains an ANSI C reference version of DUT
- If output is incorrect, displays location of discrepancy and correct value for debugging purposes

Results

Place and route results:

Total Area	5.27 mm^2
Critical Path Delay	32.89 ns

XBS testing results:

Module	Throughput					
	Input bits per cycle			OFDM symbols per cycle		
Scrambler	24	24	24	1	0.5	0.25
Convolutional Encoder	24	24	24	1	0.5	0.25
Interleaver	12	12	12	0.5	0.25	0.125
Mapper	12	16	19.2	0.5	0.333	0.2
IFFT	6	12	24	0.25	0.25	0.25
Cyclic Extend	24	48	96	1	1	1
Transmitter System	**6**	**12**	**12**	**0.25**	**0.25**	**0.125**

= 6 Mbps

= 12 Mbps

= 24 Mbps

Evaluation

- Our design fully conforms to the IEEE 802.11a standard
- Our design meets timing for the 6, 12, and 24 Mbps transmission rates
  - Total system throughput (24 Mbps) = 12 bits / cycle
  - Clock Frequency = 30.4 MHz
  - Maximum data rate of system = 364.8 Mbps
- We can turn our timing slack into power savings by reducing V_{DD} and clock frequency
  - Clock frequency can be reduced to 2.0 MHz