The Plan

- Out-of-order
- Speculative
- Physical register file
- Single-issue
- Non-blocking, in-order memory unit
- Branch prediction
- Precise exceptions

The Basic Design: Data Flow

The Basic Design: Branch Taken
Design Exploration: Data Flow

Design Exploration:
- Branch Predictor

- Use a standard 2-bit predictor
- No global history (even though it was originally planned)
- Carry a "branchTaken" bit to allow Execute to check if prediction was correct
Design Exploration:
- Branch Predictor
  - Hash on bottom bits of instruction PC
  - Initialize to WT
  - Predict all branch instructions and force take J and JAL

Design Exploration:
- Out of Order Scheduling
  - Find which instructions are ready to go
  - Dispatch memory operations in order (speculatively)
  - Send stores to memory when retired
  - Use barrier instructions for COP0

Design Exploration:
- Out of Order Scheduling
  - Schedule in-order and out-of-order instructions separately
  - Be careful about the wrap-around

Place and Route

ROB
IPCF
REGS
EXEC
RENAME
MMU
Results

- Final clock period was 9.803ns
- Final area 458569.6 μm²
- qsort retires 24249 instructions (ipc=0.4)
- vvadd retires 18026 instructions (ipc=0.5)
- vvadd loop: 10 instructions, 16 cycles
- using our own harness, still adapting to Chris’s
- Number of cycles to complete benchmark:

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<thead>
<tr>
<th></th>
<th>basic</th>
<th>bp</th>
<th>ooo</th>
<th>bp/ooo</th>
<th>fast mispredict</th>
<th>fast predict</th>
<th>speculative memory unit</th>
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<td>qsort</td>
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Interesting Problems

- Bluespec infinite compile times: 12-entry ROB compiles in 2 mins; 14-entry ROB hangs forever
- RWires are necessary but EVIL
- Branch predict: Bug with predicting JR and JALR, noting it’s been “taken” but going to the wrong target!
- Lots of bug in decode and execute: all fixed once we passed self_test, test_spin and test_all (renaming/out-of-order didn’t introduce execution bugs)

Special Thanks To:

- 6884-bluespec
- Chris

The End