

PIPE DREAM

Out-of-Order Speculative CPU

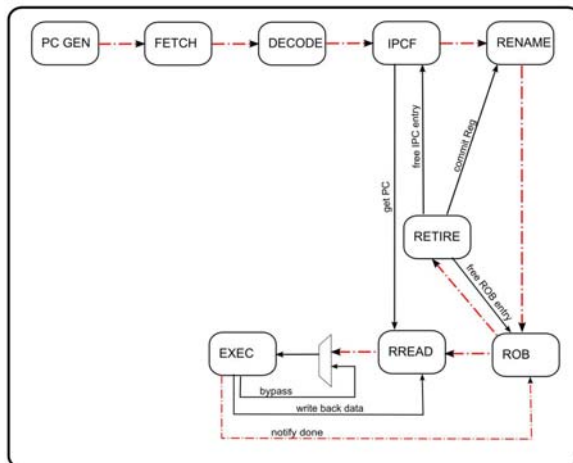
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May 9, 2005

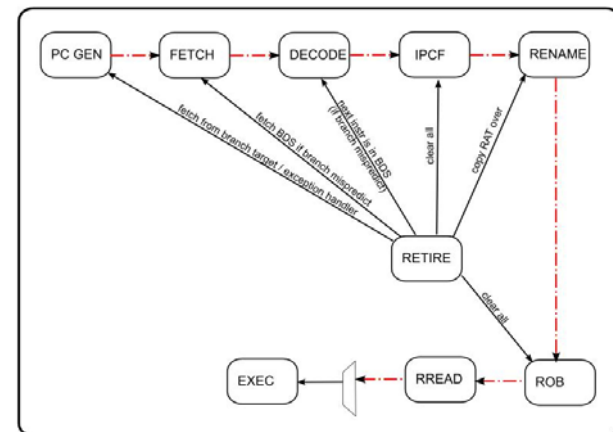
The Plan

- Out-of-order
- Speculative
- Physical register file
- Single-issue
- Non-blocking, in-order memory unit
- Branch prediction
- Precise exceptions

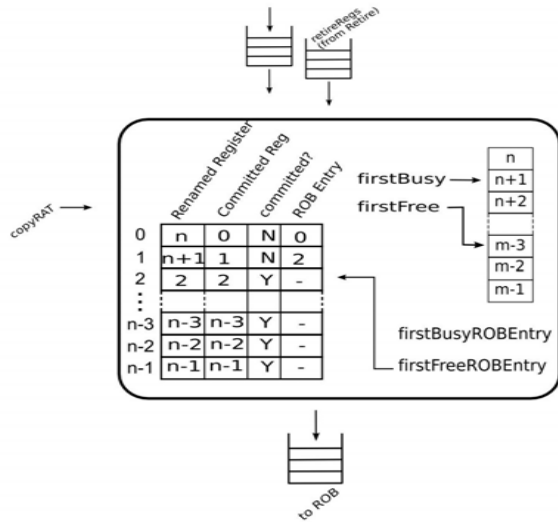
The Basic Design: Data Flow



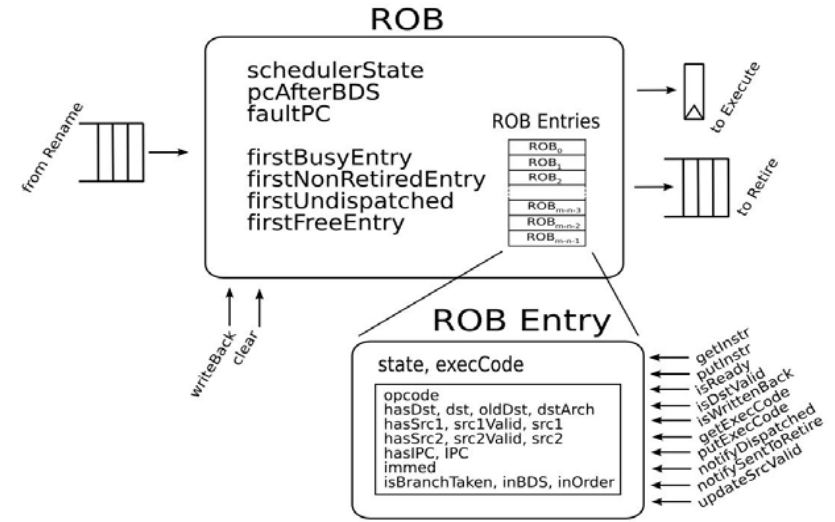
The Basic Design: Branch Taken



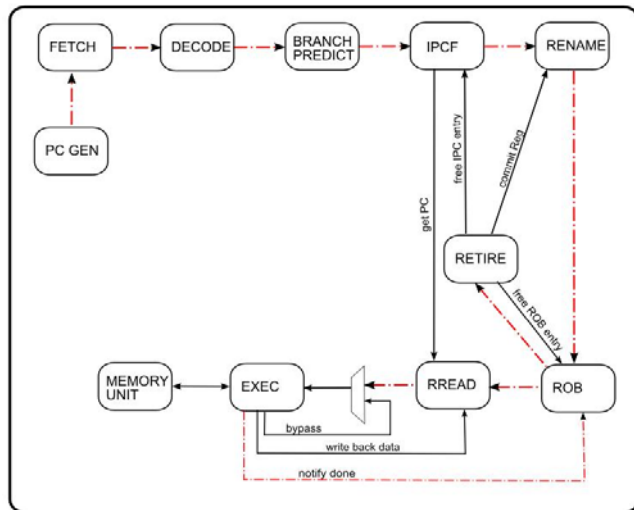
Register Rename Unit



Re-order Buffer



Design Exploration: Data Flow

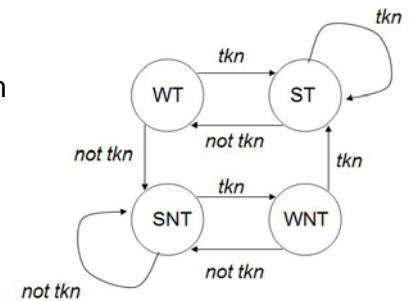


Design Exploration:

- Branch Predictor

- Use a standard 2-bit predictor
- No global history (even though it was originally planned)
- Carry a "branchTaken" bit to allow Execute to check if prediction was correct

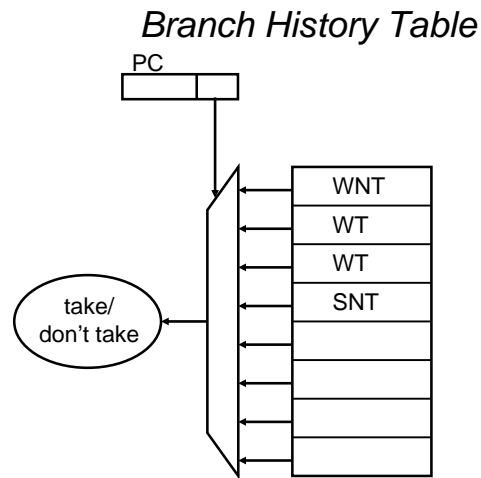
2-bit Branch Predictor



Design Exploration:

- Branch Predictor

- Hash on bottom bits of instruction PC
- Initialize to WT
- Predict all branch instructions and force take J and JAL



Design Exploration:

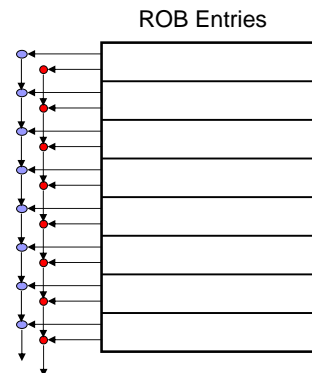
- Out of Order Scheduling

- Find which instructions are ready to go
- Dispatch memory operations in order (speculatively)
- Send stores to memory when retired
- Use **barrier** instructions for COP0

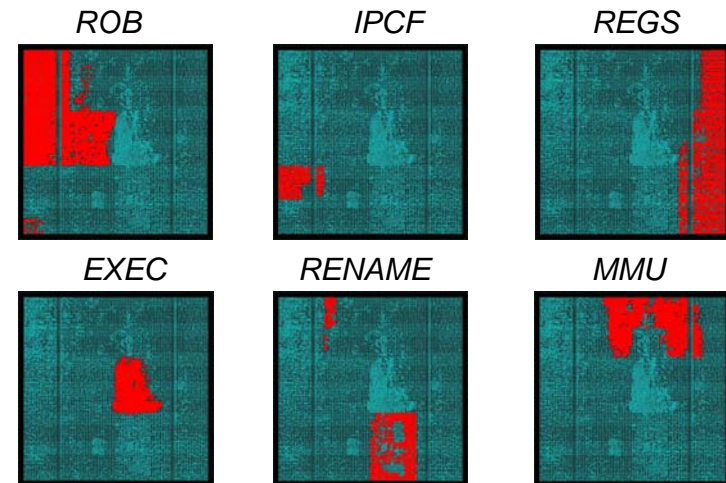
Design Exploration:

- Out of Order Scheduling

- Schedule in-order and out-of-order instructions separately
- Be careful about the wrap-around



Place and Route



Results

- Final clock period was 9.803ns
- Final area 458569.6 μm^2
- qsort retires 24249 instructions (ipc=0.4)
- vvadd retires 18026 instructions (ipc=0.5)
- vvadd loop: 10 instructions, 16 cycles
- using our own harness, still adapting to Chris's
- Number of cycles to complete benchmark:

	basic	bp	ooo	bp/ooo	fast mispredict	fast predict	speculative memory unit
qsort	97909	101139	87675	72549	68861	66473	61275
vvadd	96123	102127	100131	49196	49174	45170	36163

Interesting Problems

- Bluespec infinite compile times: 12-entry ROB compiles in 2 mins; 14-entry ROB hangs forever
- RWires are necessary but *EVIL*
- Branch predict: Bug with predicting JR and JALR, noting it's been "taken" but going to the wrong target!
- Lots of bug in decode and execute: all fixed once we passed self_test, test_spim and test_all (renaming/out-of-order didn't introduce execution bugs)

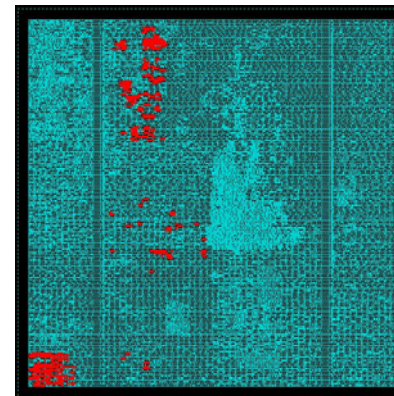
Special Thanks To:

- 6884-bluespec
- Chris

The End

Slowest Data Path

retireInstrQ



retireIPCQ

