Complete Information Flow Tracking from Gates Up

Mohit Tiwari, Xun Li, Hassan M G Wassel, Frederic T Chong, Timothy Sherwood

Presented by Mengjia Yan
Based on slides from Mohit Tiwari
Goal: Non-Interference
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- **Non-Interference**: a change in a High input can never be observed or inferred from changes in the Low output. That is, High data should never leak to Low.
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- **Confidentiality-Integrity Duality**: “High” is more conservative label. Secret or Tainted/Untrusted.
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Information Flow for Privacy

• General lattice policies

• Secret vs. Unclassified Data
  • Secret: data with restricted access permission
  • Unclassified: data with unrestricted access
Information Flow for Privacy

• General lattice policies
• Secret vs. Unclassified Data
  • Secret: data with restricted access permission
  • Unclassified: data with unrestricted access
• Enforce the property of non-interference:
  • Verify information never flows from high to low.
  • Secret information is never used to modify unclassified data
Information Flow for Integrity

• Trusted vs. Untrusted Tasks
  • **Trusted**: processes which are critical to the correct functionality of the space vehicle systems
  • **Untrusted**: mission processes, diagnostics, anything whose malfunction will not cause a vehicle loss
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  • **Trusted**: processes which are critical to the correct functionality of the space vehicle systems
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• Enforce the property of non-interference:
  • Verify information never flows from high to low.
  • **Untrusted** information is never used to make critical (trusted) decisions nor to determine the schedule (real-time)
Threat Model

• Low output can include
  • Program output
  • Timing
  • Contention on system resources
Threat Model

• Low output can include
  • Program output
  • Timing
  • Contention on system resources

• Not include
  • Untrusted hardware component problem
  • Physical attacks that may tamper with memory
  • Non-digital side-channel attacks (power distribution and RF signals)
Highlights

• A secure SW/HW co-design which is verifiable

• Gate-level information flow tracking
  • More precise than conventional IFT

• ISA restrictions to prevent taint explosion
  • Handling conditional branch
  • Handling loops
  • Handling loads/stores
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A new way to look at IFT from a new perspective.
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A new way to look at IFT from a new perspective.

Usage: GLIFT + Information Flow Policy
The Vision: Hardware Design for Software Security Verification
The Vision: Hardware Design for Software Security Verification

Sound Information Flow Analysis
The Vision: Hardware Design for Software Security Verification

Sound Information Flow Analysis

Hardware/Software Design for Verifiable Security
The Vision: Hardware Design for Software Security Verification

<table>
<thead>
<tr>
<th>Security Properties</th>
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<tbody>
<tr>
<td>Logic Gates</td>
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<td>Microarchitecture</td>
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Hardware/Software Design for Verifiable Security
The Vision: Hardware Design for Software Security Verification

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- Language
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- Logic Gates

Security Properties
Information Flow Analysis

• Information flows through **Space**
  • Registers, Memory, Micro-architectural state etc.
Information Flow Analysis

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\[ \text{out}1 = \text{ld} (\text{high}) \]

(*explicit flow*)
Information Flow Analysis

• Information flows through **Space**
  • Registers, Memory, Micro-architectural state etc.

\[
\text{out1} = \text{ld}(\text{high})
\]

\[
\begin{align*}
\text{if } (\text{high} == 1) \\
& \quad \text{out1} = 1 \\
\text{else} \\
& \quad \text{out2} = 0
\end{align*}
\]

(implicit flow) (explicit flow)
Out1 = ld(high)
Out2 = ld(low)

if (high == 1)
    out1 = 1
else
    out2 = 0

(explicit flow)

(out1 = ld(high)
out2 = ld(low)

(implicit flow)
Static and Dynamic Information Flow Tracking

• Static analysis is conservative (need alias analysis for precise results)
• Dynamic analysis has difficulty in analyzing implicit flow

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if (high == 1)
    out1 = 1
else
    out2 = 0
```

(out1 = ld(high)
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(implicit flow)

(explicit flow)
Static and Dynamic Information Flow Tracking

• Static analysis is conservative (need alias analysis for precise results)
• Dynamic analysis has difficulty in analyzing implicit flow

\[
\text{out1} = \text{ld(} \text{high} \text{)}
\]

\[
\text{out2} = \text{ld(} \text{low} \text{)}
\]

(out \text{explicit flow})

\[
\text{if (} \text{high} == 1 \text{)}
\]
\[
\text{out1} = 1
\]
\[
\text{else}
\]
\[
\text{out2} = 0
\]

(implicit flow)

out2 is tainted if the address or the memory value is tainted
Information Flow Analysis

• Information flows through **Space**
  • Registers, Memory, Micro-architectural state etc.

• Information flows through **Time**
  • Observable events such as PC, I/O channels etc.
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• Information flows through **Time**
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The paper addresses two challenges

• How to account for all information flows in a system?

• How to construct practical systems that won’t leak?
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  ➔ Avoid taint explosion

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• How to account for all information flows in a system?
  → So that the security property can be verifiable
  → Avoid taint explosion

• How to construct practical systems that won’t leak?
  → Use the concept of GLIFT to guide the design
High-level View: Track all flows

Secure System

Separation Kernel

P0

P1

Mem

I/O Dev

CPU

S/W

H/W
High-level View: Track all flows

- Flatten design to a (giant) state machine
High-level View: Track all flows

- Flatten design to a (giant) state machine
- Does every output have desired label?

Separation Kernel

CPU

Mem

I/O Dev

Secure System

Combination Logic

Equivalent State Machine

- 1001110101111011
- 0001011001111111

External inputs

0001000101

External outputs

0010011001111111

Clock

State
High-level View: Track all flows

- Flatten design to a (giant) state machine
- Does every output have desired label?
High-level View: Track all flows

- Insight: All flows explicit at the gate level
High-level View: Track all flows

- Outputs: Logic function of state and inputs
- Output Labels: Logic func. of state, inputs, and labels
Analysis Technique: GLIFT

AND
Analysis Technique: GLIFT

AND

Shadow AND for labels
Analysis Technique: GLIFT

AND

Shadow AND for labels

Conservative.
If one of a and b is tainted, the output is tainted.
Motivation: Require Precise Information Flow

• Conventional OR-ing of labels *monotonic*
Motivation: Require Precise Information Flow

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• Conventional OR-ing of labels *monotonic*
### Precise Information Flow: AND Gate

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<thead>
<tr>
<th></th>
<th>a</th>
<th>b</th>
<th>o</th>
</tr>
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<tbody>
<tr>
<td>untainted</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tainted</td>
<td></td>
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![AND Gate Diagram](image-url)
Precise Information Flow: AND Gate

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</tr>
<tr>
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untainted vs tainted
### Precise Information Flow: AND Gate

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When \( a = 0 \), \( b \) cannot affect the value of the output. → no-interference
Precise Information Flow: AND Gate

When a=0, b can not affect the value of the output.
→ no-interference
Precise Information Flow: AND Gate

Use both inputs and input labels

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When a=0, b can not affect the value of the output. → no-interference
Analysis Technique: GLIFT
Sound Composition of Shadow Logic

[Diagram of a logic circuit with inputs s, a, b, and outputs t1, t2, o]
Sound Composition of Shadow Logic

\[ s_t a_t a s \]
\[ s_t b_t b s \]
\[ t1 \]
\[ t2 \]

\[ o_t \]
MUX: Gatekeeper of trust
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Implicit Information Flows: Taint Explosion

Diagram:
- Instr Mem
- PC
- through decode
- Reg File
- +4
- jump target
- is jump?
- R1
- R2
Implicit Information Flows: Taint Explosion

if (secret==1)
    out = 1
tmp = 5
Implicit Information Flows: Taint Explosion

if (secret == 1)  
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Reg File

R1

R2

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Conditional execution taints critical state (PC)

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Convert Implicit Flow to Explicit Flow

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P0 = secret
(P0) out = 1
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Similar Mechanisms for Loop/Load/Store

- Variable length loops $\rightarrow$ fixed size loops (bounding)
- Indirect loads/stores $\rightarrow$ Direct loads/stores
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- Recommend to read their follow-on work:
  - *Execution Leases: A Hardware-Supported Mechanism for Enforcing Strong Non-Interference*; Tiwari et al.; MICRO’09
Evaluation

+ Security
- Area overhead/Power consumption
- Performance overhead
- Programmability
Evaluation

+ Security
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- Performance overhead
- Programmability

Appropriate use cases:

• When critical or sensitive operations need to be performed, a co-processor augmented with these abilities could be an attractive option.
Discussion Questions
Discussion Questions on Taint Tracking

• Who designates an input as untrusted/trusted? Where in the architecture/implementation does an input first get marked as untrustworthy?
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• Can/should there be a method of promoting data from untrusted to trusted? (from High to Low)
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- Who designates an input as untrusted/trusted? Where in the architecture/implementation does an input first get marked as untrustworthy?

- Can/should there be a method of promoting data from untrusted to trusted? (from High to Low)

- How does the GLIFT method handle optimizations such as out-of-order execution, speculation etc? Will the proposed architecture be able to detect covert and side channel attacks such as Meltdown and Spectre?
Example MLS System

Example Satellite Application. [Tzvetan Metodi, Aerospace Corp.]
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Note: Since this is not a real schedule, the processes are not in any sensible execution order.
Example MLS System

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Interrupt Handlers (Sensitive)


Interrupt Handlers (Non-sensitive)

Primary Execution Schedule

Execution Time

Note: Since this is not a real schedule, the processes are not in any sensible execution order
Example MLS System

Example Satellite Application. [Tzvetan Metodi, Aerospace Corp.]

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Example: Satellite System
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Untrusted & Secret

Untrusted & Unclassified

Trusted & Secret

Trusted & Unclassified
Example: Satellite System

Untrusted & Secret

Untrusted & Unclassified  Trusted & Secret

Trusted & Unclassified

Kernel, Interrupt Handlers (Unclassified), Time Keeping Programs
Example: Satellite System

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Untrusted & Unclassified
Diagnostics, Telemetry Interfaces

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Trusted & Secret
Custom code on Secret data

Trusted & Unclassified
Kernel, Interrupt Handlers (Unclassified), Time Keeping Programs
Example: Satellite System

Untrusted & Secret
Libraries (e.g. encryption) that operate on Secret data

Untrusted & Unclassified
Diagnostics, Telemetry Interfaces

Trusted & Secret
Custom code on Secret data

Trusted & Unclassified
Kernel, Interrupt Handlers (Unclassified), Time Keeping Programs
Discussion Questions on Use Cases

• One specific use case: What if we needed to load in a new firmware blob to compute a new function. Could we send it in encrypted and have a way of validating and then trusting it?
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• This kind of processor would be a pain to program. If most applications on it are small, important kernels, such as AES, would it not be better to produce a specially tuned ASIC/IP core?
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• This kind of processor would be a pain to program. If most applications on it are small, important kernels, such as AES, would it not be better to produce a specially tuned ASIC/IP core?

• Are there any programs or algorithms that are rendered impossible (or extremely difficult) to write as a result of the limitations that they've placed on loops?
Discussion Questions on Future Work

• Rather than implementing a CPU with this restricted ISA, since this is used only for edge case computation, could an FPGA-based enclave in a traditional CPU be used with this ISA instead as a cost-effective implementation?
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Great idea.
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• If we do not plan to use GLIFT to track side channel leakage, do we need to ISA restriction on indirect loads? (not indirect stores)

• How GLIFT different from static taint analysis and traditional dynamic taint analysis?