

6.S078 Handout

SMIPSV2 Instruction Encoding Summary

February 17, 2012

31	26	25	21	20	16	15	11	10	6	5	0	
opcode		rs		rt		rd		shamt		funct		R-type
opcode		rs		rt		immediate						I-type
opcode		target										J-type
Load and Store Instructions												
100011		base		dest		signed offset						LW rt, offset(rs)
101011		base		dest		signed offset						SW rt, offset(rs)
I-Type Computational Instructions												
001001		src		dest		signed immediate						ADDIU rt, rs, signed-imm.
001010		src		dest		signed immediate						SLTI rt, rs, signed-imm.
001011		src		dest		signed immediate						SLTIU rt, rs, signed-imm.
001100		src		dest		zero-ext. immediate						ANDI rt, rs, zero-ext-imm.
001101		src		dest		zero-ext. immediate						ORI rt, rs, zero-ext-imm.
001110		src		dest		zero-ext. immediate						XORI rt, rs, zero-ext-imm.
001111		00000		dest		zero-ext. immediate						LUI rt, zero-ext-imm.
R-Type Computational Instructions												
000000		00000		src		dest		shamt		000000		SLL rd, rt, shamt
000000		00000		src		dest		shamt		000010		SRL rd, rt, shamt
000000		00000		src		dest		shamt		000011		SRA rd, rt, shamt
000000		rshamt		src		dest		00000		000100		SLLV rd, rt, rs
000000		rshamt		src		dest		00000		000110		SRLV rd, rt, rs
000000		rshamt		src		dest		00000		000111		SRAV rd, rt, rs
000000		src1		src2		dest		00000		100001		ADDU rd, rs, rt
000000		src1		src2		dest		00000		100011		SUBU rd, rs, rt
000000		src1		src2		dest		00000		100100		AND rd, rs, rt
000000		src1		src2		dest		00000		100101		OR rd, rs, rt
000000		src1		src2		dest		00000		100110		XOR rd, rs, rt
000000		src1		src2		dest		00000		100111		NOR rd, rs, rt
000000		src1		src2		dest		00000		101010		SLT rd, rs, rt
000000		src1		src2		dest		00000		101011		SLTU rd, rs, rt
Jump and Branch Instructions												
000010		target										J target
000011		target										JAL target
000000		src		00000		00000		00000		001000		JR rs
000000		src		00000		dest		00000		001001		JALR rd, rs
000100		src1		src2		signed offset						BEQ rs, rt, offset
000101		src1		src2		signed offset						BNE rs, rt, offset
000110		src		00000		signed offset						BLEZ rs, offset
000111		src		00000		signed offset						BGTZ rs, offset
000001		src		00000		signed offset						BLTZ rs, offset
000001		src		00001		signed offset						BGEZ rs, offset
System Coprocessor (COP0) Instructions												
010000		00000		dest		cop0src		00000		000000		MFC0 rt, rd
010000		00100		src		cop0dest		00000		000000		MTC0 rt, rd