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NESTING AND PROJECTION OF PROCEDURES IN A SIMPLIFIED MEMORY

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In this note we discuss the hardware and programming mechanisms necessary to implement the generalized nesting of procedures, where a procedure at one level may call another procedure, which may call others, and so on -- perhaps involving a call on itself (recursion). We start from the following set of assumptions.

- 1) Memory is addressed fundamentally by word addresses each consisting of a digital base and a word address. (See MAC 08-11 for an exposition of representation.)
- 2) A processor has a small finite number of general registers for performing arithmetic and logical operations on quantities, and a small finite number of attachment registers that contain segment names for making the addressing of memory more efficient.
- 3) Procedure segments are in pure procedure form that is their execution does not result in their modification.
- 4) We desire principles that will permit nesting to an arbitrary depth without alteration of conventions or technique.

Current flow may be established as a procedure does not have to know at what level in the hierarchy it will be called or what procedure it might itself call (names of procedures might be supplied as parameters).

An Example

As an example of what can happen, suppose we are given the procedures $Ff()$, $Gg()$, and $Hh()$, having the structure shown in Figure 1. For simplicity we suppose that these procedures are not used as functions. That is, the names of the procedures do not appear in the left hand of assignment statements with a colon bodies.

We restrict the parameters of a procedure to be any objects representable as a single word - e.g., a single quantity, or the word name of a word that is either single quantity, the entry point of a procedure or the word name of another word. A parameter used by one procedure in calling another may be one of the parameters by which it itself was called.

In our example, procedure $Ff()$ has three parameters, X , Y and Z . It contains a direct reference to cd , references to private variables p and q , and calls a three parameter procedure $Gg()$ with the following actual parameters: (1) the parameter X , (2) the name y of a private variable, and (3) the parameter Z . Procedure $Gg(X, y, Z)$ uses its parameter Z as the name of a procedure that it calls with the following actual parameters: (1) the parameter Y , and (2) the parameter cd . A third procedure $Hh(X, Y)$ calls Ff as a two parameter procedure with the actual parameters X and Y . In our illustration of mechanisms for handling communication among procedures we consider the consequences of a call on $Ff()$ with the following as actual parameters: (1) the name of the word Zx ; (2) the name of the procedure Hh ; and (3) the name of the procedure Hh .

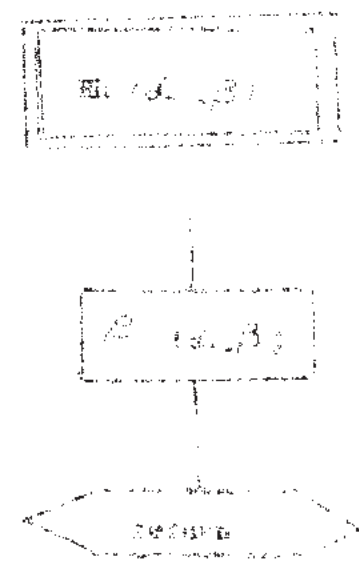
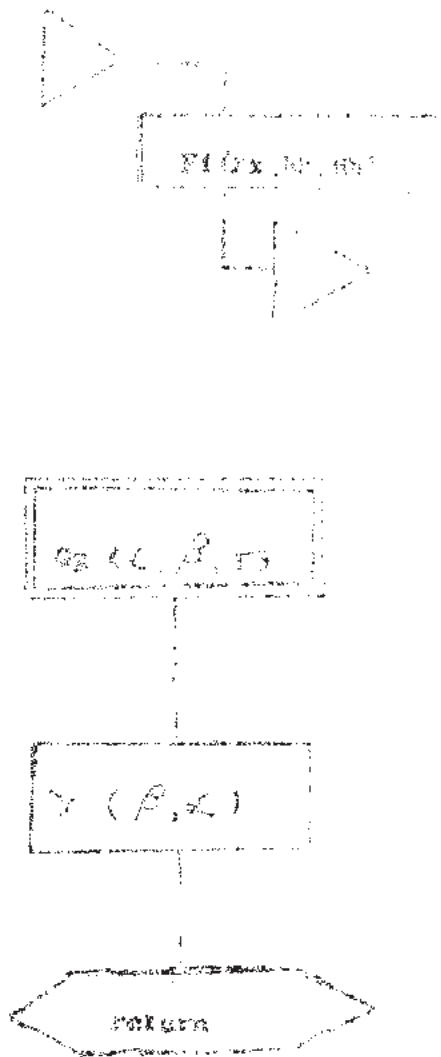


Figure 1 - An example of neural network

Segmentation

To keep the discussion general, we shall assume that each procedure is coded into a subroutine which enters into a particular procedure segment. We further suppose that each segment is coded as a push down stack for holding return addresses and other data that is private to a particular call upon a procedure. The code for a procedure to be in yet another segment.

The Stack Pointer

The push down stack must be private to the particular process executing the nested procedure. A stack pointer must be associated with the process to indicate which quantities in the stack are pertinent to the procedure whose instructions are currently being executed. We choose to have the stack pointer indicate the first quantity in the stack which is pertinent to the current procedure. Each time a new subroutine is entered, the stack pointer is increased to point to the first location in the stack that is not used by the calling procedure. Each time a subroutine returns, the stack pointer is restored to the value which it had immediately prior to that subroutine's call.

Conveyance of Parameter Information

In the remainder of this note, we distinguish between a subroutine's actual parameter information, and a subroutine's actual parameters themselves. Generally a subroutine must execute some sort of addressing algorithm in order to obtain its actual parameters. This addressing

algorithm generally requires the subroutine to fetch certain intermediate linkage information in order to locate its actual parameters. The first of these linkage words that a subroutine examines which contains information unique to a particular parameter is said to contain the parameter information for that parameter.

We consider three methods by which parameter information may be conveyed between a calling pure procedure subroutine and a called pure procedure subroutine.

- 1) Stacking - The calling subroutine places parameter information in the stack segment following the word that the stack pointer will point to upon entry to the called subroutine.
- 2) Followers* - Parameter information is placed within the calling procedure segment immediately after the procedure call instruction.
- 3) Operand registers - Parameter information is placed in the operand registers of the processor by the calling subroutine.

It is possible to use one, two, or all of these methods during a given calculation. Our object here is not to describe an optimum method of parameter linkage, but to characterize some of the possible methods. We will therefore restrict our attention to schemes which rely solely on one of the three methods mentioned above.

The stacking technique is straightforward and well known from its use in interpreters for algebraic languages. The techniques of followers and operand registers are in general use in conventional machine language coding. To our knowledge, the provisions necessary for the general

* After A.A. Smith

application of the follower technique to pass parameters during the call and
unlike case, data parameters.

Certain characteristics of the stacking and follower techniques are
apparent without much consideration. If the parameter information is
stacked, then all forms of information can be transmitted in binary
quantities modified by the operation of the procedure whereby the
information is imbedded in pure procedure coding, then the instructions
cannot be so modified. In particular, the information in the following
cannot be argument names as these are discarded at execution of the call.
On the other hand the stacking of parameter information requires the calling
procedure to move information into the stack prior to the call. This leads
to extra procedure steps that increase execution time and occupy memory.
Followers offer the possibility of reducing the memory space required to
transmit parameter information, provided a suitable addressing mechanism
can be formulated.

The method of passing parameter information through operand registers
is conceptually the simplest of the three methods. Each subroutine can
be written to pick up information about its first parameter in a particular
operand register, information about its second parameter in another
particular operand register, etc. If a certain subroutine's particular
linkage registers are being used to hold other quantities at the time when it
is called, then the calling subroutine must save, in other operand registers
or in the stack, the contents of these linkage registers before loading
them with appropriate parameter information. After the called subroutine

returns, the calling subroutine usually releases these quantities into their former registers. Since the number of operand registers is generally on the order of 10, these stackless operations occur quite frequently in a procedure with moderate depth entry. This fact makes the method of operand registers not much more efficient than the stacking method. Moreover, information about only a small number of parameters can be passed through operand registers.

In the remainder of this note we will examine the problems involved in the implementation of the stacking and follower mechanisms in the context of segmentation.

Addressing of Actual Parameters

Having listed three methods of transmitting parameter information, we now turn our attention to the nature of the information which is transmitted. We again consider, by coincidence, three addressing alternatives:

- 1) Immediate - the transmitted information is the parameter itself.
- 2) Direct - the transmitted information points to the parameter.
- 3) Indirect - the transmitted information points to a chain of indirect words which leads to the parameter.

In general, each of these three addressing techniques may be used with either the stacking or the follower transmission methods. However, immediate addressing and the follower method are incompatible in a pure procedure context, because under these circumstances the actual parameters of each procedure call cannot be changed by the calling procedure in accordance with its own actual parameters.

Addressing Segments Within a Procedure

We consider now a sub-problem of the problem of addressing actual parameters, namely the problem of enabling a procedure to access segments whose names are unknown to it prior to a call by another procedure.

This may be done by either of the following two methods:

- 1) Name passing - Segment names are passed as parameters.
- 2) Tag passing - Attachment tags are passed as parameters.

The name passing technique is perfectly general. In a procedure having n attachment registers, the tag passing technique is subject to the following restrictions.

- 1) The actual parameters of each procedure may reside in no more than n different segments.
- 2) In a computation involving more than n segments, subroutines may have to save and restore the contents of some of the attachment registers before calling other subroutines.

Summary

Figure 2 summarizes the various combinations of techniques which have been discussed thus far. The rest of this note will be devoted to detailed examples of three implementations of the procedure nest diagrammed in figure 1. These three implementations are: (1) stacking with direct addressing and name passing, (2) stacking with indirect addressing and tag passing, and (3) followers with direct addressing and name passing.

		Stacking	Followers	Operands Registers
Name Passing	Immediate		impossible for pure procedure	
	Direct	first detailed example	third detailed example	
	Indirect			
Tag Passing	Immediate		impossible for pure procedure	
	Direct			
	Indirect	second detailed example		

Figure 2: Summary of methods discussed

Operand Register Conventions

For generality we assume that each procedure is coded independently and without regard to the coding of the other procedures except according to well defined conventions. Conventions regarding the use of operand registers and attachment registers, therefore, must apply uniformly over all procedures that might be coded. The following conventions are made here and are examples of what is permissible.

- 1) Attachment register 0 contains the name of the stack segment.
- 2) Index register 0 contains the word address which is the stack pointer.

A further convention is made (although it is not essential as will be seen) regarding the use of processor registers for transmitting the return address (the word name of the procedure entry instruction) to the called procedure.

- 3) Attachment register 1 conveys the segment name of the calling procedure.
- 4) Index register 1 conveys the word address of the calling instruction in the calling procedure.

In the third detailed example, the following additional convention will be introduced.

- 5) Index register 3 conveys the word address which is the base stack address (defined below) of the calling procedure.

As with conventions 3) and 4), convention 5) is not essential, but is introduced for convenience only.

Addressing Notation

We use upper case letters to represent segment names as follows:

P, Q, R - procedures P(), Q(), and R()

S - push down stack

M - main procedure

X - segment containing the public variable X

Lower case letters such as l, p, v represent the word address of objects. The notation

A/b

represents the word name consisting of the segment name A and the word address b. The attachment tags are written as a0, a1, a2, ... while x0, x1, x2, ... represent the content of index registers. An address word

a1/b

consists of an attachment tag a1 and a word address b. The notation

[a1/b]

represents the word addressed by the address word. For convenience we will sometimes write <A> to mean the attachment tag of an attachment register containing the segment name A. We presume the existence of an instruction (or macro) of the form

attach S, a0

that causes the segment name S to be placed in attachment register a0 if S is valid in the sphere of protection of the current procedure. The names of private variables of a procedure (such as p and q in our examples) the letters represent the words themselves.

Certain processor registers must be identified, namely those that contain the address word of the current procedure step (or frame pointer).

the stack pointer register is decremented by the number of words in the argument list and the stack pointer register is incremented by the number of words in the argument list.

Organization of the Stack Frame

Let the stack frame of a procedure be divided into the following fields:

1. the stack pointer register value at the time of the procedure call
2. the argument list of the calling procedure
3. the return address of the calling instruction to the calling procedure

Words 3, 4, ... relative to the base stack address contain the parameter information for the actual parameters of the call. Subsequent registers are used for private variables required by the called procedure. The (frame-relative) word address of the first four words in the stack segment is the base stack address for any procedure called by the caller.

Return from Procedure

The subroutine entry instruction (or macro) takes the following form:

$M(n), \quad \text{CALL} \langle X \rangle, \quad \text{CALL}$

Here $M(n)$ and X are the word address of the n -th instruction in the called procedure and the return address to the procedure $M(n)$ respectively. The CALL instruction is the instruction in the stack pointer register.

operation of the `<return>` instruction is as follows:

i) Save the stack pointer of the new frame address:

$$sp \rightarrow [sp/4 + 1]$$

ii) Increment the stack pointer:

$$sp \rightarrow sp + 4$$

iii) Save the return word name:

return name:

$$[sp] \rightarrow [a1]$$

word address:

$$PWA \rightarrow a1$$

iv) Establish contents of the subroutines:

$$\langle r \rangle \rightarrow PWA$$

$$r \rightarrow PWA$$

Before calling another procedure, `<return>` must enter the return word name in the stack as private data, for example:

$$[a1] \rightarrow [sp/4 + 1]$$

$$a1 \rightarrow [sp/4 + 2]$$

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The reverse must be performed before returning to the main program:

$$[sp/4 + 1] \rightarrow [a1]$$

$$[sp/4 + 2] \rightarrow a1$$

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The `<return>` instruction performs the following steps:

i) Take up stack pointer:

$$[sp/4] \rightarrow sp$$

ii) Reverse contents of the calling procedure:

$$[a1] \rightarrow [PWA]$$

$$a1 \rightarrow PWA$$

The program is designed to calculate the value of the function $f(x) = \frac{a_0}{x^0} + \frac{a_1}{x^1} + \frac{a_2}{x^2} + \frac{a_3}{x^3} + \frac{a_4}{x^4} + \frac{a_5}{x^5}$ for a given value of x and coefficients $a_0, a_1, a_2, a_3, a_4, a_5$.

Listing

The program is written in the following form. It shows the calculation of the function value for a given value of x and coefficients $a_0, a_1, a_2, a_3, a_4, a_5$.

Main Program

```

N/y, ans
      a0/a0 + 1.0
      a1/a1 + 1.0
      a2/a2 + 1.0
      a3/a3 + 1.0
      a4/a4 + 1.0
      a5/a5 + 1.0
      ans = a0/a0 + a1/a1 + a2/a2 + a3/a3 + a4/a4 + a5/a5
N/y, ans
      quit
  
```

Figure 3. Simulation of the program.

YIP...

P/E,

attach 6, 01

enter a2/s, 11

[a0/x0 + 3] + [a0/x0 + 10] = [a0/x0 + 13]

[a0/x0 + 5] → [a0/x0 + 6]

[a0/x0 + 5] → [a0/x0 + 13]

[a0] → [a0/x0 + 10]

x0 + 9 → [a0/x0 + 10]

[a0/x0 + 7] → [a0/x0 + 13]

[a0/x0 + 11] → [a0/x0 + 13]

attach 6, 01

P/a,

enter a2/s, 11

return

Figure 3 - continued

Procedure 07 A)

G/L



[a0/60 + 50] → [a0/60 + 10]
[a0/60 + 50] → [a0/60 + 10]
[a0/60 + 10] → [a0/60 + 10]
[a0/60 + 10] → [a0/60 + 10]
attach [a0/60 + 10] . a1

G/L, enter a1 [a0/60 + 50] . 0



return

attach (a0/x0 + 3);

R/a.

[a0/x0 + 3] → [a0/x0 + 3],
[a0/x0 + 4] → [a0/x0 + 4],
[a0/x0 + 5] → [a0/x0 + 5],
[a0/x0 + 6] → [a0/x0 + 6]

attach (a0/x0 + 5); a0

R/a.

enter a2/x0 + 6); 7

...

...

return

Figure 3 - (continued)

The Second Detailed Example - Storing PC, PC+4, and PC+8 in Register 5
Tag Allocation

We suppose that attachment tags are allocated by the compiler's
embedding in procedure. All other tags used by the compiler are
obtained by use of the meta-instruction

obtain 3 → a

that loads an available attachment register with the tag of the entry point
has the corresponding attachment tag as its value. The meta-instruction

release 5

releases the attachment register associated with the comment named 5.

We introduce one additional notation convention: denoting an
address word by an asterisk

$a0/(x0 + 4)*$

means that the addressed word is itself an address word - starred or
unstarred - that is to be used to fetch an operand (indirect addressing).

Organization of the Stack Segment

With tag passing the stack is somewhat simplified. Instead of storing
the word name of the entry instruction in registers 1 and 2 above the base
stack address, we simply store the address word of the entry point in register
1 above the base. The <enter> and <return> macros now become

M/a, enter a/b,

1) $x0 \rightarrow [a0/(x0 + 4)*]$

11) $x0 \leftarrow \Delta \rightarrow x0$

111) $PAT/PWA \rightarrow [a0/(x0 + 1)*]$

112) $a/b \rightarrow PAT/PWA$

Example

- i. $u^2 + 2u + 1 = (u+1)^2$
- ii. $u^2 + 2u + 1 = (u+1)^2$
- iii. $u^2 + 2u + 1 = (u+1)^2$

Coding

The coding of the example is given in figure 2. The condition of the stack just after the first step is the same as the condition of the stack just after the second step. The condition of the stack just after the third step is the same as the condition of the stack just after the second step.

5

Table of Contents

M/w,

0 - 20

(00000000 00000000) 00000000

(00000000 00000000) 00000000

< 00000000 (00000000 + 00000000)

M/w,

enter (00000000,0)

release X

release B

release F

quit

Figure 5 - Second detailed example

Procedure (a)

```

      .....
      .....
      a0/20 = 1/2 * (a0/10 + a0/30)
      End: a0 = 1/2 * (a0/10 + a0/30)
      .....
      a0/20 = 1/2 * (a0/10 + a0/30)
      a0/20 = 1/2 * (a0/10 + a0/30)
      a0/20 = 1/2 * (a0/10 + a0/30)
      .....
      End: a0 = 1/2 * (a0/10 + a0/30)
      .....
      End: a0 = 1/2 * (a0/10 + a0/30)
      End: a0 = 1/2 * (a0/10 + a0/30)
  
```

Procedure (b)

```

      .....
      .....
      a0/20 = 1/2 * (a0/10 + a0/30)
      a0/20 = 1/2 * (a0/10 + a0/30)
      .....
      End: a0 = 1/2 * (a0/10 + a0/30)
      .....
      End: a0 = 1/2 * (a0/10 + a0/30)
      End: a0 = 1/2 * (a0/10 + a0/30)
  
```

Procedure (c)

```

      .....
      .....
      a0/20 = 1/2 * (a0/10 + a0/30)
      a0/20 = 1/2 * (a0/10 + a0/30)
      .....
      End: a0 = 1/2 * (a0/10 + a0/30)
      .....
      End: a0 = 1/2 * (a0/10 + a0/30)
      End: a0 = 1/2 * (a0/10 + a0/30)
  
```

Figure 5 (continued)

6. Terms relative
 to state base

Year	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	
1																						
2																						
3																						
4																						
5																						
6																						
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Figure 6 - Condition of the state in the period 1960-1980

The Third Detailed Example - Subroutine with Stack Addressing on IAS - Part 2

Organization of the Stack Segment

The stack segment is organized in this example as follows in the next example.

Subroutine Entry

In this example we will introduce (for convenience, the customary convention that upon subroutine entry it contains the base stack address of the calling subroutine). Also, in this example, as a convention we use a return instruction which specifies a memory location to be used as the return word address so that control can be returned to the instructions following the following.

To accomplish these two objectives, we let the entry instruction be identical to that used in the first example, except for the following additional step after step 1):

$x0 \rightarrow x3$

We postulate a new return instruction,

return $\{$

which performs the following steps

1) unless the return flag is set:

$[a0/x0 + 1] \rightarrow [a1]$

$[a0/x0 + 1] \leftarrow \frac{1}{2} [a1]$

2) back up the stack pointer

$[a0/x0] \leftarrow x0$

134. Restore the original stack pointer:

$[a0/x0] \rightarrow x0$

135. Resume execution of the calling subroutine:

$[a] \rightarrow [PAA]$

$x1 \rightarrow PWA$

Addressing of Parameters

In this example, the following gives each parameter a unique location in the stack region of the called subroutine's stack parameters relative to the base stack address of the calling subroutine.

Comparison with the First Detailed Example

The first and third examples both show parameter information being moved from one location in the stack to another at each call. However, in the third example, the coding which does this exists in the caller's subroutine, and hence exists only once in storage for each subroutine. In the first example, the coding to do this movement must exist in storage for as many times as the subroutine is called. Looking at it another way, if a subroutine calls several other subroutines, it need only get data from its callers' register of the stack only once. It then delivers this information to other routines by sequential, starting pointers in the followers of the call. Of course these followers save up data, but not as much as the coding necessary to perform the data movements that would be necessary on each call in the first example. Hence we see that the method of the third example consumes less storage than the method

of the first operand is determined by the number of registers used in the other procedures.

Figure 7 compares the number of stack cycles for different parameters under various criteria of which characteristics are given. We see that the number of stack cycles is lower for the first three registers.

Position of parameter in call of procedure

		Stack	Operand Register
Position of parameter in called subroutine	Stack	ax 1 - 2	ax 1 - 1
	ax	ax 1 - 3	ax 1 - 3
Operand Register	ax 1 - 1	ax 1 - 1	ax 1 - 2
	ax 1 - 2	ax 1 - 2	ax 1 - 3

Figure 7 - Number of stack cycles for parameter transmission in example 1 and 3.

code:

The code of this example is given in Figure 8. Figure 8 shows the condition of the stack just after P02 has been reached for the second time. Notice the similarity of the stack condition to that of examples 1 and 2.

Main Procedure

```
W/O,   0 -> x0
        x -> [x0/x0]
        x -> [x0/x0 + 1]
        W/O, [x0/x0 + 2]
        x -> [x0/x0 + 3]
        attach P, 02
W/O,   enter #2/P, 0
        0
        1
        2
        3
        4
        5
        6
        7
        8
        9
        quit
```

Figure 8 - Third detailed example

Procedure Y11

P/E

$$[a0/x0 + [a1/(x0 - 1)] - a2] \rightarrow [a0/x0 + 3a2]$$

$$[a0/x0 + [a1/(x0 - 1) - a2]] \rightarrow [a0/x0 + 4a2]$$

$$a1/x0 [a0/x0 + 3a2] \rightarrow a2$$

$$[a2(a0/x0 + 3a2)] \rightarrow [a0/x0 + 3a2]$$

$$[a0/x0 + 3a2] \rightarrow [a0/x0 + 10a2] \rightarrow [a0/x0 + 4a2]$$

$$[a0] \rightarrow [a0/x0 + 1a2]$$

$$x0 = 3 \rightarrow [a0] [a0 + 3a2]$$

diffsch G. a2

P/a

enter a2/g. 11

5

6

11

11

7

8

TABLE 1

Figure B - (continued)

Figure 1 (continued)

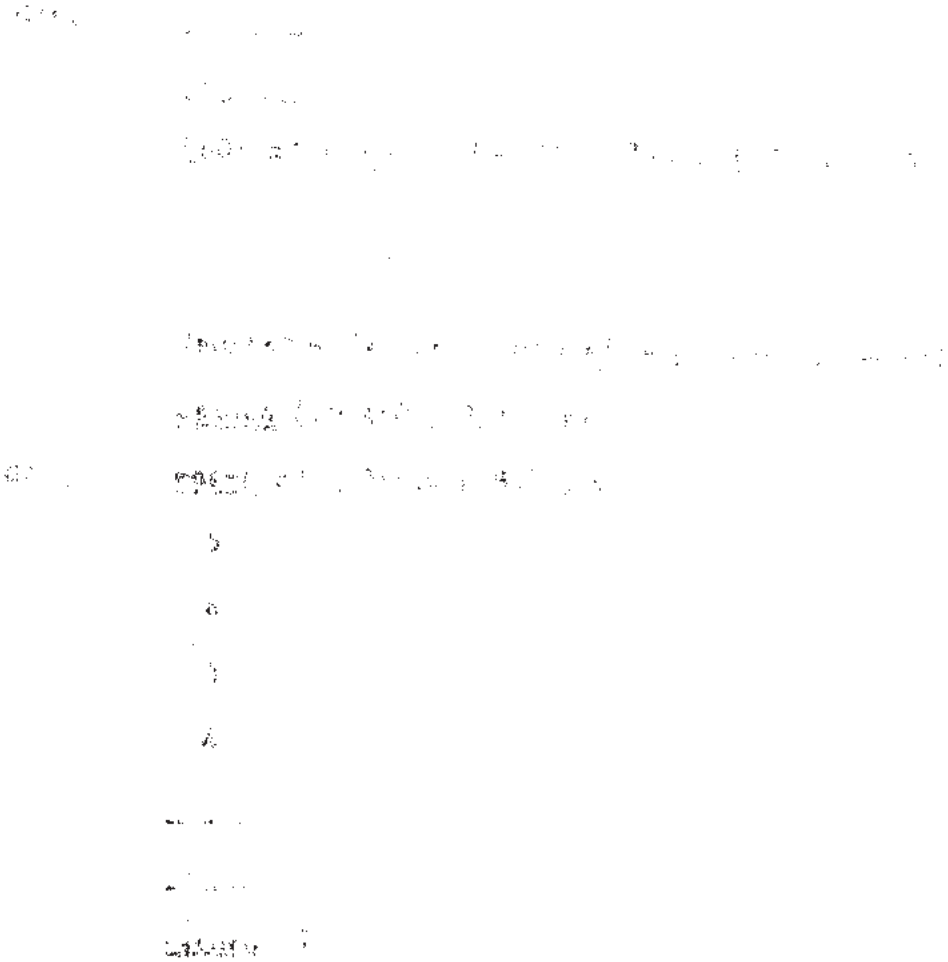


Figure 2 (continued)

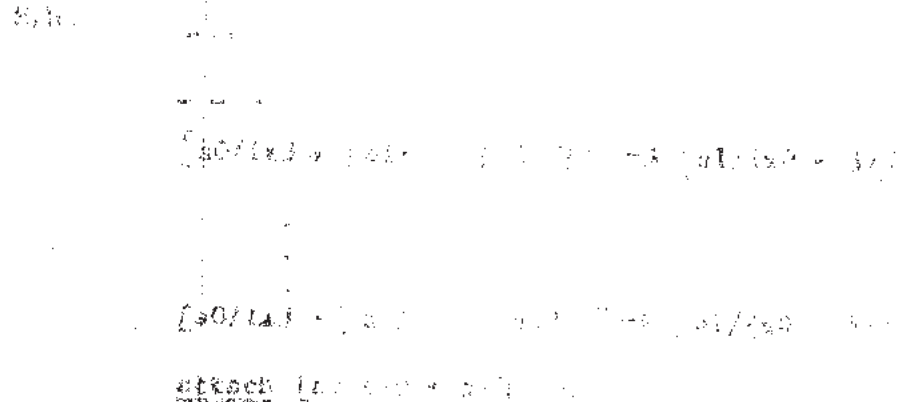


Figure 2 (continued)

```
H/u,   enter [a2 [a0/(x0 + 6)] , 7
        3
        4
        5
        6
        - - -
        - - -
        return 5
```

Figure 8 - (continued)

stack word address

address relative to stack base

contents

					0		
					1		
					2		
					3		
					4		
					5		
					6		
					7		
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					44		
					45		
					46		

Figure 9 - Condition of the stack in the third detailed example