FFT Compiler:
From Math to Efficient Hardware

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joint work with Peter A. Milder, Franz Franchetti, and Markus Pueschel in the SPIRAL project

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The SPIRAL Project

♦ High performance implementations of linear DSP transforms (DFT, DCT, DWT, filters, etc) are an important class of design problems

♦ Hand design and tuning is tricky and expensive
  - needs both math and implementation knowledge
  - time-consuming and tedious
  - needs to repeat effort for every new context

♦ SPIRAL research goal: A flexible push-button design generation framework that produces SW and HW implementations equal or better than expert hand design
  Today I focus on FFT for HW
Why we can do better than hand design

♦ SPIRAL is only focused on linear DSP transforms

♦ These transforms are highly structured, highly regular and very well understood mathematically

♦ Algorithmic implementations of a transform can be enumerated following a known set of rules

♦ For a given objective function and mapping target, a computer generates a solution at least as good as the best human effort—by trying enough implementations

Outline

♦ SPIRAL Formula Framework

♦ SPIRAL for HW FFT cores

♦ Conclusions
Linear Transforms

- Linear transform is matrix-vector multiplication
  - computing by definition takes $O(N^2)$ operations
  - the matrix has structure

- E.g. discrete Fourier transform: $y = DFT_N \cdot x$

  $y_0$
  $y_1$
  $\vdots$
  $y_j$
  $\vdots$
  $y_{N-1}$

$ = \begin{bmatrix}
  x_0 \\
  x_1 \\
  \vdots \\
  x_k \\
  \vdots \\
  x_{N-1}
\end{bmatrix} \cdot \begin{bmatrix}
  k \rightarrow 0 \ldots N-1 \\
  j \rightarrow 0 \ldots N-1 \\
  e^{-i2\pi jk/N}
\end{bmatrix}$

“Fast” Algorithms

- a “fast” algorithm factors the matrix into a sequence of structured, sparse matrices
  - cheaper sparse multiplies $\Rightarrow O(N \log(N))$ operations

- E.g. Cooley-Tukey Factorization of $\text{DFT}_4$

$ = \begin{bmatrix}
  1 & 1 & 1 & 1 \\
  1 & i & -1 & -i \\
  1 & -1 & 1 & -1 \\
  1 & -i & -1 & i
\end{bmatrix} = \begin{bmatrix}
  1 & 1 & 1 & 1 \\
  1 & -1 & 1 & -1 \\
  1 & -1 & 1 & -1 \\
  1 & 1 & 1 & 1
\end{bmatrix} \cdot \begin{bmatrix}
  1 & 1 & 1 & 1 \\
  1 & -1 & 1 & -1 \\
  1 & -1 & 1 & -1 \\
  1 & 1 & 1 & 1
\end{bmatrix}$

Matrix formula representation

\[ DFT_{n \times m} = (DFT_n \otimes I_m) D_{n \times m} (I_n \otimes DFT_m) L_{n \times m} \]
“Fast” Fourier Transform Algorithms

- Recursively factorize by the Cooley-Tukey rule until only leaf cases remain (e.g. $DFT_r$ for radix-$r$)

$$DFT_8 = (DFT_2 \otimes I_4)D_2^8(I_2 \otimes DFT_4)L_2^8$$

$$= (DFT_2 \otimes I_4)D_2^8(I_2 \otimes (DFT_2 \otimes I_2)D_2^4(I_2 \otimes DFT_2)L_2^4)L_2^8$$

- Exponential number of alternatives

- Each rule tree corresponds a different algorithm
- All cost $O(N \log(N))$

Formula to HW (Combinational)

- Given $y = M \cdot x$ where $M$ is:
  - $M = A \cdot B$ apply $B$, then $A$
  - $M$ is a permutation permute $x$
  - $M = I_n \otimes A$ apply $A$, $n$ times in parallel
  - $M$ is a diagonal scale $x$

$$y = (A \cdot B) \cdot x$$

$$y = (I_2 \otimes A) \cdot x$$

$$y = (I_2 \otimes A) \cdot x$$
How about good HW?

♦ Matrix formulas have a natural mapping to dataflow and hence combinational datapath

♦ However, real hardware designs must fit a given resource constraint
  ⇒ sequential datapath that reuse available HW
  - identify repeated kernels
  - instantiate kernels under resource constraints
  - schedule computation to reuse instantiated kernels

We want to do the analysis, mapping and scheduling at formula level, with high-level algorithm knowledge

Regular Structure for HW

♦ Simple regular structure embodied in Pease FFT

\[
DFT_{2^k} = R_{2^k} \left( \prod_{i=0}^{k-1} T_i (I_{2^{k-1}} \otimes F_2)L_{2^{k-1}}^{2^k} \right)
\]

♦ Example:

\[
DFT_8 = R_8 \left( T_0 (I_4 \otimes F_2)L_4^8 \right) \left( T_1 (I_4 \otimes F_2)L_4^8 \right) \left( T_2 (I_4 \otimes F_2)L_4^8 \right)
\]
Pease DFT Example: $\text{DFT}_8$

$$\text{DFT}_8 = R_8 \cdot T_3(I_4 \otimes F_2)L_4^8 \cdot T_1(I_4 \otimes F_2)L_4^8 \cdot T_0(I_4 \otimes F_2)L_4^8$$

(formula is applied from right to left)

Horizontal folding

- a baseline datapath for DFT (sans bit-reverse)
- degree of freedom: vertical parallelism
  - parameter $p$
Vertical (V-)folding according to $p$

$p = 1, 2, 4, \ldots n/2$

$\text{cost} \propto p \quad \text{latency} \propto \frac{1}{p}$

Fine-grained control over cost/latency tradeoff

DFTgen [Milder, et al., DAC’05, FPGA’06]

<table>
<thead>
<tr>
<th>parameter</th>
<th>value</th>
<th>range</th>
<th>usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>2048</td>
<td>4–16384</td>
<td>DFT size [2]</td>
</tr>
<tr>
<td>data width</td>
<td>16</td>
<td>4–32</td>
<td>dataset width, fixed point precision [3]</td>
</tr>
<tr>
<td>twiddle width</td>
<td>16</td>
<td>2–16</td>
<td>twiddle factor bitwidth [4]</td>
</tr>
<tr>
<td>data ordering</td>
<td>bit-reversed out</td>
<td></td>
<td>bit-reversed input or output [5]</td>
</tr>
<tr>
<td>scaling mode</td>
<td>unscaled</td>
<td></td>
<td>unscaled or scaled arithmetic [2]</td>
</tr>
<tr>
<td>$p$</td>
<td>1</td>
<td>1–1024</td>
<td>degree of parallelism [3]</td>
</tr>
<tr>
<td>twiddle storage</td>
<td>block RAM</td>
<td></td>
<td>store twiddles in dist. RAM or BRAM [2]</td>
</tr>
<tr>
<td>FIFO threshold</td>
<td>Select</td>
<td>2–1024</td>
<td>FIFO of $p$ depth will be built as BRAM [2]</td>
</tr>
</tbody>
</table>

Core characteristics and resource usage (dynamically updated)

<table>
<thead>
<tr>
<th>char./rec.</th>
<th>value</th>
<th>how obtained</th>
</tr>
</thead>
<tbody>
<tr>
<td>cycles</td>
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<td>exact formula</td>
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<tr>
<td>size</td>
<td>876</td>
<td>estimated with linear fit formula</td>
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<tr>
<td>BRAM</td>
<td>44</td>
<td>exact formula</td>
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<tr>
<td>multipliers</td>
<td>4</td>
<td>exact formula</td>
</tr>
<tr>
<td>num. error</td>
<td></td>
<td>to be implemented</td>
</tr>
</tbody>
</table>
Cost Performance Tradeoff

![Graph showing latency versus slices for DFT64, DFT256, and DFT1024]

Structures of Interest for Parameterized Cores

- Simple regular structure embodied in formula
  \[ DFT_{2^k} = R_{2^k} \left( \prod_{i=0}^{k-1} T_{2} \otimes F_{2} \otimes L_{2^{k-1}} \right) \]
- Product: Horizontal folding
- Tensor Product: parallelism or streaming vertical folding
- Stride permutation: rewiring or buffer/delay
Applicability to other transforms?

- DFT radix 2
  \[ R^{k-1}_{2^k} \prod_{i=0}^{k-1} \left( T_i \left( I_{2^{k-1}} \otimes DFT_{2^1} \right) L^{2^1} \right) \]

- DFT radix 2^r
  \[ R^{k/r-1}_{2^k} \prod_{i=0}^{k/r-1} \left( T_i \left( I_{2^{k/r}} \otimes DFT_{2^r} \right) L^{2^r} \right) \]

- 2-D DFT_{nxn}
  \[ \prod_{i=0}^{1/n} \left( L^{2^i} \left( I_{n} \otimes DFT_{n} \right) \right) \]

- WHT
  \[ \prod_{i=0}^{k/r-1} \left( I_{2^{k/r}} \otimes WHT_{2^r} \right) L^{2^r} \]

- DCT (type II)
  \[ DP \prod_{i=0}^{k-1} \left[ A_{k-i} \cdot L^{2^i} \right] L^{2^{k-1}} L^{2^{k-1}} P^H \]

Conclusions

- Mathematical approach to DSP transform implementation

- Encapsulating domain knowledge in a domain specific tool for **100% automatic** design generation and optimization

- Generalizable to other linear DSP transforms

- Thank you (Arvind)