IBM T. J. Watson Research Center

The PowerPC Models in Bluespec

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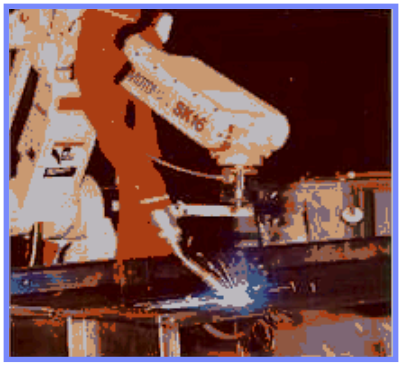
PowerPC Architecture Spans Wide Range of Markets

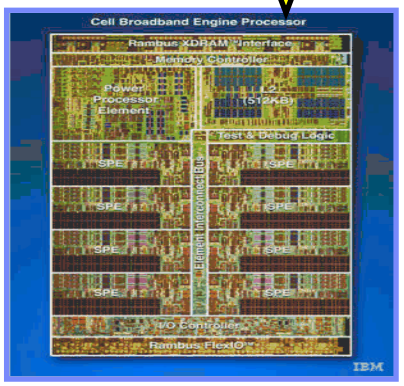


embedded systems

automotives

game consoles

power architecture



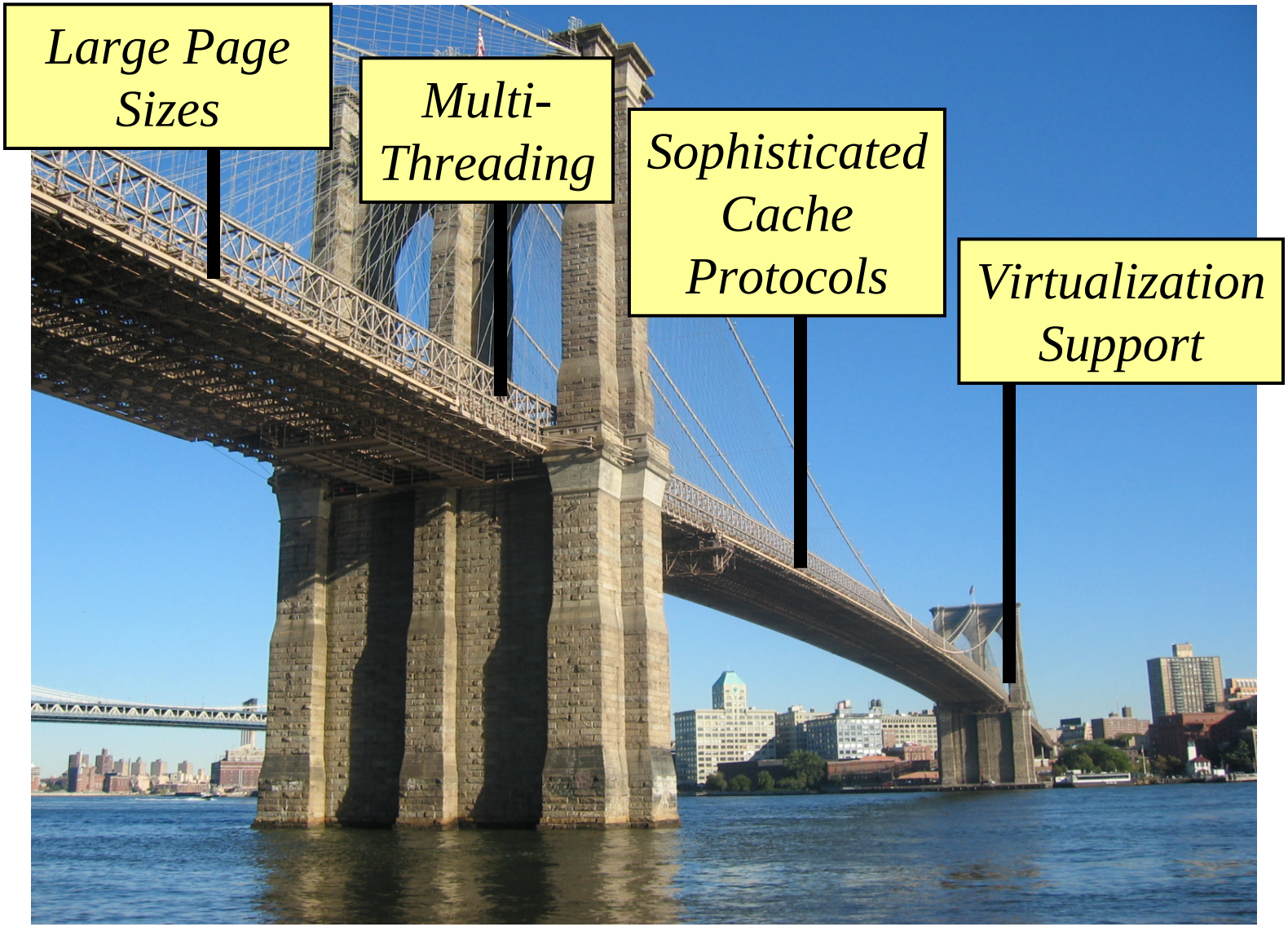
cell broadband engine

servers

journey to mars

super computers (BG/L)

Flexible Support Structures For Software



Our Research Goal and Vision

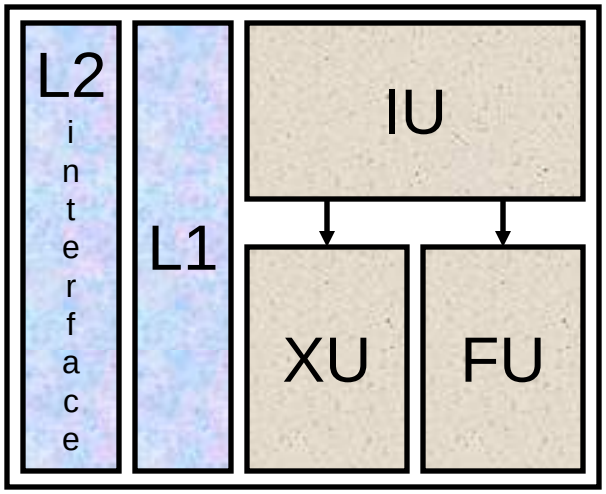
- **Goal:**
  - Promote Power architecture as building block for a wide range of systems and find innovative ways to extend Power architecture with accelerator for specific applications.
- **Vision:**
  - Create an ecosystem to foster Power architecture and ese of its use for system research by the community.

Bluespec PowerPC Processor Model

- **Since Bluespec advertises itself as a high-level synthesis solution that can reduce the design and modeling times, it is ideal for rapid design changes and experimentations.**
  - Collaborate with MIT to create a public PowerPC ISA compatible core from the public available documents (Book I, II, and III) using Bluespec.
  - Further synthesize the Bluespec generated verilog code onto FPGAs for real-time evaluation and simulation.

The Basic PowerPC Processor Model

- **Simple in-order pipeline, with standard PowerPC ISA.**
- **Support for multiple threads per core.**
- **Support for address translation with variable page sizes.**
- **Support for multiple cores with shared caches in a node.**
- **Support for coherency and synchronization across nodes.**



Thank you!

