Bluespec at Qualcomm

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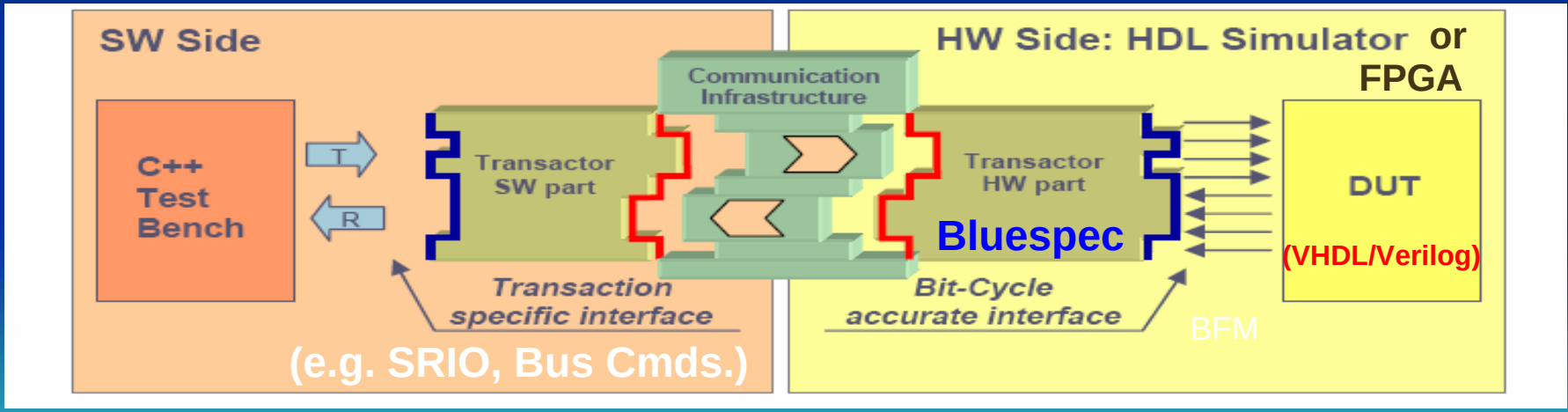
From Eval to Production

- Bluespec provided training:
  - 6 month long eval with several onsite visits by Steve Allen
  - Followed by management visits by Bob and Shiv
- The eval resulted in an integrated flow with the EVE's FPGA platform
- MIT provided training/interns:
  - Lecture series by Prof. Arvind on Bluespec semantics
  - Interns from MIT (Alfred and Abhinav)
- Currently using Bluespec to develop bus level transactors to interface with the Qualcomm RTL-IP

Bus Performance Modeling

- Hardware part of the transactor is written in Bluespec
  - EVE provides inport, outports and clock control mechanisms
  - Bluespec provided all the wrappers for EVE's infrastructure IP
- Software part of the transactor is written in SystemC
  - Threads manage bus concurrency
  - Untimed transaction level models of traffic generators, score boards etc.



HW Transactor in Bluespec

- HW transactor makes maximum use of
  - Bluespec library components
  - Bluespec interface semantics
  - Guard conditions etc.
- To model
  - valid/ready handshake
    - between s/w testbench and h/w transactor
    - between h/w transactor and the DUT
  - Control advancement of the DUT clock
  - Clock synchronization between the DUT clock and the user clock
  - Multiple instantiations of xactors (masters, slaves, etc.)
  - Sharing a resource in multiple rules in the same clock cycle (EHRR)
  - Wrappers to existing DUT-RTL code
- Designing a transactor is almost becoming like a software design experience

From production to Deployment

- Deployment aids
  - Training, tutorials, primers, examples, bill boards
  - Work with the experienced Bluespec/RTL engineers (clone Bluespec Inc.)
  - Bluespec Wikipedia (Google search for EHRR?)
  - Bluespec Workshops (like this one! Every 6 months?)
  - Standardize Bluespec/EVE at universities
- Main challenge
  - Establishing a new comfort zone beyond RTL and HVL
  - How far can we go with Bluespec?

Top-Down Modeling Flow