MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Project MAC

Computation Structures Group Memo No. 40

Macro-modular Circuit Design

Suhas S. Patil

May 1969

This memo is identical to a 6.232 memo entitled "Macromodular Circuits Design" dated February 1968.

INTRODUCTION

Most of the computer hardware designed so far has been synchronous in character. Synchronous hardware employs a central clock which times all the activities taking place in the machine. This requires complete management of the timing between different actions and between different parts. One reason why synchronous approach to hardware design has been so popular is that one knows precisely what is happenning at each place at every instant of time and therefore races and other problems can be easily removed. Even though this approach is simple for small machines its complexity grows very rapidly with the size of machine. Another great draw back of this method is that two fault free machines can not be easily connected together to form a bigger fault free machine. Asynchronous circuits on the other hand have no clock and instead proper timing is obtained through local constrains. Therefore it is much easier to connect more than one machine together to form a bigger fault free machine.

With increasing size of computer hardware concurrent use of different parts of hardware is becoming very important. It is not impossible to to perform concurrent computations in a synchronous system, but because each time has to be pre planned and since each operation has to be alloted a fixed amount of time, not much concurrency in hardware utilization is possible. Asynchronous circuit is, however, very well suited for concurrent utilization of different parts of hardware because of the manner in which the timing constrains are met and the way actions of different parts are co-ordinated.

Other important issues are the ease of understanding, construction and operation of system. From this point of view the design should be modular. Also the development of integrated circuit has provided cheaper hardware but it is in the form of small modules and no given integrated circuits can be changed internally with ease. Only the terminal characteristics of such circuits govern their behavior in a system; so long as their terminal behavior remains the same their implementation is of little concern.

The study of modular asynchronous circuits is therefore very important. The following sections give one approach to the design of modular asynchronous circuits.

Section II

Macromodular Asynchronous Circuits

The asynchronous circuits using macromodules consist of two closely interconnected parts called data-flow structure and control structure. The storage of data, the flow of data and the operations performed on them take place in the data-flow structure, and the different operations concurrently taking place in the data-flow structure are coordinated by the control structure.

Each operational unit of the data-flow structure has, in in addition to the data links, a control link connecting it to some part of the control structure. A control link consists of two wires called ready line and acknowledge line. In order to make an operator operate on an input the input is made available to it on the input data link and a ready signal is sent to it on the ready line of the control link. After the the operation has been performed and the output has been placed on the output data-link the operator returns an acknowledge signal on the acknowledge line. The time difference between the arrival of the ready signal and the return of the acknowledge is arbitrary and may depend on the operator, the input and can even be randum so long as the acknowledge signal correctly implies the completion of the operation.

The function of the control structure is to co-ordinate the different operational units of the data-flow structure. Such co-ordination is necessary because other wise the data-flow structure by itself may not be output functional† because of possible races.

---

† A circuit is output functional if for a given input it always results in the same output.

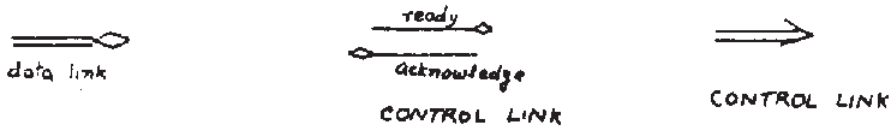


Figure 2.1

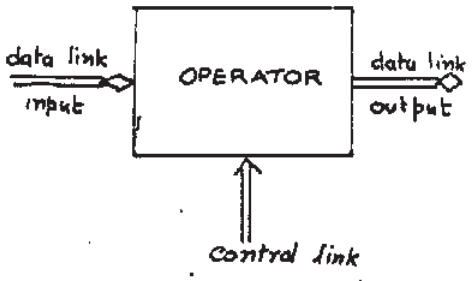


Figure 2.2

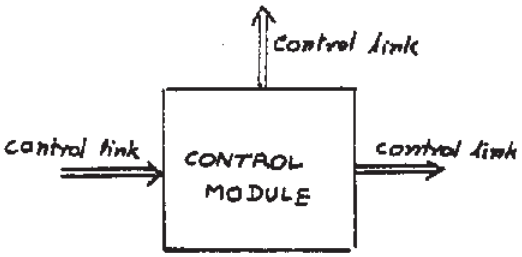


Figure 2.3

The control structure consists of control modules interconnected among themselves and to the data-flow structure through control links. A control link has two parts, the ready line and the acknowledge line. Signals propagate in the forward direction on the ready lines and in the opposite direction on the acknowledge lines. The direction of a control link is the direction in which the signals propagate on its ready line.

A control module has one or more control links incident on it (i.e. one or more control links are its input), and one or more control links originate from it (i.e. one or more control links form its output). Exception to this are the iter and sel modules which have a level-input associated with one control link. The function of a control module is to send acknowledge and ready signals on appopriate links on receiving either ready or acknowledge signals on some links.

Sending of a ready signal to an operator by a control module is eqivalent ot a request by the control module to the operator to perform necessary operation on the input. The control module is hopeful that the operator will act on the request and eventualy when the output is ready, the operator will return an acknowledge signal to the control module. A ready signal sent to a control module is a permission given to it to carry out the operations controled by it. When some appropriale condition is reached the control module returns an acknowledge in response to the ready signal.

Before going further it will be appropriate to discuss a simple example. Figure 2.4 shows a circuit that computes $2*x^2$ where x is the input. This circuit's data structure consists of the operators

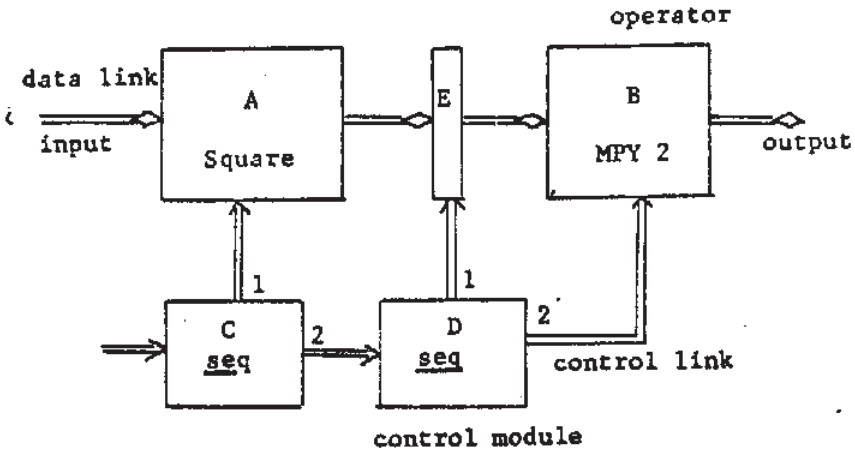

operator
data link
input
A
Square
E
B
MPY 2
output
1
1
C
seq
2
D
seq
2
control link
control module

Figure 2.4

A, B and E . The operator A multiplies the input by itself and the operator B multiplies its input by 2 . The operator E is a register which updates its output to correspond to its input on reciving a ready signal and then returns an acknowledge. The operator E holds the output at this value, ignoring any changes in the input, until the next ready signal.

The control structure consists of the control modules C and D both of which are seq (sequencer) modules. A seq module has the property that on receiving a ready signal on the input control link, a ready signal is sent on the control link marked 1, and when an acknowledge is obtained, a ready signal is sent on the control link marked 2 . Finally when an acknowkedge is obtained on the control link marked 2 an acknowledge signal is returned on the input control link. In other words the seq module first applies the operator connected to the control link marked 1 and then the one connected to the control link marked 2 .

The operation of the circuit is as follows. In order to compute $2*x^2$ the number x is placed on the input data link i and a ready signal is sent to the control module C . In turn C sends a ready signal to the operator A . On receiving the ready signal the operator A computes x**x , places this on the output data link and then returns an acknowledge signal to C . The control module C then sends a ready signal to the control module D. which in turn first causes the register E to update its output and then causes the operator B to produce $2**x^2$ at the output data link. The operator B then sends an acknowledge signal to D, D sends the acknowledge signal to C and finally C returns an acknowledge signal on the input control link. With this the action is complete.

In the circuit discussed above at most one operator operated at any given time. A circuit of this kind is called a totally ordered circuit. A partially ordered circuit is one in which more than one operators may operate concurrently. With the seq module alone it is not possible to construct circuits in which concurrent operations take place. A convenient set of control modules will be introduced in next section which will allow construction of partially ordered circuits.

Before introducing the control modules it is appropriate to tell what represent the ready and the acknowledge signals. A value 0 or 1 can be associated with both the ready and the acknowledge lines of a control link. A change in the value of the ready line from 0 to 1 or from 1 to 0 is interpreted as ready signal, and similarly a change in the value of the acknowledge line from 0 to 1 or from 1 to 0 is interpreted as an acknowledge signal. Also, under idle condition both the ready line and the acknowledge line have the same value associated with it. In the time interval between a ready signal and the return of the acknowledge signal a control link is said to be active; an active control link has opposite values associated with its ready and acknowledge lines.

Section III

The Control Modules

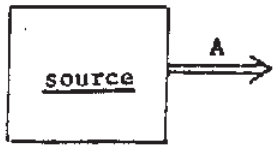
The action of the control modules has been described through action-graphs which should be interpreted in conjuction with figures of the corresponding control modules. In the action-graphs an arrow indicates an action that the control module takes in response to the input to the left of the arrow; $R_a \rightarrow R_b$ indicates that a ready signal on the input link A results in a ready signal on the output link B. A straight line indicates what input the control circuit expects to get in response to the output written to the left of the line. The time difference between the occurance of the signals to the left of the line and those at the right of the line is governed by the circuit external to the module. The right braces indicate that the action to their right take place only on occurance of all signals to their left. Left braces indicate that the signals to their left result in signals to their right.

source Module

This module is shown in figure 3.1 . It has only one control link. The control link is an output link. After the circuit is intializes the source module first sends one ready signal on the control link and then it sends a fresh ready signal on the control link for each acknowledge received on it.

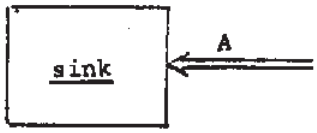
sink Module

This module, shown in figure 3.2, returns an acknowledge signal on the control link in response to each ready signal received on the control link.



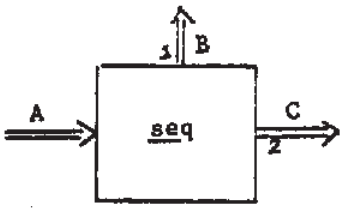
$- A_a \rightarrow R_a -$

Figure 3.1



$- R_a \rightarrow A_a -$

Figure 3.2



$- R_a \rightarrow R_b - A_b \rightarrow R_c - A_c \rightarrow A_a -$

Figure 3.3

seq Module

A seq (sequence) module was described in connection with the example discussed in last section. It is included here to make the list of control modules presented in this section complete.

The action diagram of the seq module is given in figure 3.3 . Initially all the control links are idle. On receiving a ready signal on the control link A a ready signal is sent on the control link B (the control link labelled 1). When in response to this ready signal an acknowledge signal is obtained on the control link B, a ready signal is sent on the control link C (the one labelled 2). Finally when an acknowledge signal is received on C an acknowledge signal is returned on the control link A . With this the circuit is back to the idle condition.

trig Module (trigger module)

This is the module which was called X module in the class. Figure 3.4 shows the action diagram of this module. On receiving a signal on the control link A a ready signal is immediately sent on the control link B if the control link C is already idle, otherwise the action of sending a ready signal on the control link B is delayed till an acknowledge signal is obtained on the control link C. When an acknowledge signal is obtained on the control link B in response to the ready signal, a ready signal is sent on the control link C and an acknowledge is sent on the control link A. A fresh ready signal may now be received on the control link A before or after an acknowledge is obtained on the control link C.

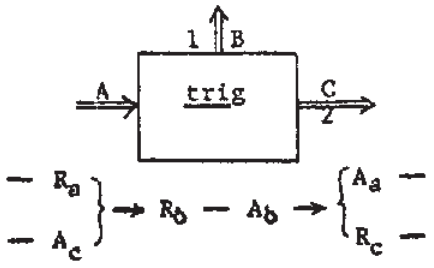


Figure 3.4

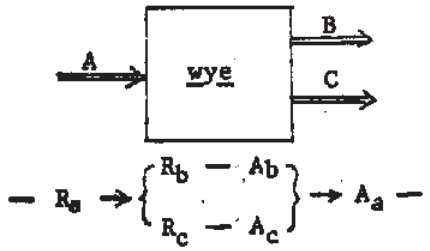


Figure 3.5

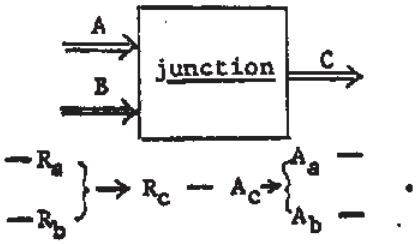


Figure 3.6

wye Module

A wye module is used to control the action of two units through one control link. Its action diagram is presented in figure 3.5 . Initially all the control links are idle. On receiving a ready signal on the control link A , a ready signal is sent on both control links B and C. When acknowledge signals are obtained on both control links B and C, an acknowledge signal is returned on A. With this the circuit returns to idle condition.

junction Module

A junction module sends a ready signal on the control link C on receiving ready signals on both the control link A and the control link B. In response to the ready signal when an acknowledge signal is obtained on the control link C acknowledge signals are returned on both control links A and B. A junction module is used to delay the execution of a unit till some other units have completed their actions.

sel Modules

The sel module is a conditional module. It sends a ready signal on either the control link C or the control link D depending on the boolean condition of the input b . Figure 3.7 shows the action diagram of the sel module.

A zero on b represents a 'false' condition while a 1 on b represents a 'true' condition. To set the condition of the module an appropriate signal is placed on b and a ready signal is sent to the module on the control link B. The module then returns an acknowledge signal on the

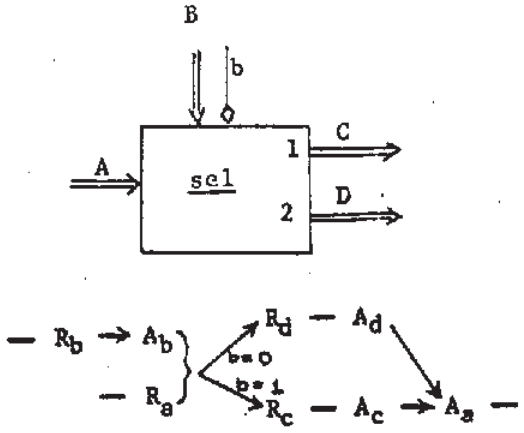


Figure 3.7

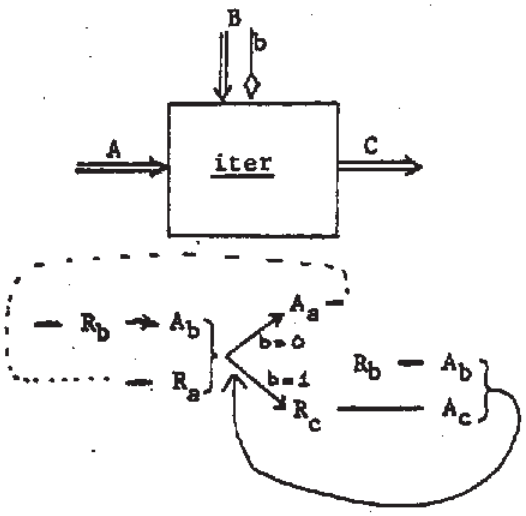


Figure 3.8

control link B after setting its condition to that of b .

On receiving a ready signal on the control link A, if the condition of the module has already been set by the control link B, it sends a ready signal on either the control link C or the control link D depending on whether its condition is 'true' or 'false', else the module awaits for the control link B to set its condition before taking above action. When an acknowledge signal is obtained on the control link C or the control link D,as the case may be, an acknowledge signal is returned on the control link A and the module is reset. The control link B must set the module once again before another such action may take place.

iter Module

The iter module is for iteratively using part of an asynchronous circuit. The action diagram of an iter module is shown in figure 3.5 .

Just as in the case of a sel module a zero on b represents a 'false' condition while a 1 represents a 'true' condition. To set the condition of an iter module an appropriate signal is placed on b and a ready signal is sent on the control link B. The module then sets its condition to that of b and returns an acknowledge signal on the control link B.

On receiving a ready signal on the control link A if the condition of the iter module has already been set by the control link B, either a ready signal is sent on the control link C or an acknowledge signal is returned on the control link A depending on wether the module is in 'true' condition or in 'false' condition, else the action is delayed till the control link B sets the condition of the module. With above action the condition of the module is reset. If the above action leads

to a ready signal on the control link C, the acknowledge signal returning on the control link C causes the module to go through the above action once again.

It should be noted that not all modules introduced in this section are all necessary, for some of them can be realized in term of other modules. For example the trig module can be realized in terms of seq, junction, source and sink modules.

Examples of asynchronous circuits using these modules have not been presented here because they appear in the notes written by Prof. Dennis.