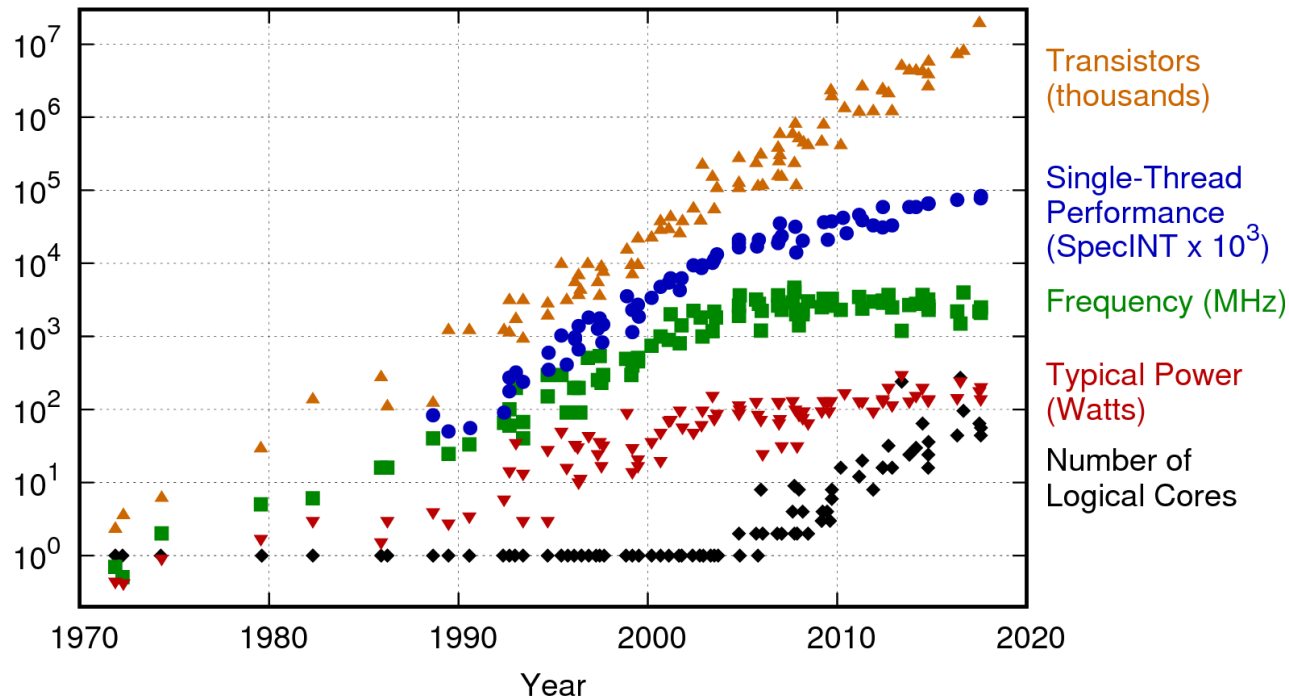


Cache Coherence

Mengjia Yan

Computer Science & Artificial Intelligence Lab
M.I.T.

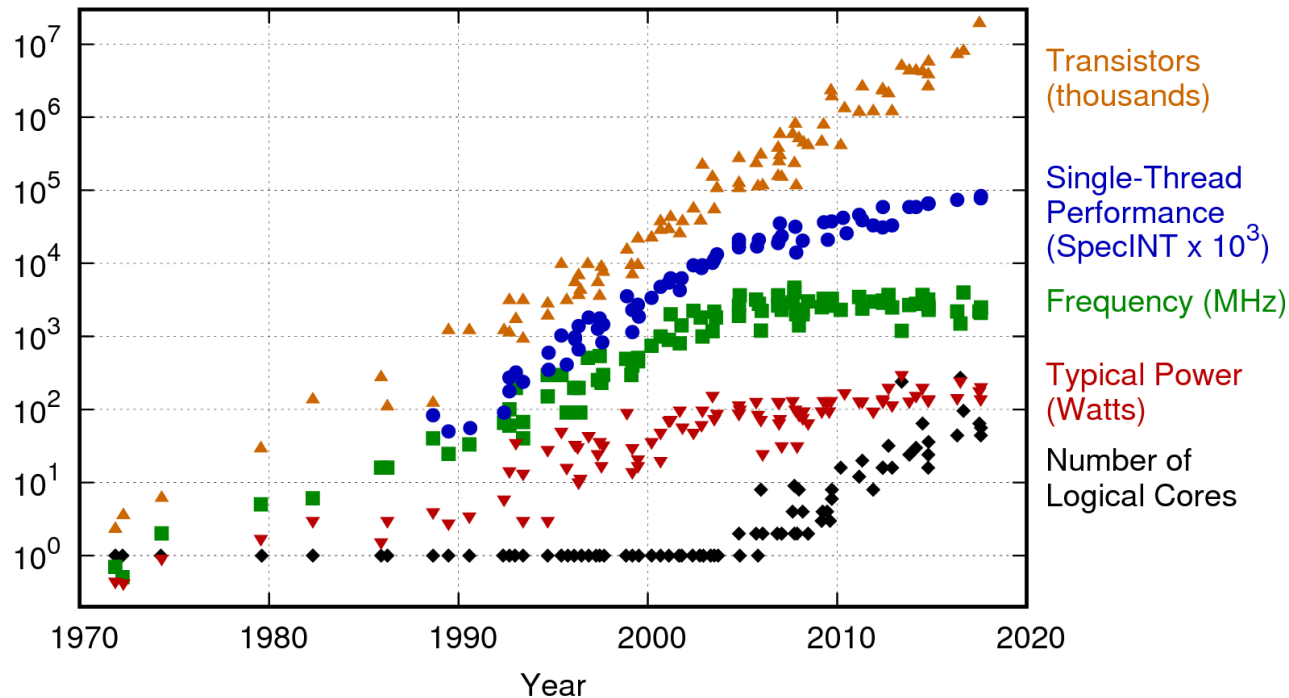
The Shift to Multicore



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten

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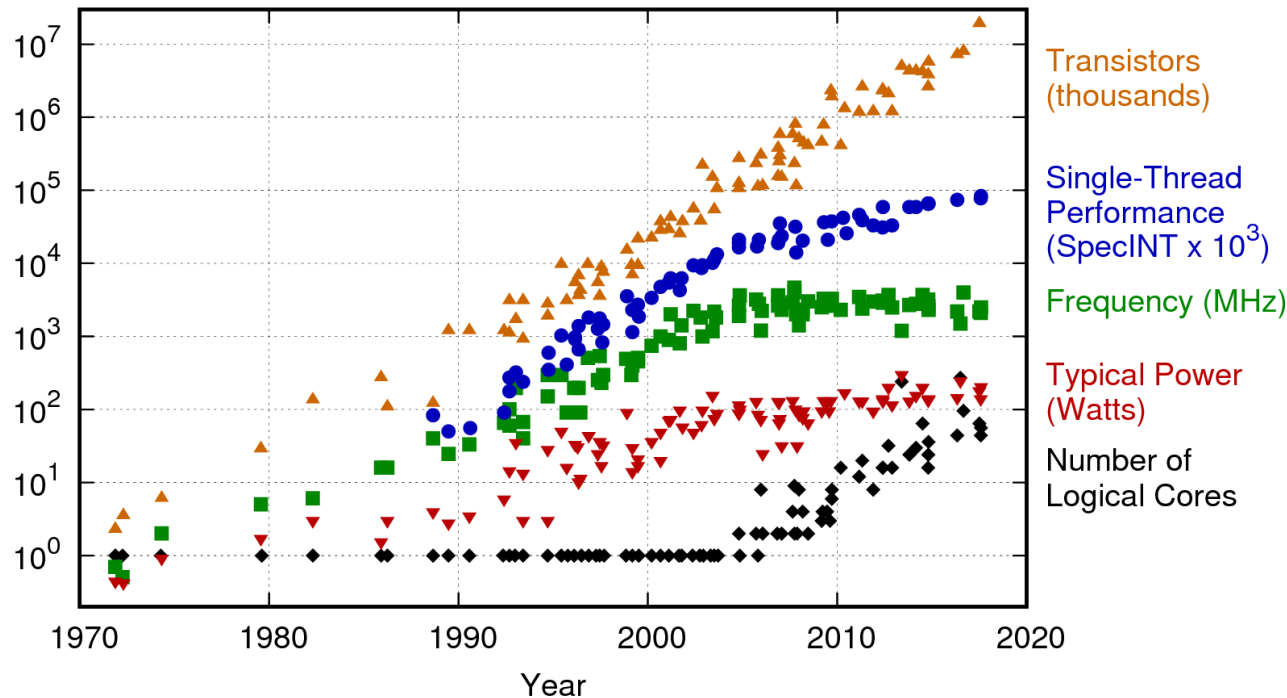


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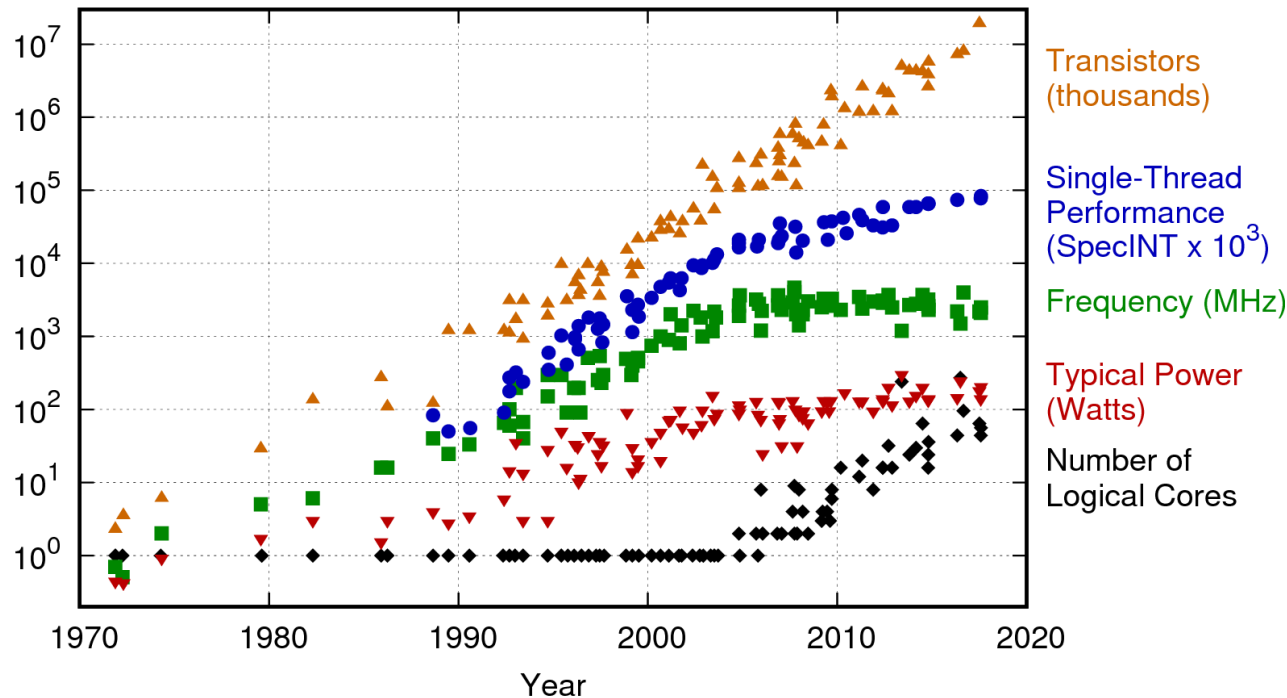


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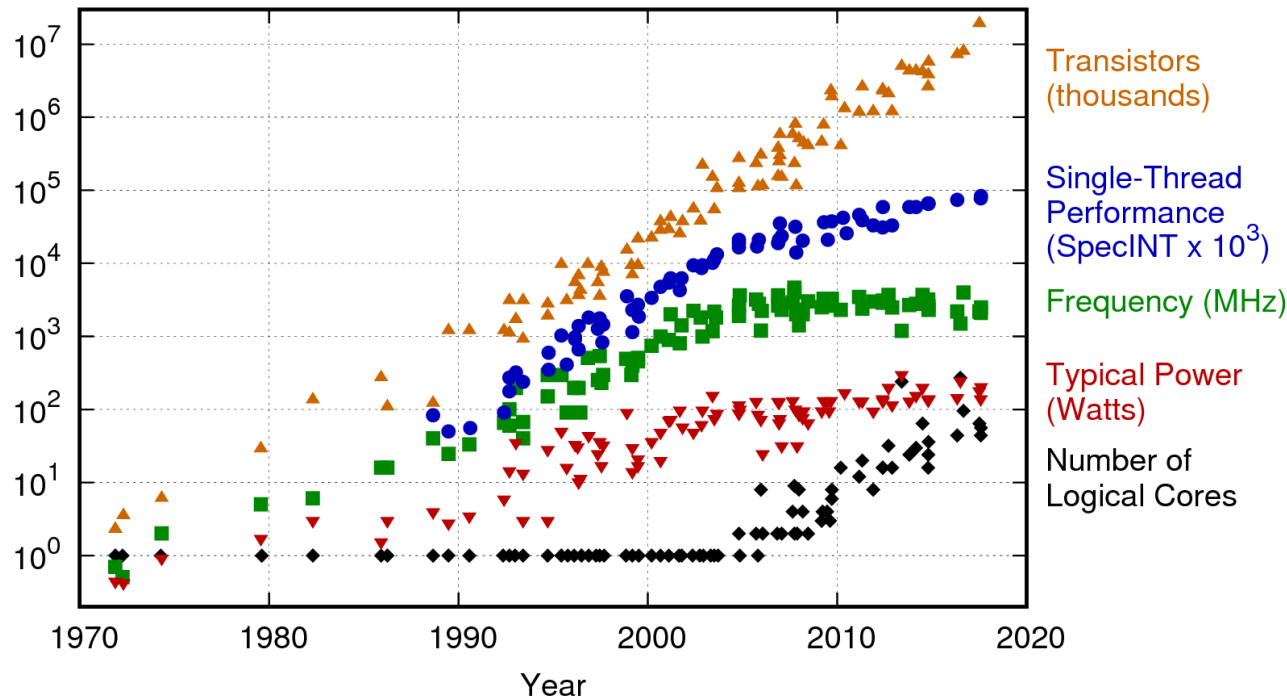


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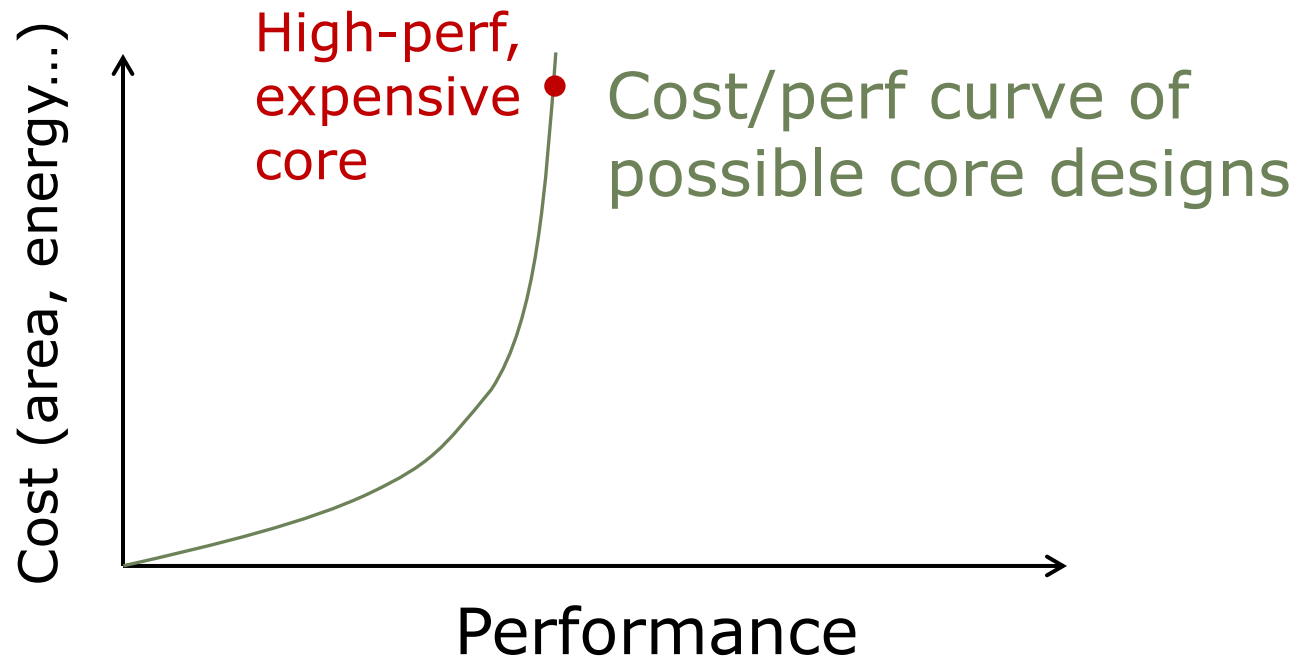


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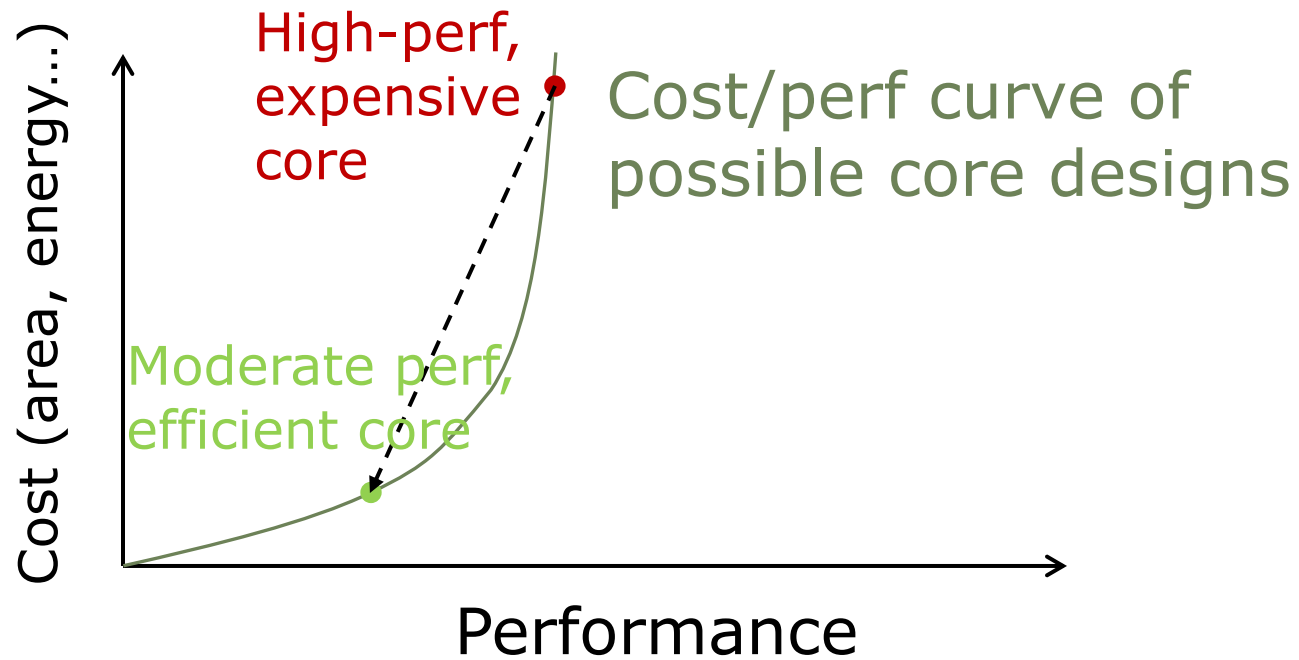
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Limited instruction-level parallelism

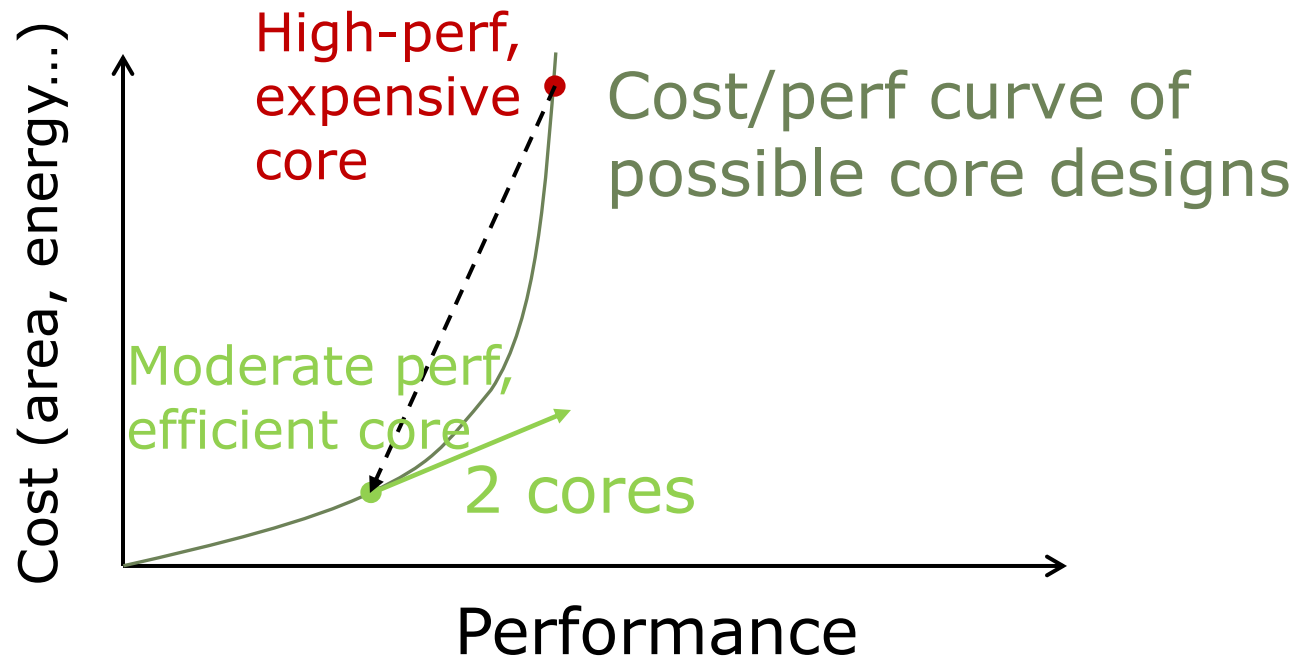
Multicore Performance



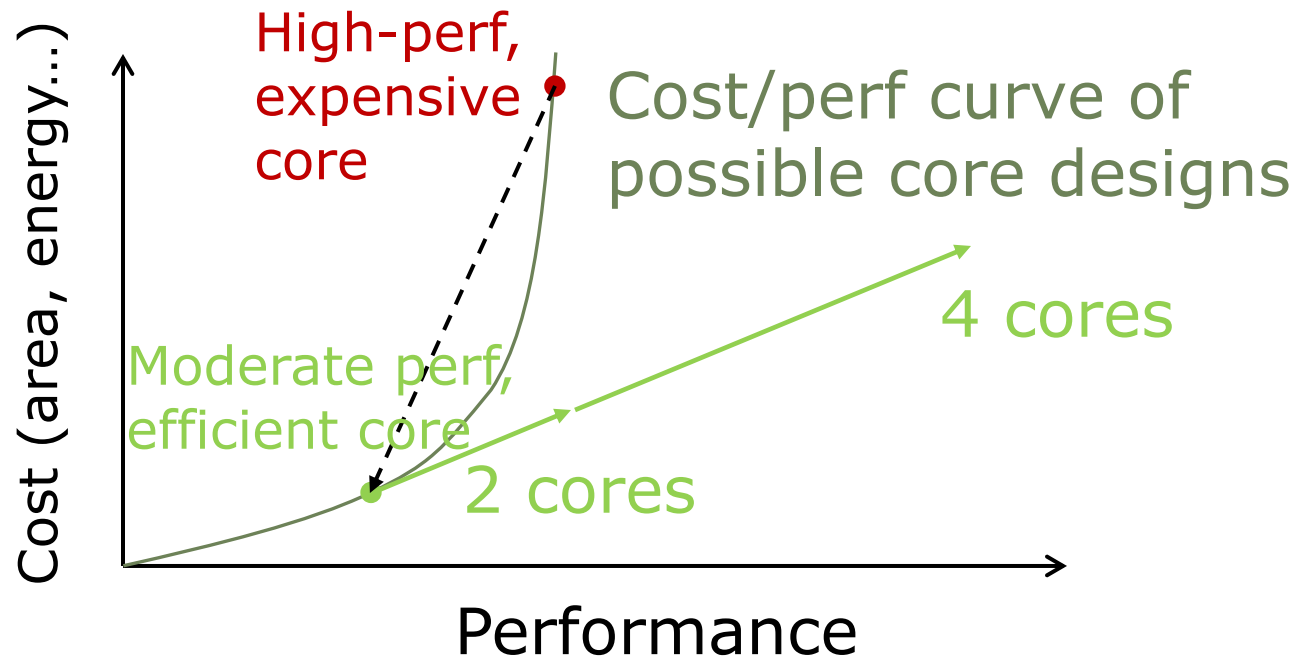
Multicore Performance



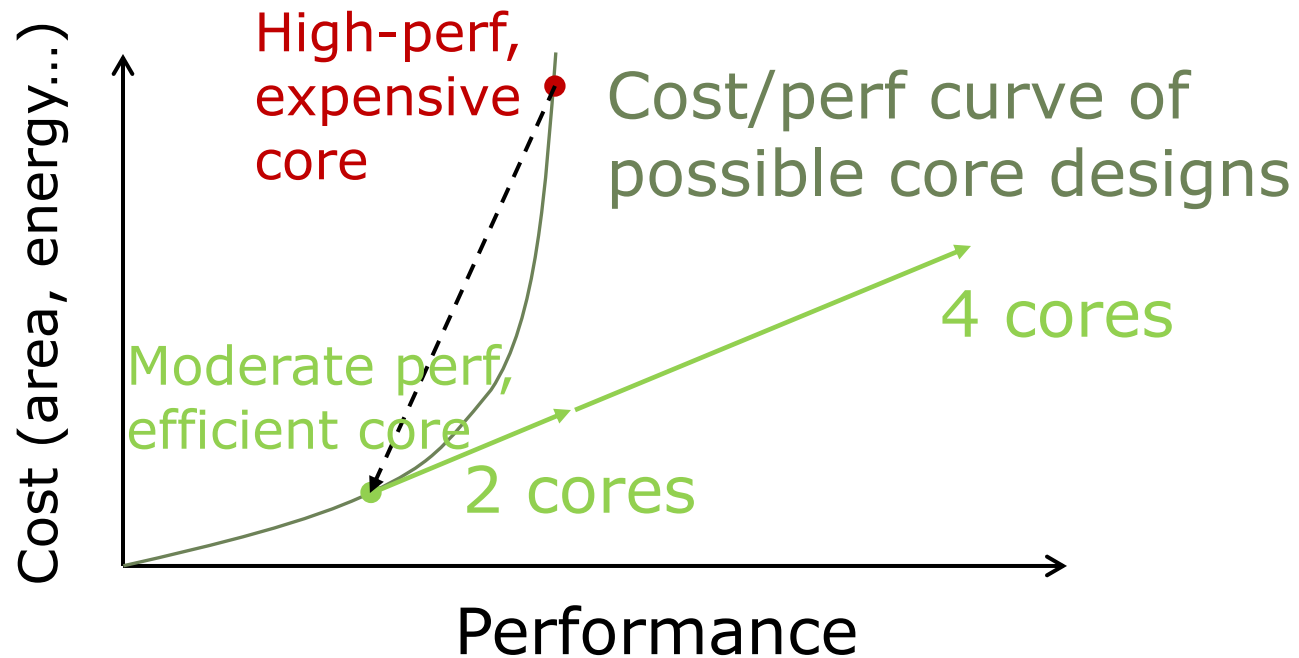
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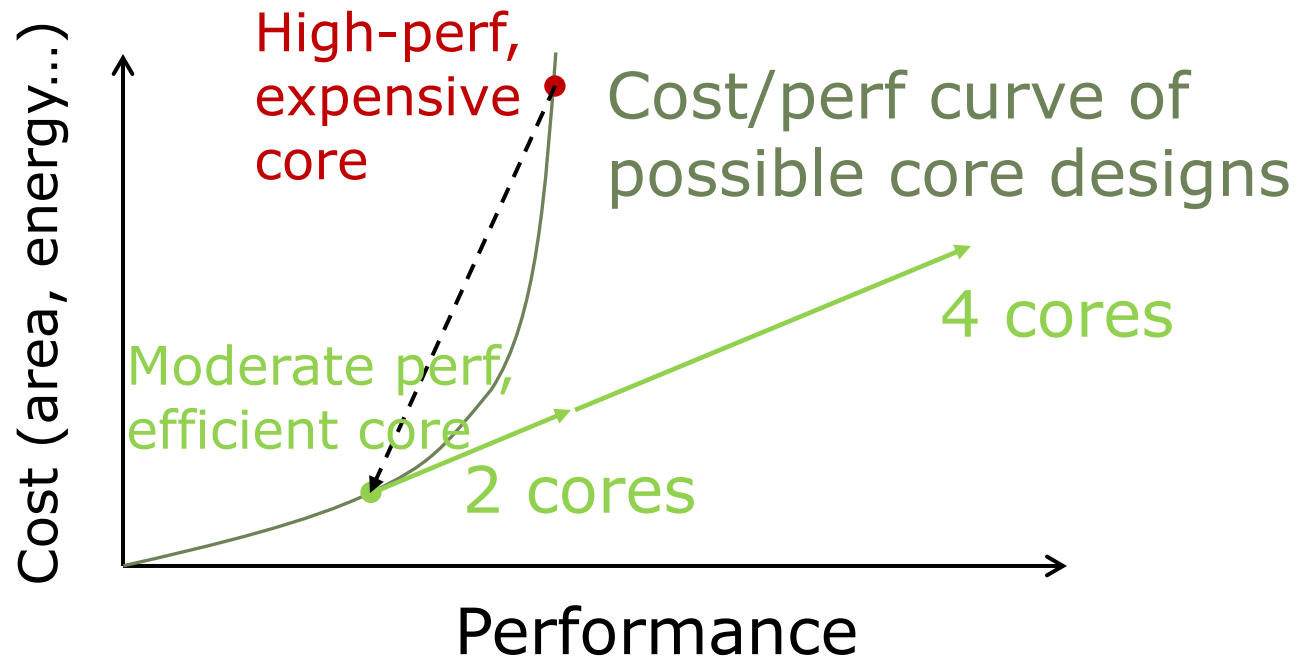


Multicore Performance



What factors may limit multicore performance?

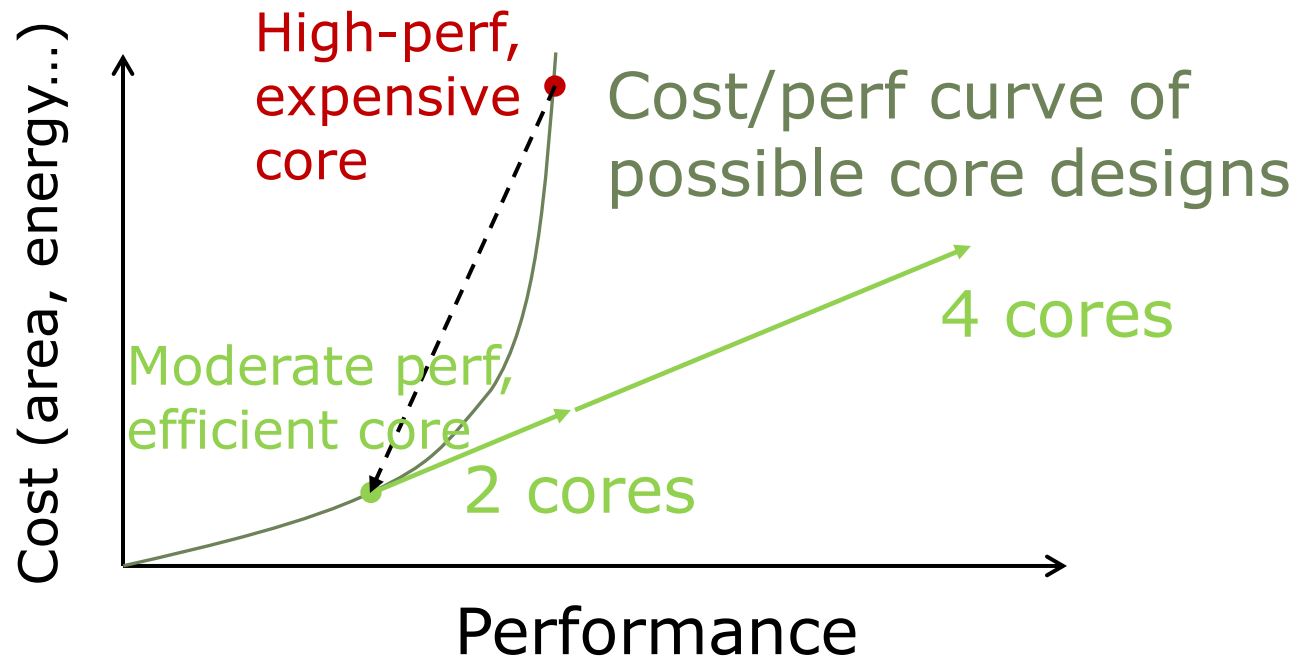
Multicore Performance



What factors may limit multicore performance?

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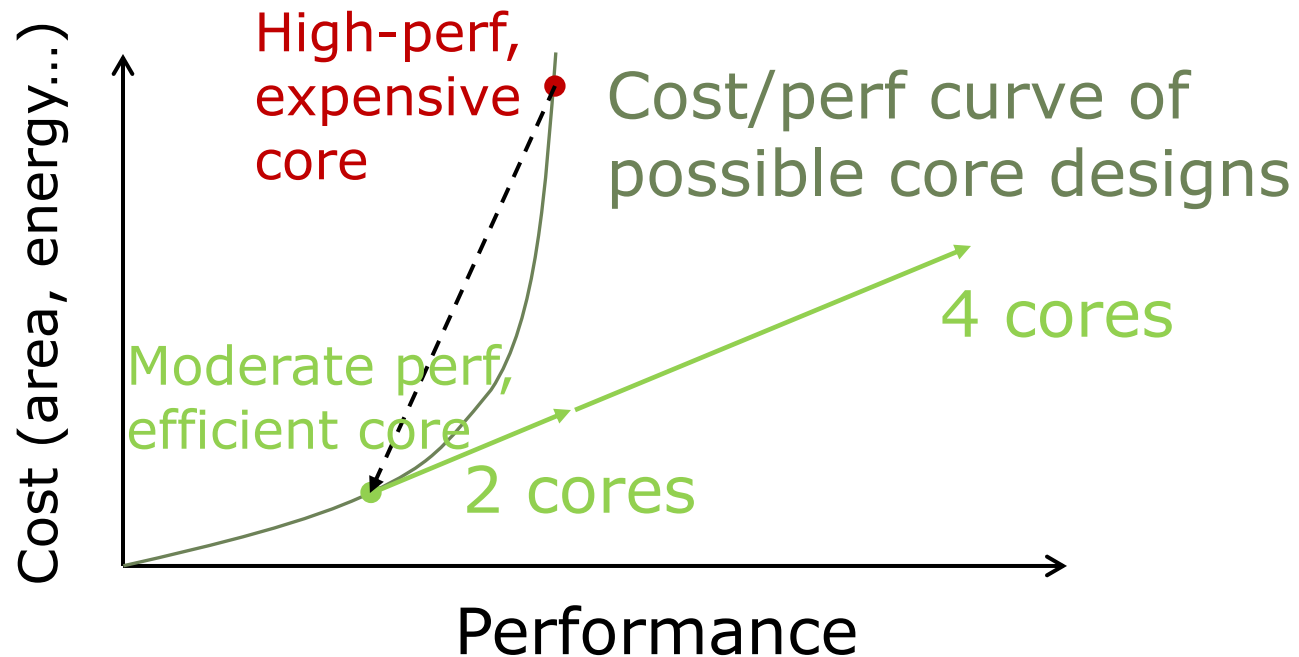
Multicore Performance



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Multicore Performance

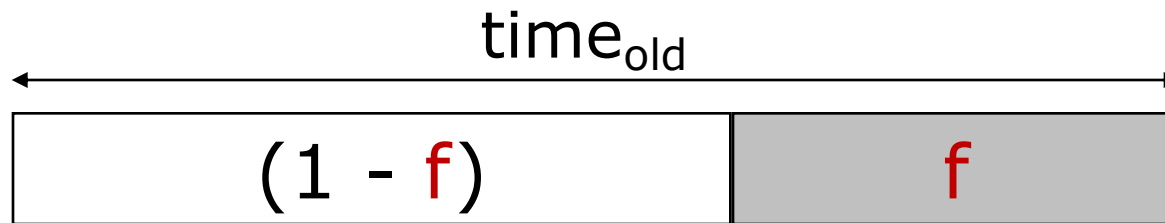


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- Limited application parallelism
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- Programming complexity

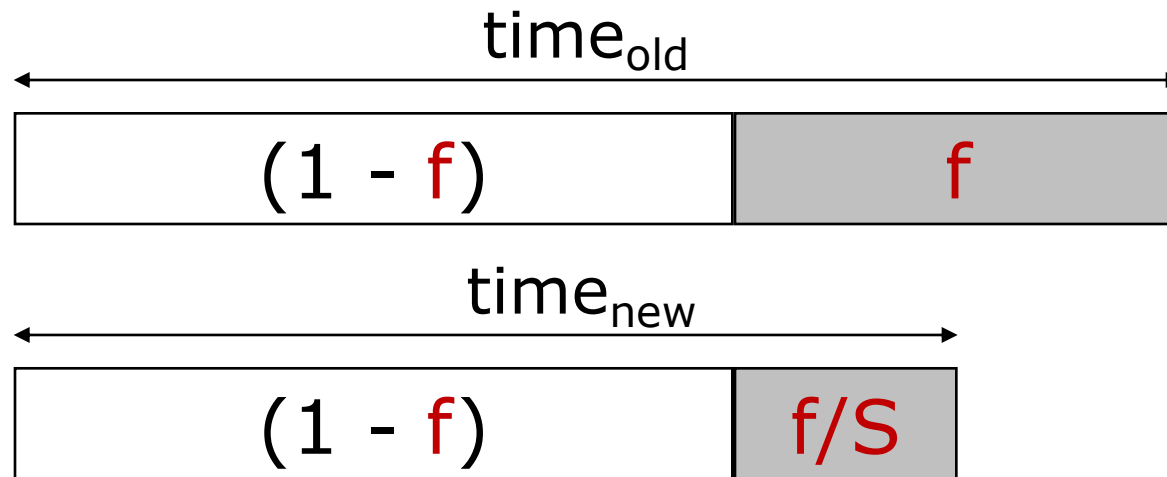
Amdahl's Law

- Speedup = $\text{time}_{\text{without enhancement}} / \text{time}_{\text{with enhancement}}$
- Suppose an enhancement speeds up a fraction f of a task by a factor of S



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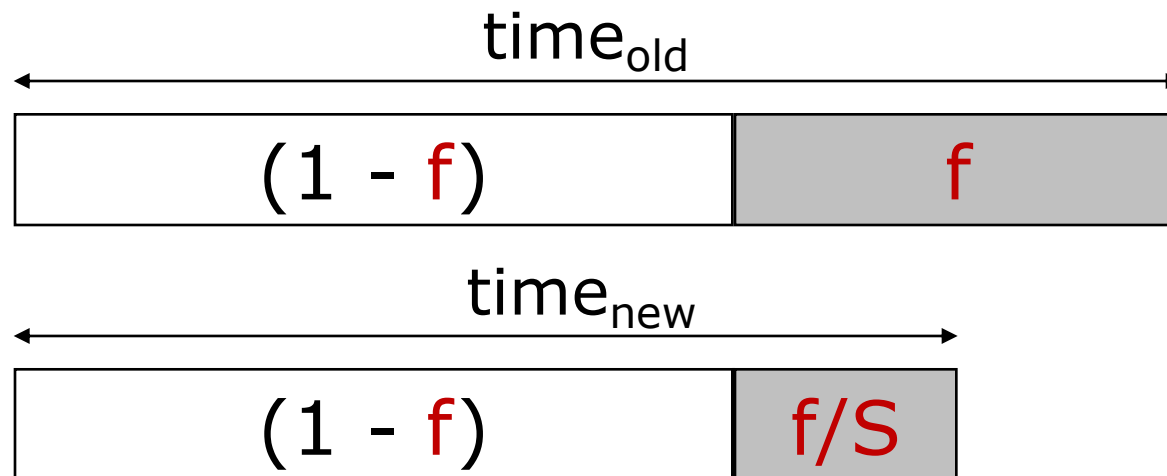
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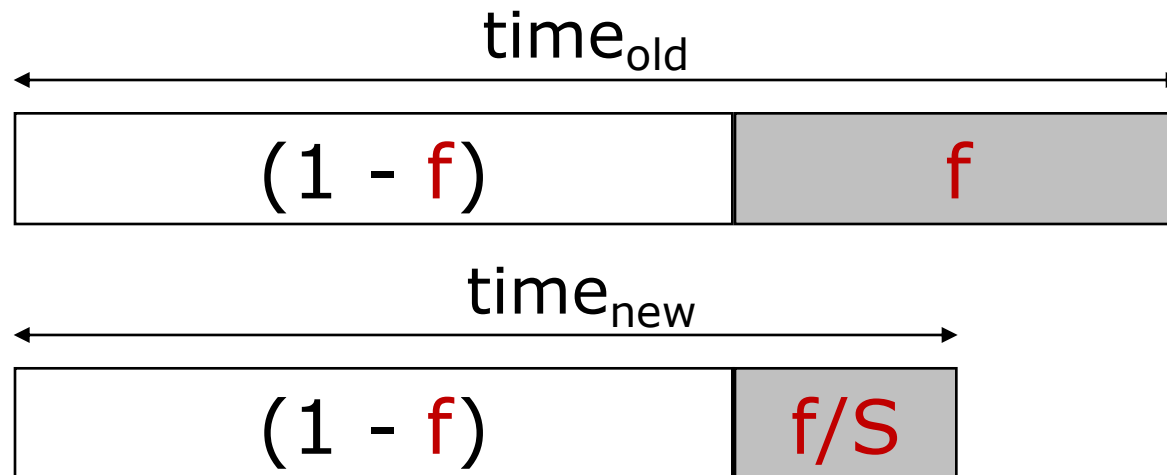


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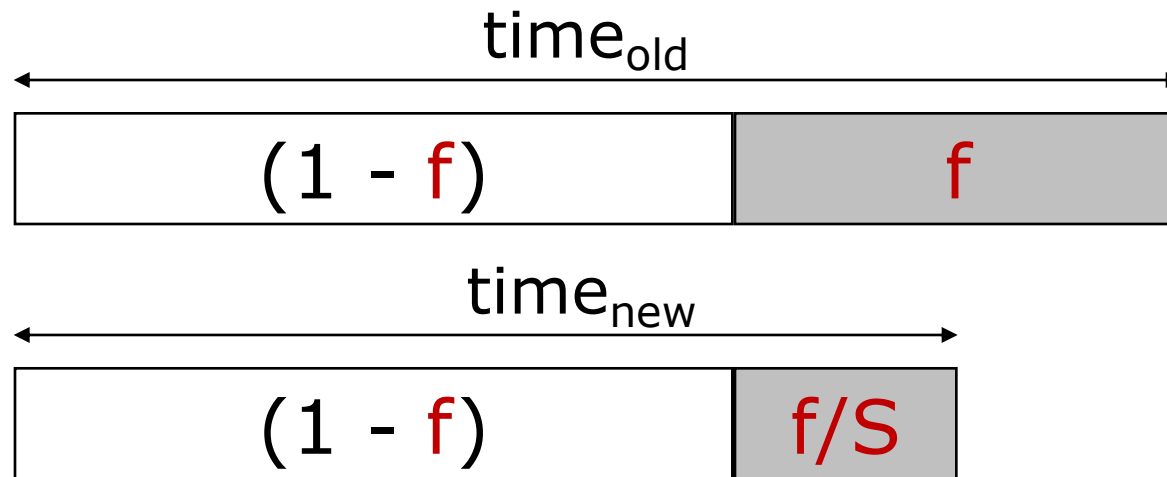


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Corollary: Make the common case fast

Amdahl's Law and Parallelism

- Say you write a program that can do 90% of the work in parallel, but the other 10% is sequential
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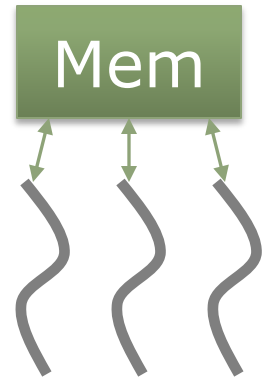
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What f do you need to use a 1000-core machine well?

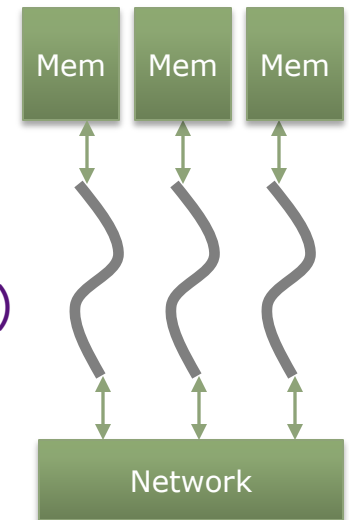
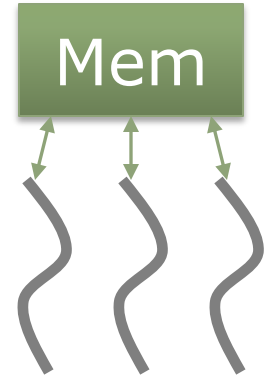
Communication Models

- Shared memory:
 - Single address space
 - Implicit communication by reading/writing memory
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 - Control (semaphores, locks, barriers, ...)
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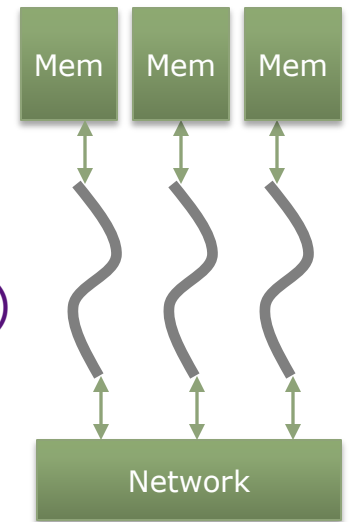
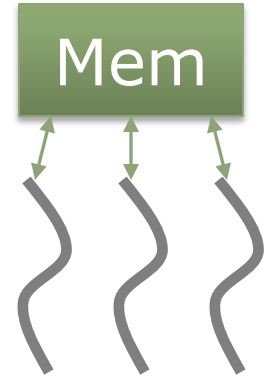
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- Pros/cons of each model?



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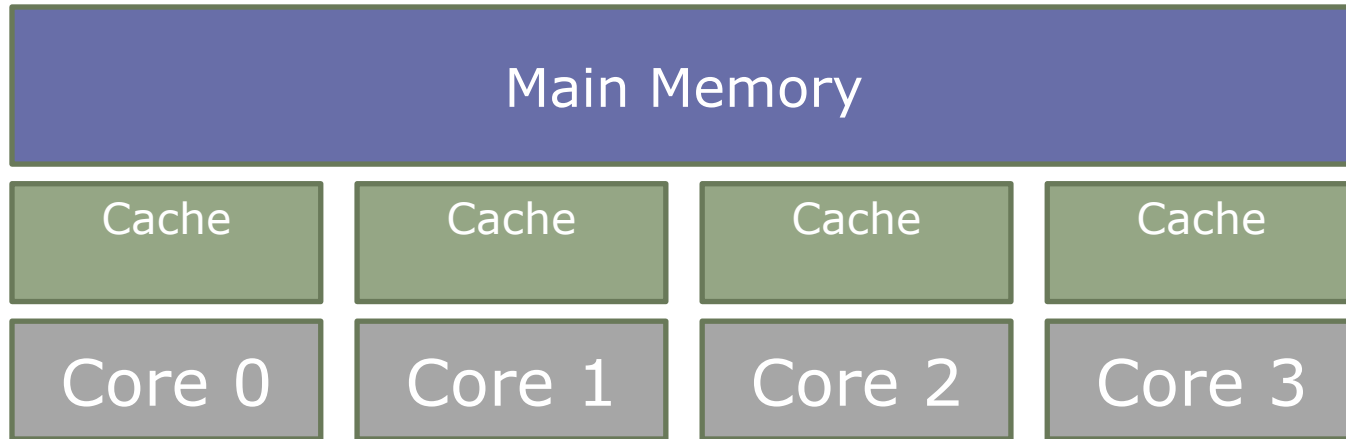
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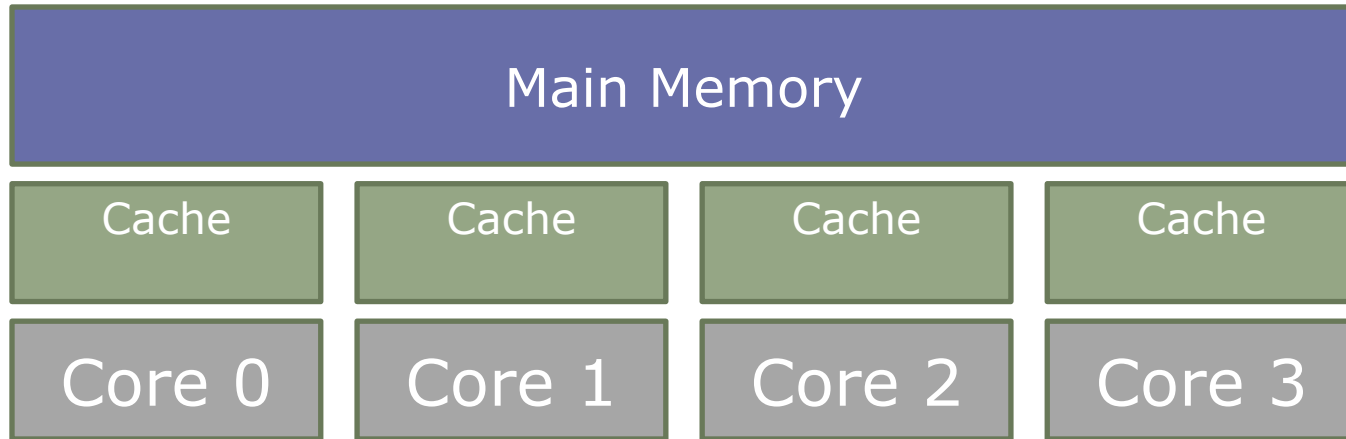
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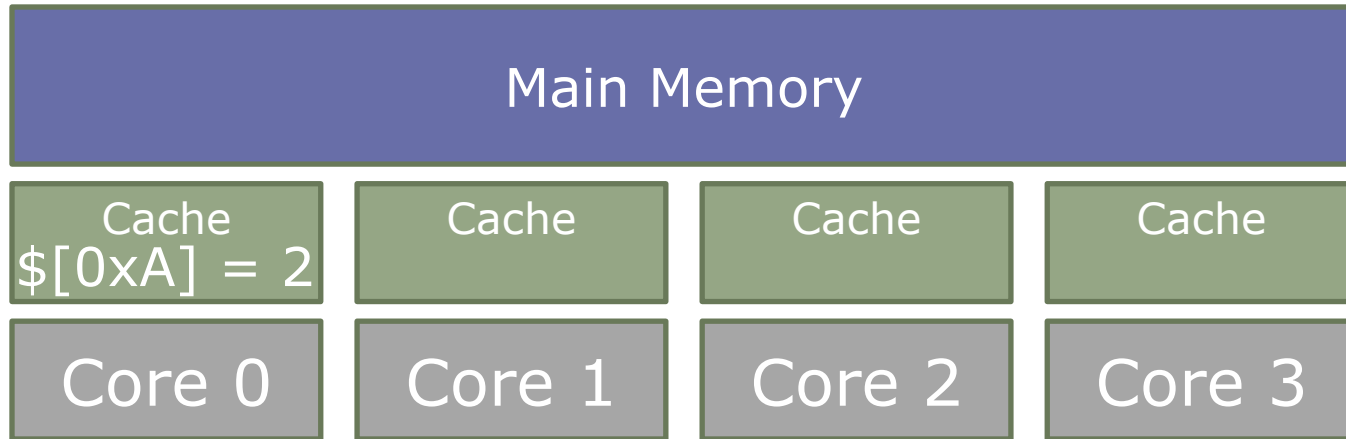


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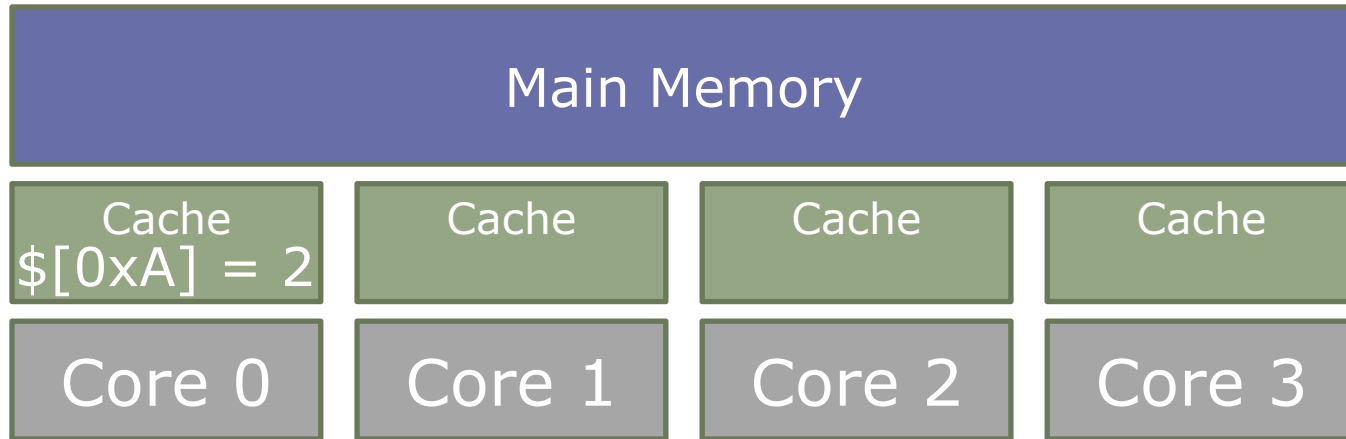
1 LD 0xA → 2

Cache Coherence Avoids Stale Data



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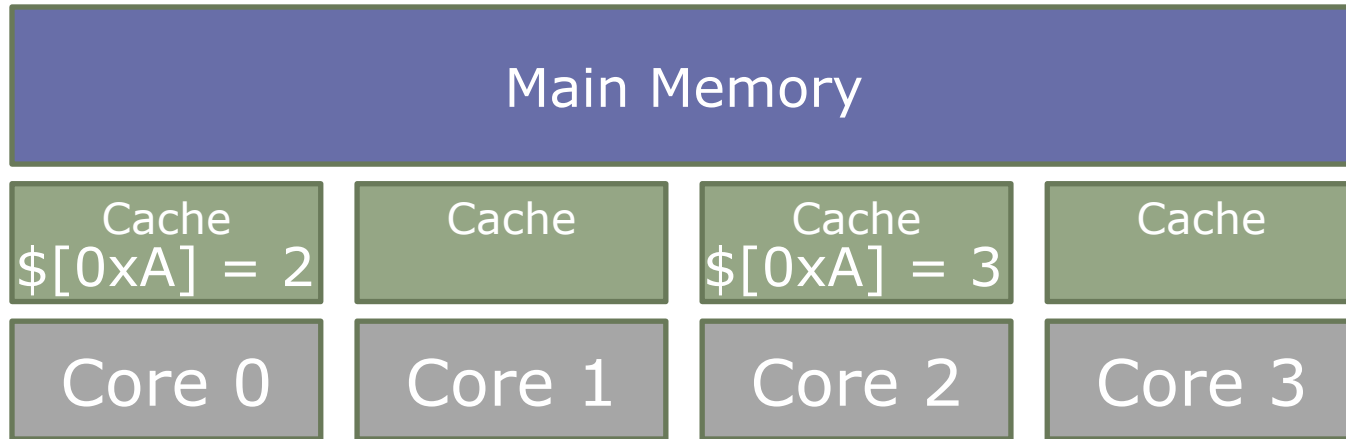
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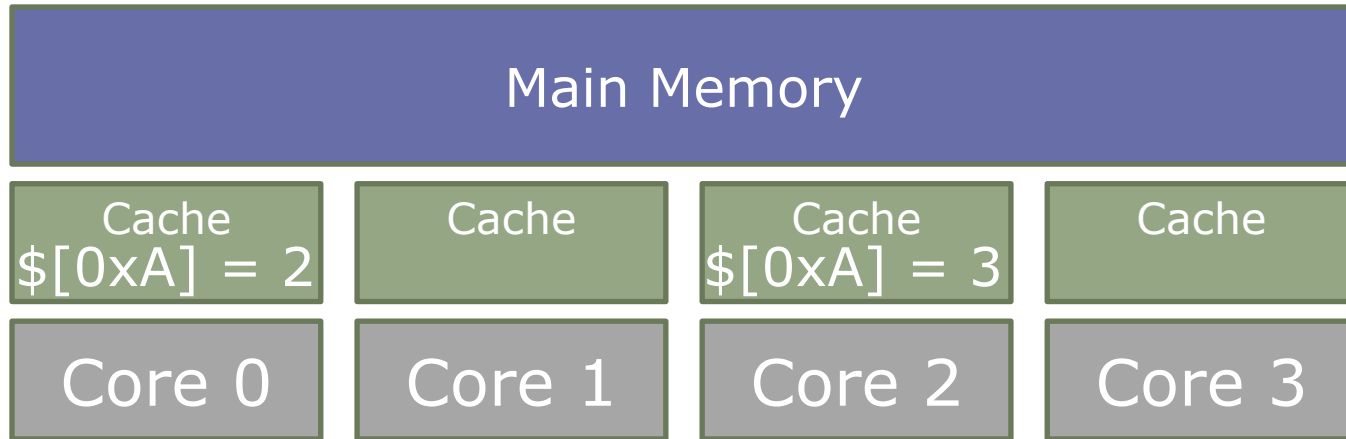
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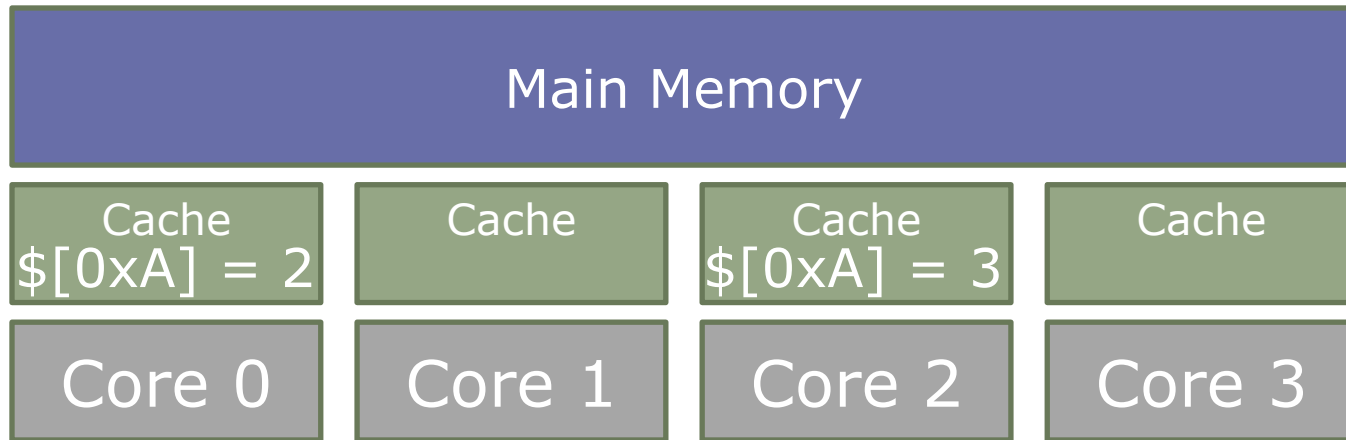


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3 LD $0xA \rightarrow 2$ (stale!)

Cache Coherence Avoids Stale Data



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- A **cache coherence protocol** controls cache contents to avoid stale cache lines

Implementing Cache Coherence

- Coherence protocols must enforce two rules:
 - *Write propagation*: Writes eventually become visible to all processors
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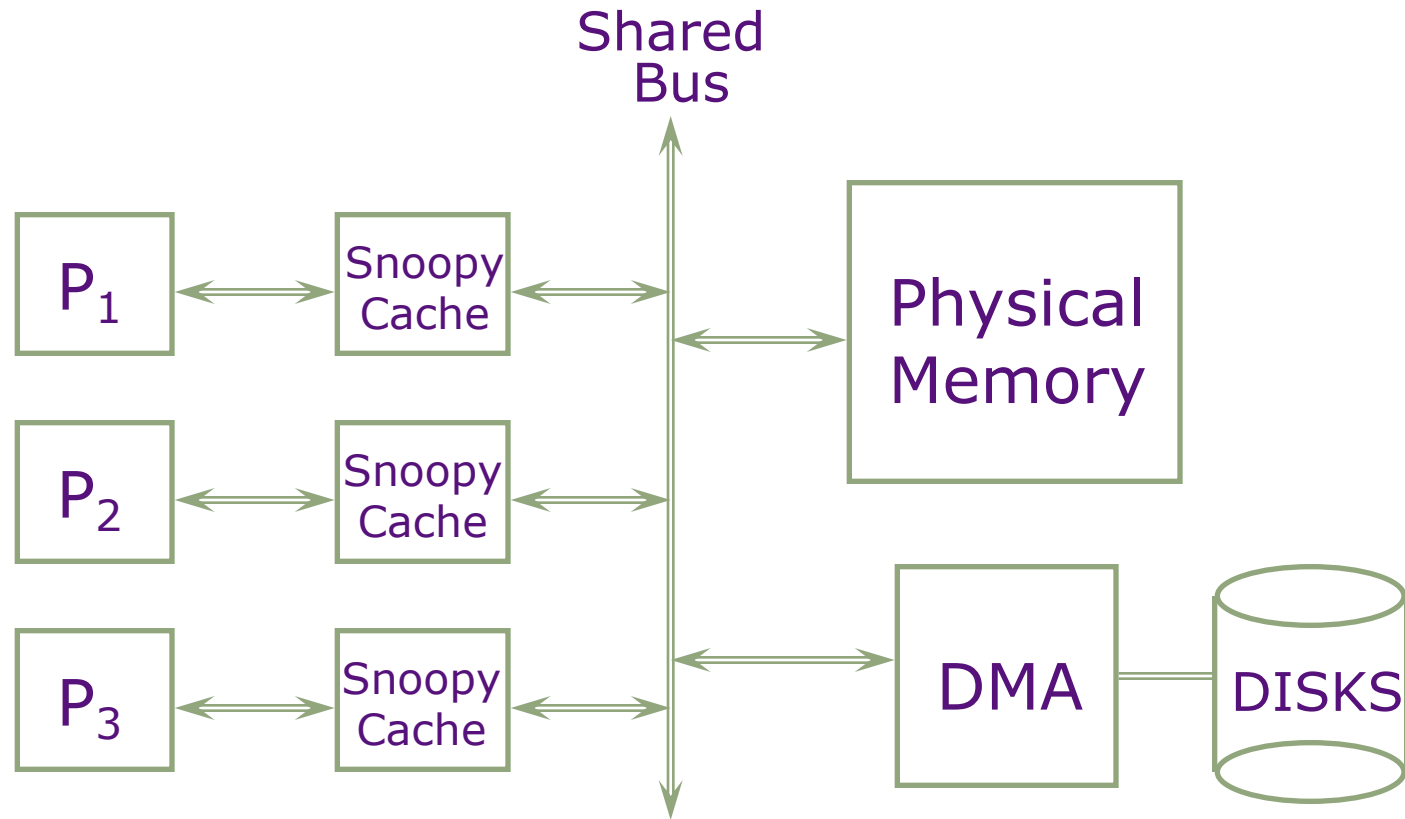
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- How to track sharing state of cached data and serialize requests to the same address?
 - *Snooping-based protocols*: All caches observe each other's actions through a shared bus (bus is the serialization point)
 - *Directory-based protocols*: A coherence directory tracks contents of private caches and serializes requests (directory is the serialization point)

Snooping-Based Coherence

(Goodman, 1983)



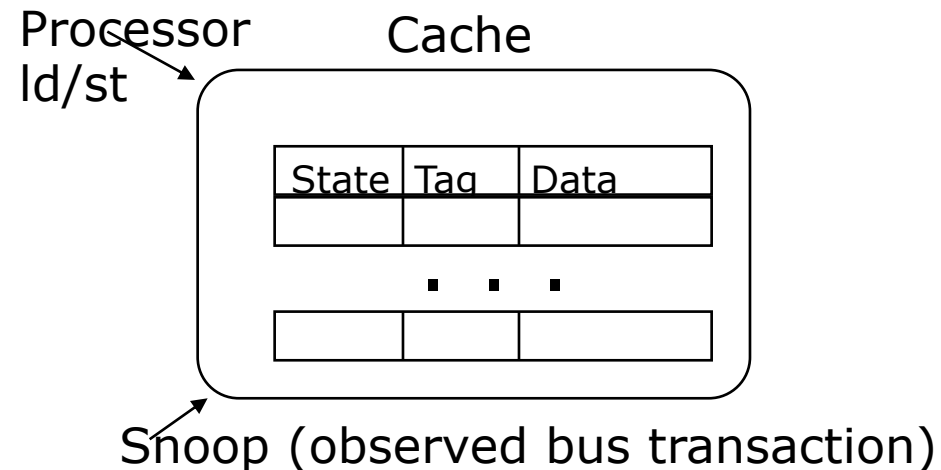
Caches watch (snoop on) bus to keep all processors' view of memory coherent

Snooping-Based Coherence

- Bus provides serialization point
 - Broadcast, totally **ordered**

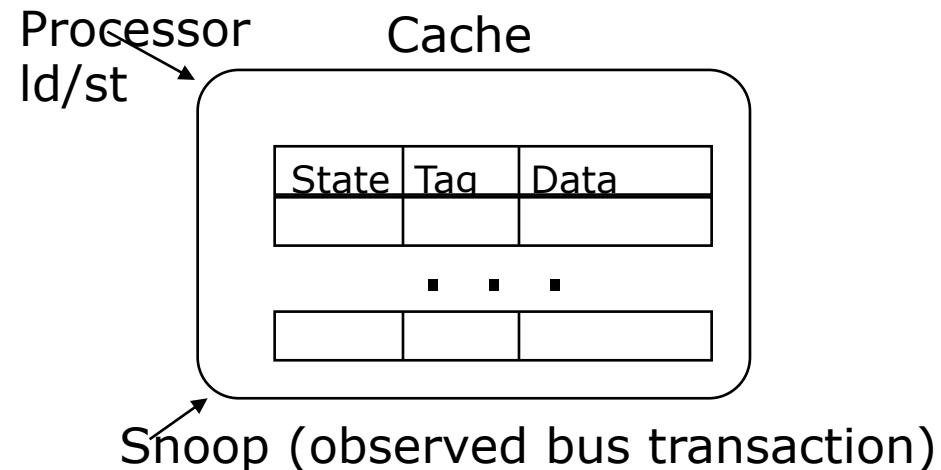
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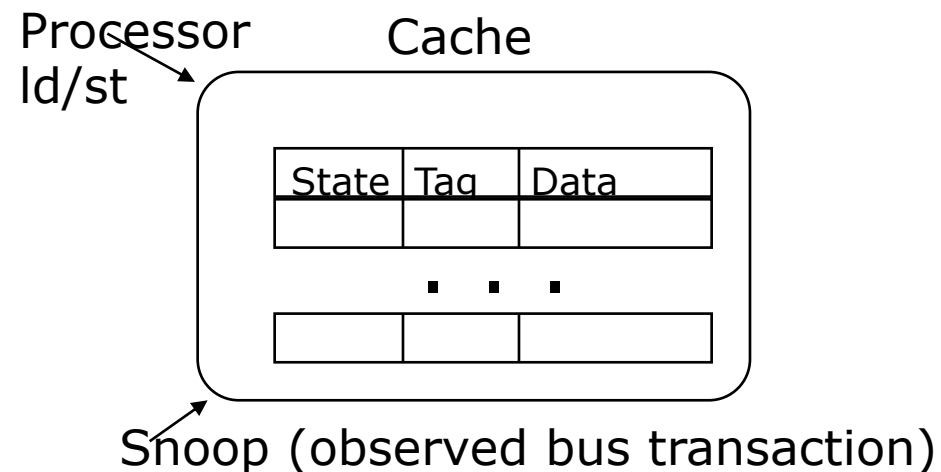
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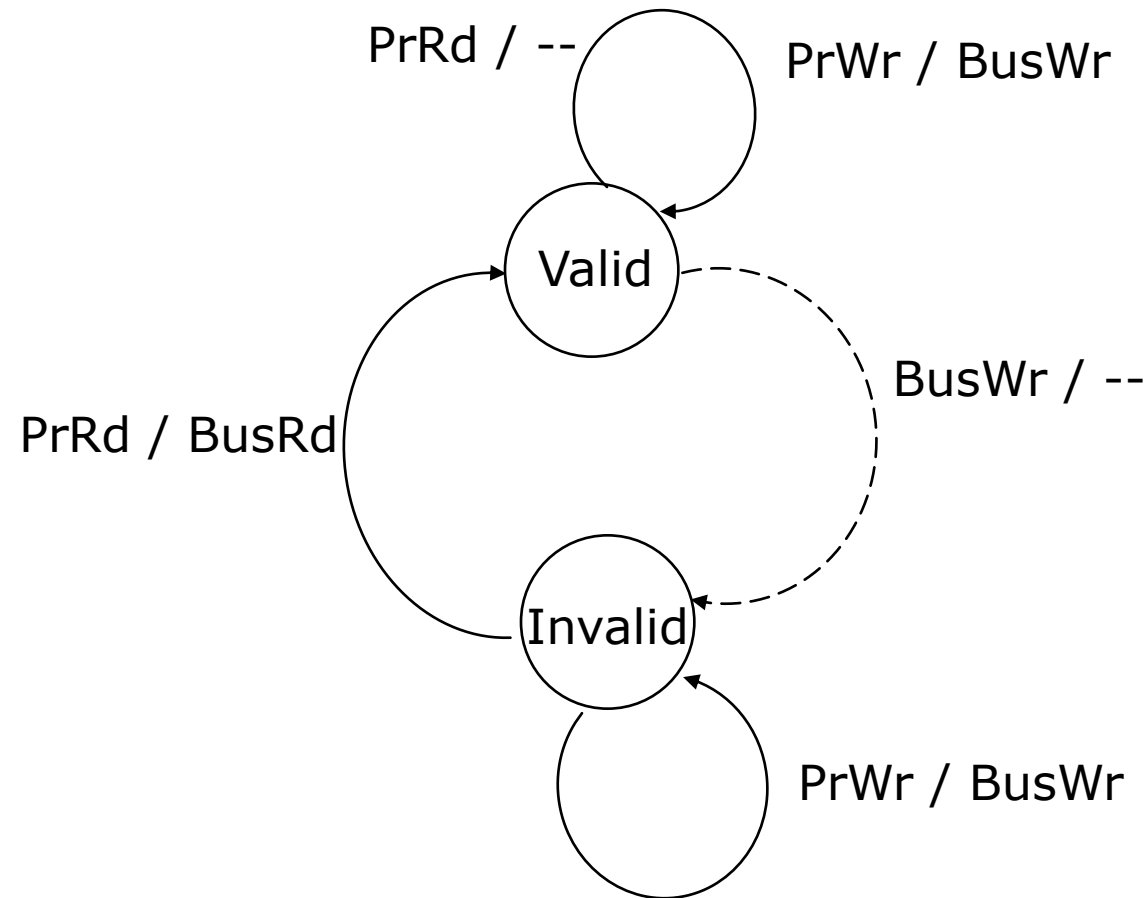


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- Handling writes:
 - Write-invalidate
 - Write-update



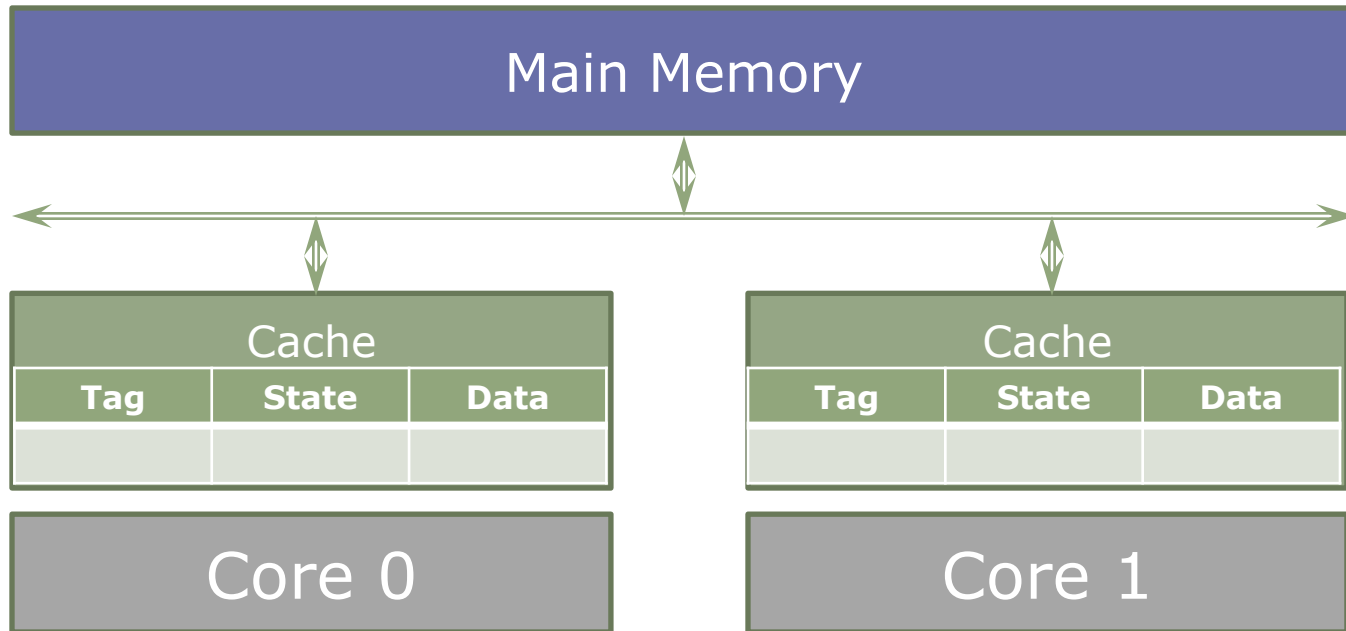
A Simple Protocol: Valid/Invalid (VI)



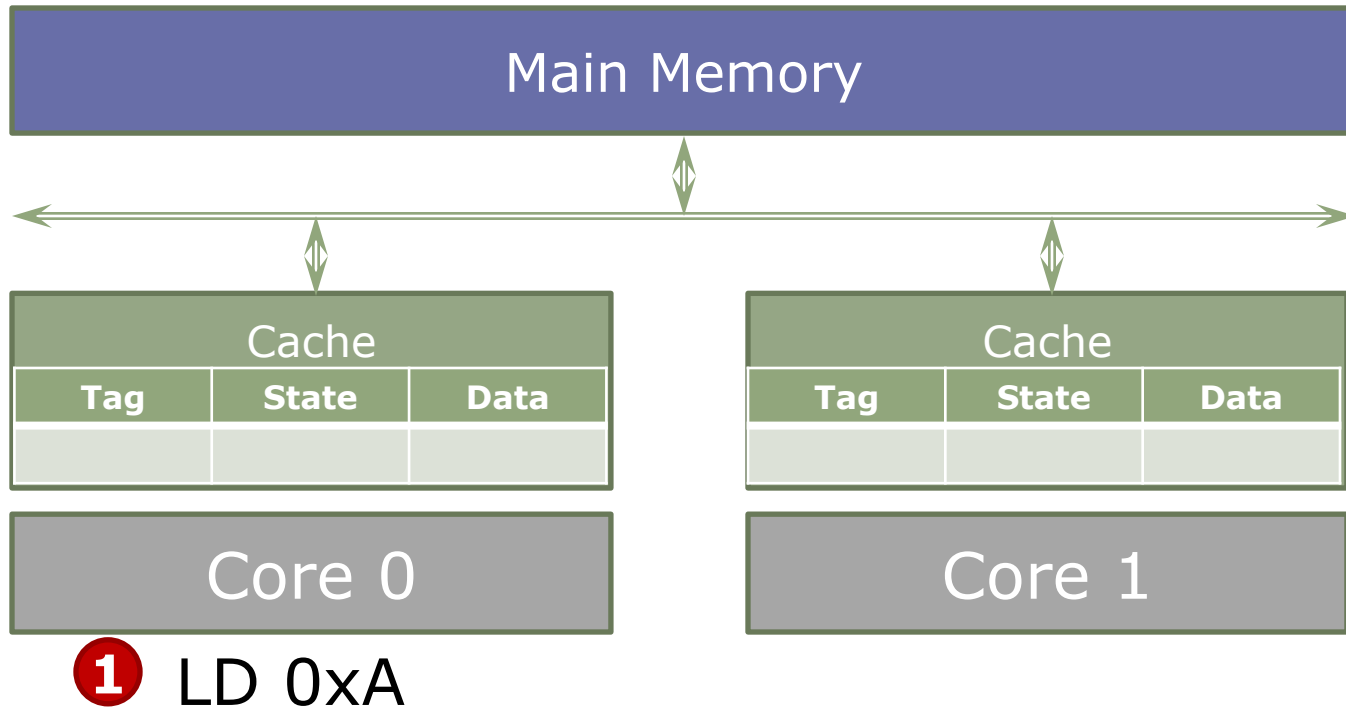
- Assume write-through caches
- Transition nomenclature:
triggering action / taken action(s)

| Actions |
|------------------------|
| Processor Read (PrRd) |
| Processor Write (PrWr) |
| Bus Read (BusRd) |
| Bus Write (BusWr) |

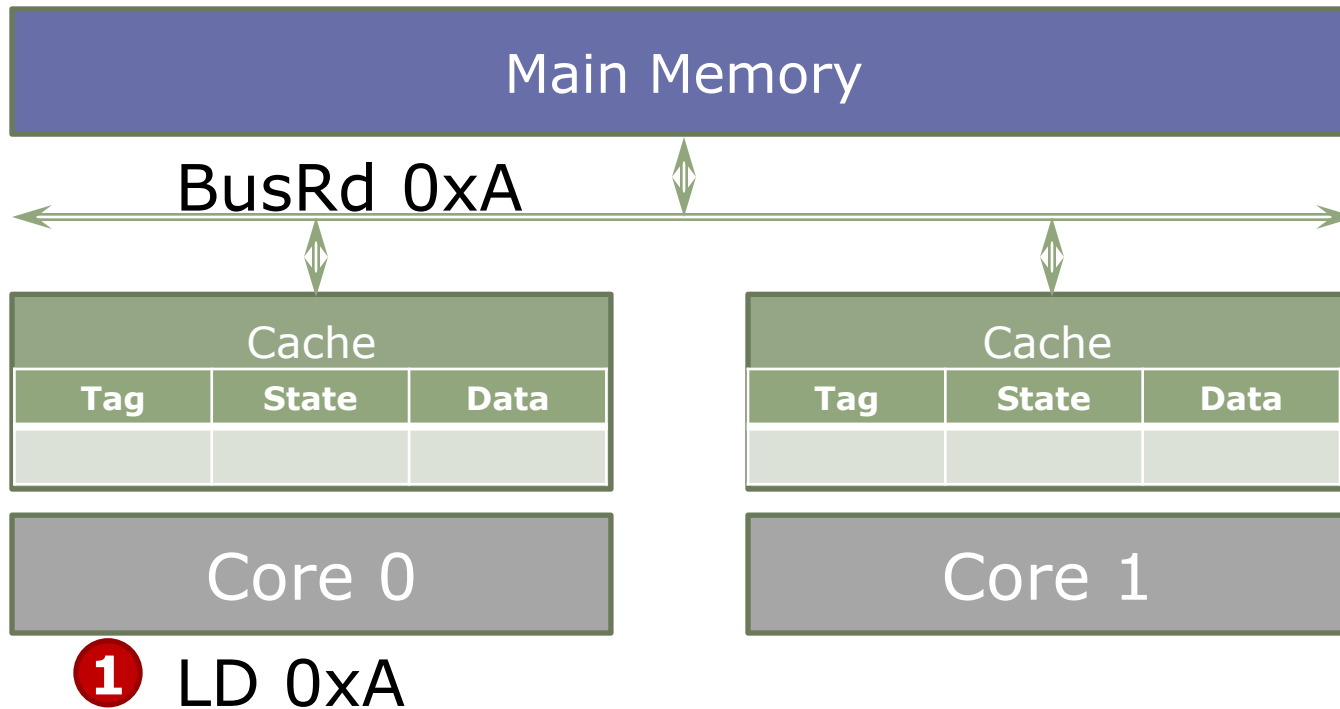
Valid/Invalid Example



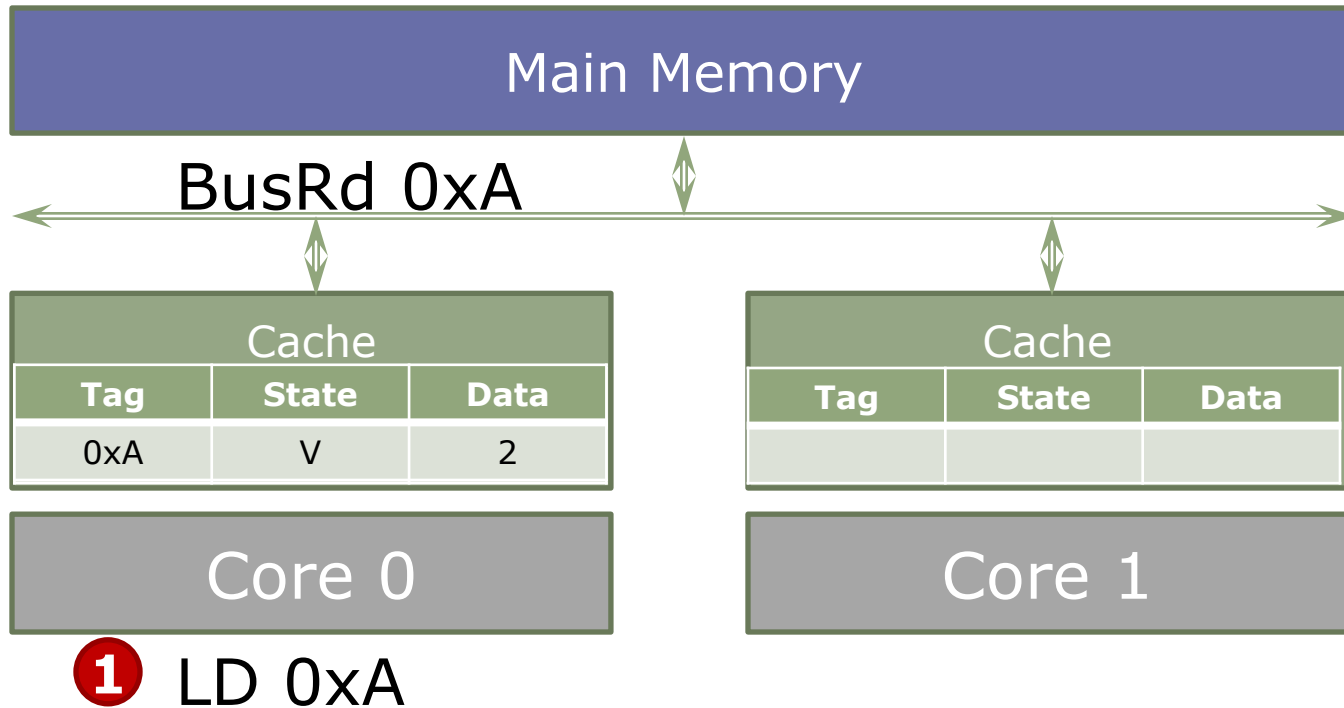
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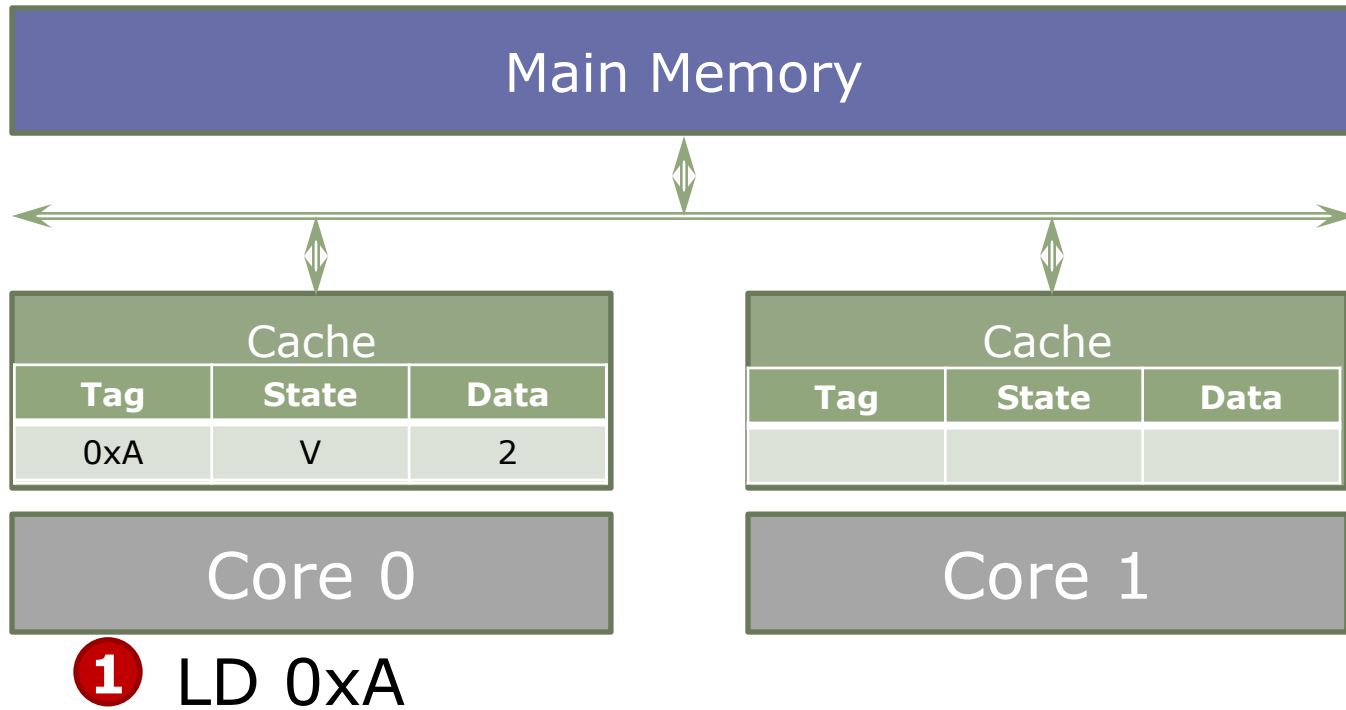
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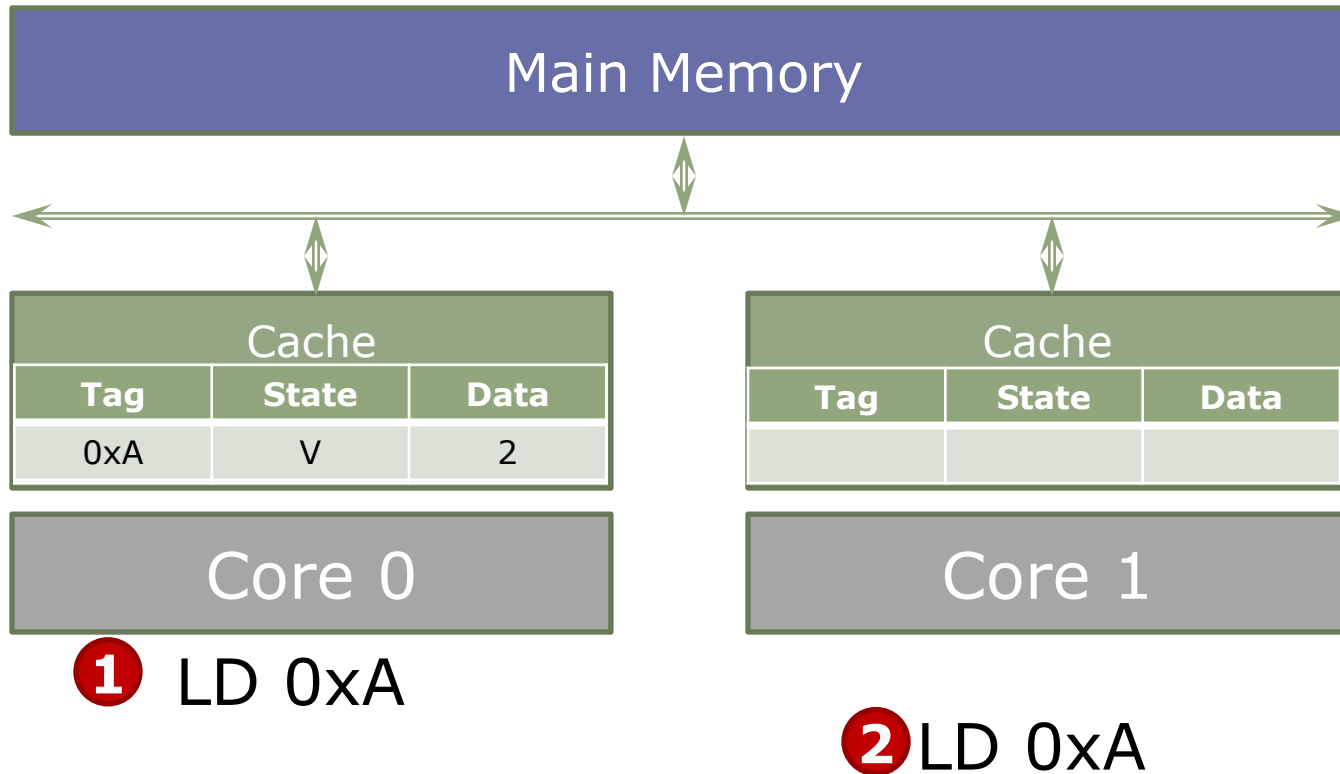
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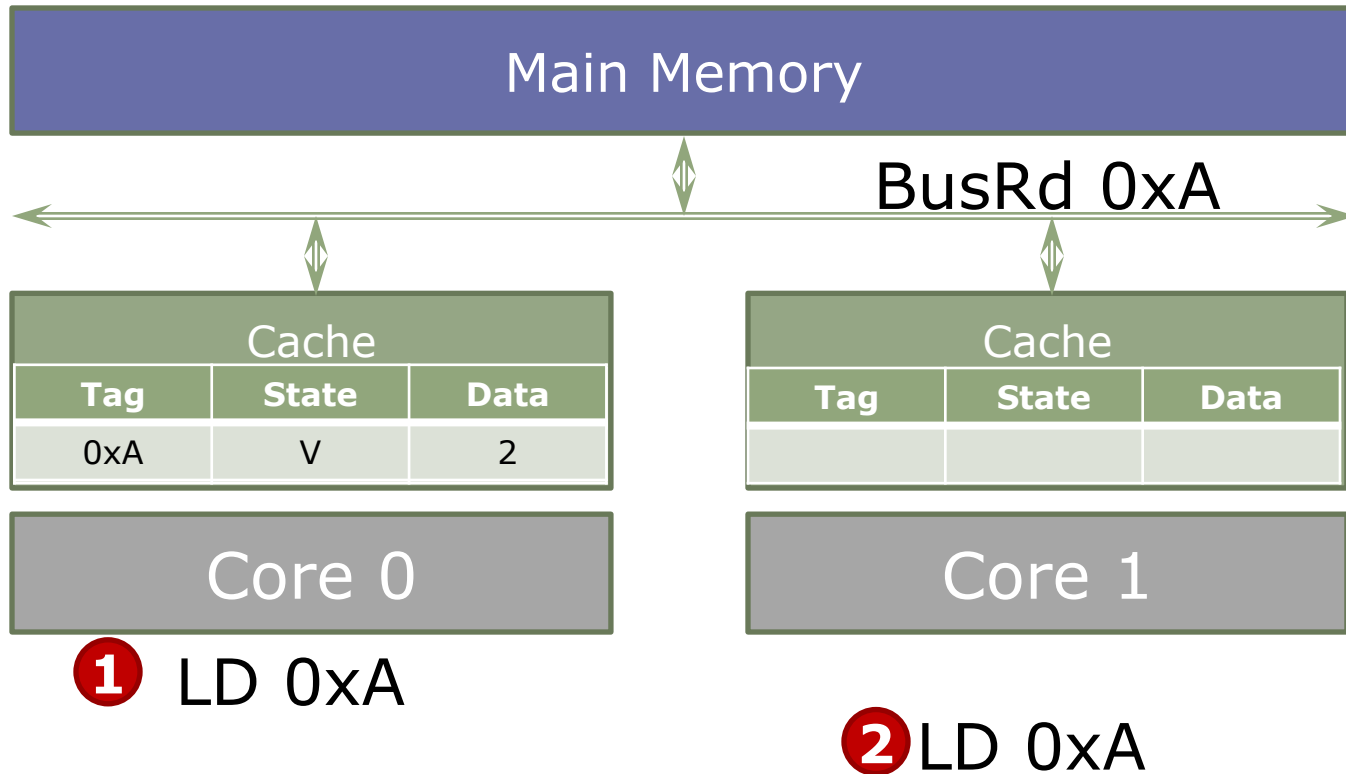
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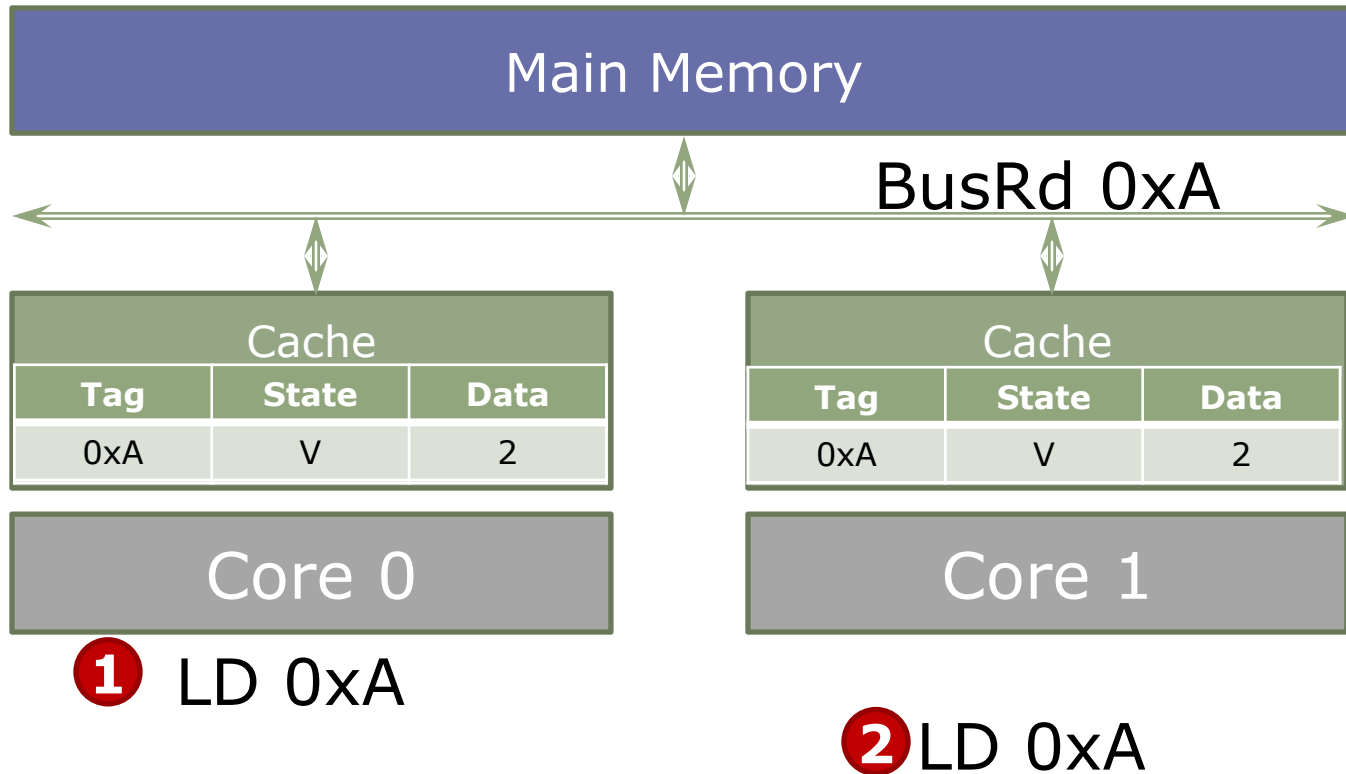
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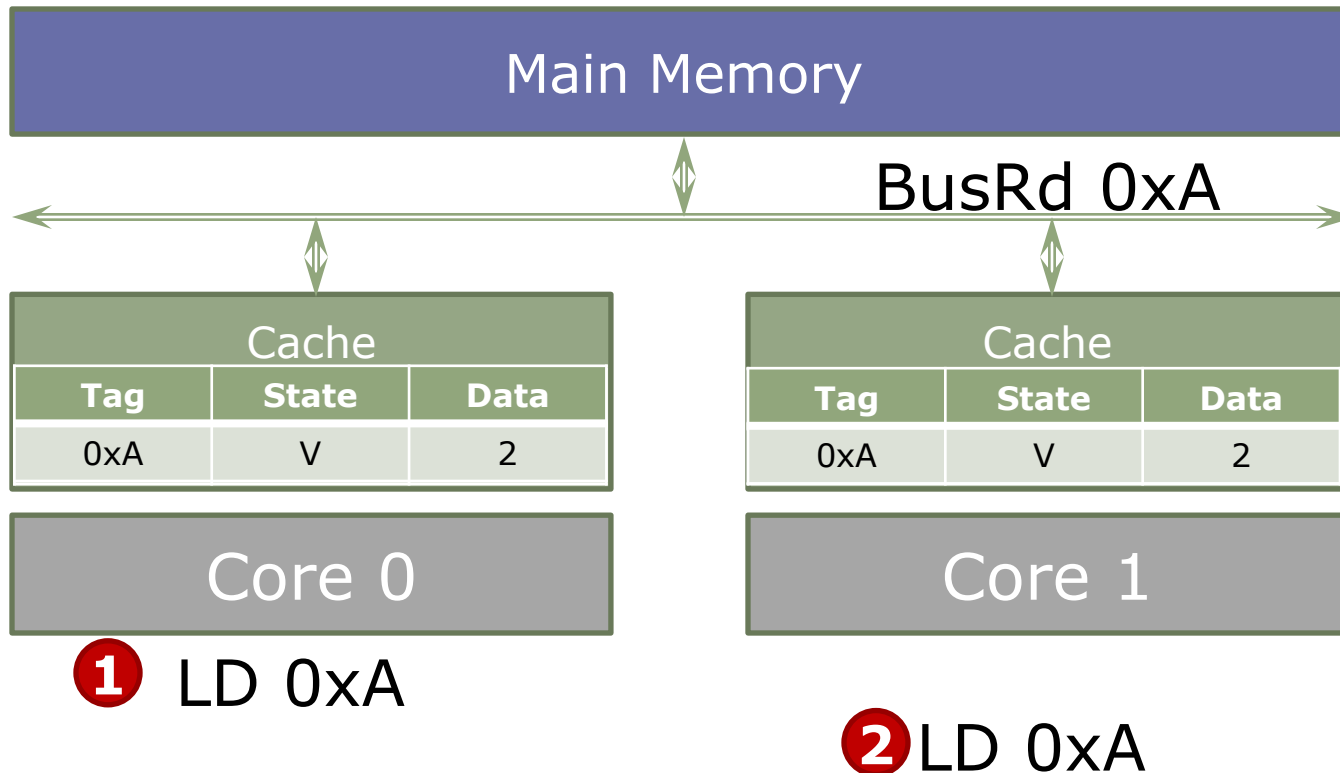
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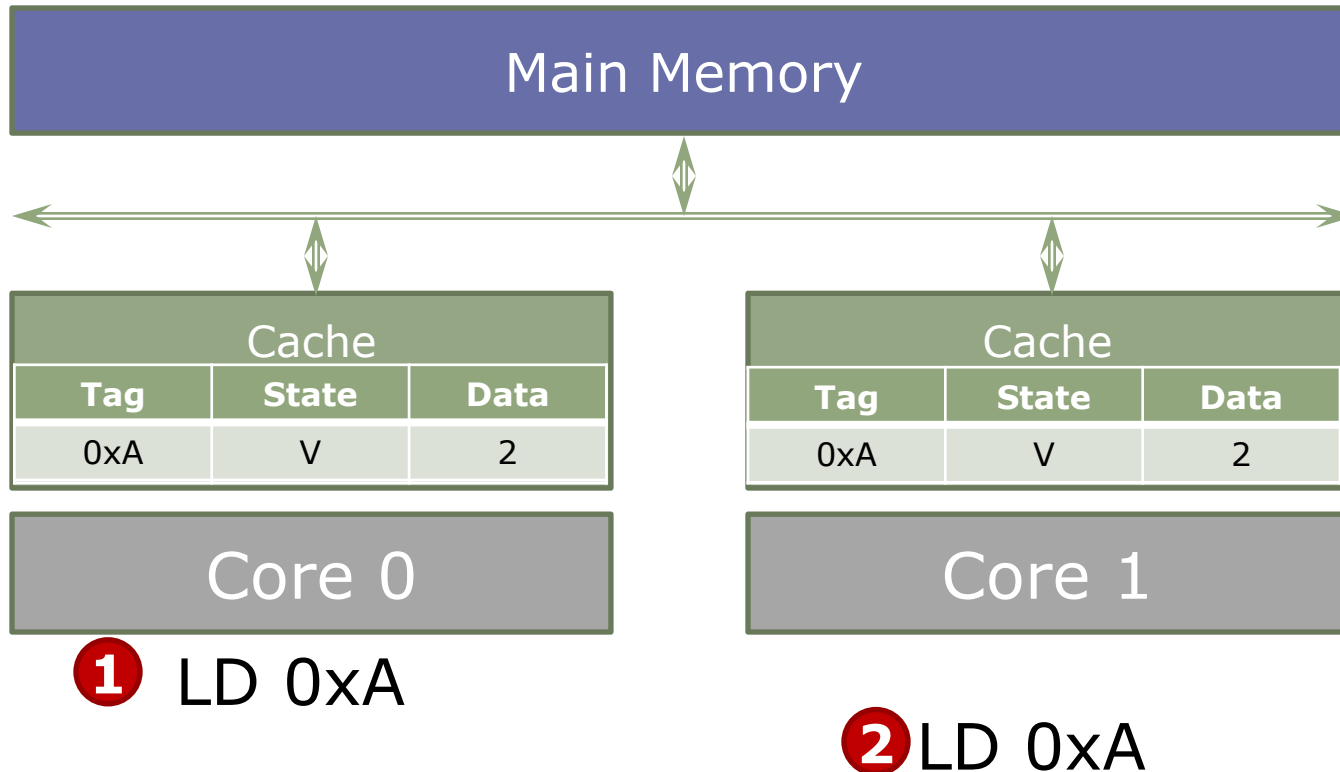


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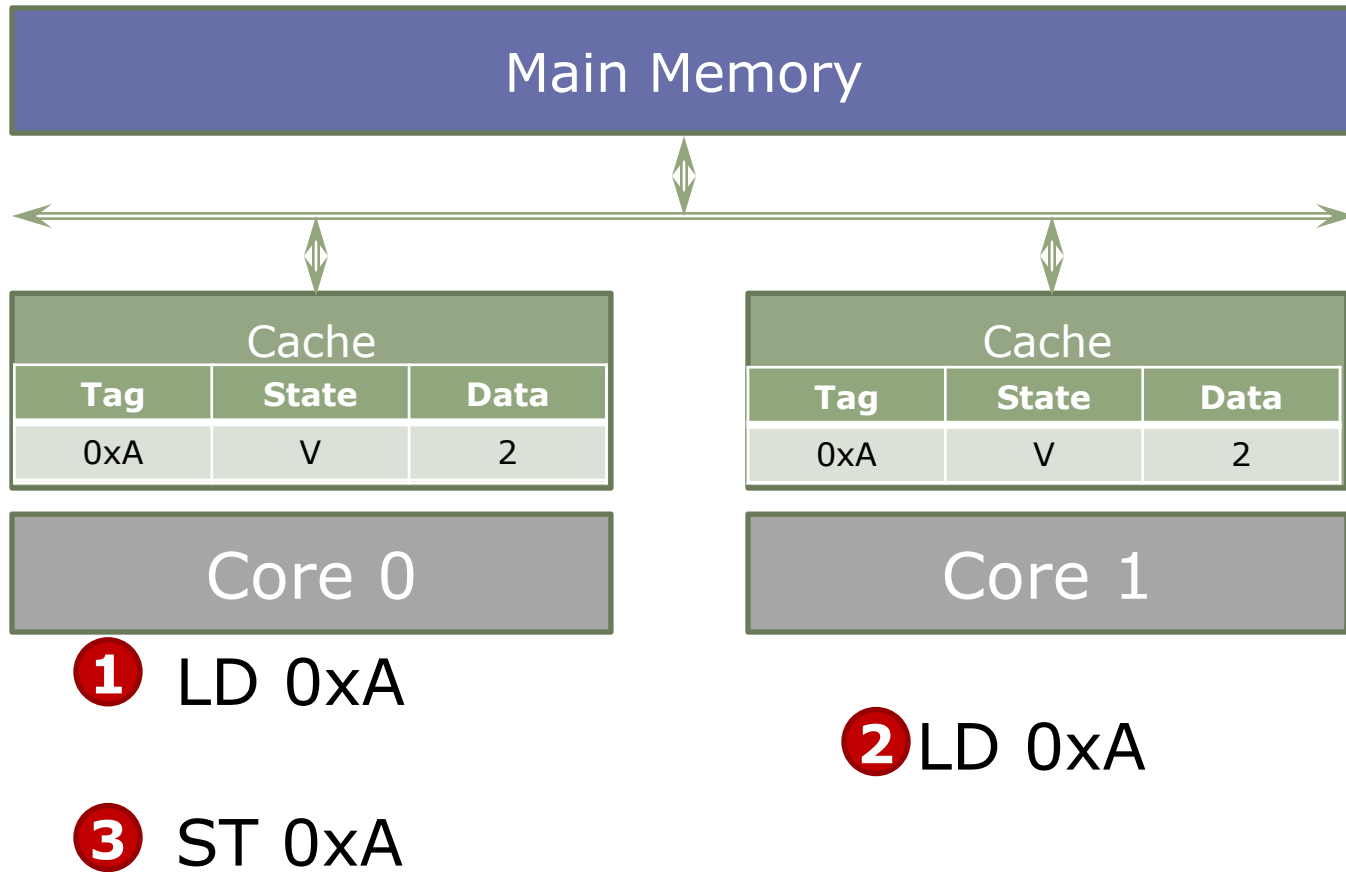


Additional loads satisfied locally, without BusRd

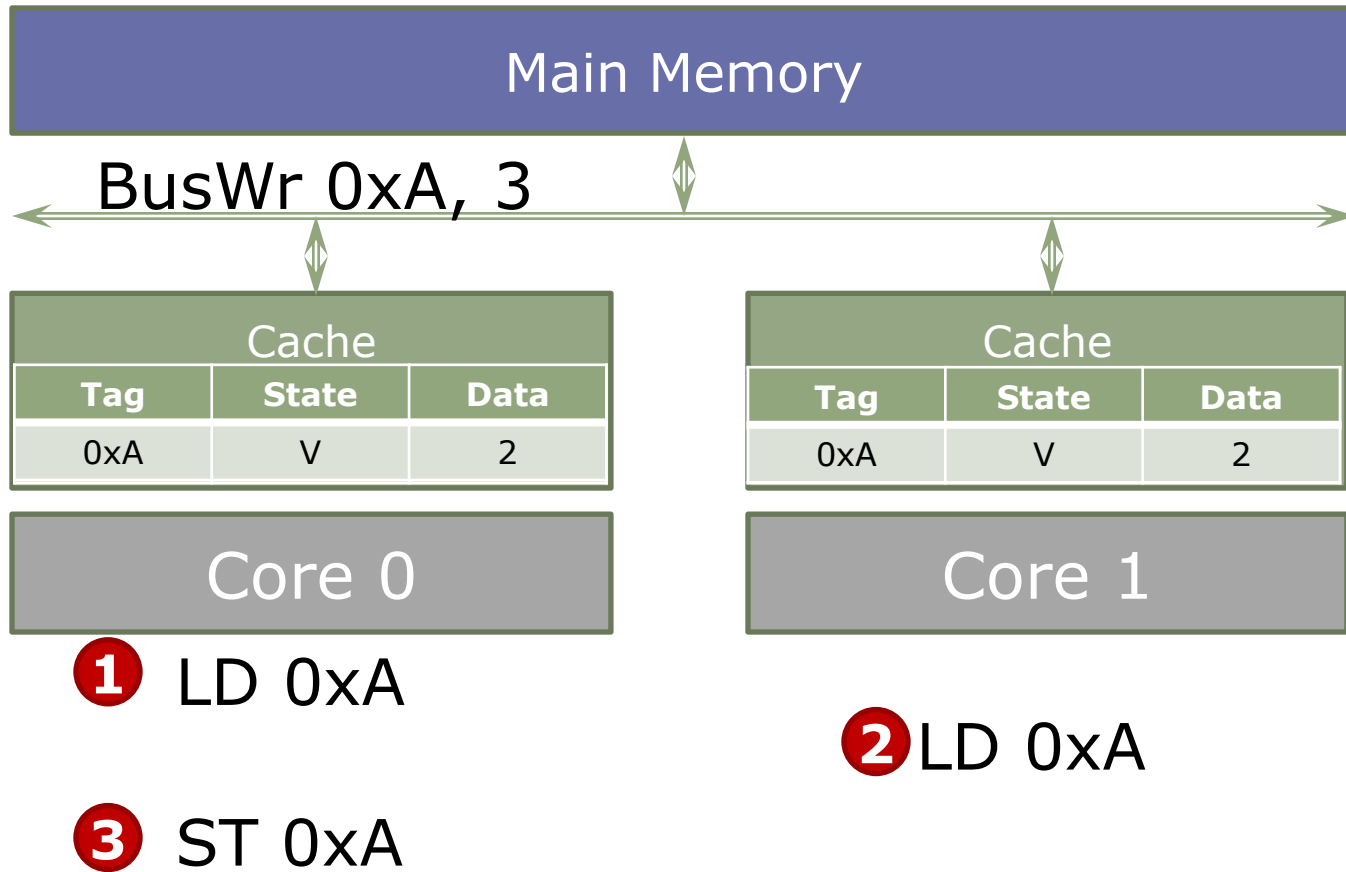
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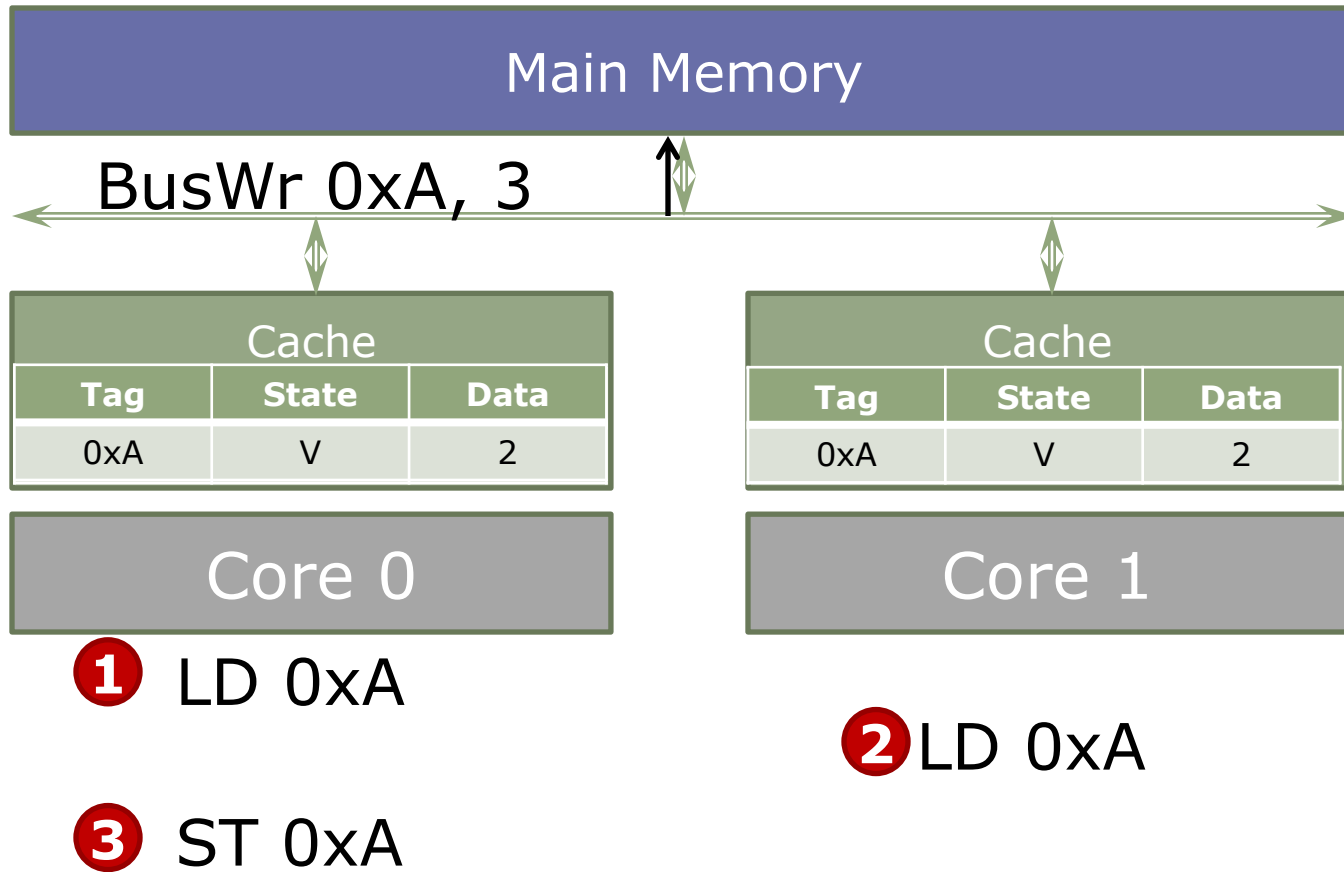
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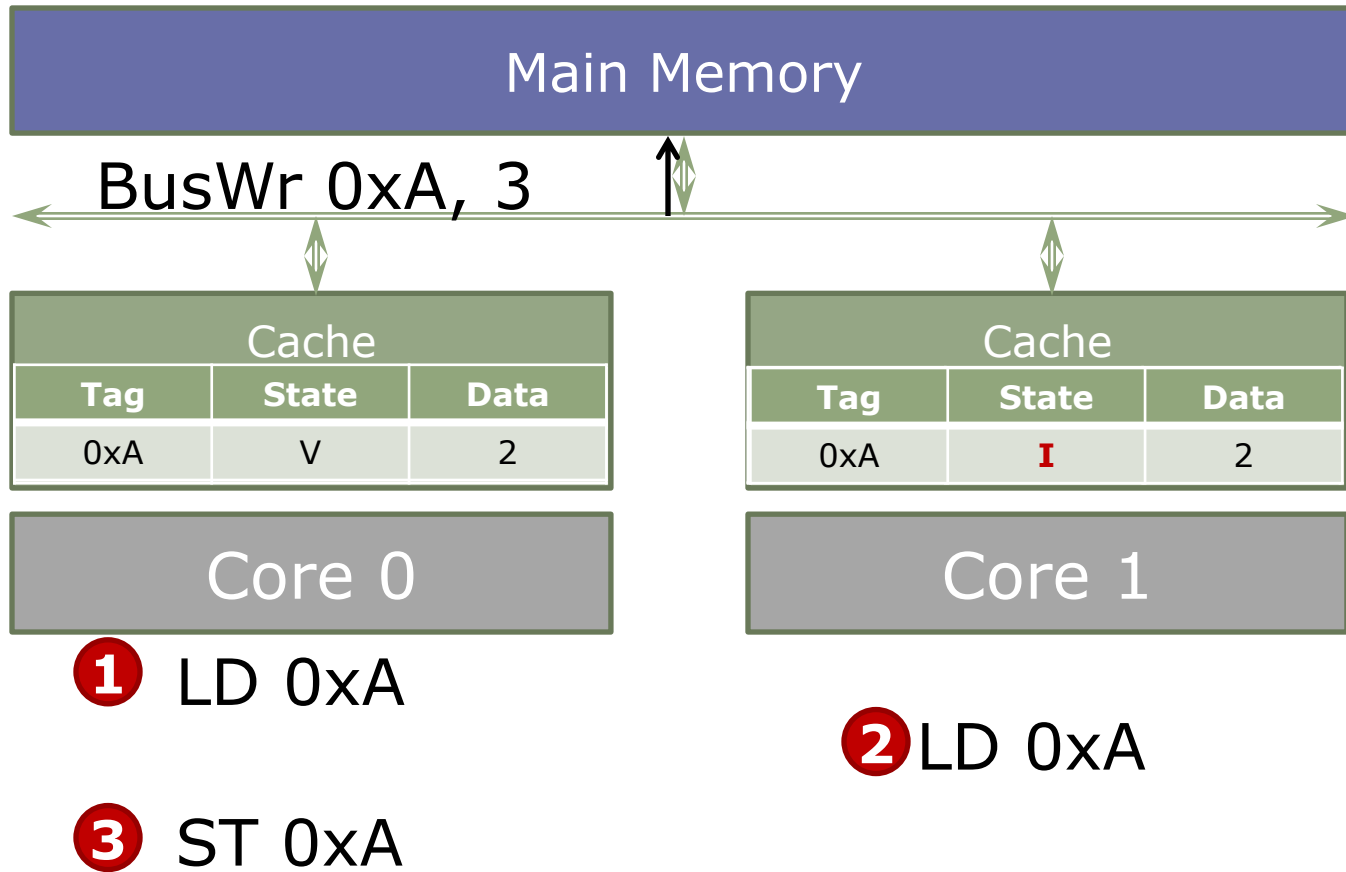
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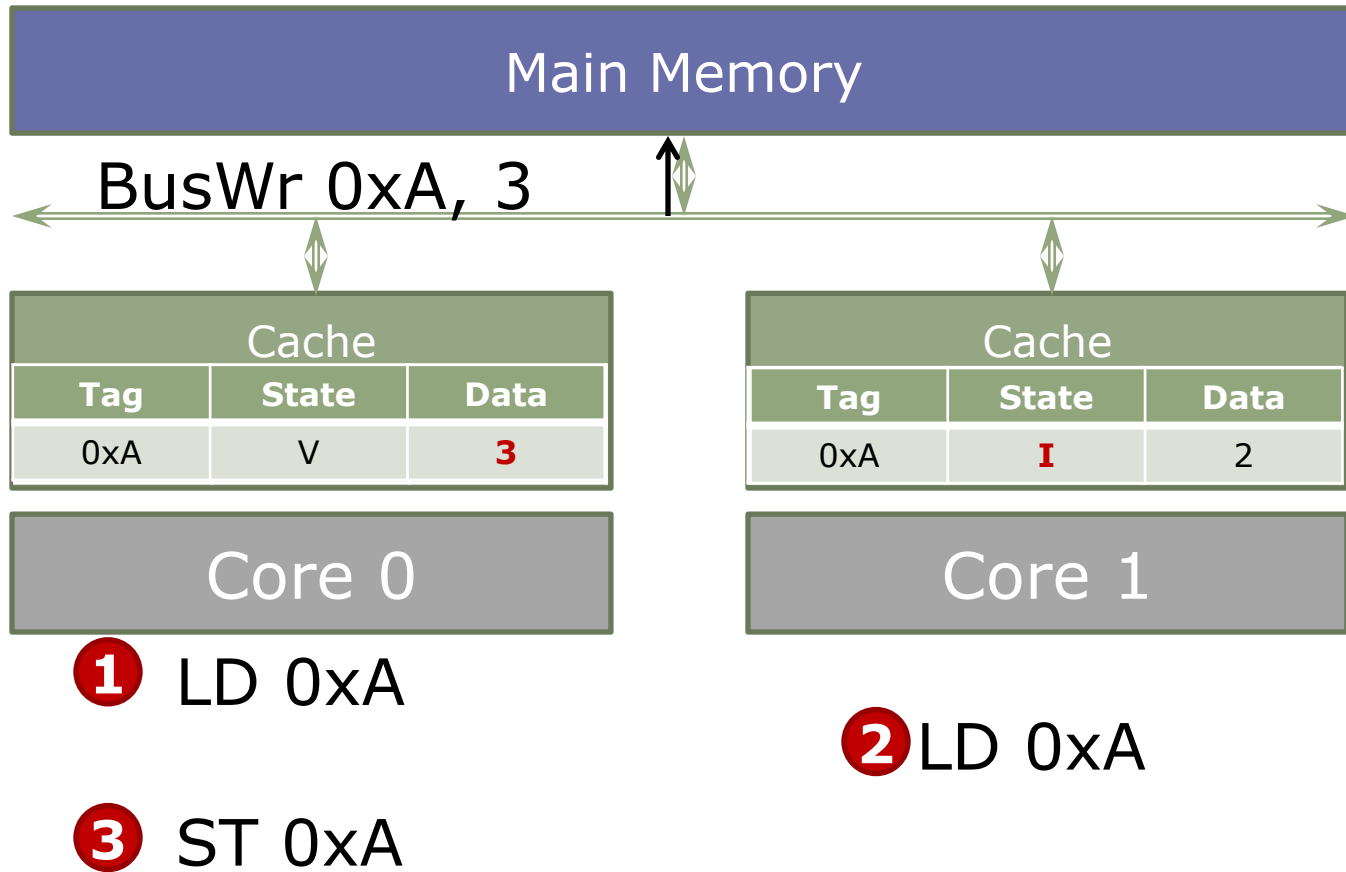
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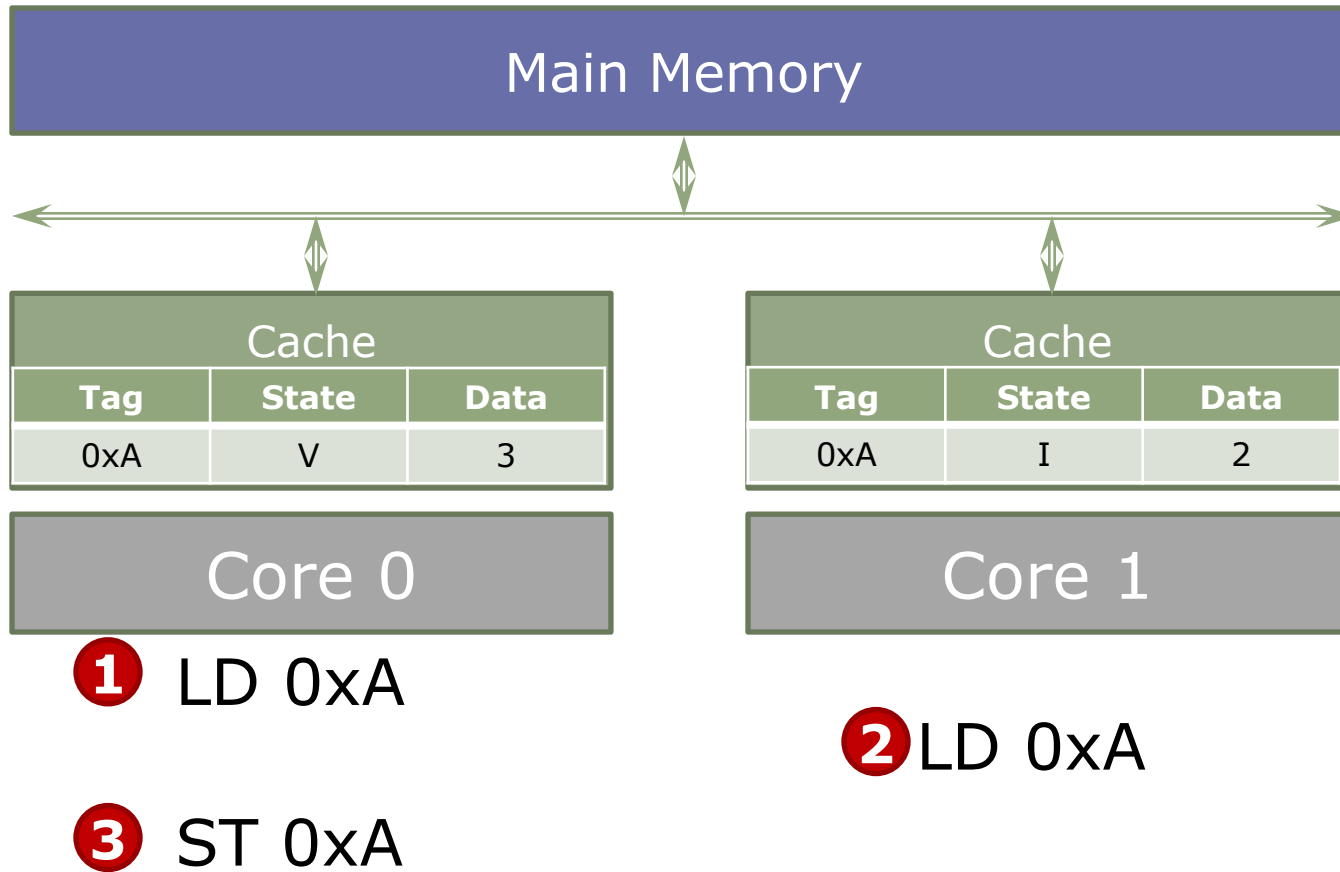
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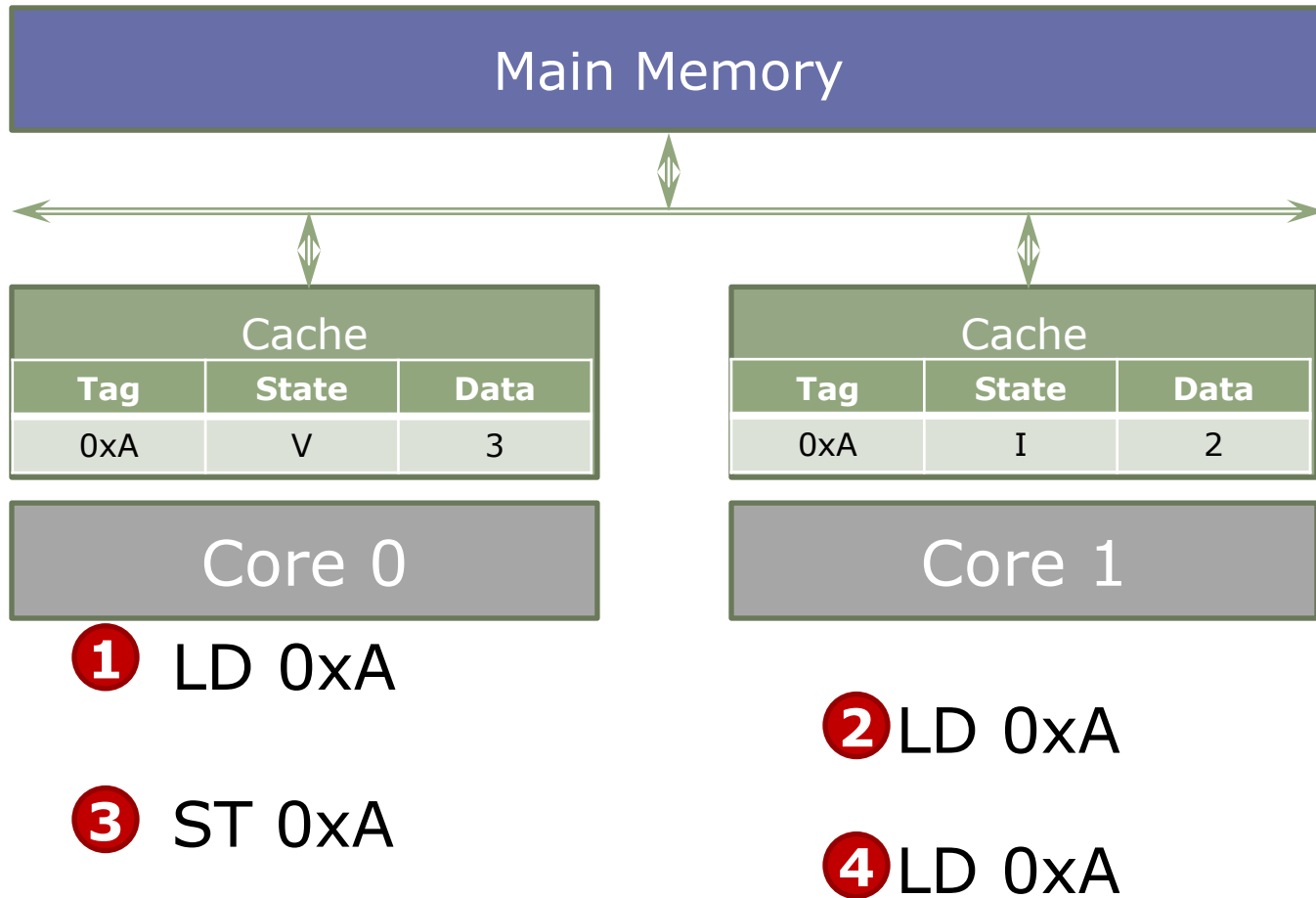
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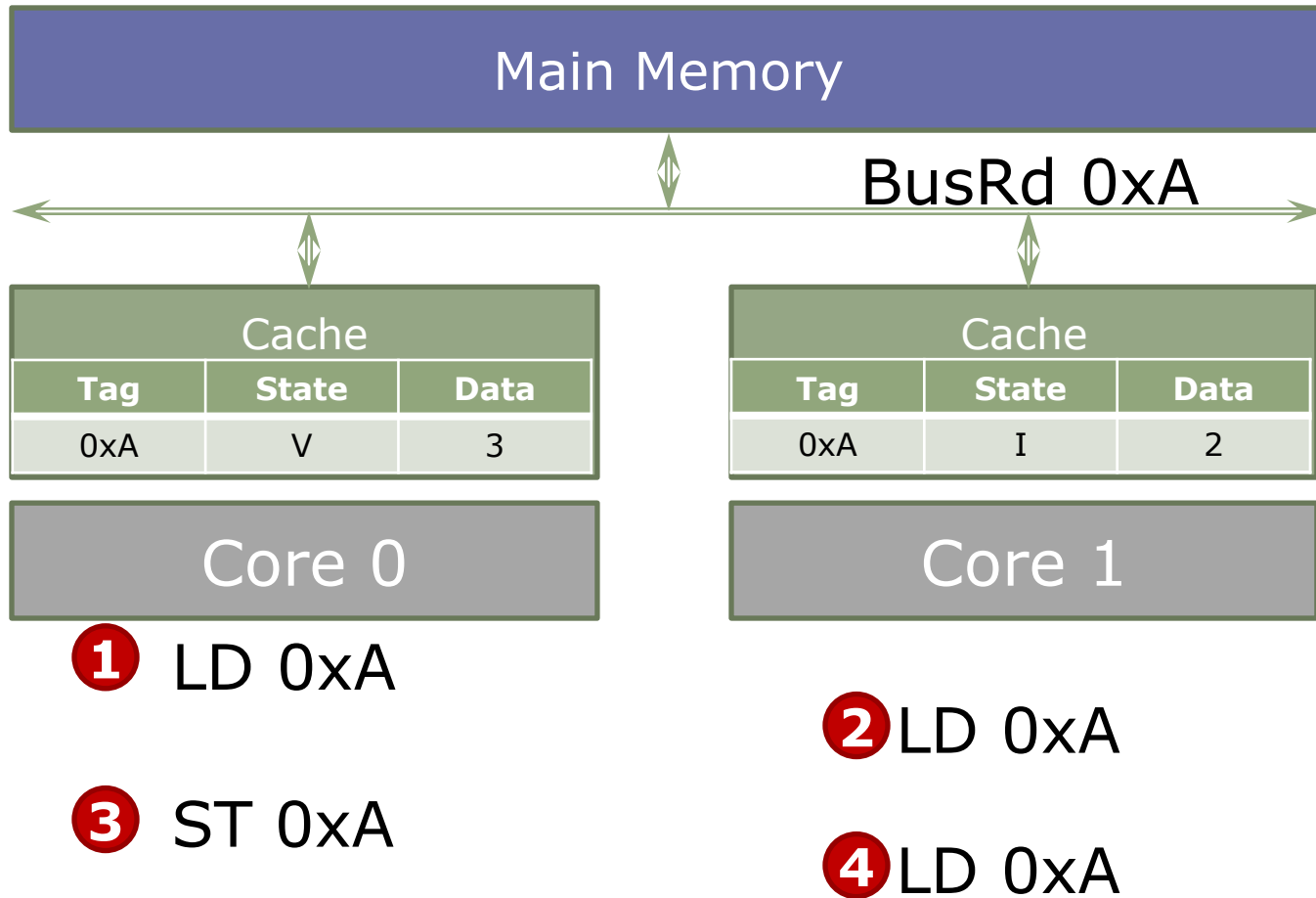
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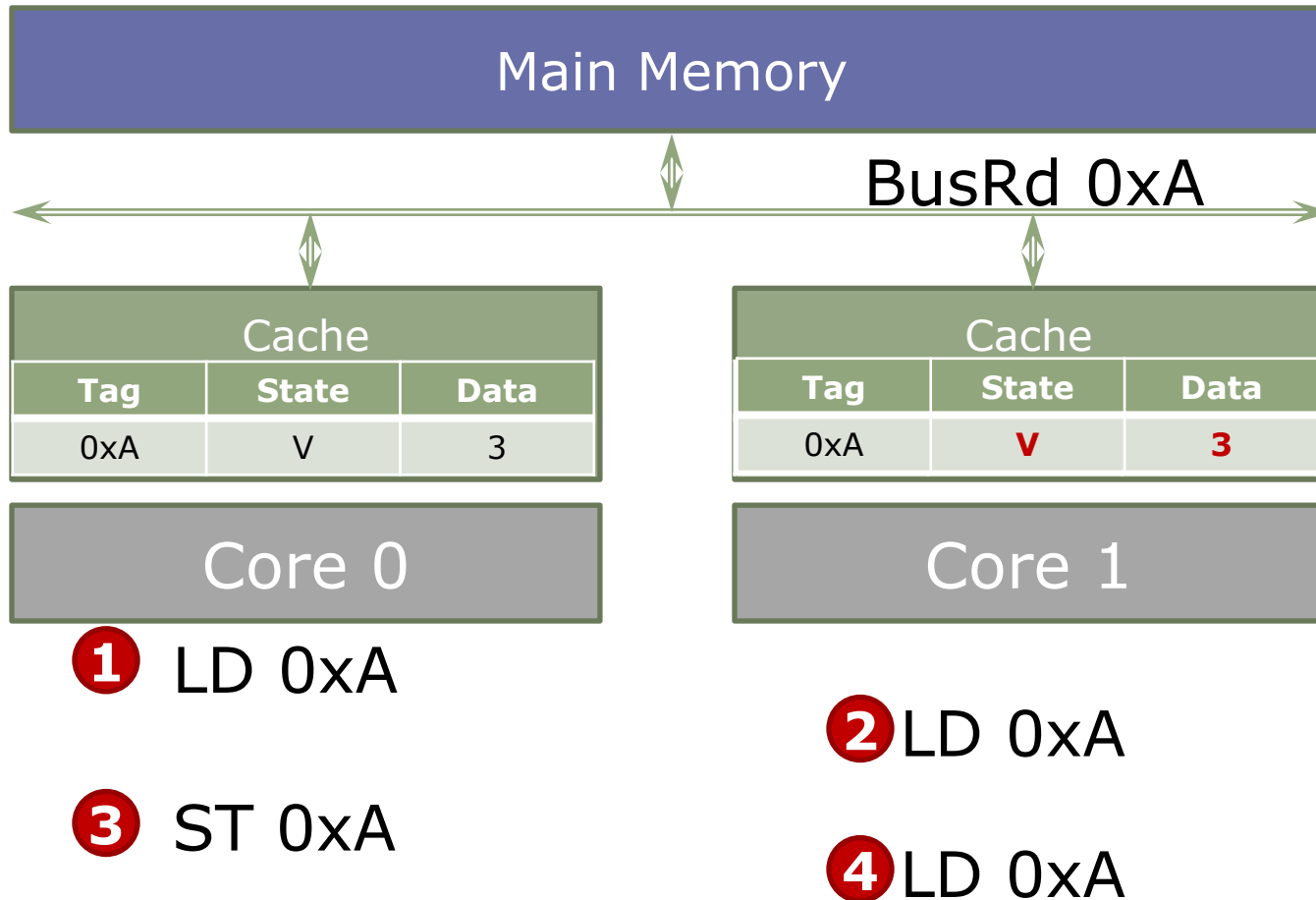
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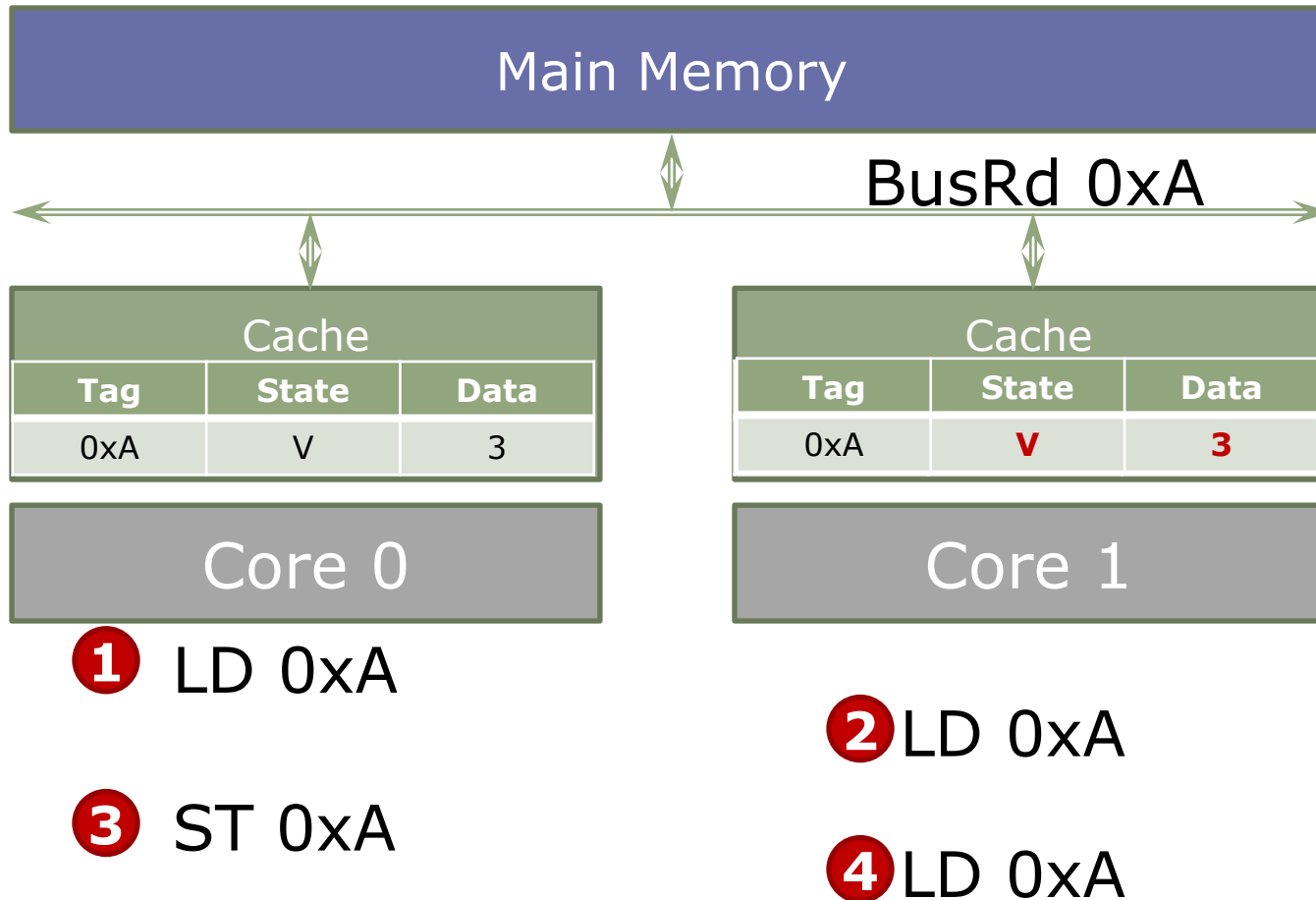
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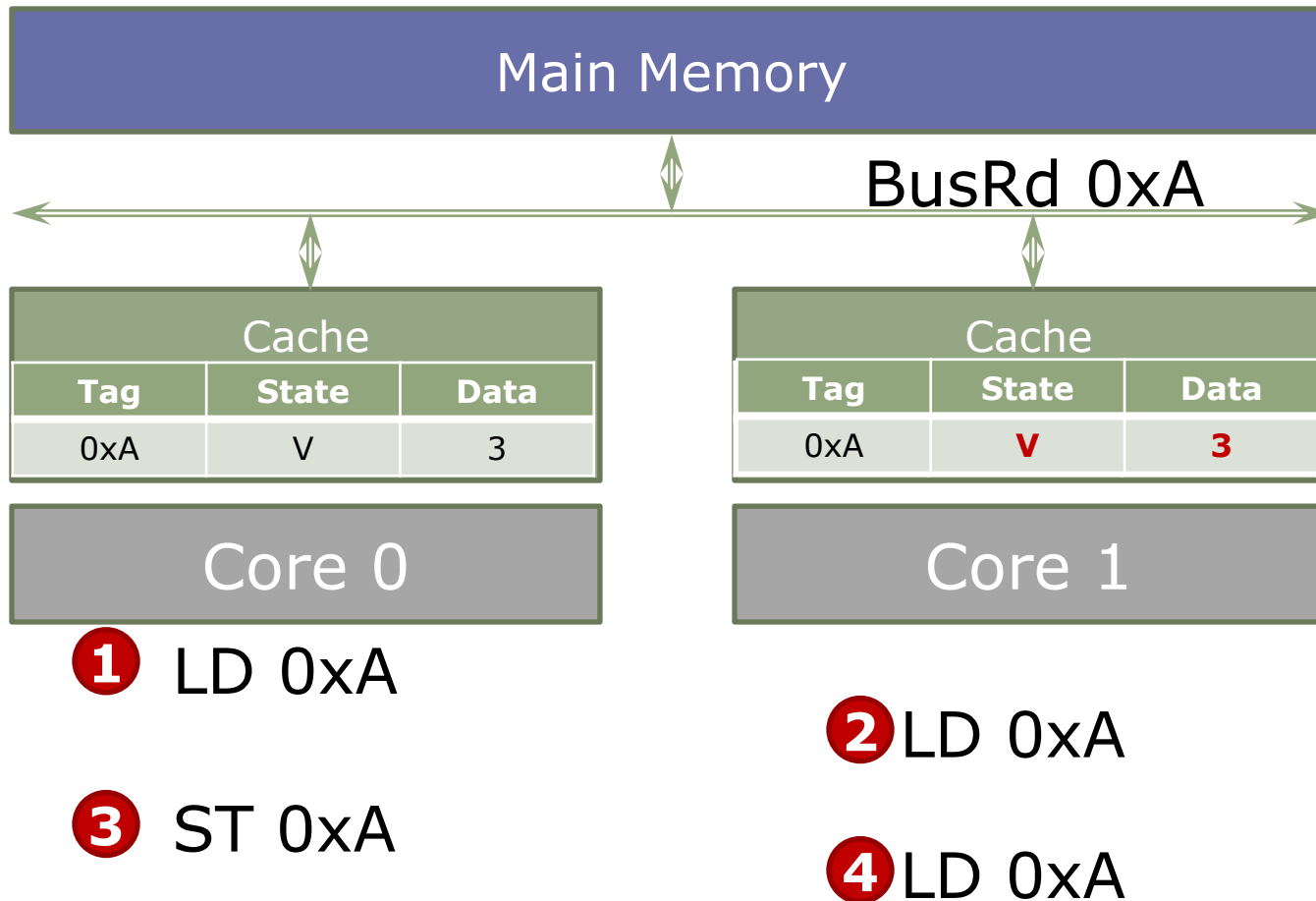


Valid/Invalid Example



VI Problems?

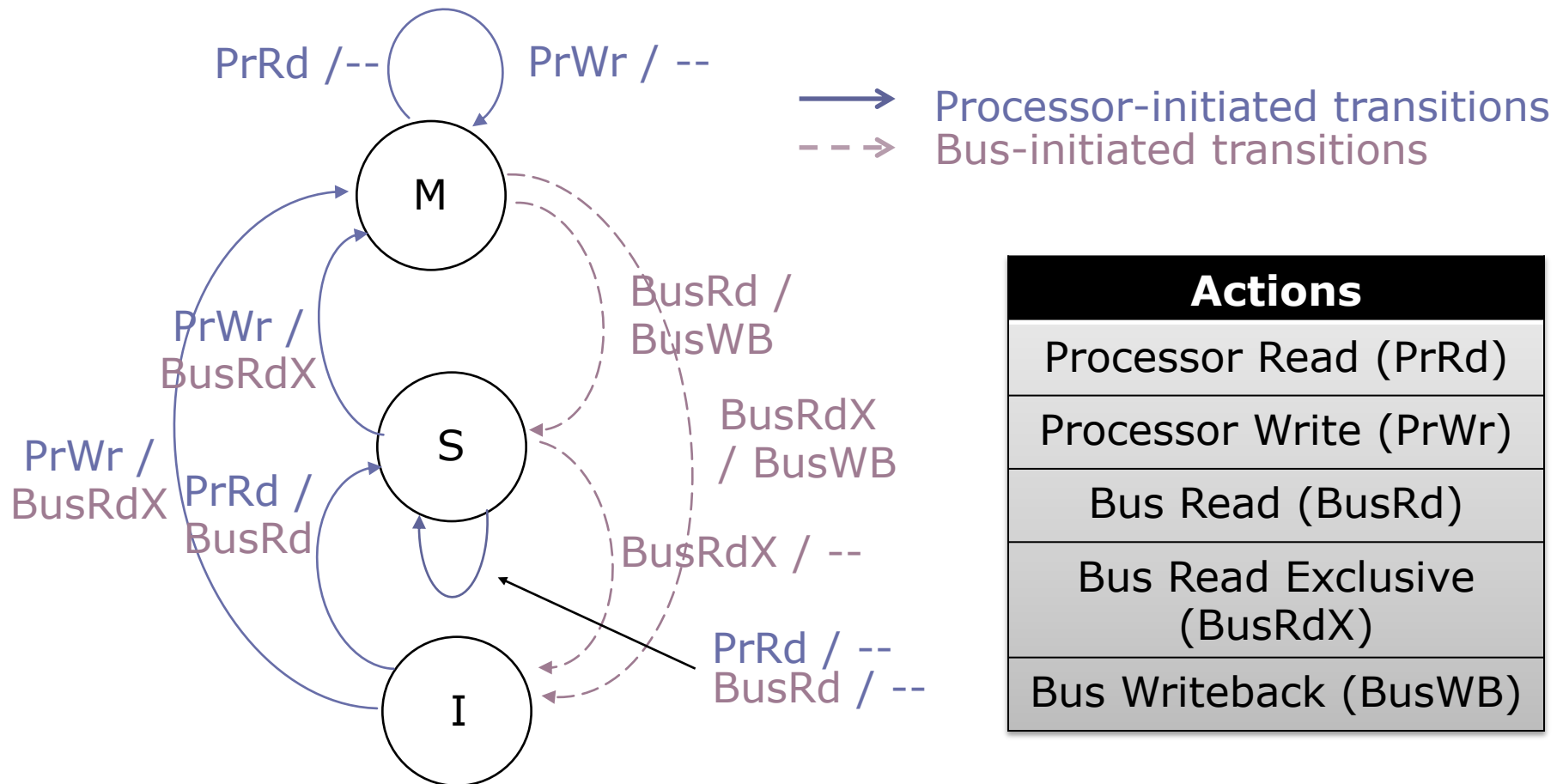
Valid/Invalid Example



VI Problems? **Every write updates main memory**
Every write requires broadcast & snoop

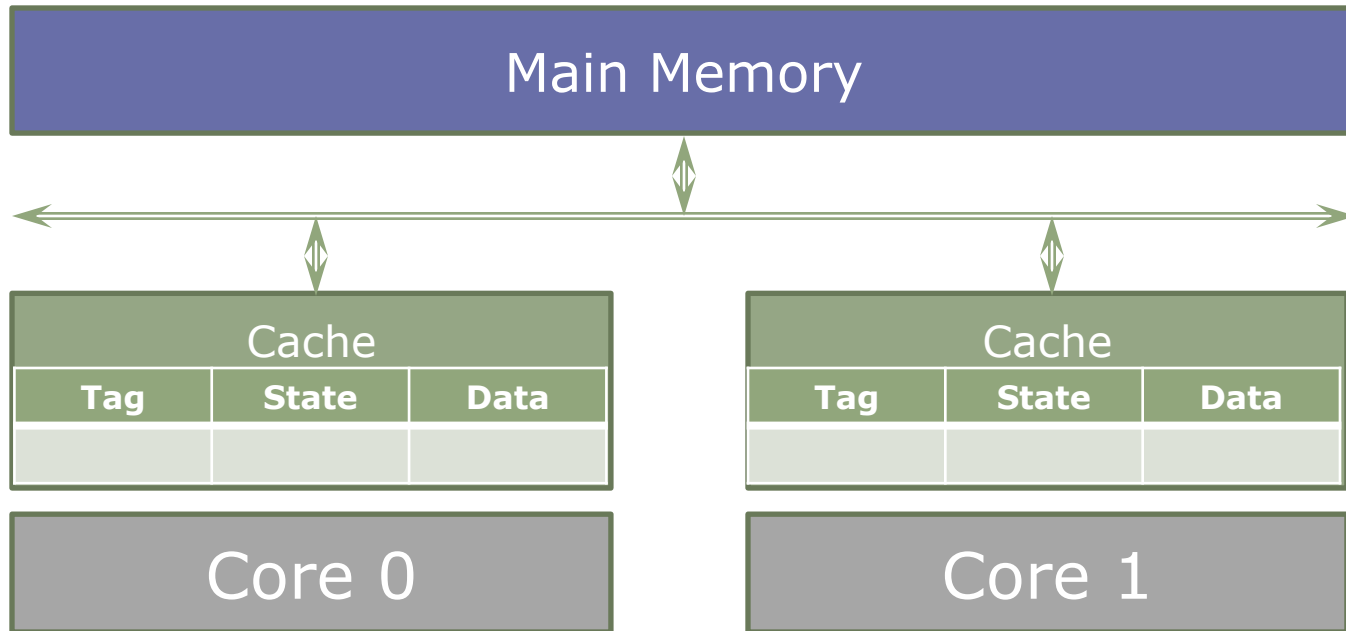
Modified/Shared/Invalid (MSI) Protocol

- Allows writeback caches + satisfying writes locally

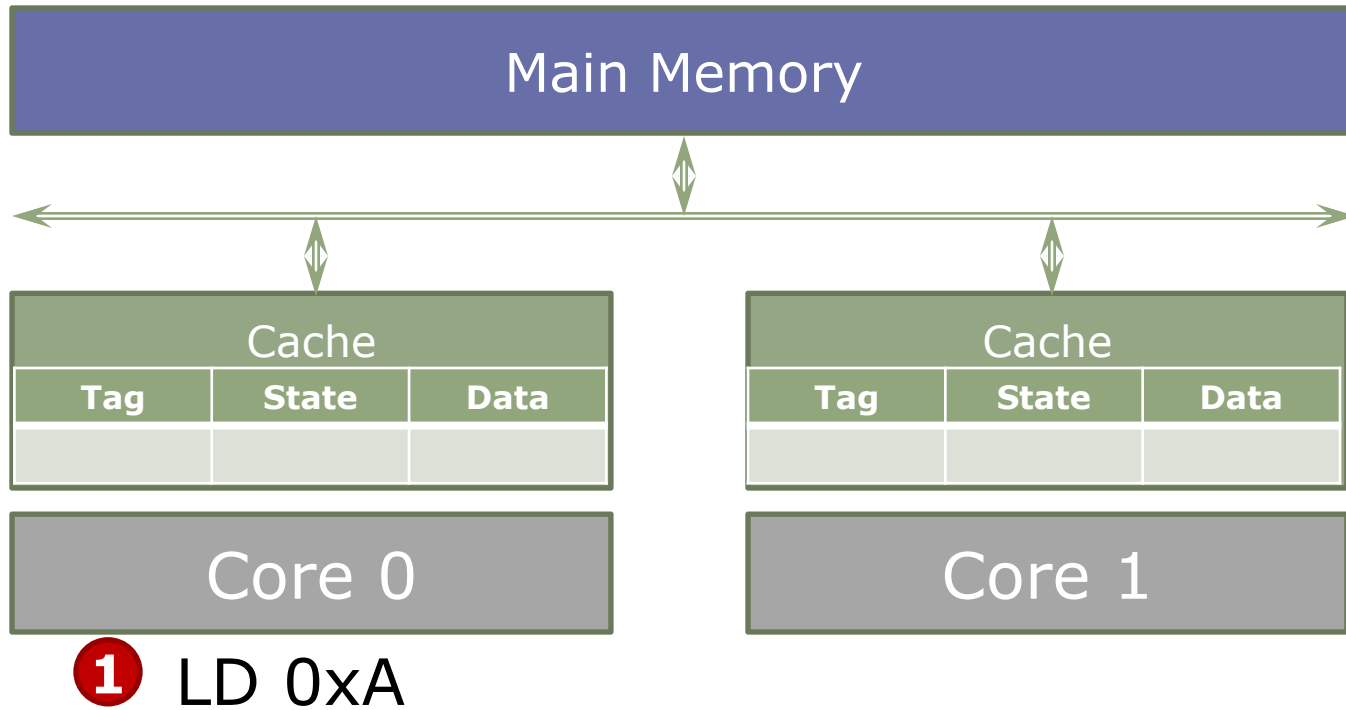


| Actions |
|-----------------------------|
| Processor Read (PrRd) |
| Processor Write (PrWr) |
| Bus Read (BusRd) |
| Bus Read Exclusive (BusRdX) |
| Bus Writeback (BusWB) |

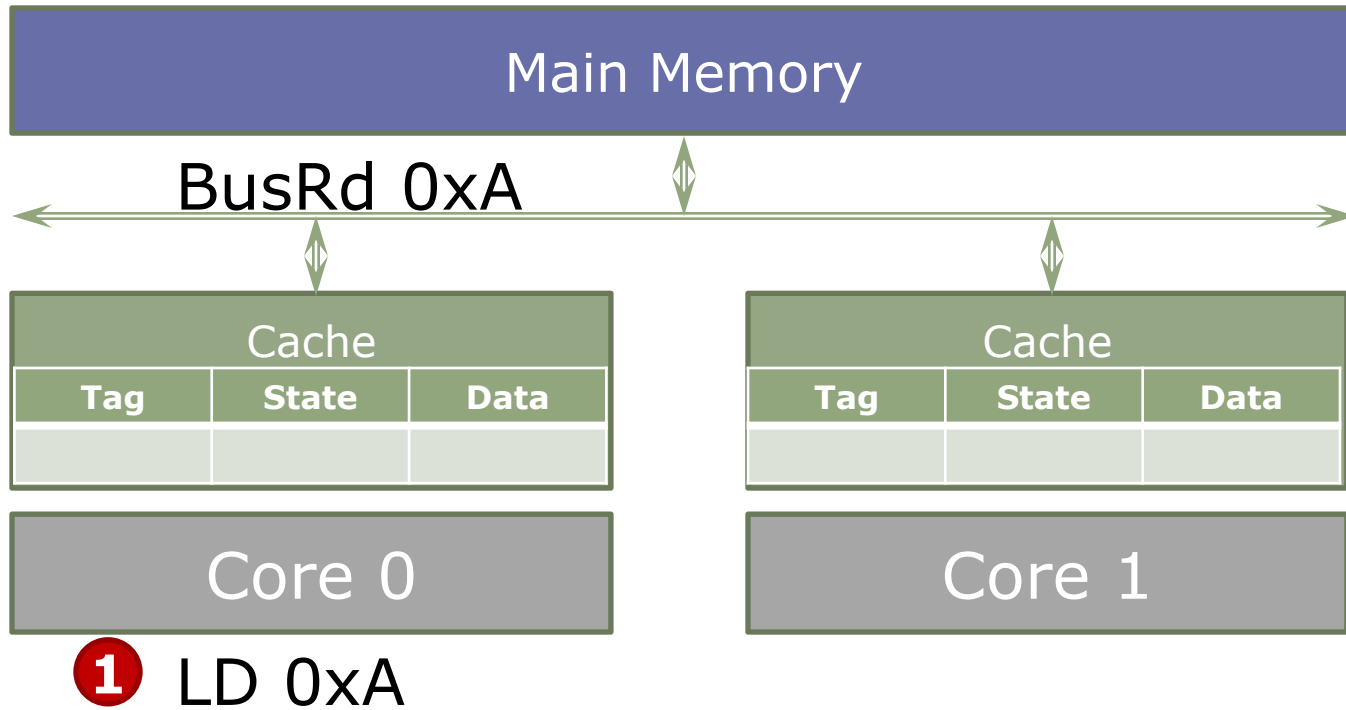
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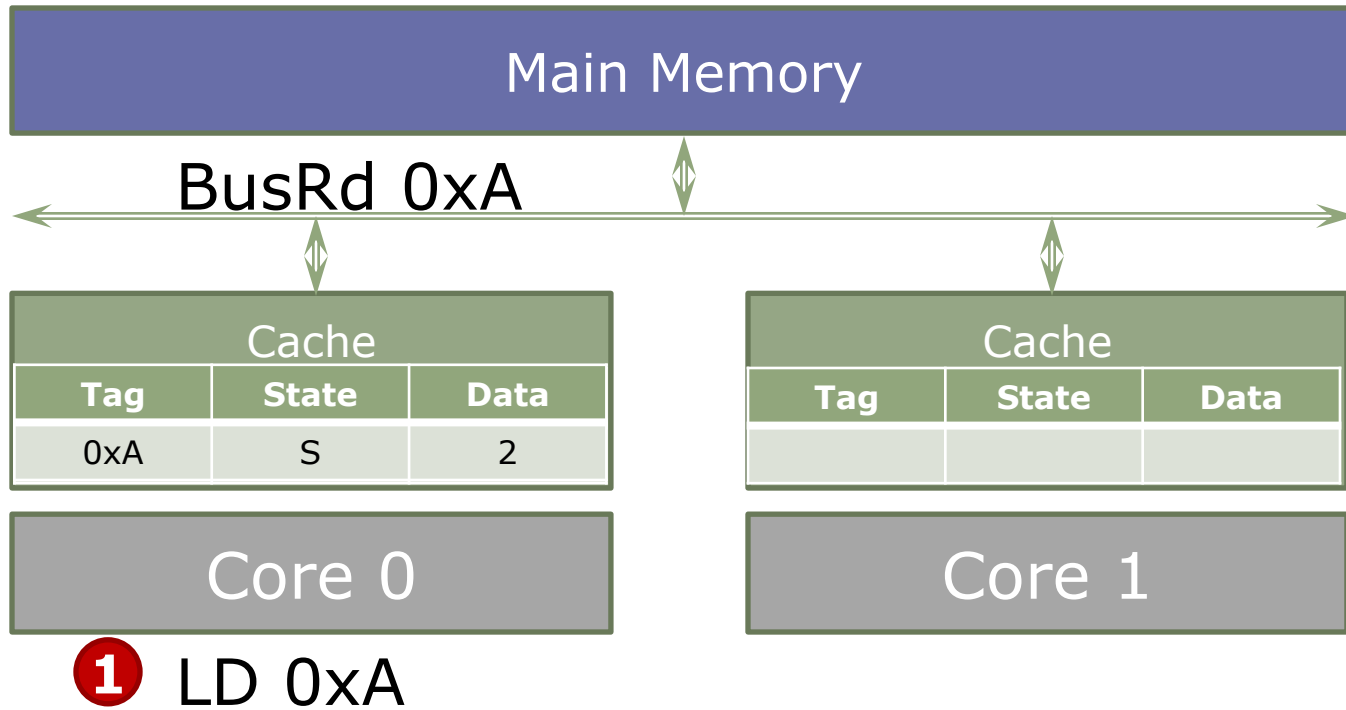
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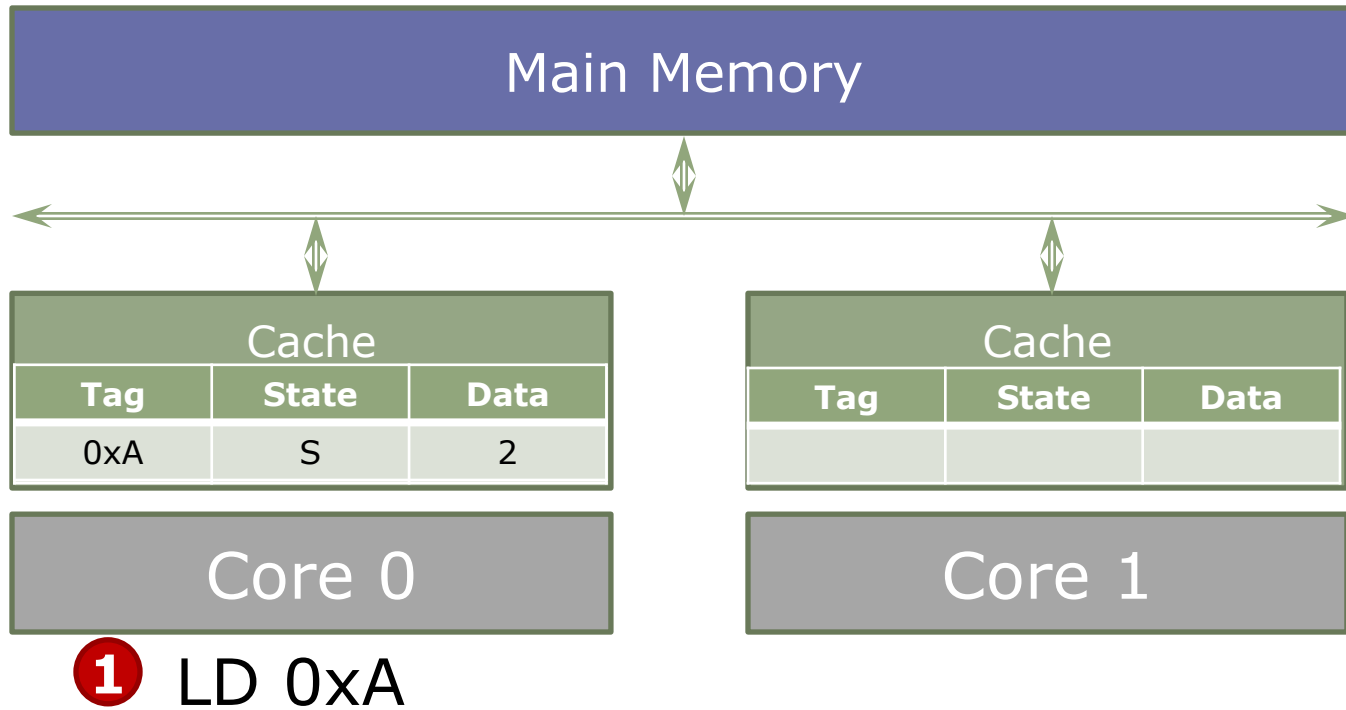
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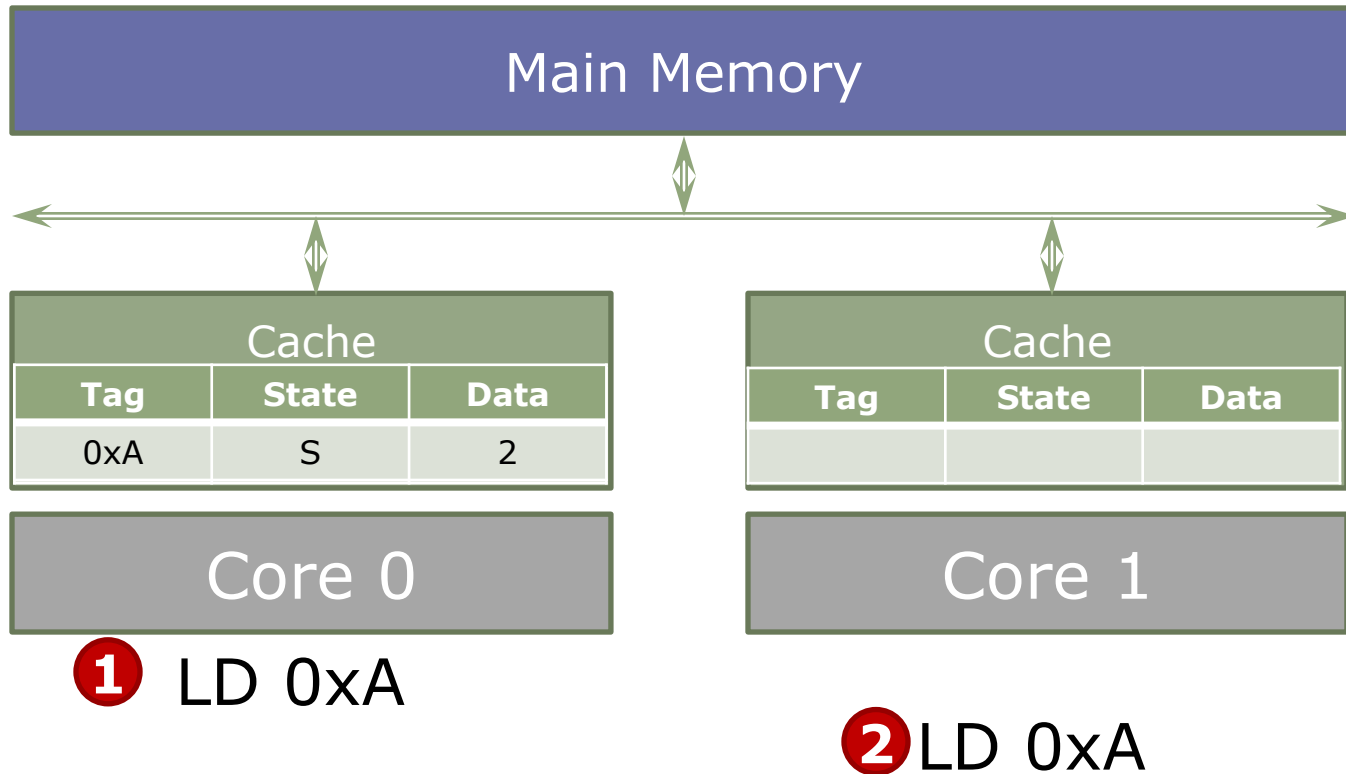
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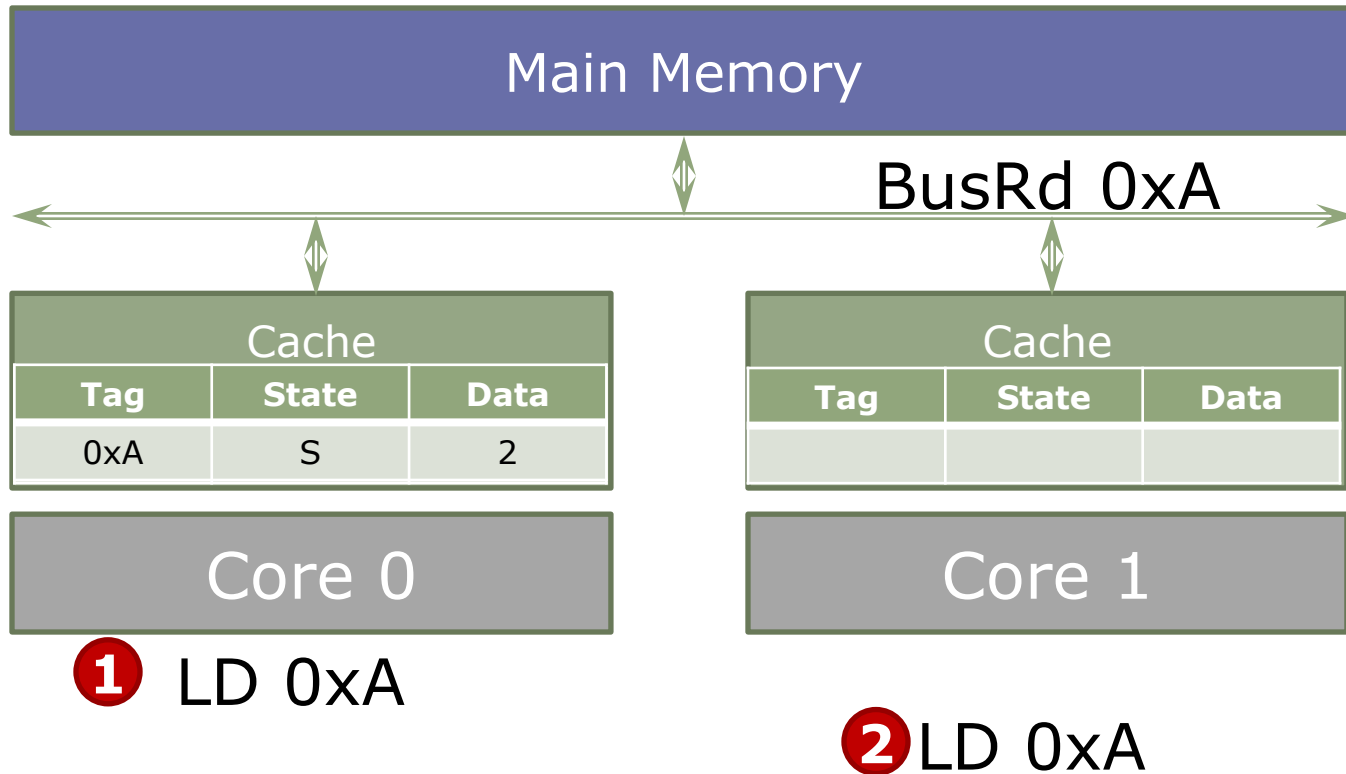
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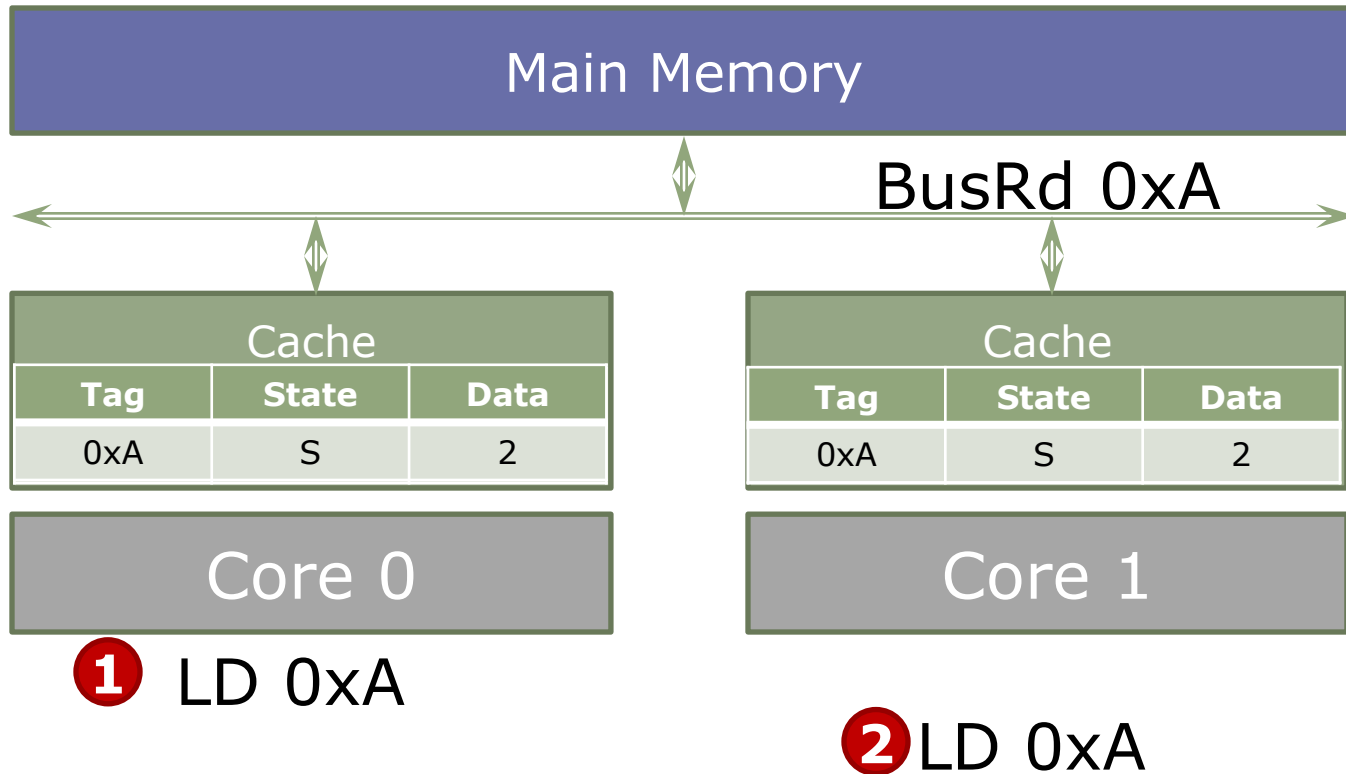
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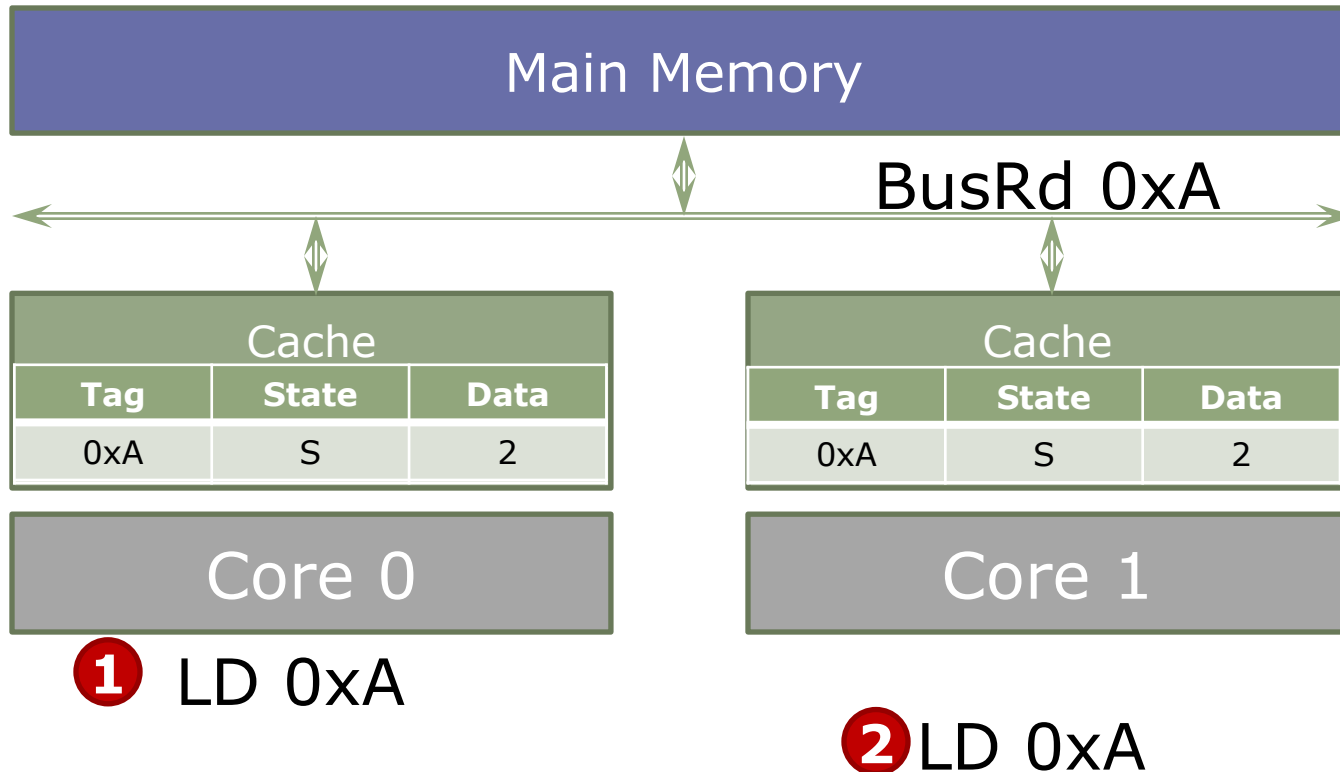
MSI Example



MSI Example

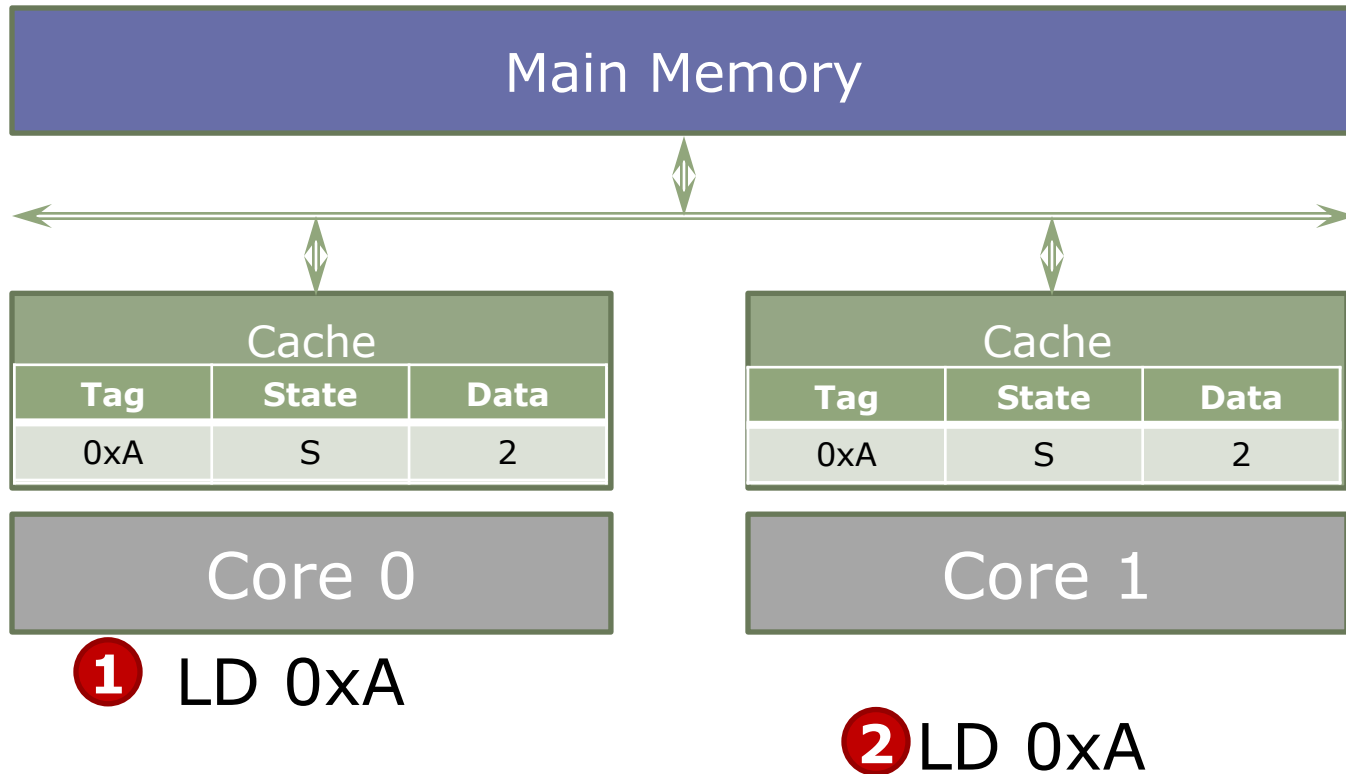


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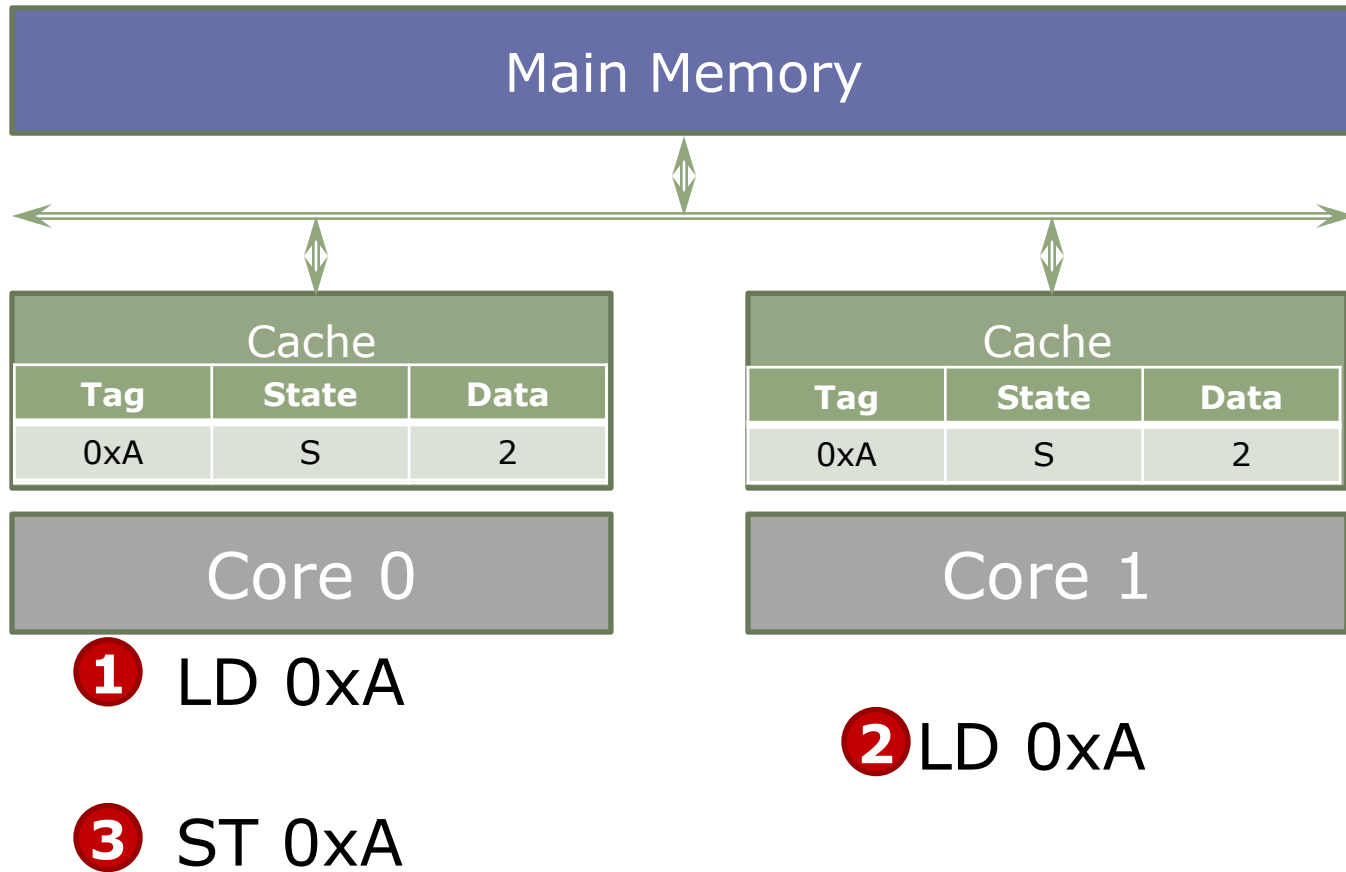


Additional loads satisfied locally, without BusRd
(like in VI)

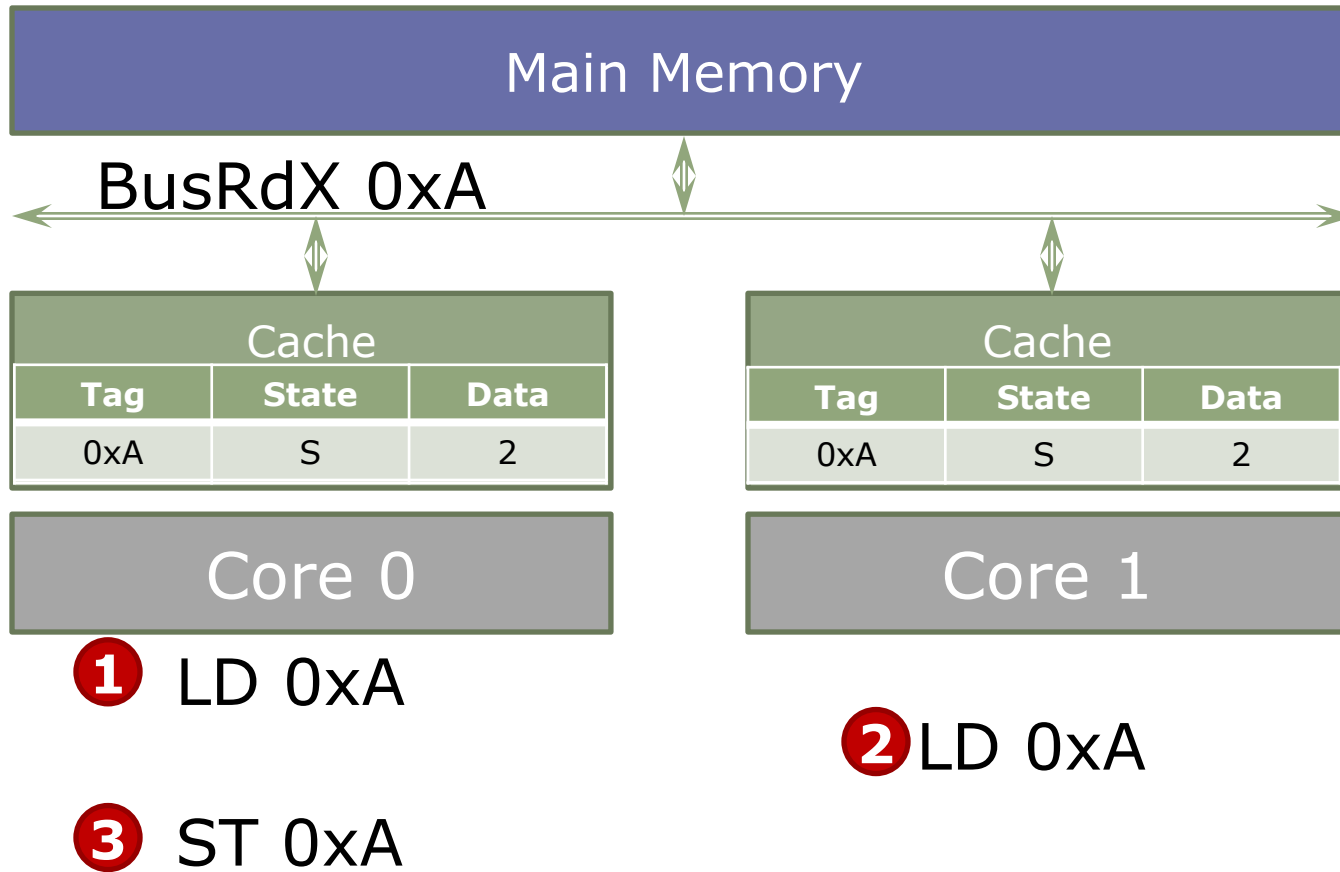
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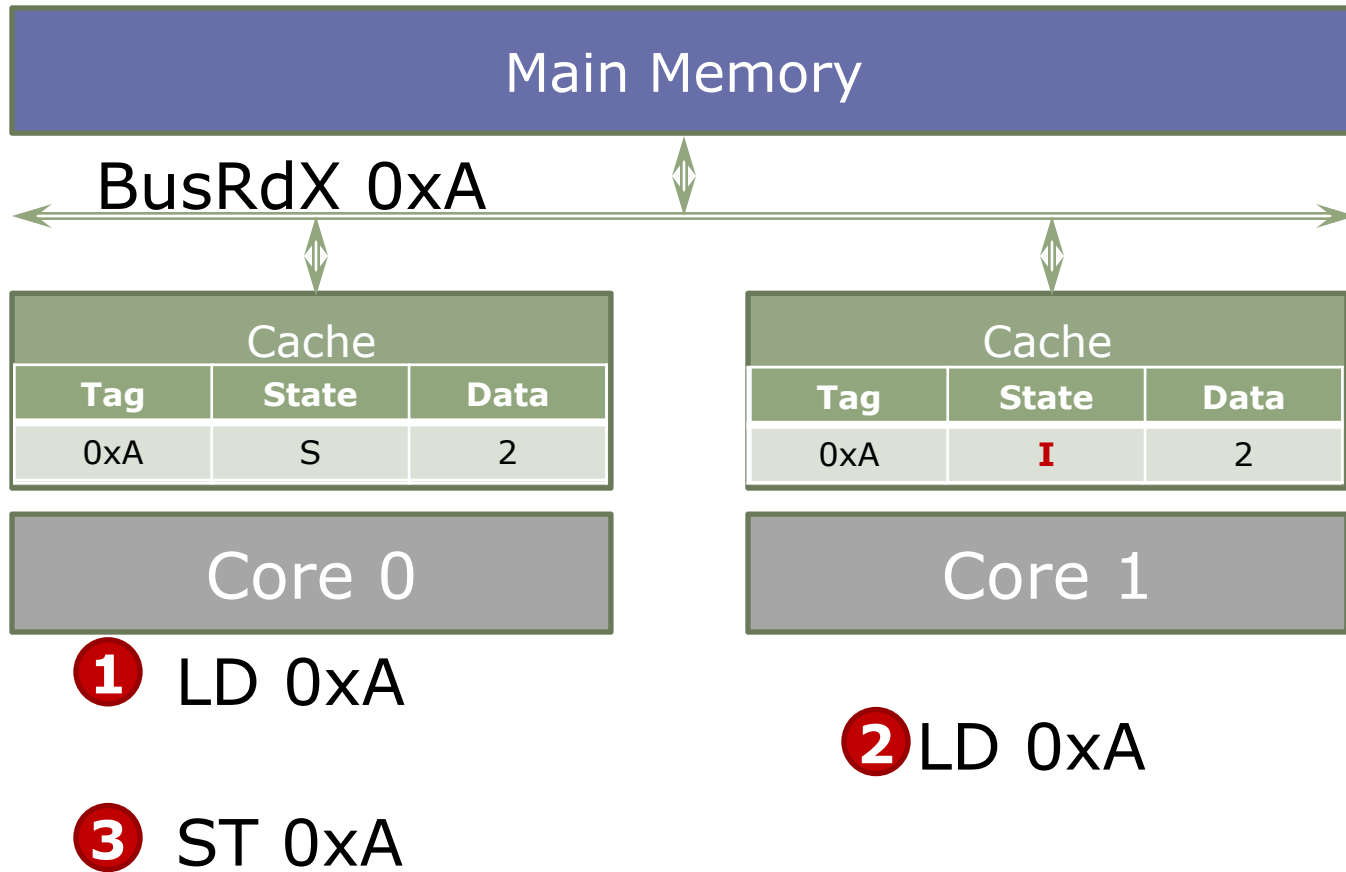
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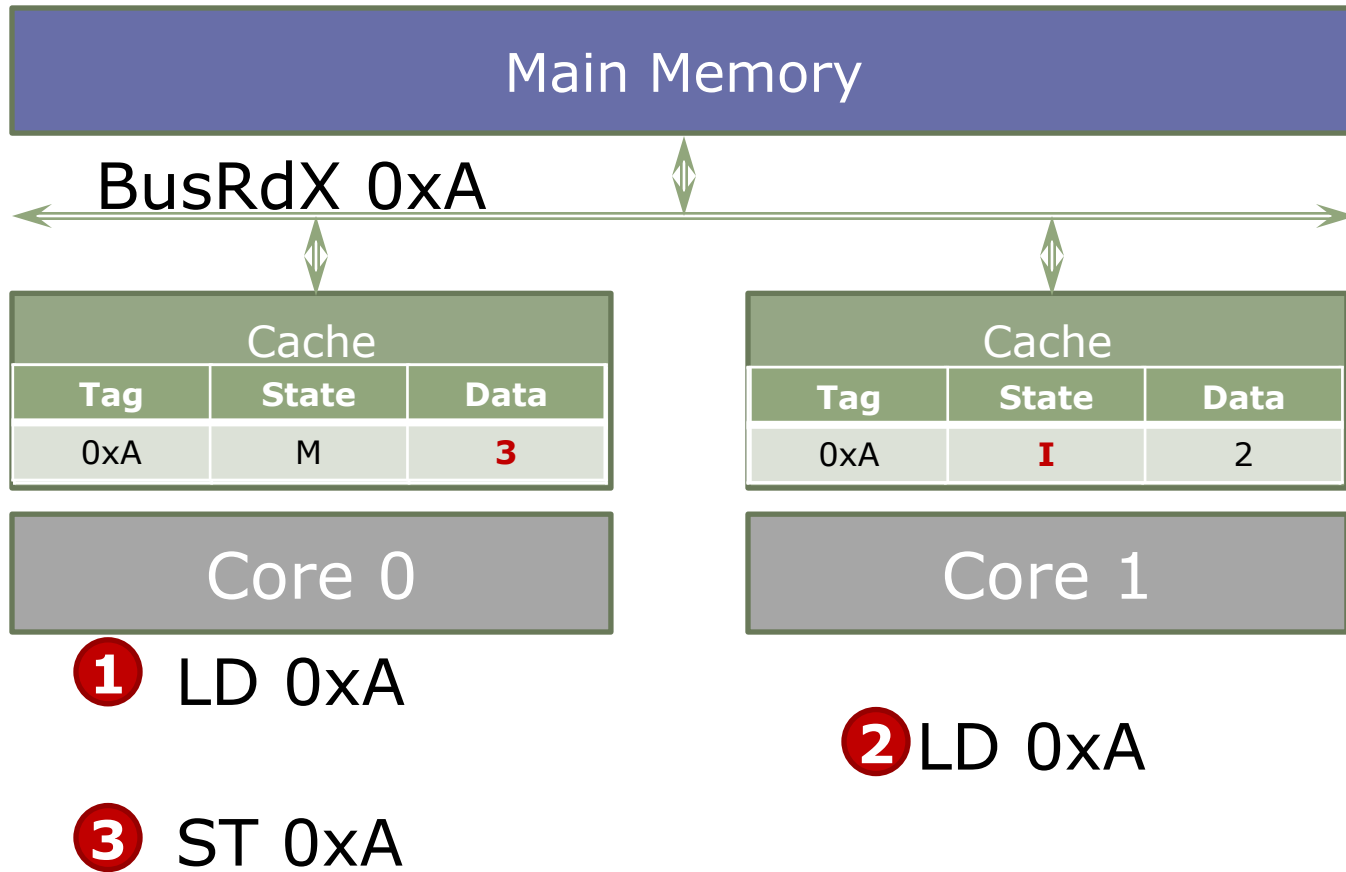
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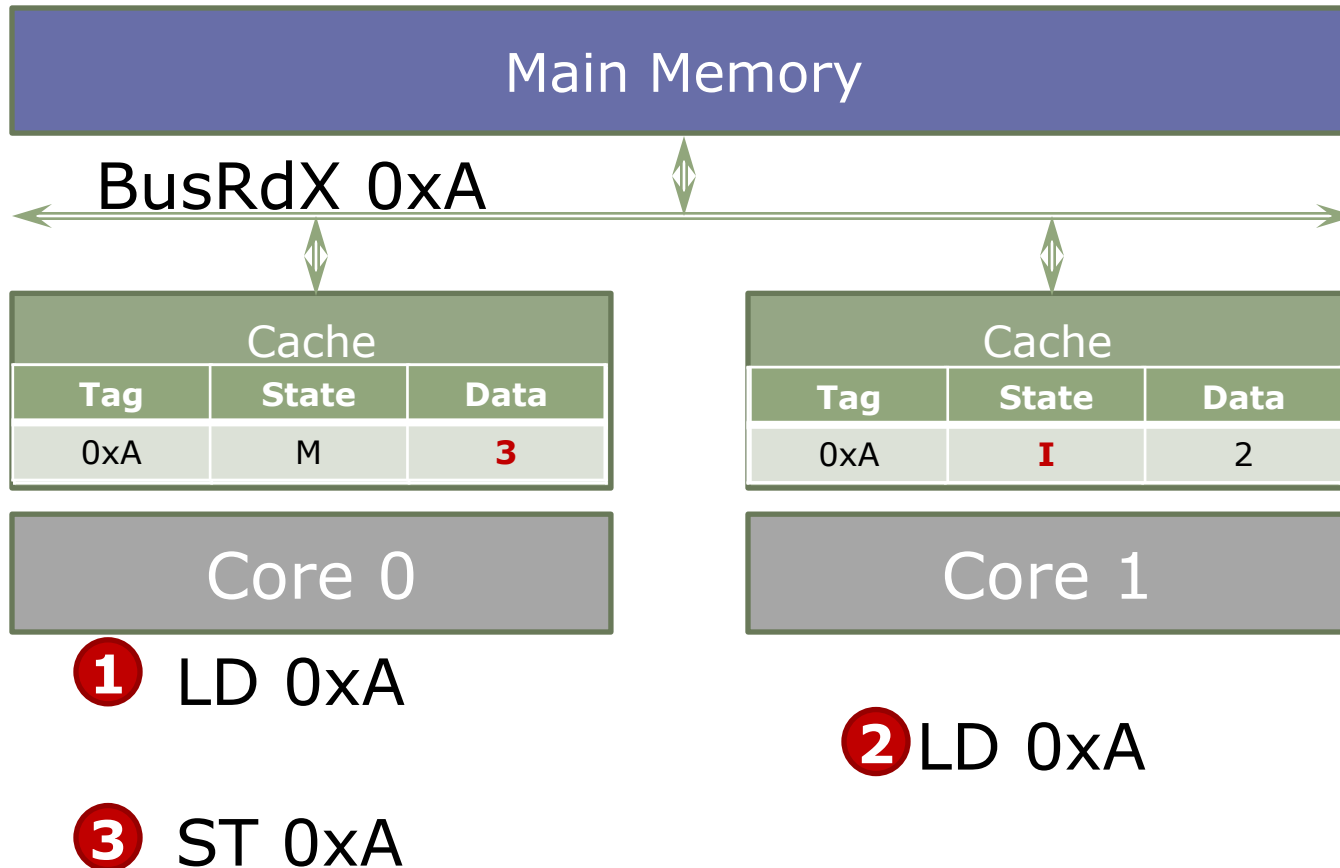
MSI Example



MSI Example

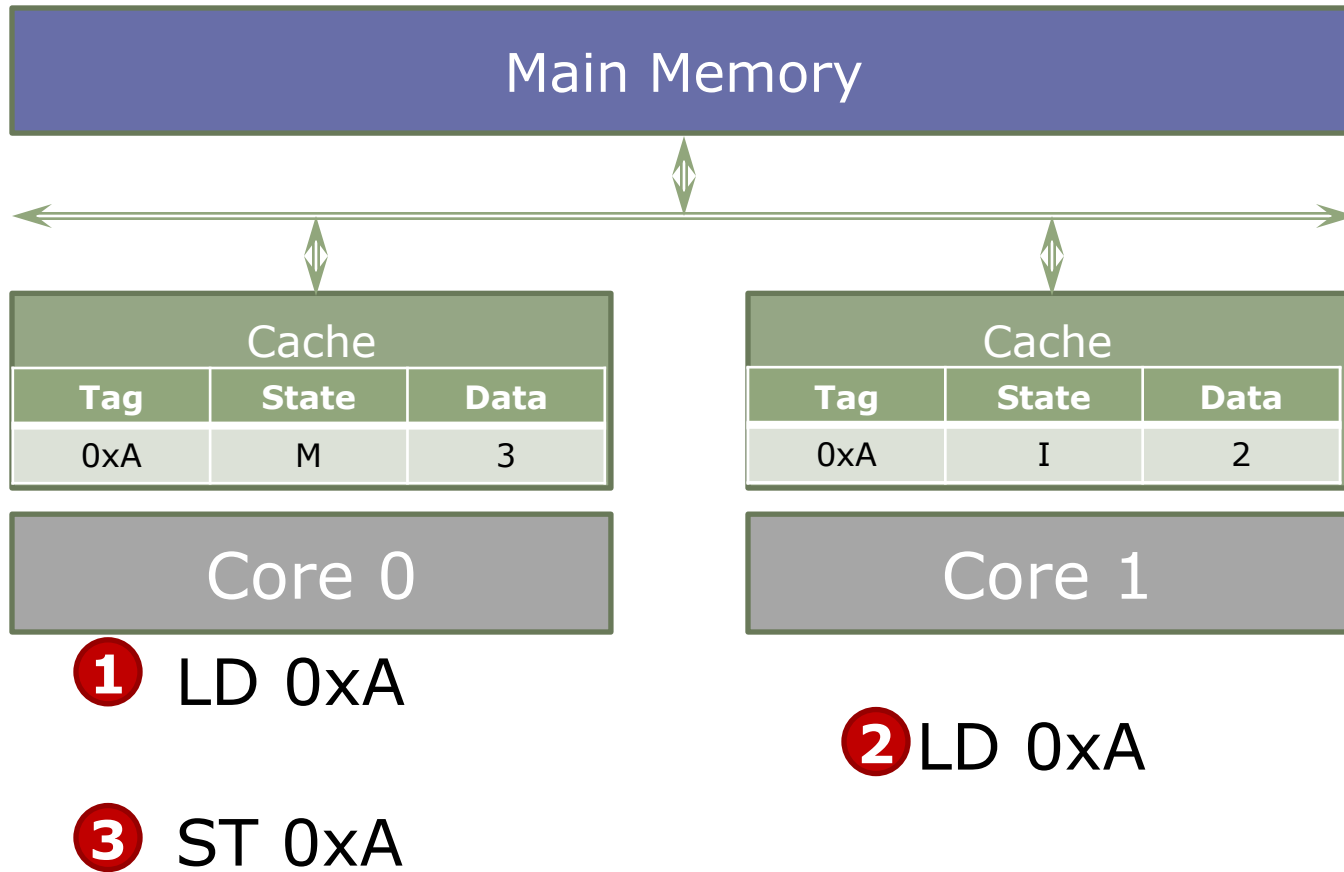


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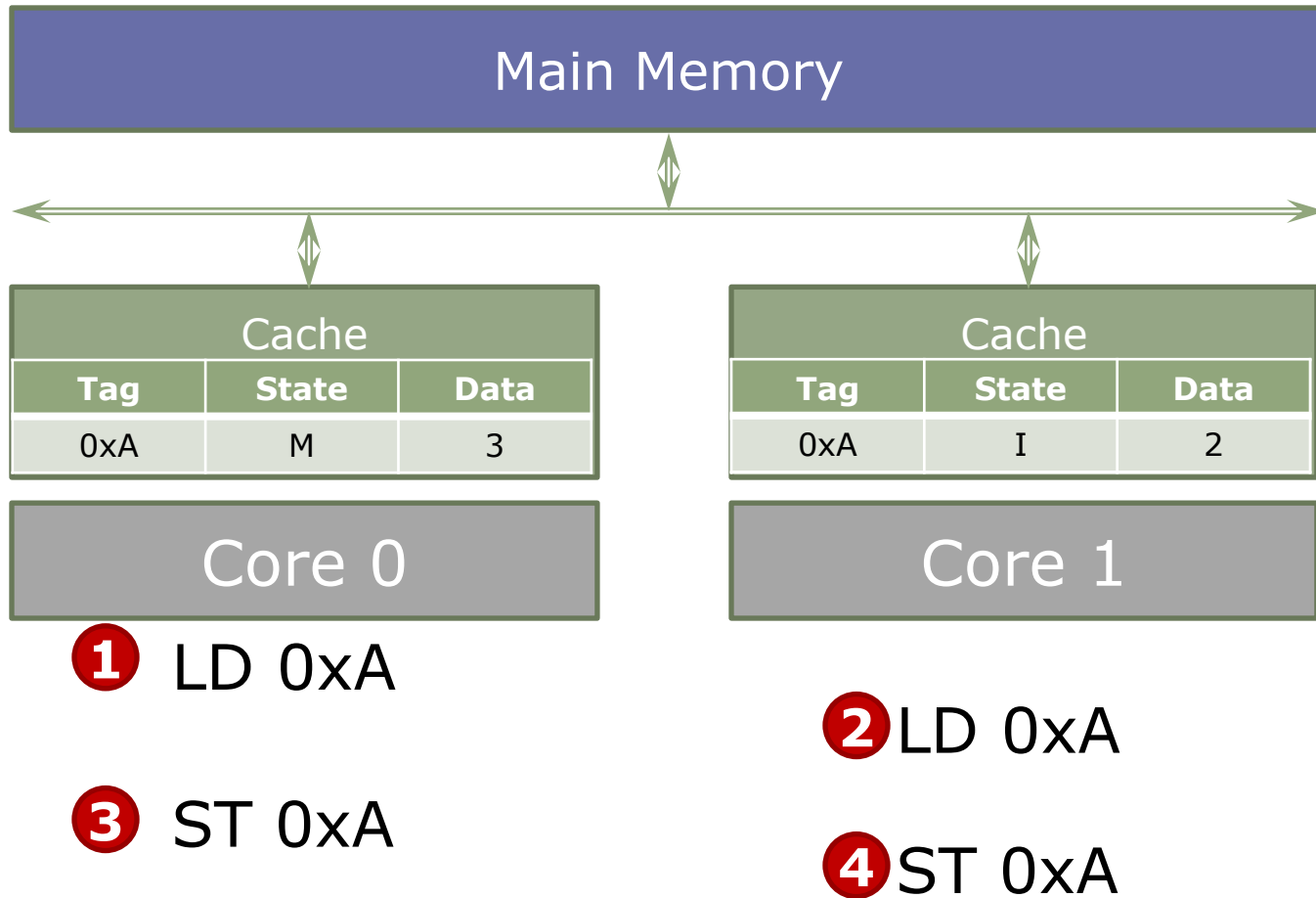


Additional loads *and* stores from core 0 satisfied locally, without bus transactions (unlike in VI)

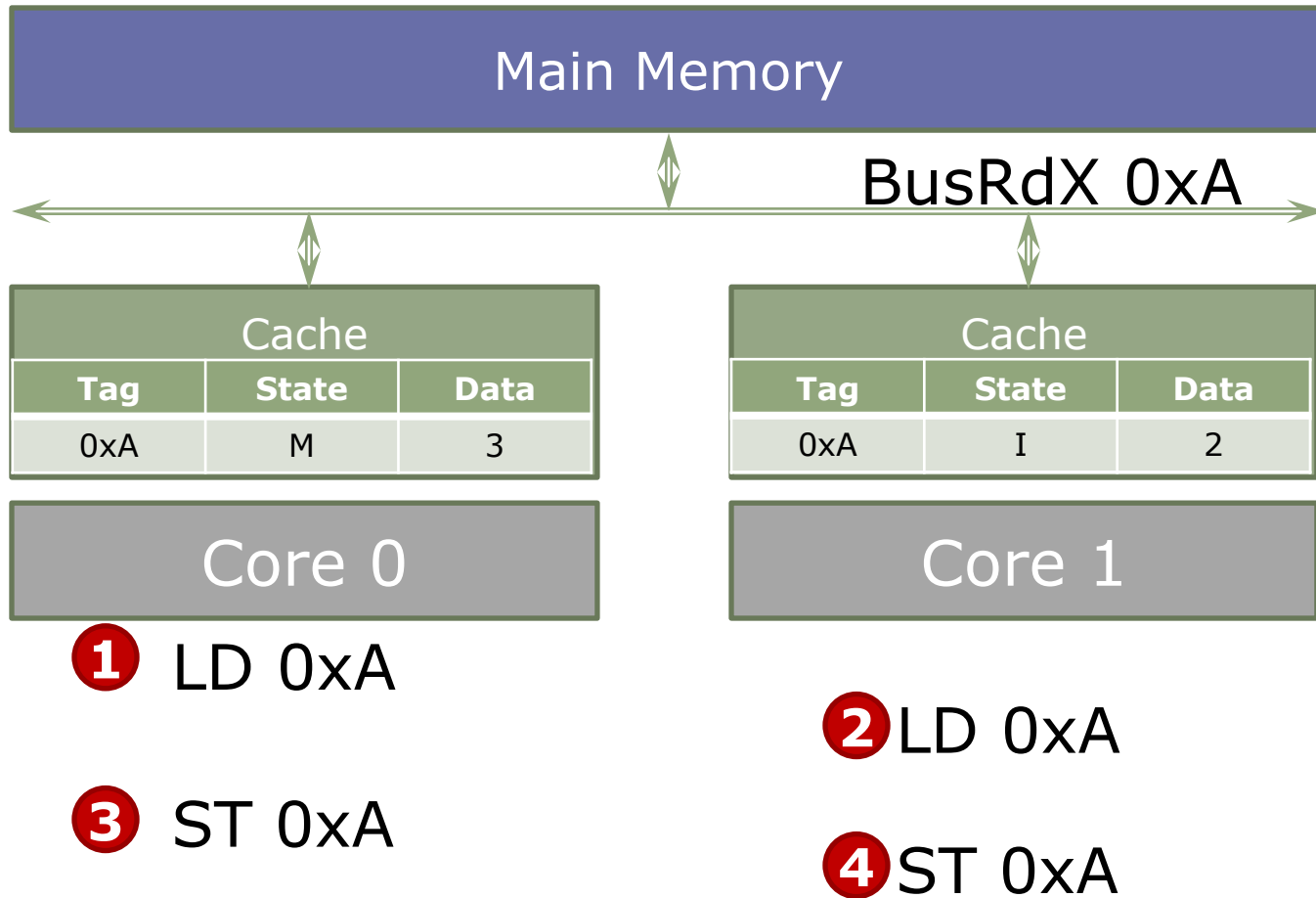
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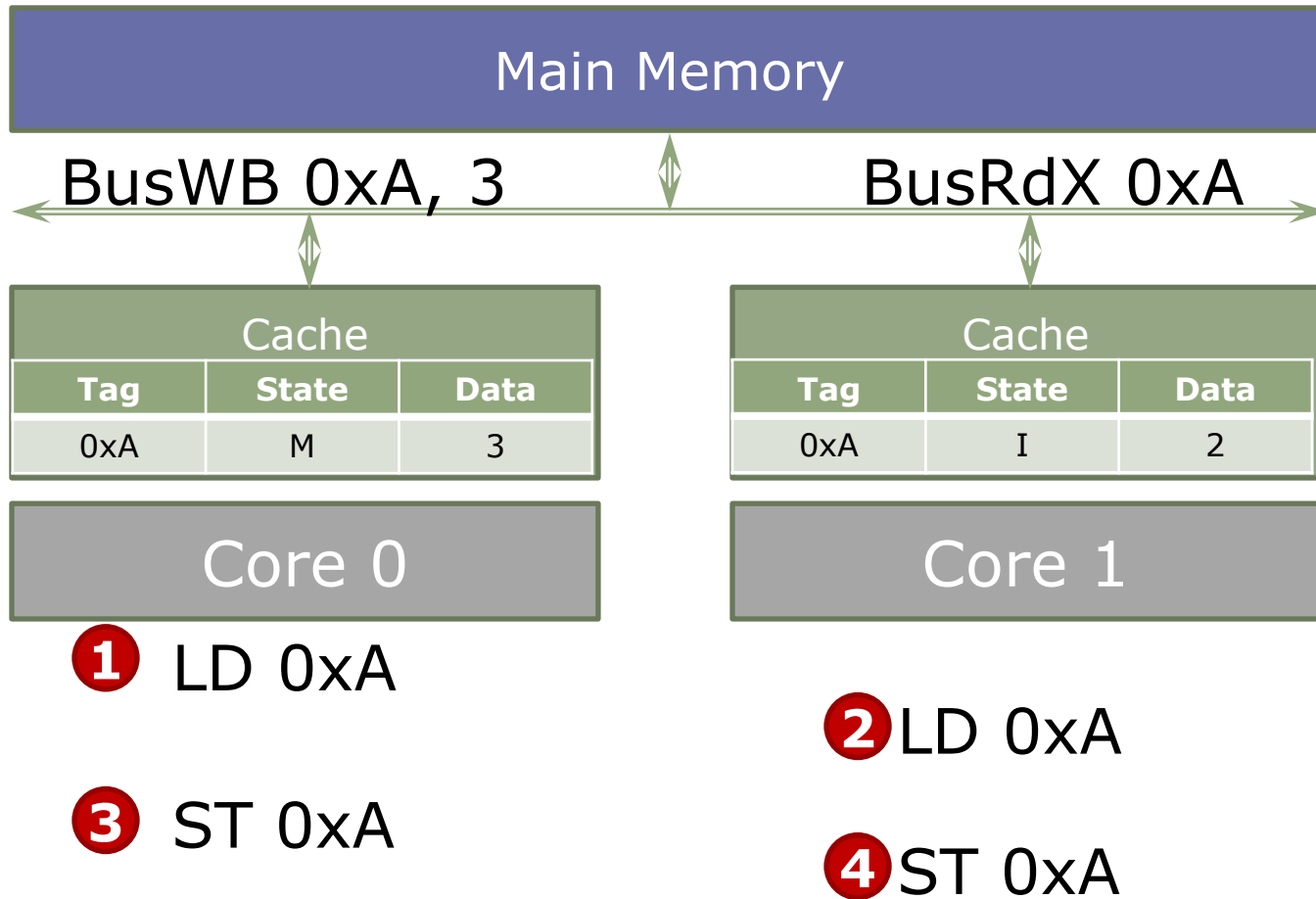
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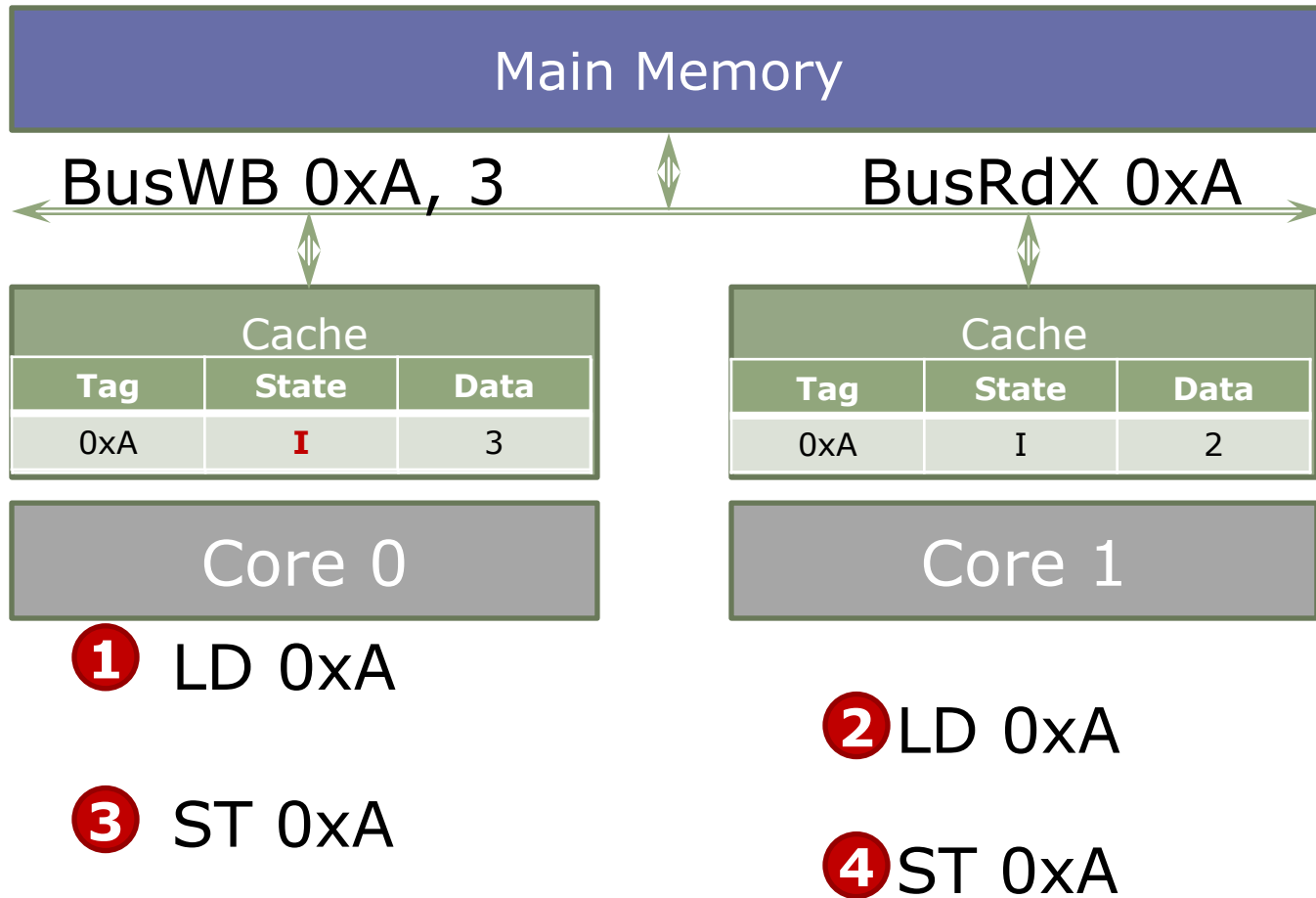
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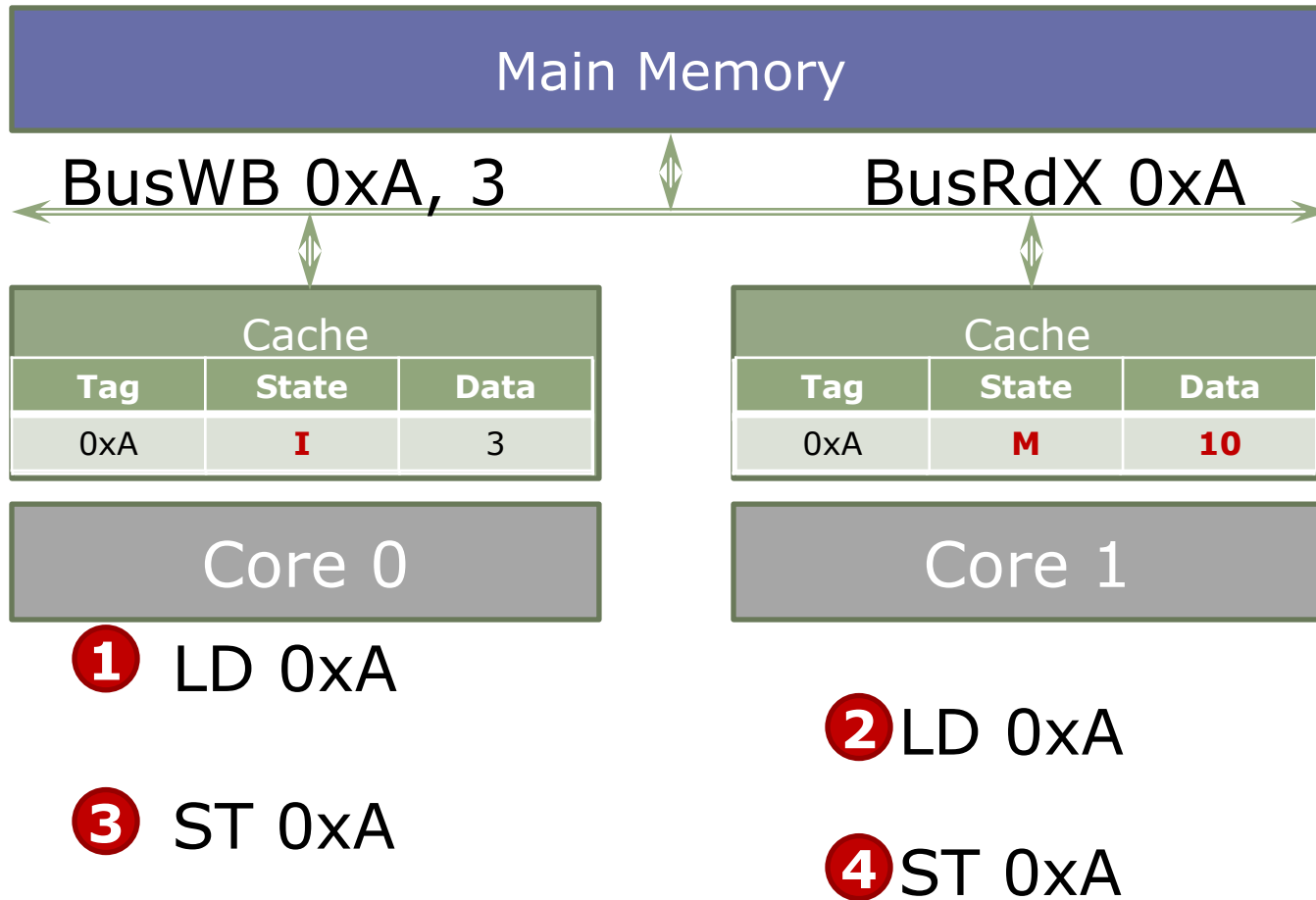
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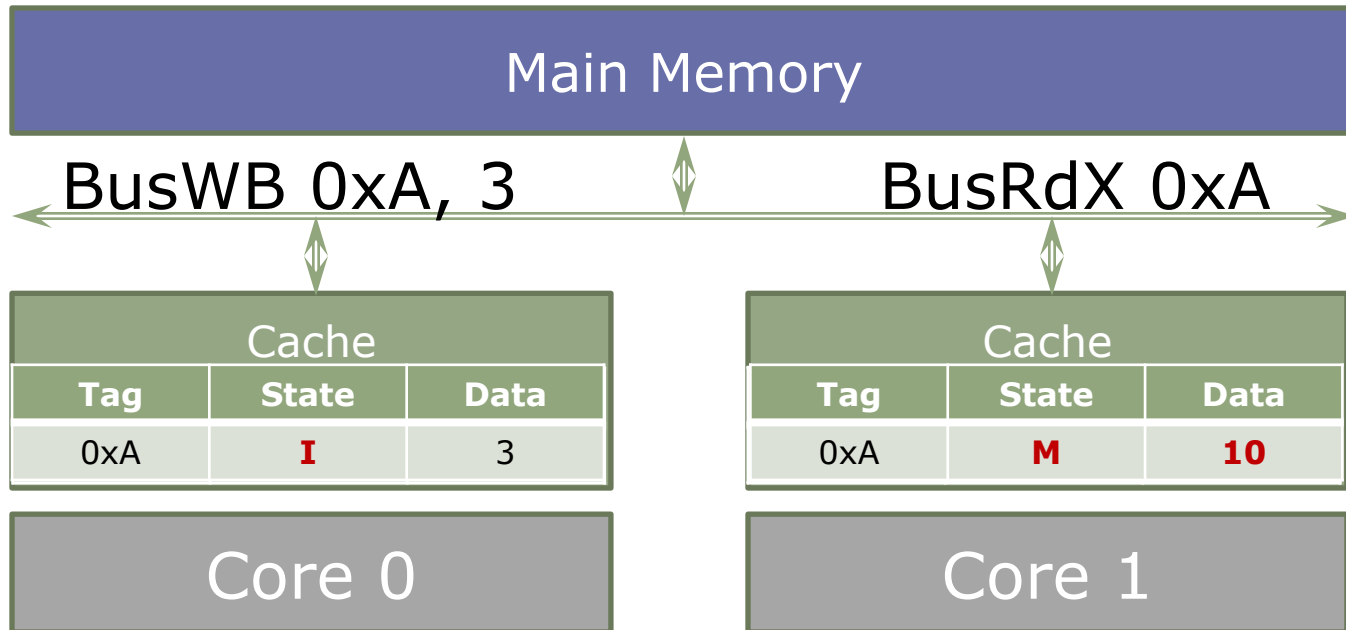
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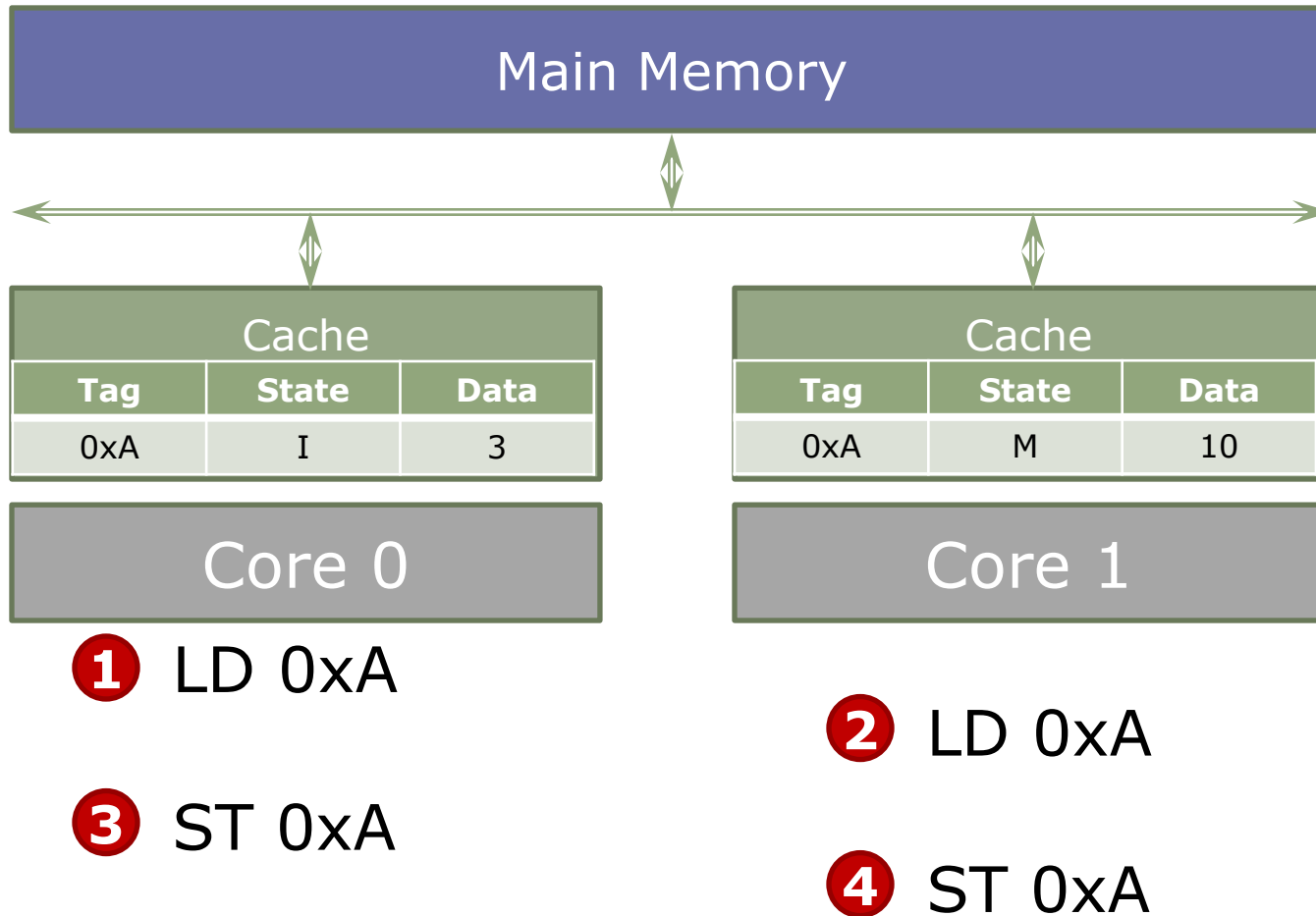


Cache interventions

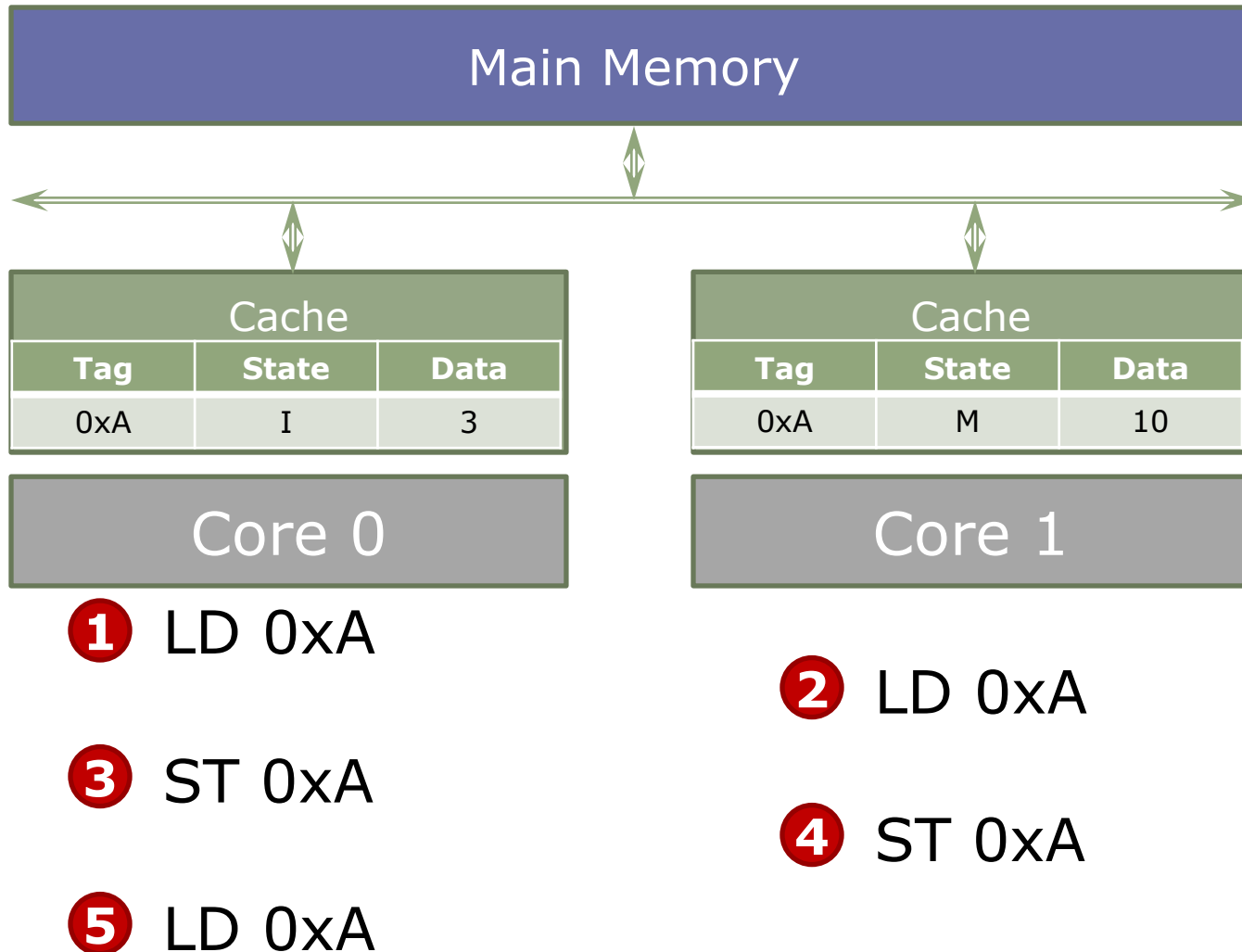


- MSI allows caches to serve writes without updating memory, so main memory can have stale data
 - Core 0's cache needs to supply data
 - But main memory may also respond!
- Cache must override response from main memory

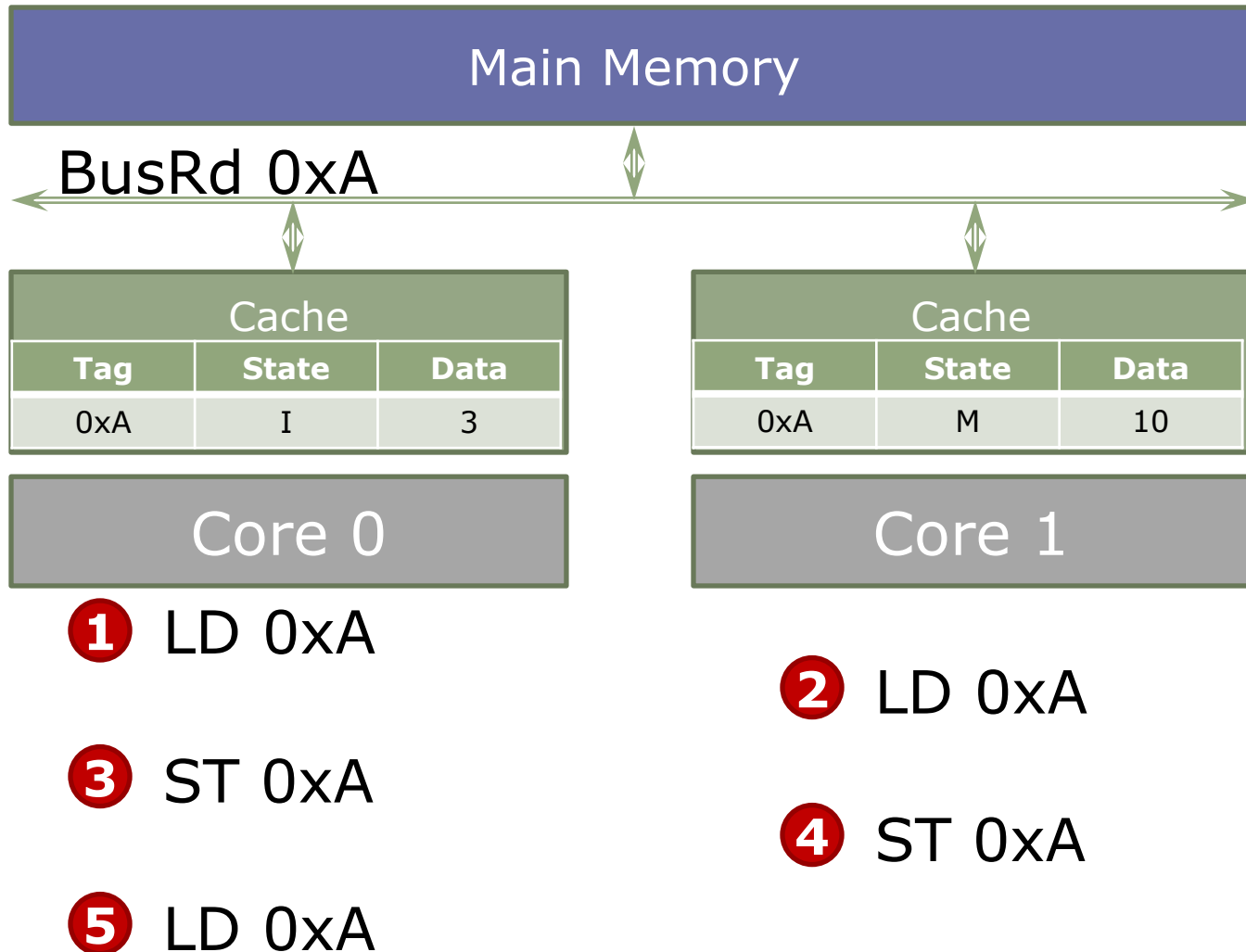
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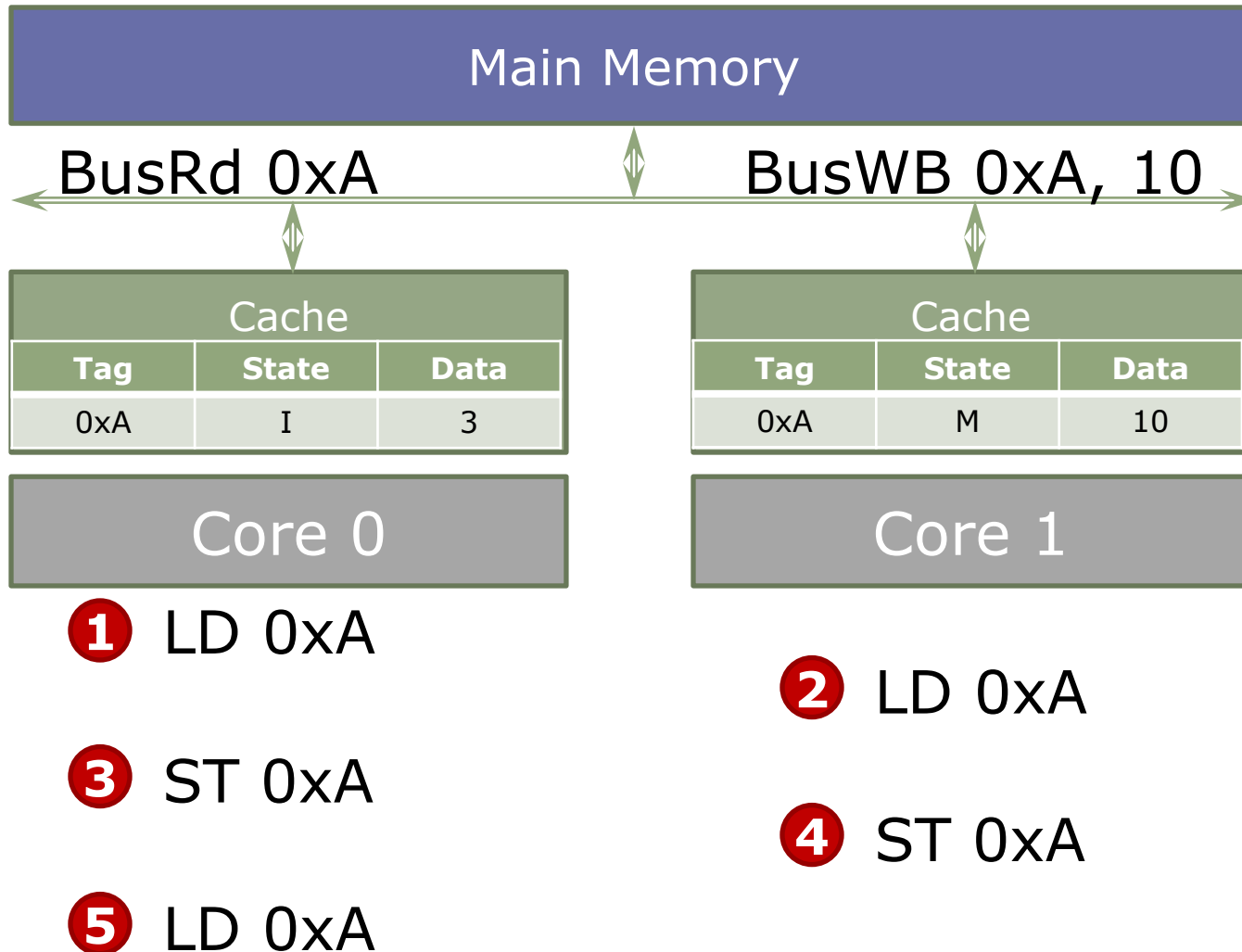
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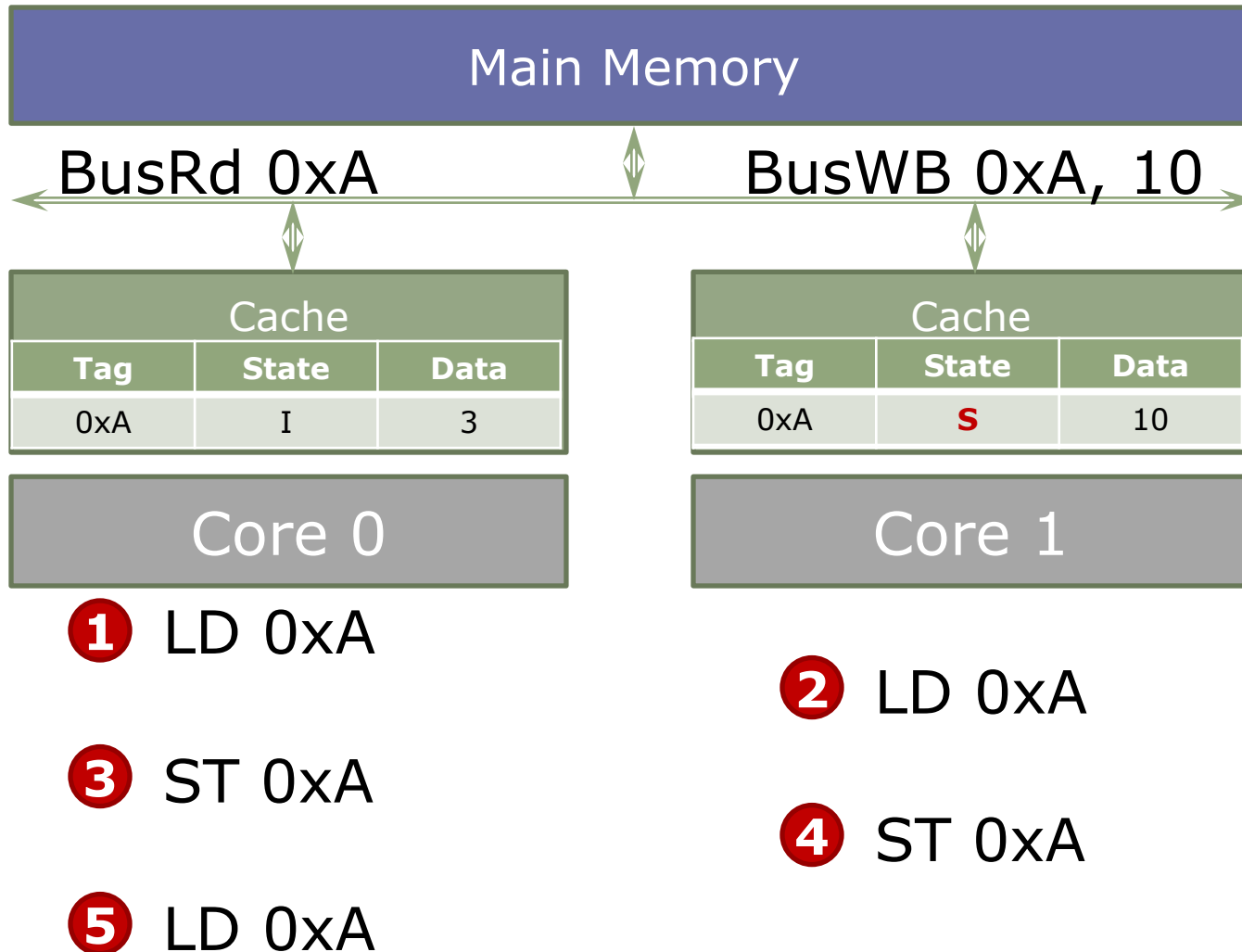
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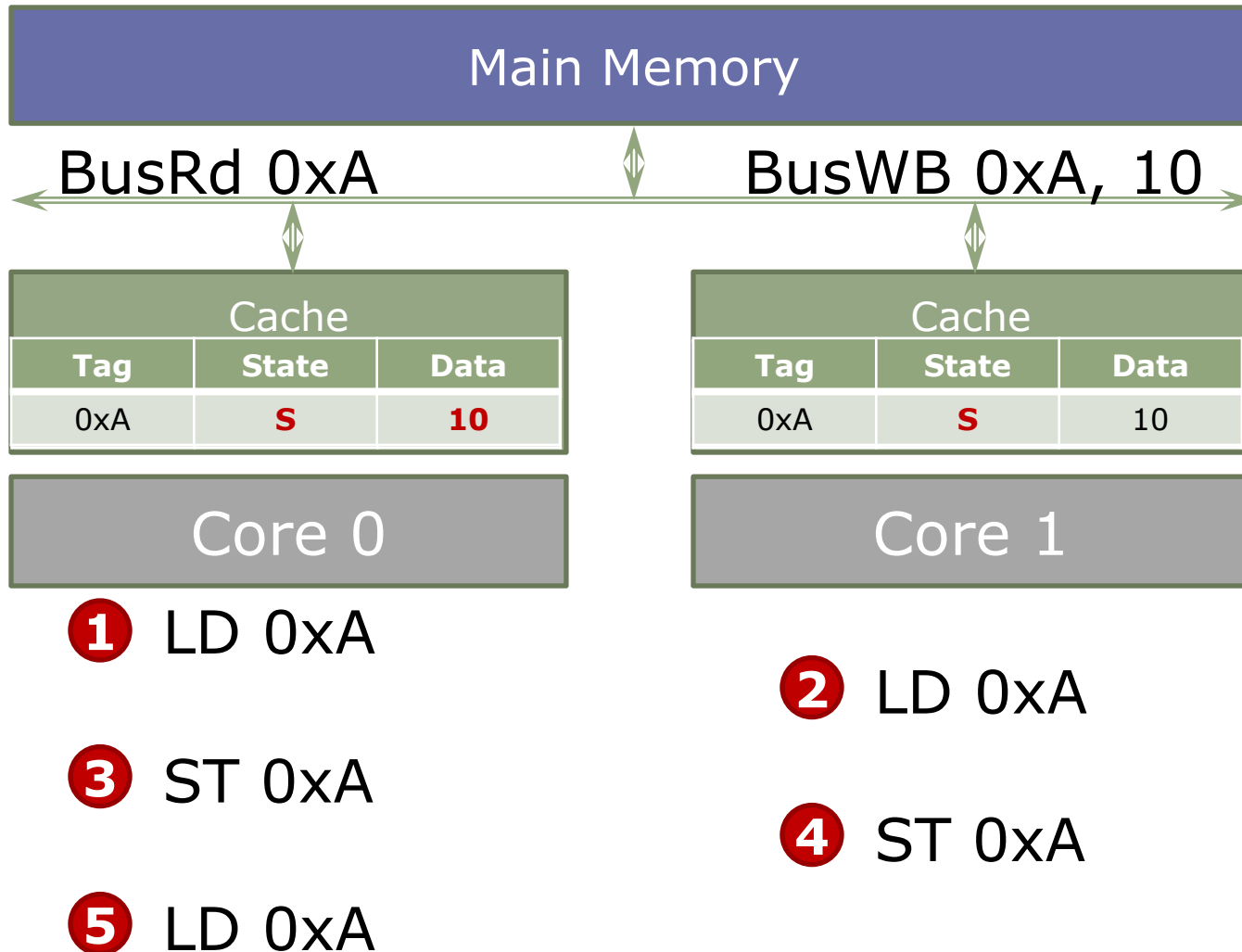
MSI Example



MSI Example



MSI Example



MSI Optimizations: Exclusive State

- Observation: Doing read-modify-write sequences on private data is common
 - What's the problem with MSI?

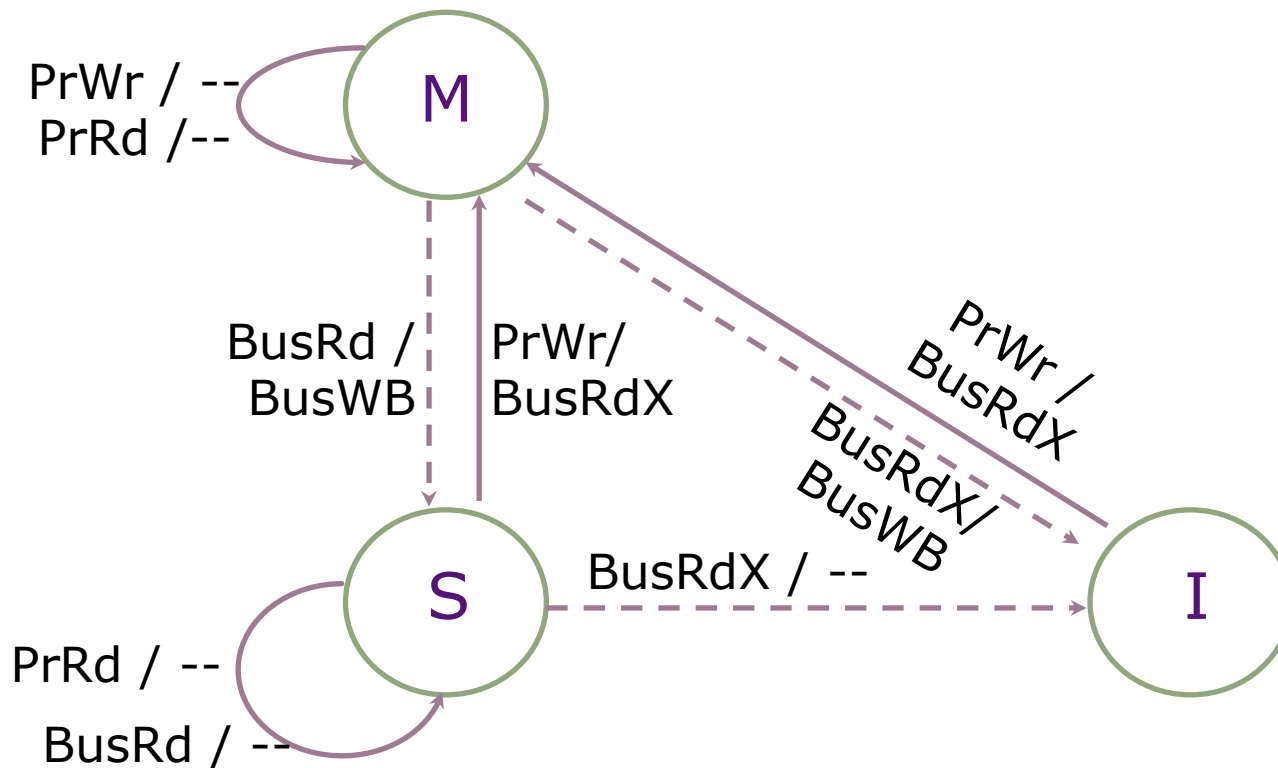
MSI Optimizations: Exclusive State

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- Solution: E state (exclusive, clean)
 - If no other sharers, a read acquires line in E instead of S
 - Writes silently cause E→M (exclusive, dirty)

MESI: An Enhanced MSI protocol

increased performance for private read-write data

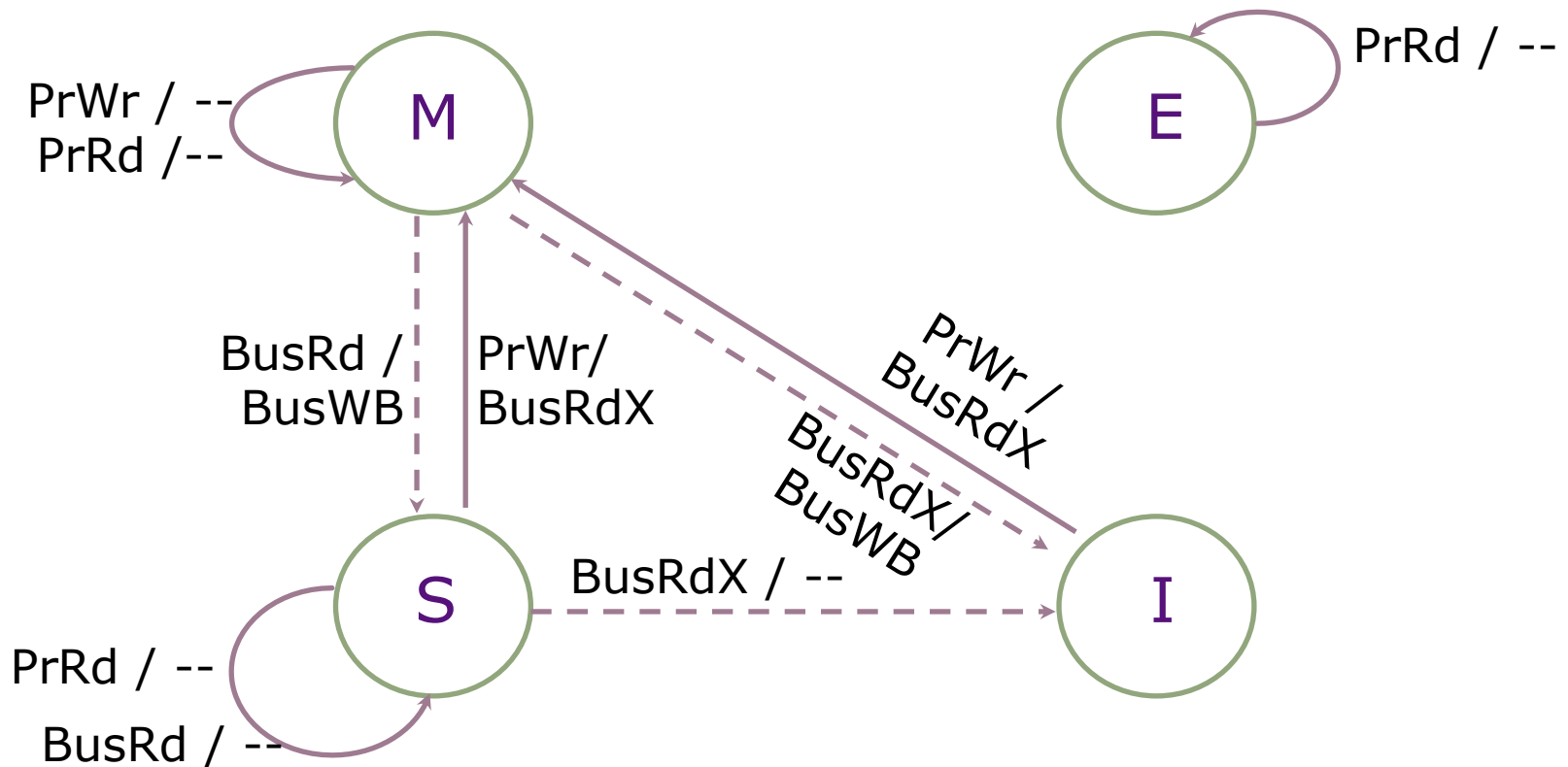
M: Modified Exclusive
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I: Invalid



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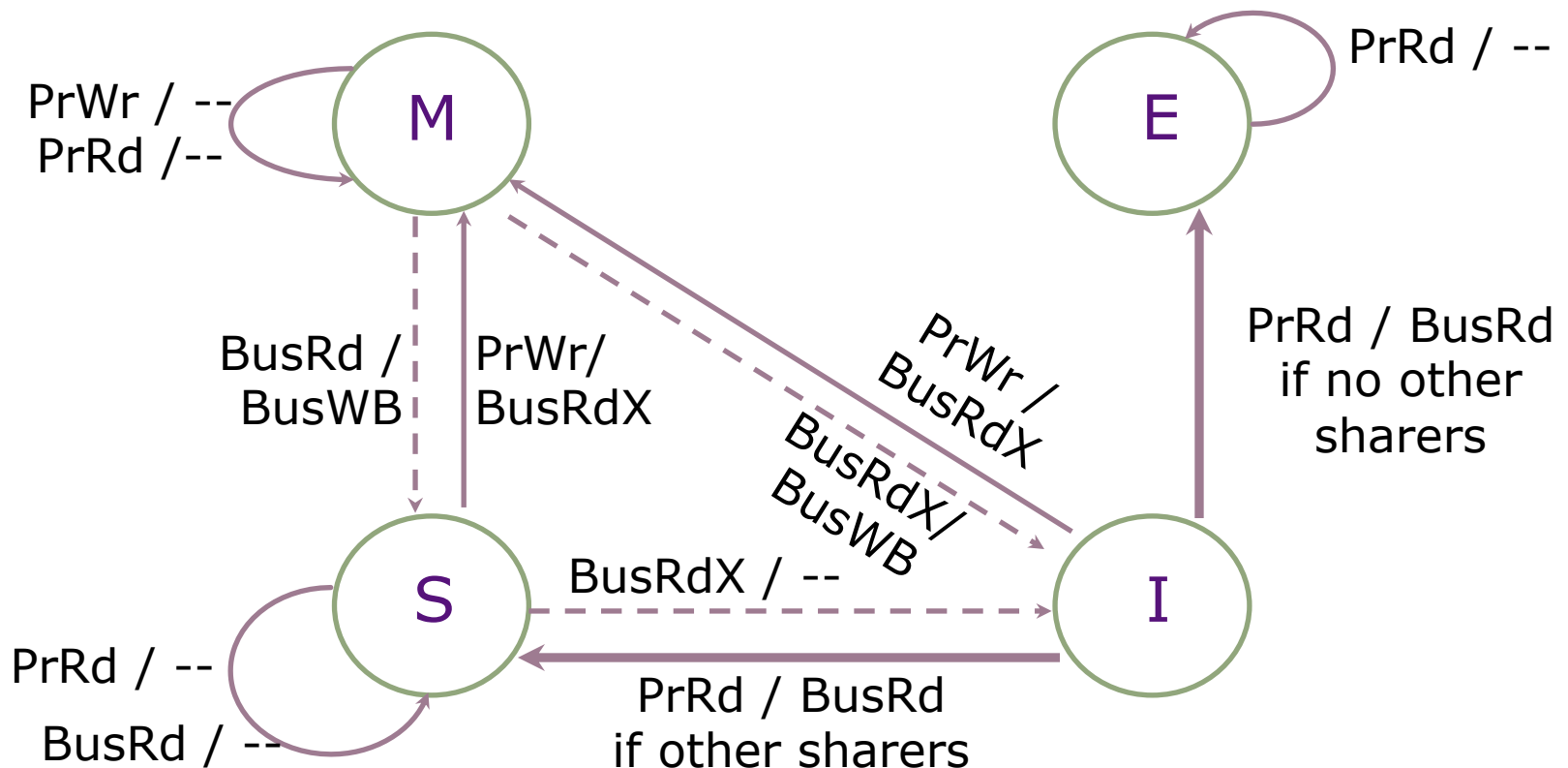
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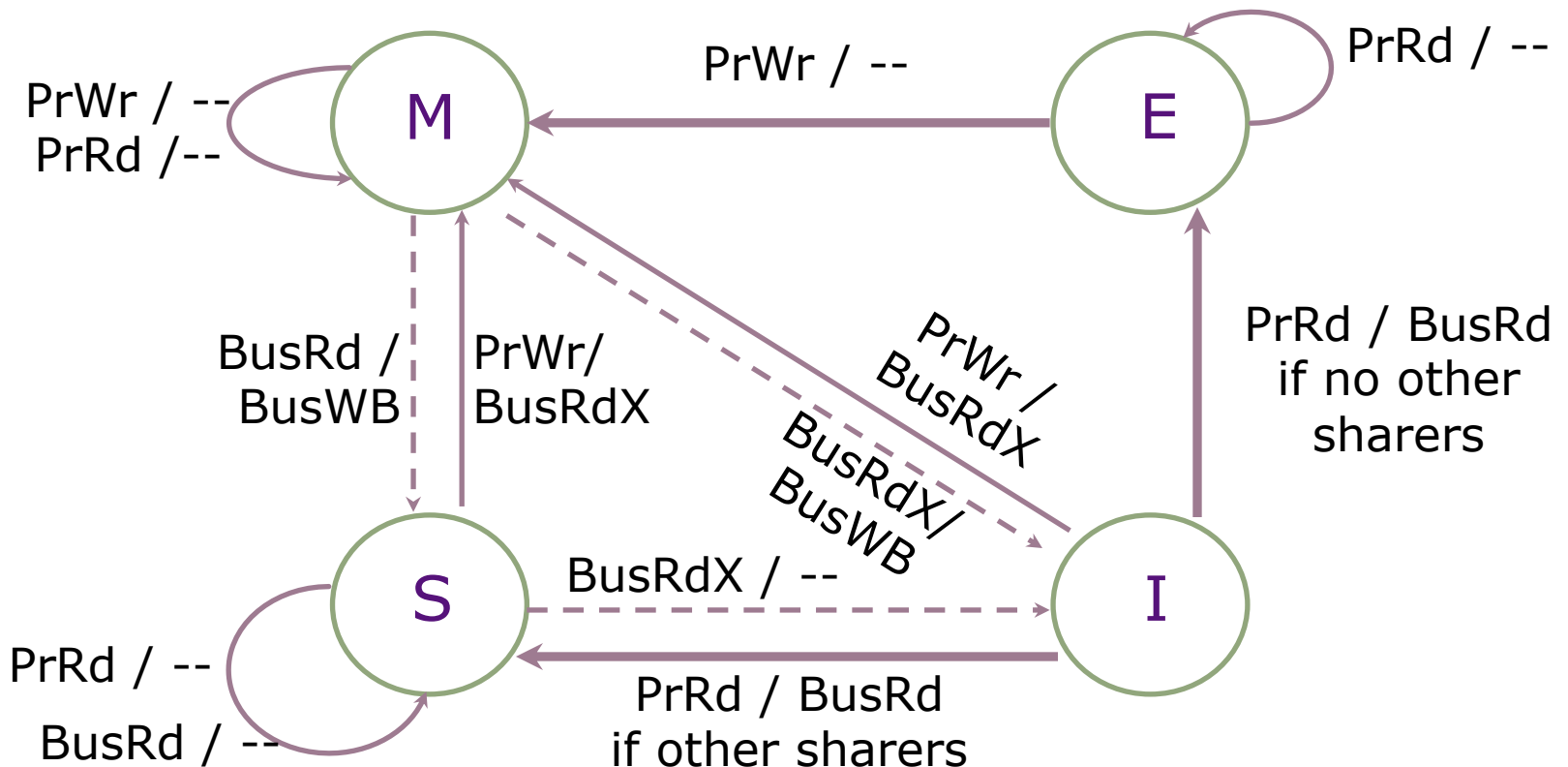
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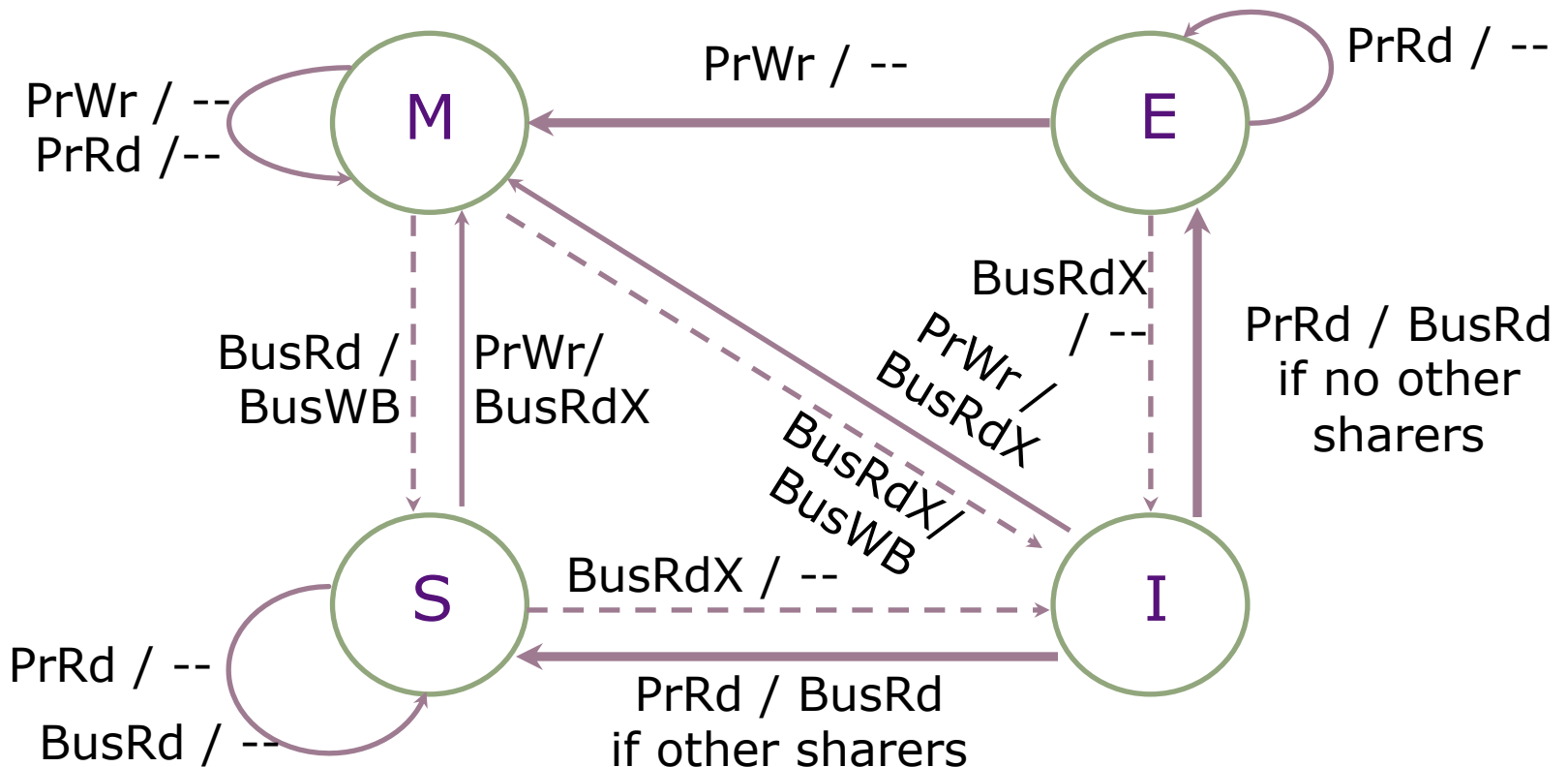
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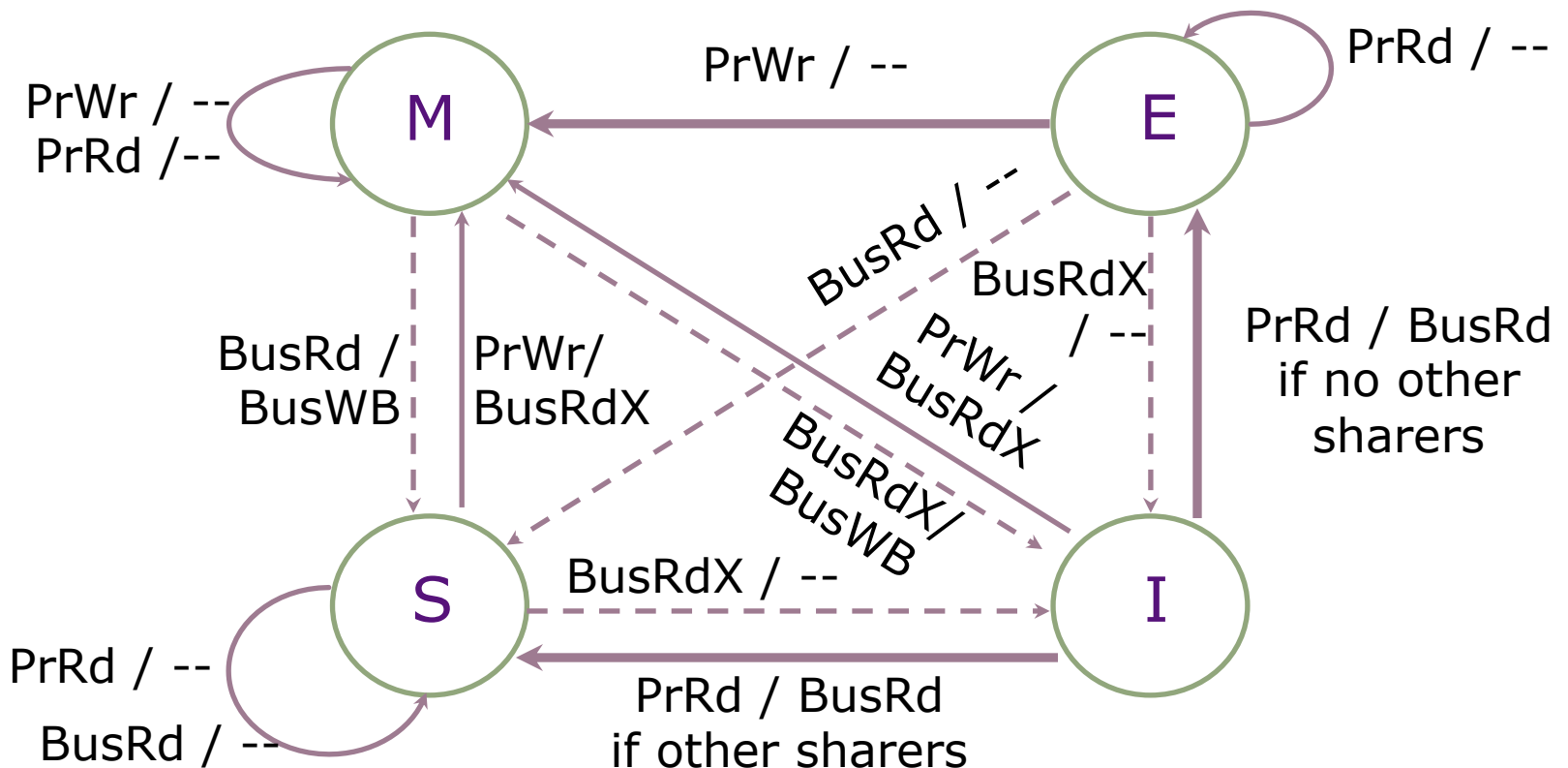
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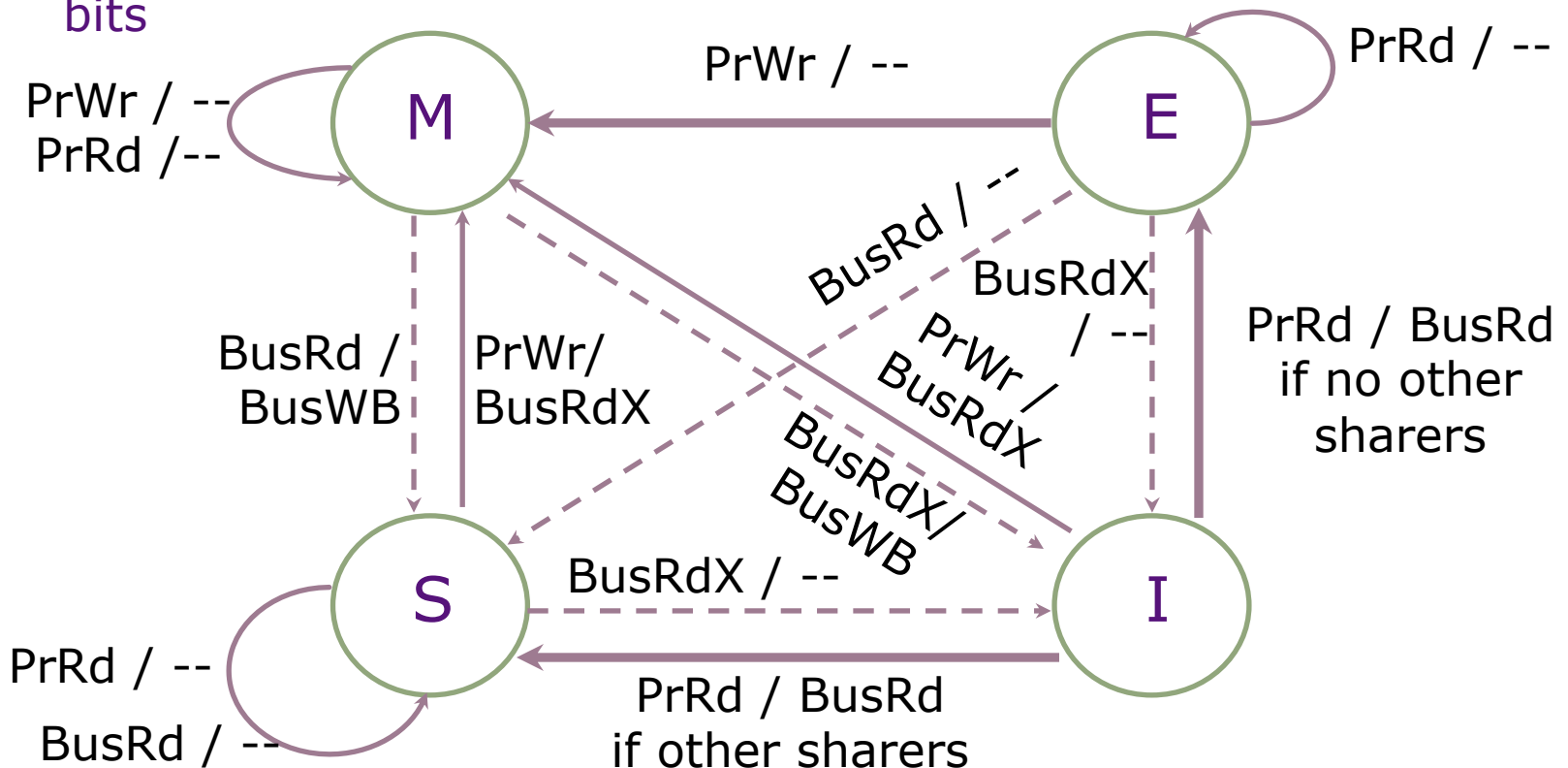
MESI: An Enhanced MSI protocol

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Each cache line has a tag



- M: Modified Exclusive
- E: Exclusive, unmodified
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MSI Optimizations: Owner State

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 - Can we defer the write after S?

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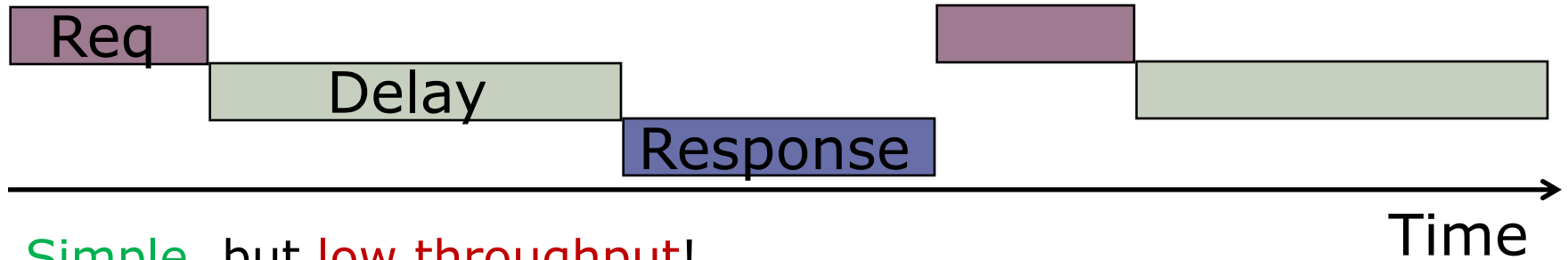
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 - Typically E if private read-write \gg shared read-only (common)
 - Typically O only if writebacks are expensive (main mem vs L3)

Split-Transaction and Pipelined Buses

Atomic Transaction Bus

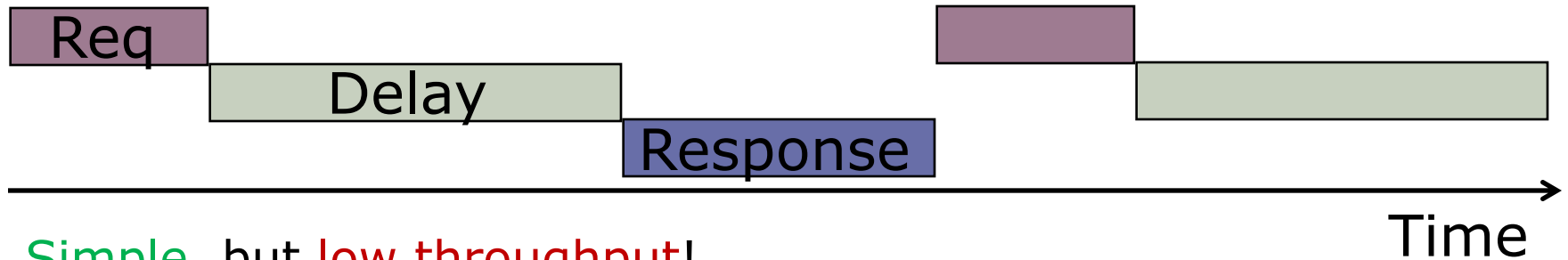


Simple, but low throughput!

Time

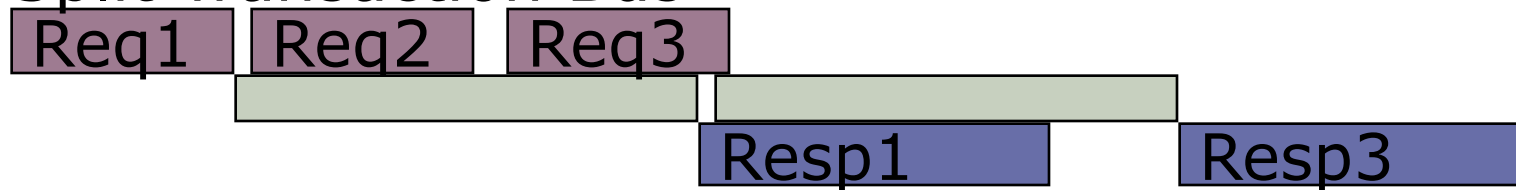
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Atomic Transaction Bus



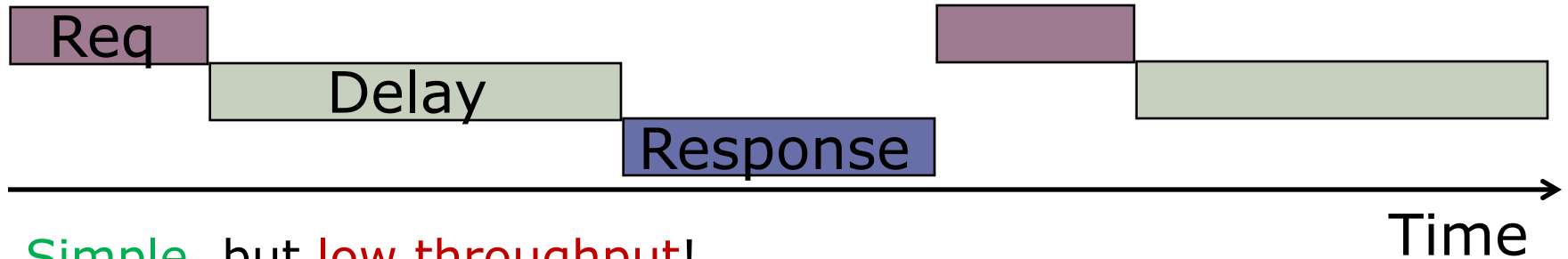
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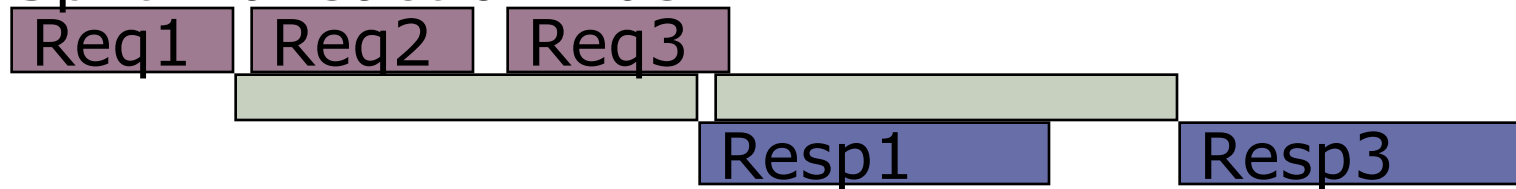
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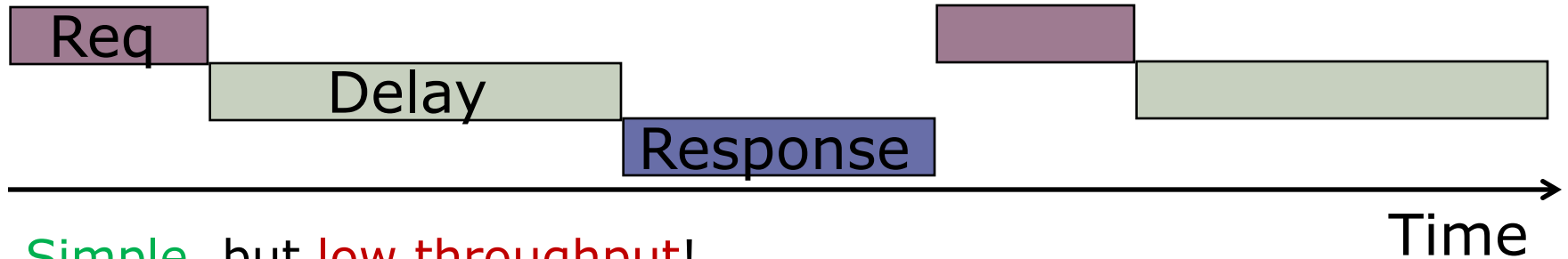
Split-Transaction Bus



- Supports multiple simultaneous transactions

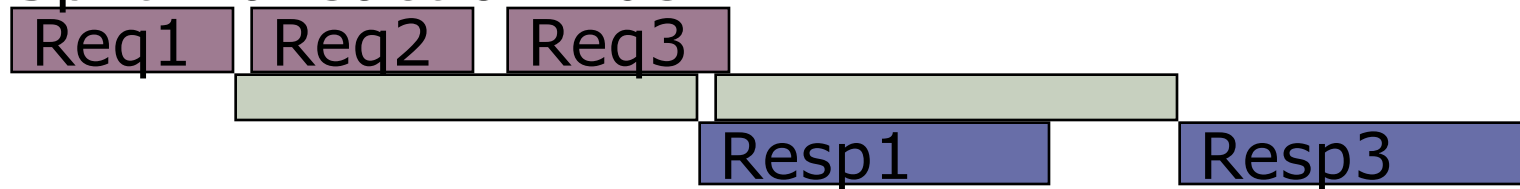
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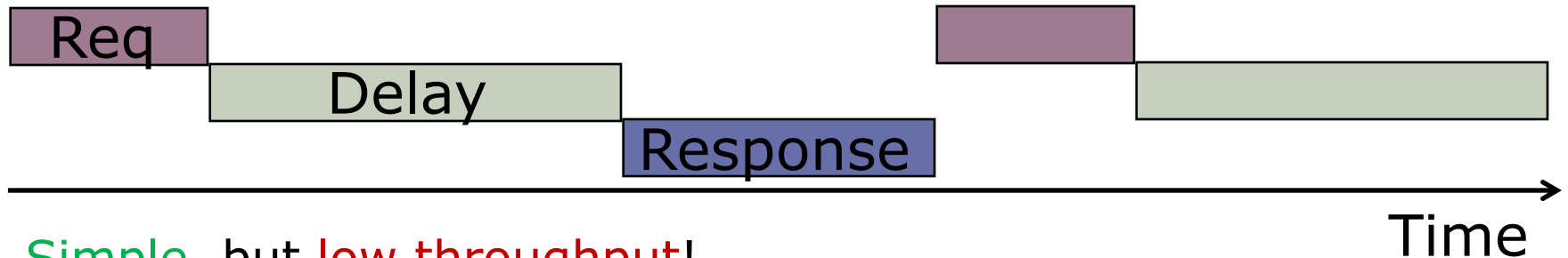
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- Supports multiple simultaneous transactions
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 - Responses may arrive out of order

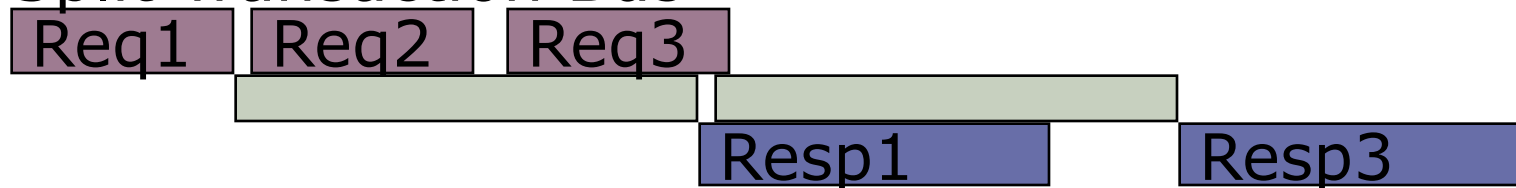
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Split-Transaction Bus

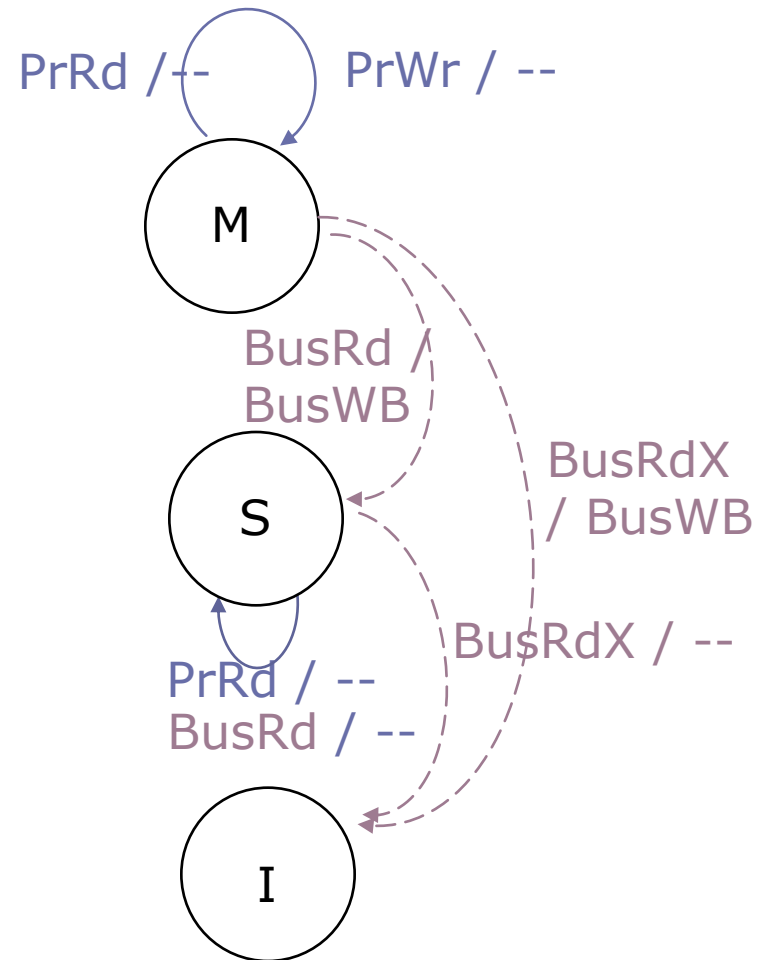


- Supports multiple simultaneous transactions
 - Higher throughput
 - Responses may arrive out of order
- Often implemented as multiple buses (req+resp)

Non-Atomicity → Transient States

- Protocol must handle lack of atomicity
- Two types of states
 - Stable (e.g. MSI)
 - Transient
- Split + race transitions
- More complex

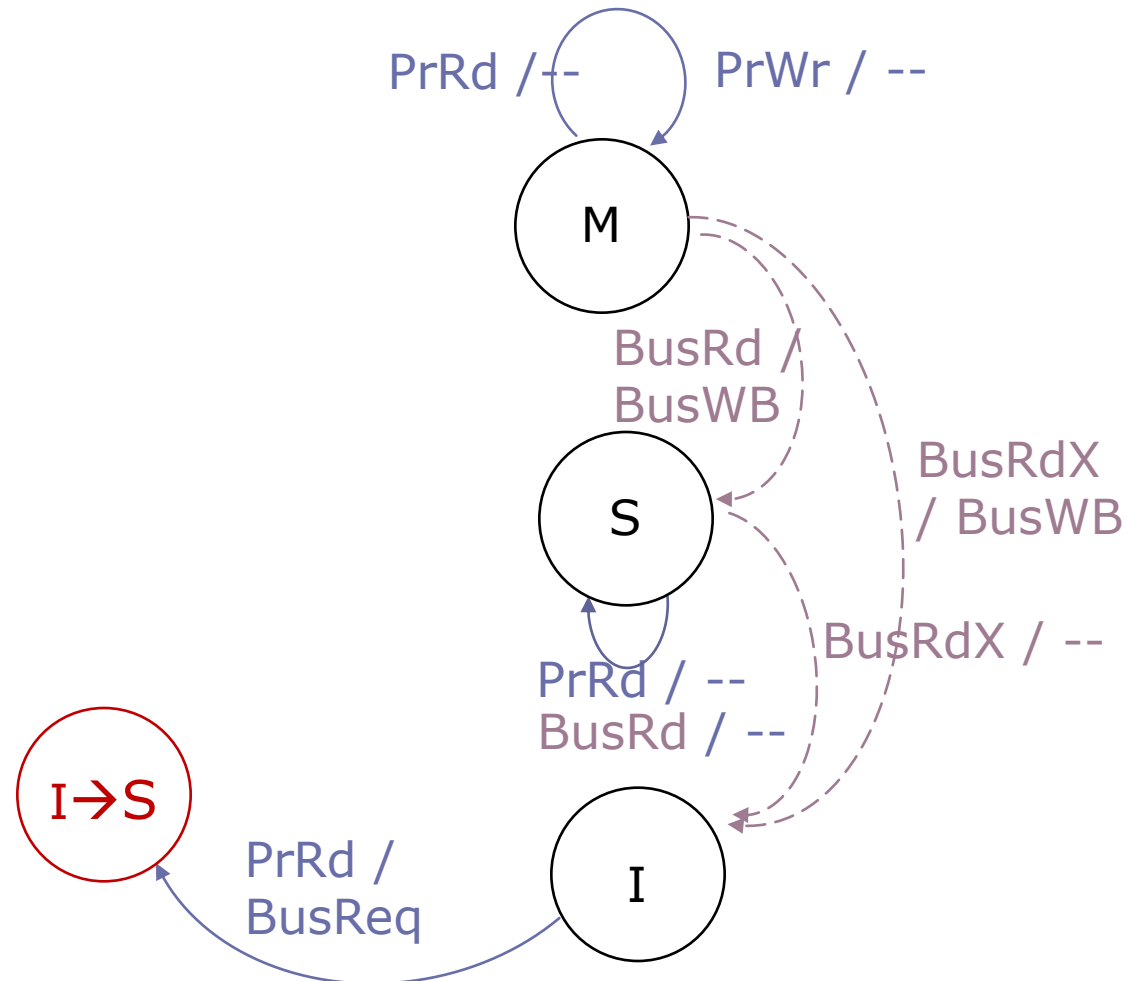
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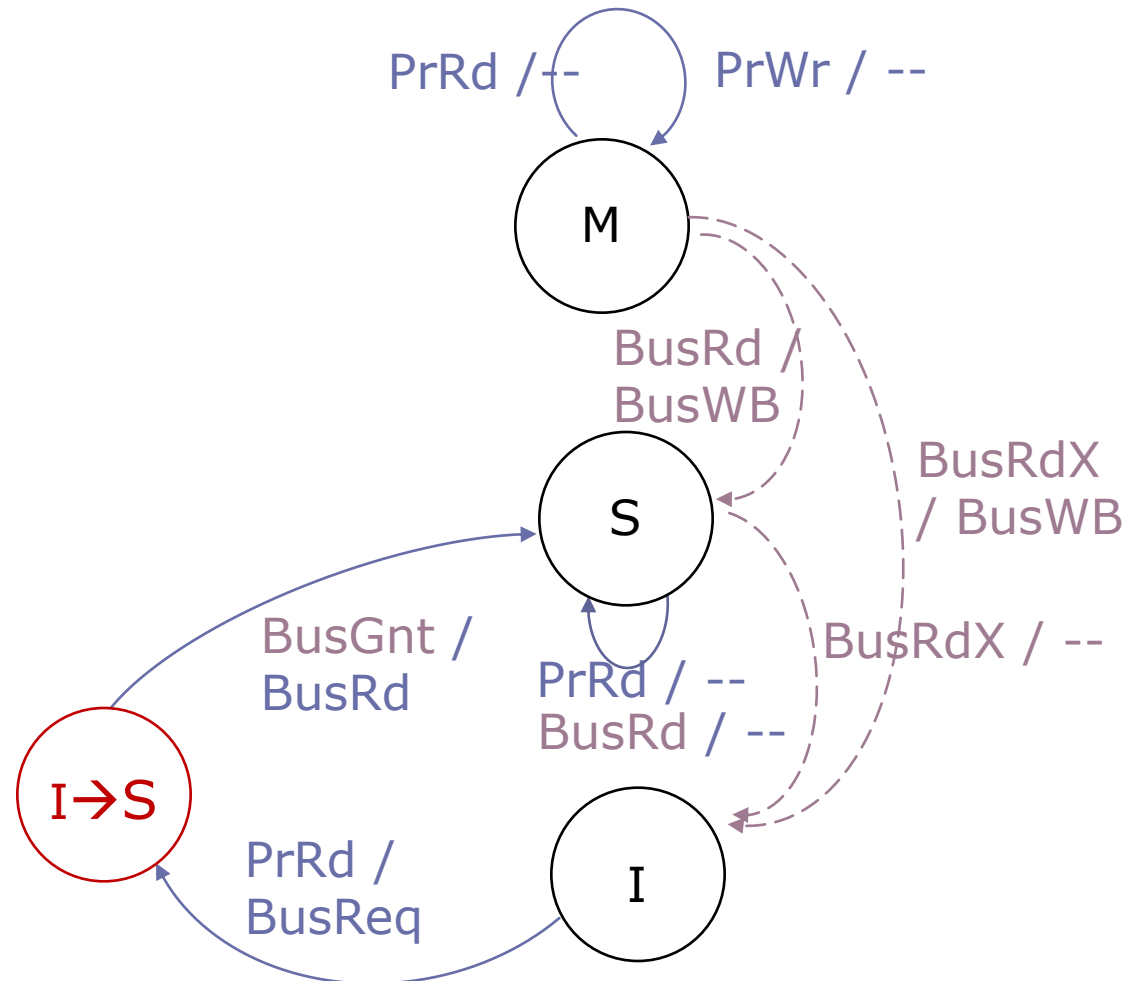
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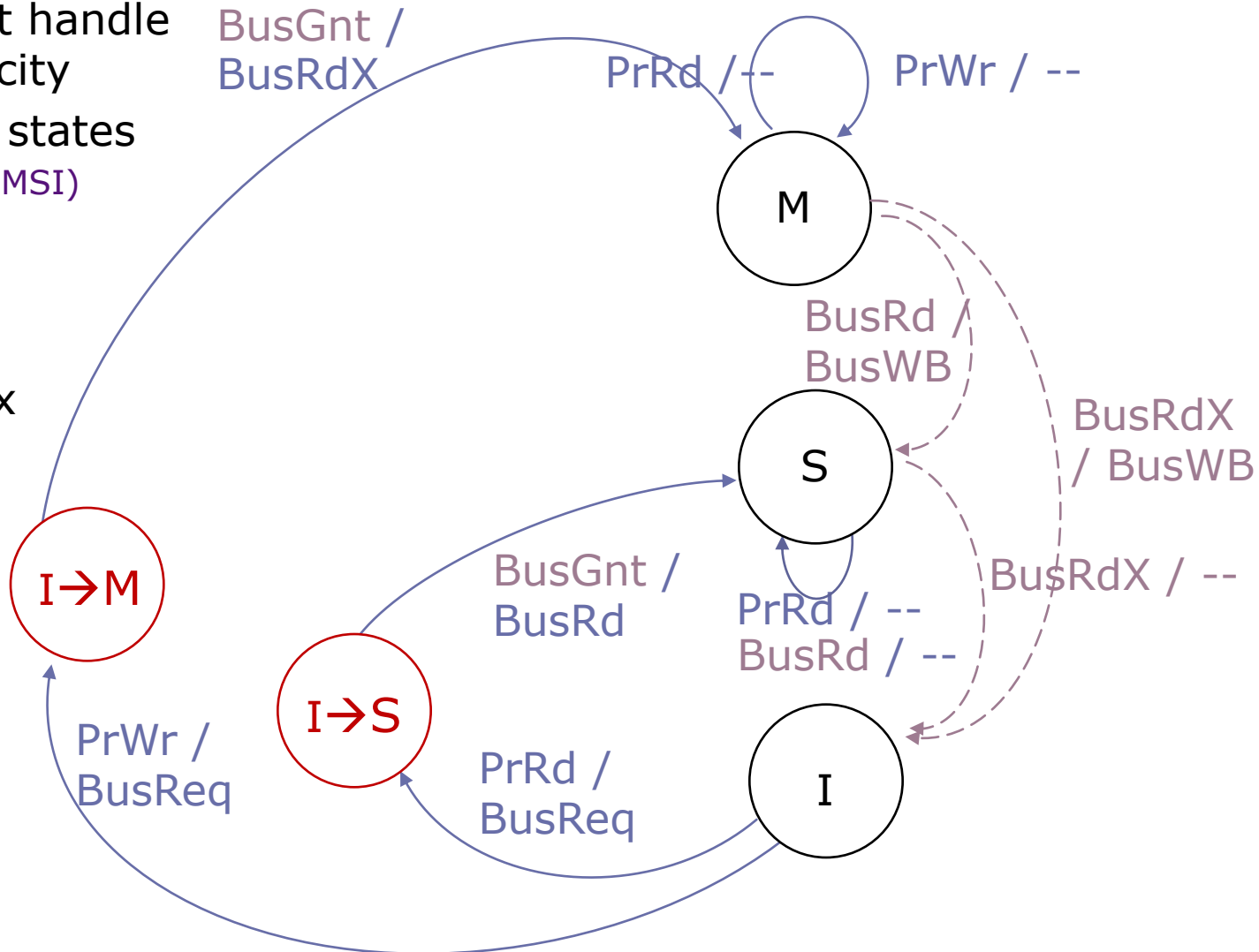
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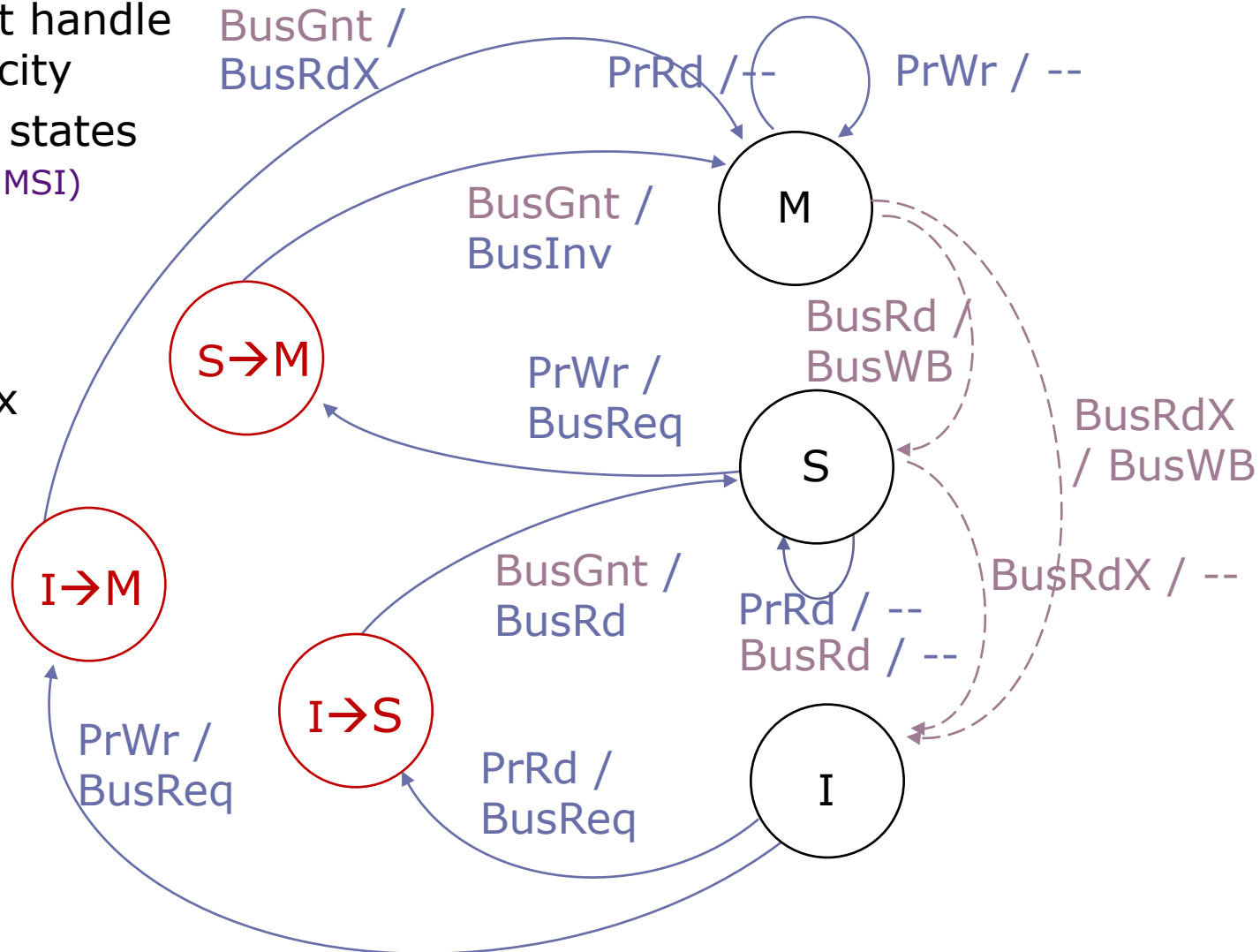
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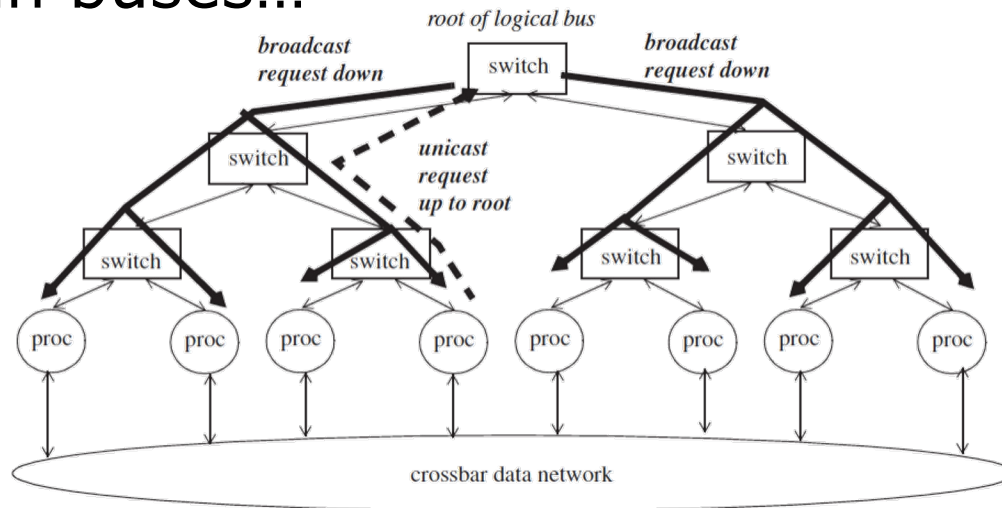
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Scaling Cache Coherence

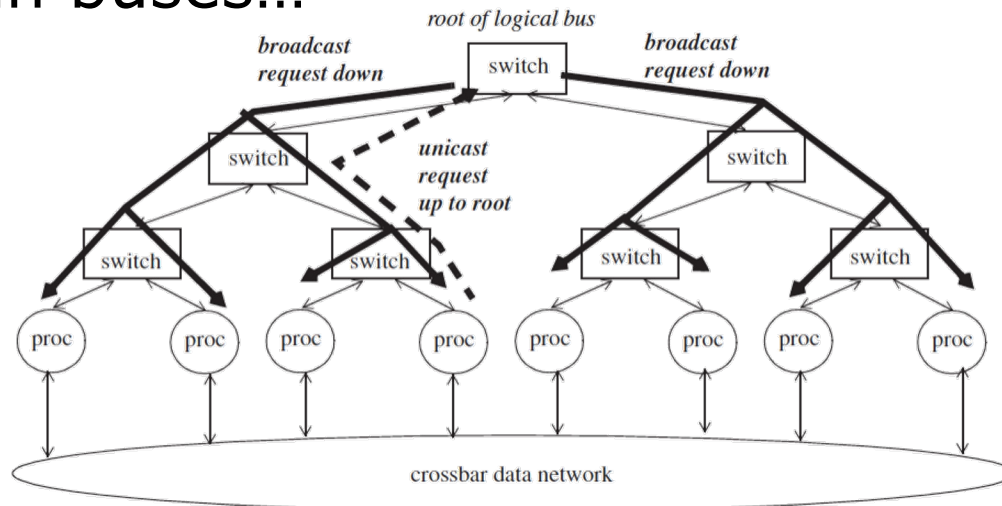
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Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors

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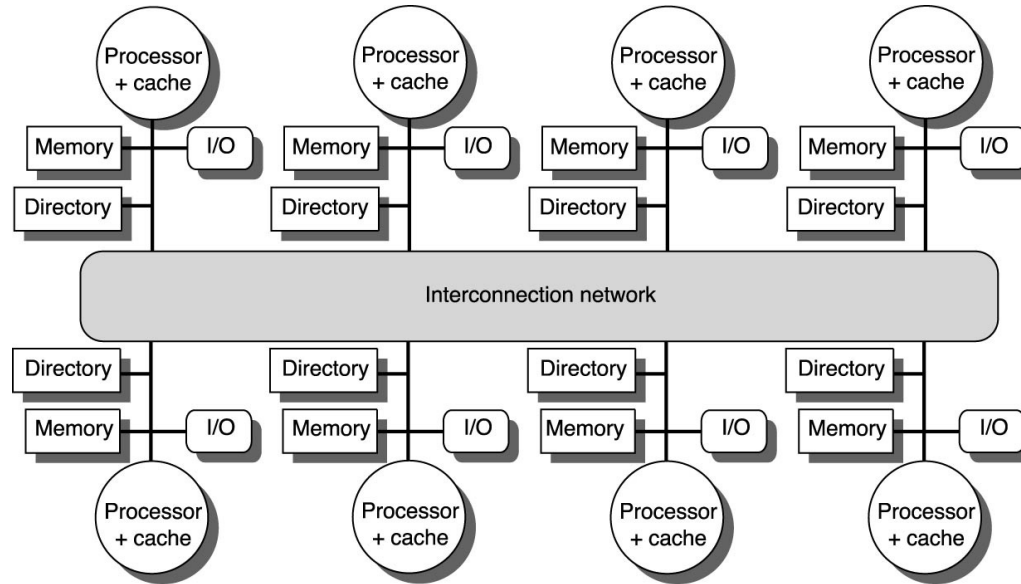
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Starfire E10000 (drawn with only eight processors for clarity). A coherence request is *unicast* up to the root, where it is serialized, before being *broadcast* down to all processors

- ... but broadcast is fundamentally unscalable
 - Bandwidth, energy of transactions with 100s of cache snoops?

Directory-Based Coherence



- Route all coherence transactions through a directory
 - Tracks contents of private caches → No broadcasts
 - Serves as ordering point for conflicting requests → Unordered networks

(more on next lecture)

Coherence and False Sharing

Performance Issue #1



A cache block contains more than one word and cache coherence is done at the block-level and not word-level

Coherence and False Sharing

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Suppose P_1 writes word_i and P_2 writes word_k and both words have the same block address.

What can happen?

Coherence and False Sharing

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What can happen? The block may be invalidated (ping-pong) many times unnecessarily because addresses are in the same block.

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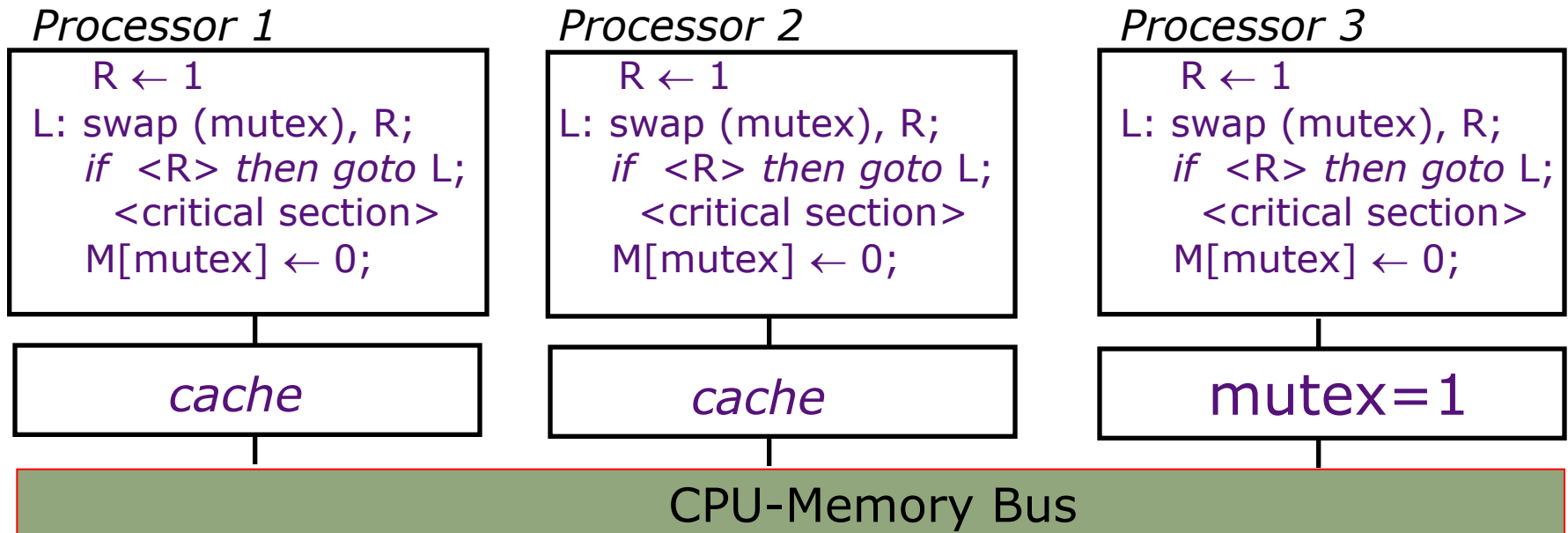
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How to address this problem?

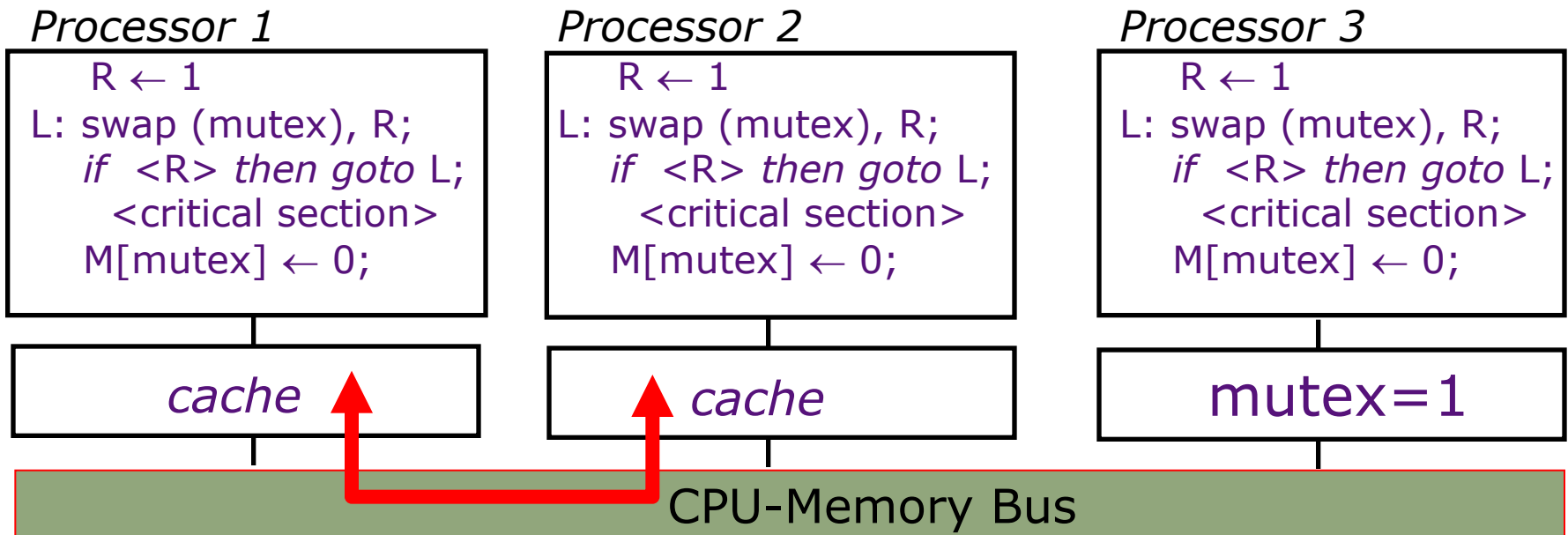
Coherence and Synchronization

Performance Issue #2



Coherence and Synchronization

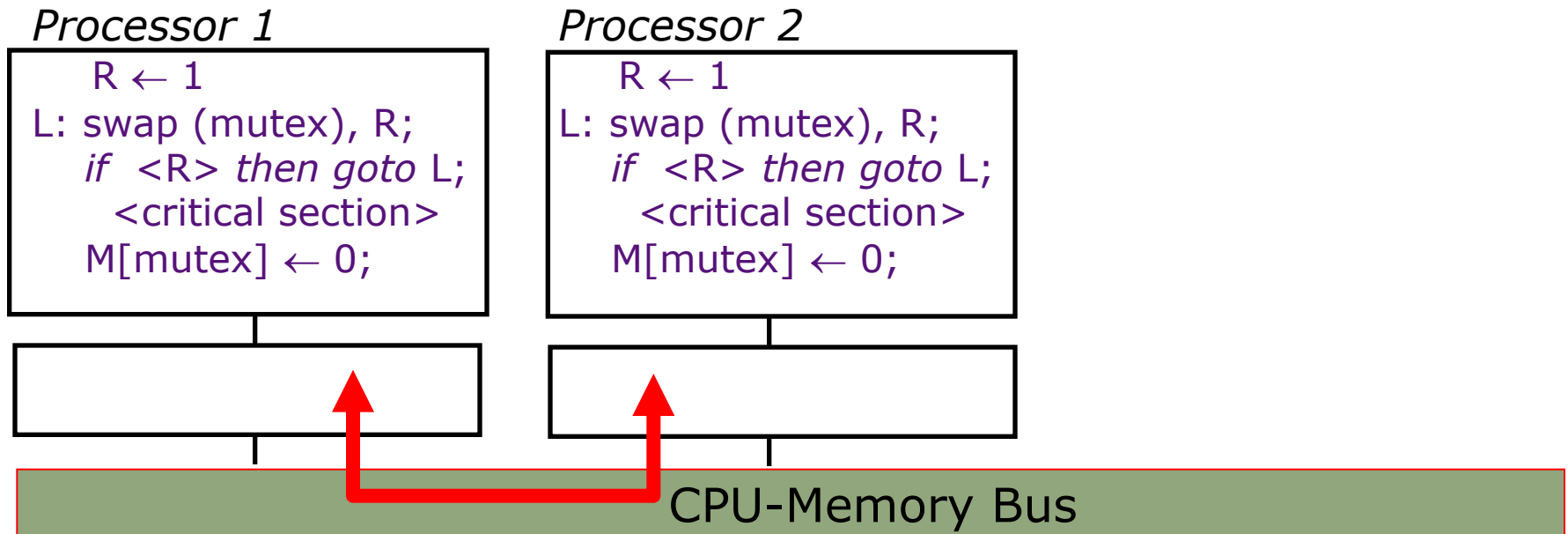
Performance Issue #2



Cache coherence protocols will cause **mutex** to *ping-pong* between P1's and P2's caches.

Coherence and Synchronization

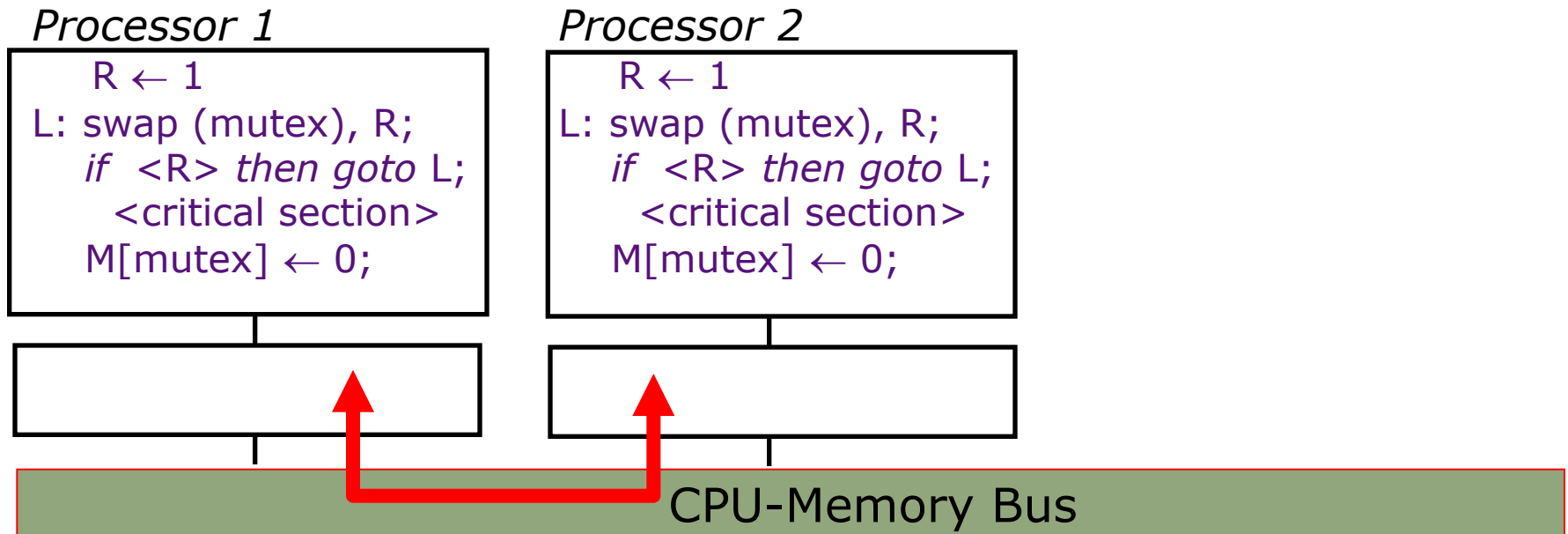
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Coherence and Synchronization

Performance Issue #2



Cache coherence protocols will cause **mutex** to *ping-pong* between P1's and P2's caches.

Ping-ponging can be reduced by first reading the **mutex** location (*non-atomically*) and executing a swap only if it is found to be zero (test&test&set).

Coherence and Bus Occupancy

Performance Issue #3

- In general, an *atomic read-modify-write* instruction requires two memory (bus) operations without intervening memory operations by other processors



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 - ⇒ expensive for simple buses
 - ⇒ *very expensive* for split-transaction buses
- modern processors use
 - load-reserve*
 - store-conditional*

Load-reserve & Store-conditional

Special register(s) to hold reservation flag and address, and the outcome of store-conditional

```
Load-reserve R, (a):  
  <flag, adr> ← <1, a>;  
  R ← □M[a];
```

```
Store-conditional (a), R:  
  if <flag, adr> == <1, a>  
  then cancel other procs'  
        reservation on a;  
        M[a] ← <R>;  
        status ← succeed;  
  else status ← fail;
```

If the snooper sees a store transaction to the address in the reserve register, the reserve bit is set to **0**

- Several processors may reserve 'a' simultaneously
- These instructions are like ordinary loads and stores with respect to the bus traffic

Performance:

Load-reserve & Store-conditional

The total number of memory (bus) transactions is not necessarily reduced, but splitting an atomic instruction into load-reserve & store-conditional:

- *increases bus utilization* (and reduces processor stall time), especially in split-transaction buses
- *reduces cache ping-pong effect* because processors trying to acquire a mutex do not have to perform stores each time

Thank you!

*Next lecture: Directory-based
Cache Coherence*