Security

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Security and Information Leakage

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- In specific, they have been used as channels to leak information!

Standard Communication Model

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1. Transmitter gets a message

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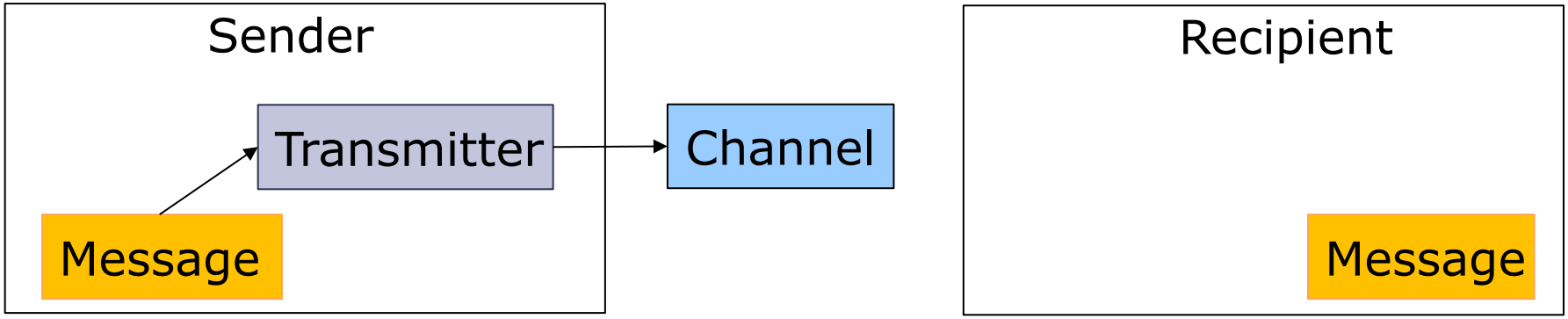

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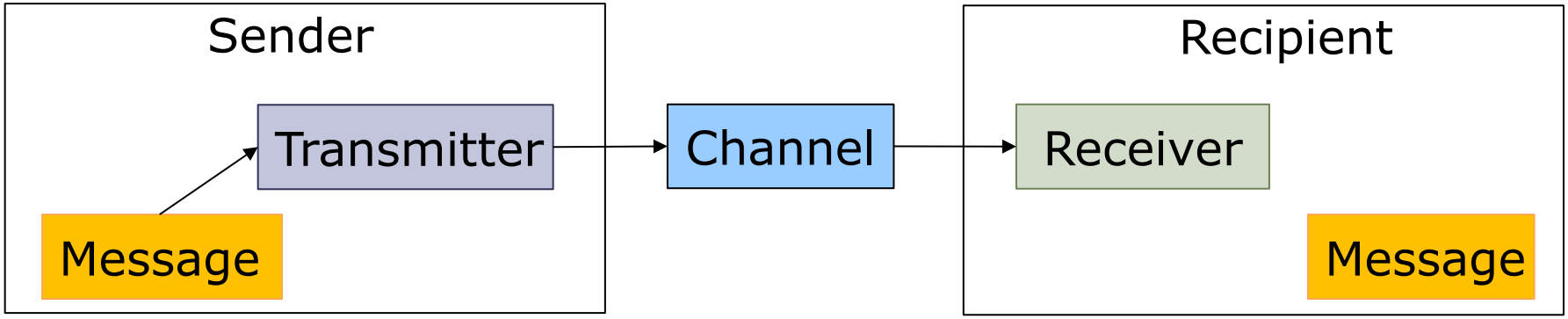

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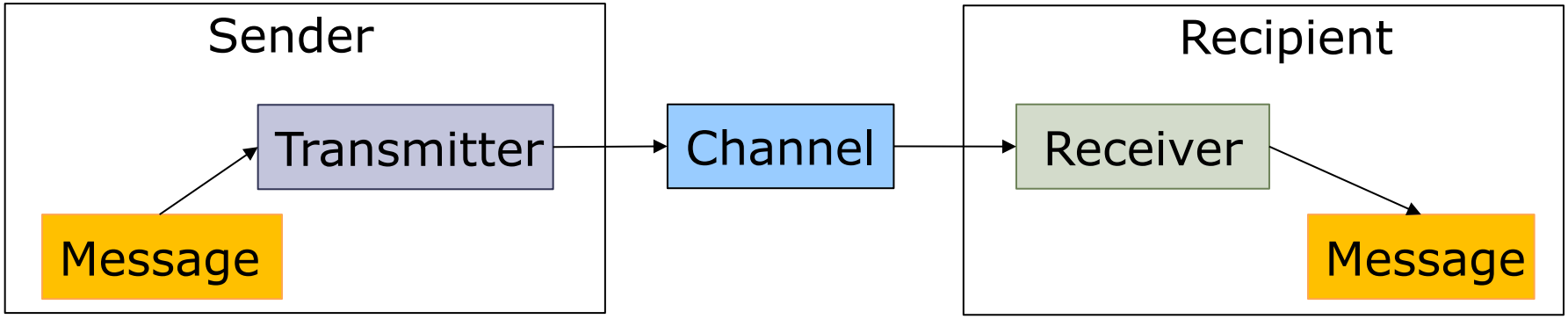
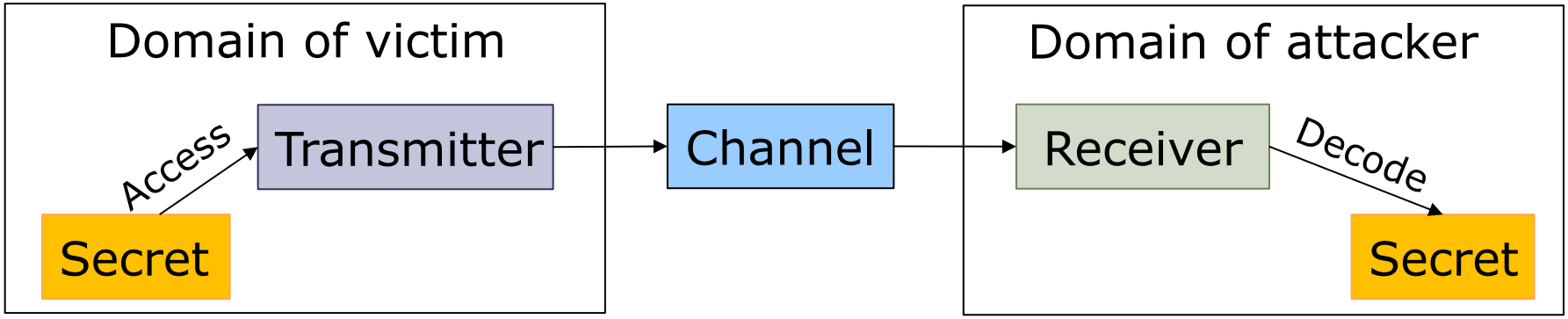


1. Transmitter gets a message
2. Transmitter modulates channel
3. Receiver detects modulation on channel
4. Receiver decodes modulation as message

Communication Model of Attacks
[Belay, Devadas, Emer]



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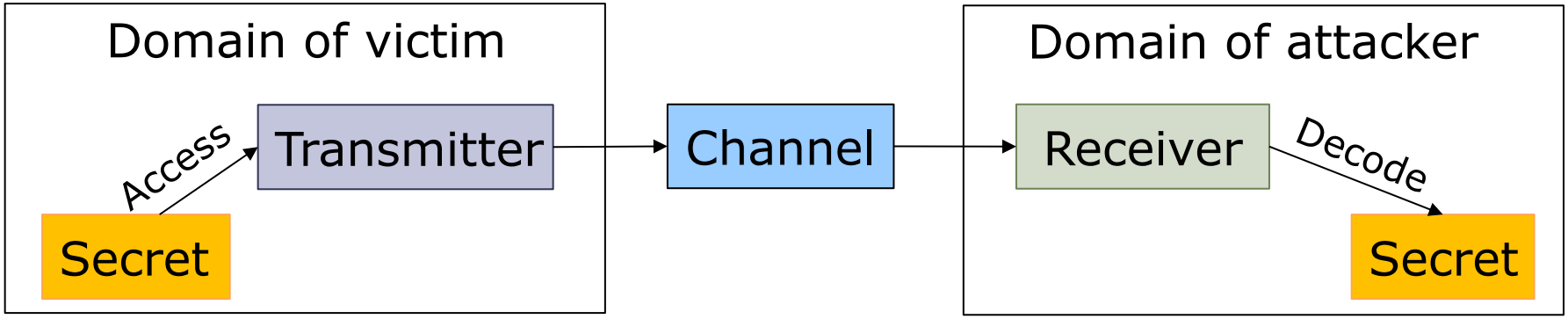

- Domains – Distinct architectural domains in which architectural state is not shared.
- Secret – the "message" that is transmitted on the channel and detected by the receiver
- Channel – some "state" that can be changed, i.e., modulated, by the "transmitter" and whose modulation can be detected by the "receiver".

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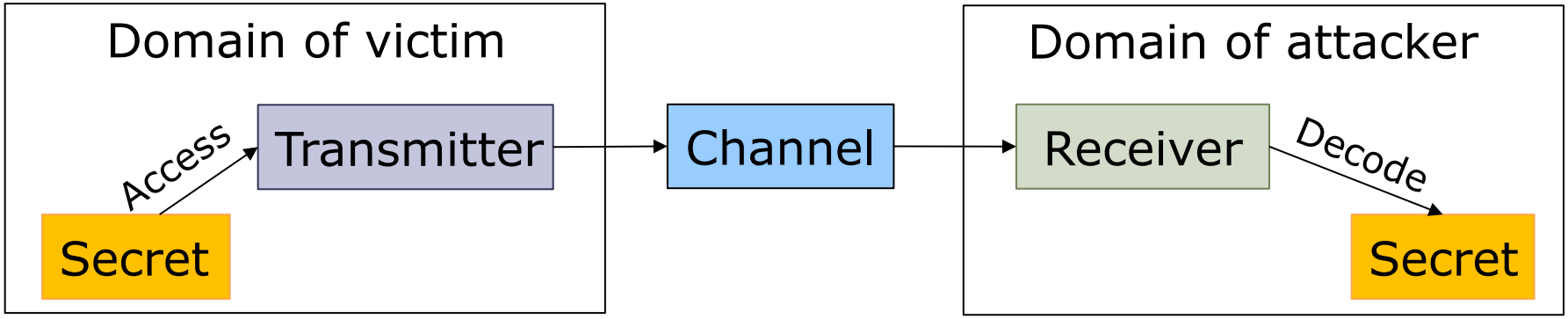

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Because channel is not a "direct" communication channel, it is often referred to as a "side channel"

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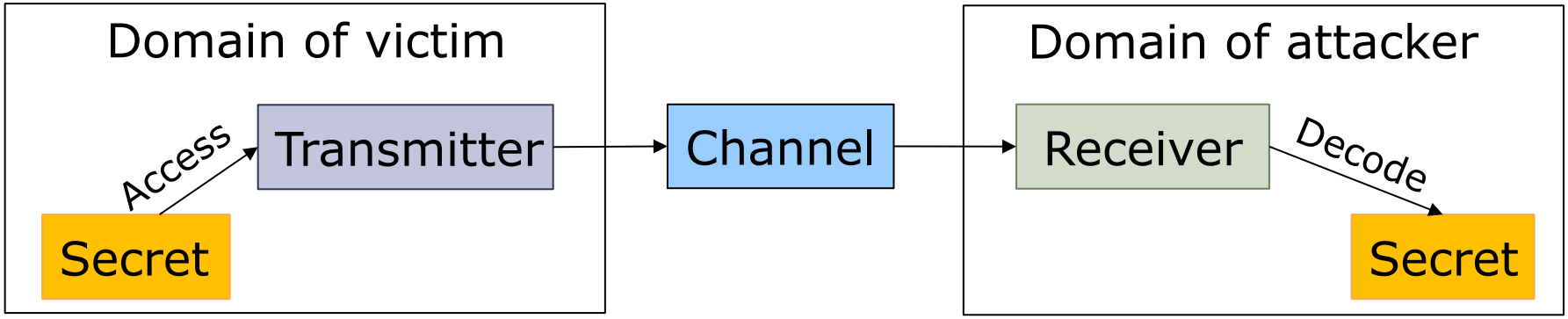
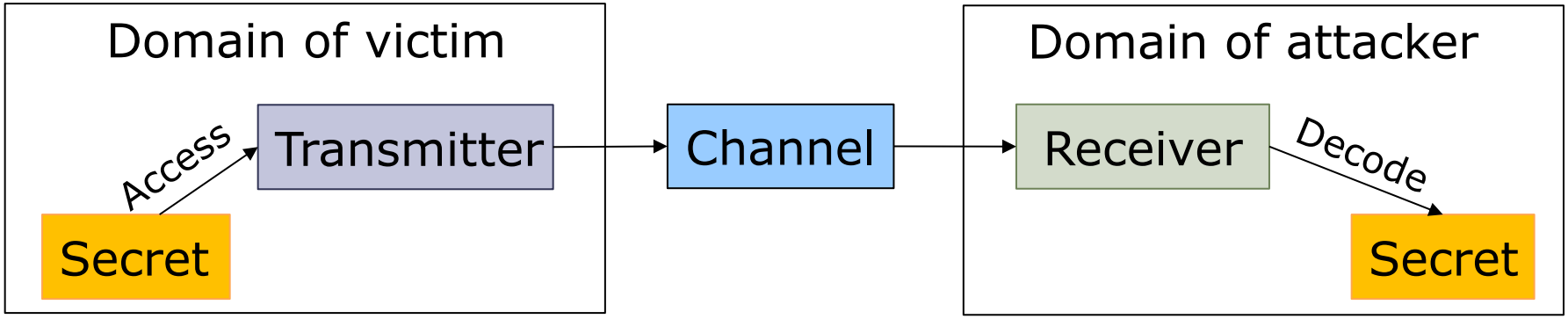


1. Transmitter "accesses" secret
2. Transmitter modulates channel *(microarchitectural state)* with a message based on secret
3. Receiver detects modulation on channel
4. Receiver decodes modulation as a message containing the secret

ATM Acoustic Channels



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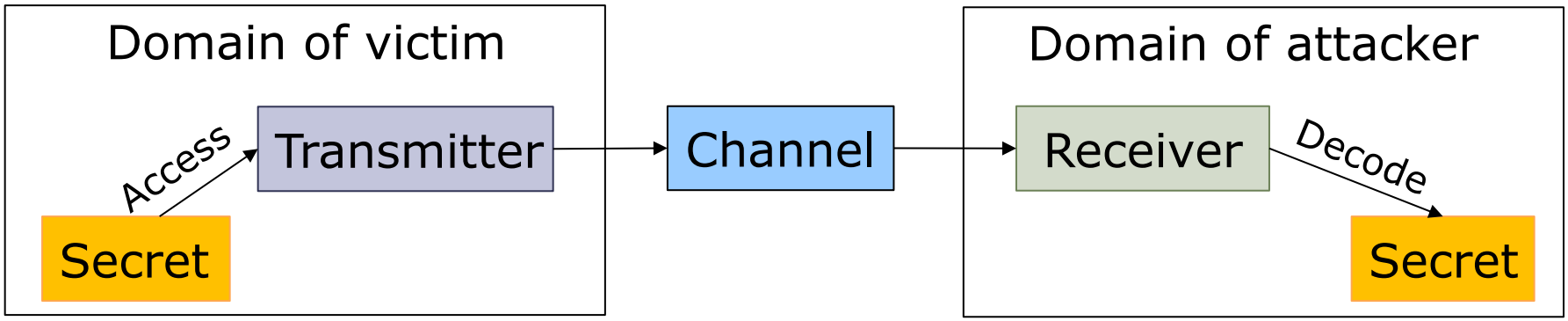

- Secret:
- Transmitter:
- Channel:
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- Decoders:

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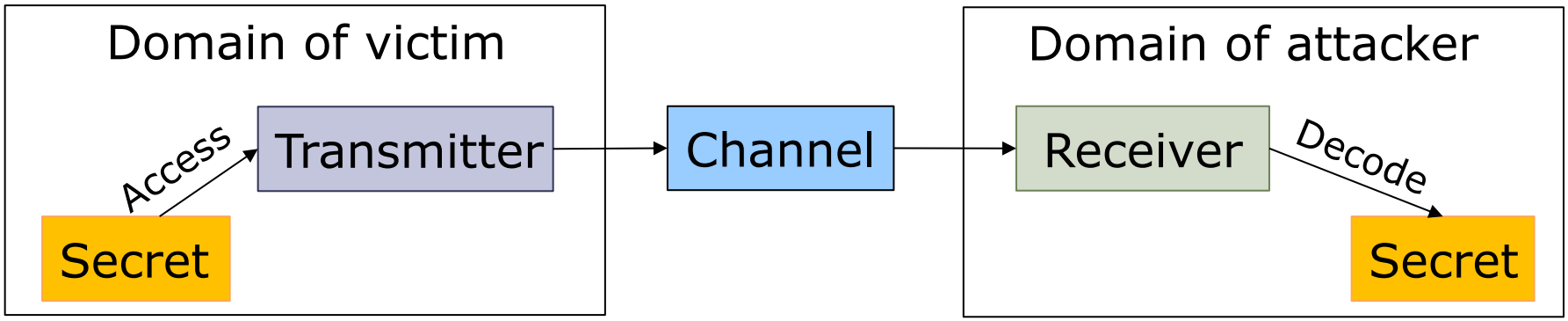

- Secret: Pin
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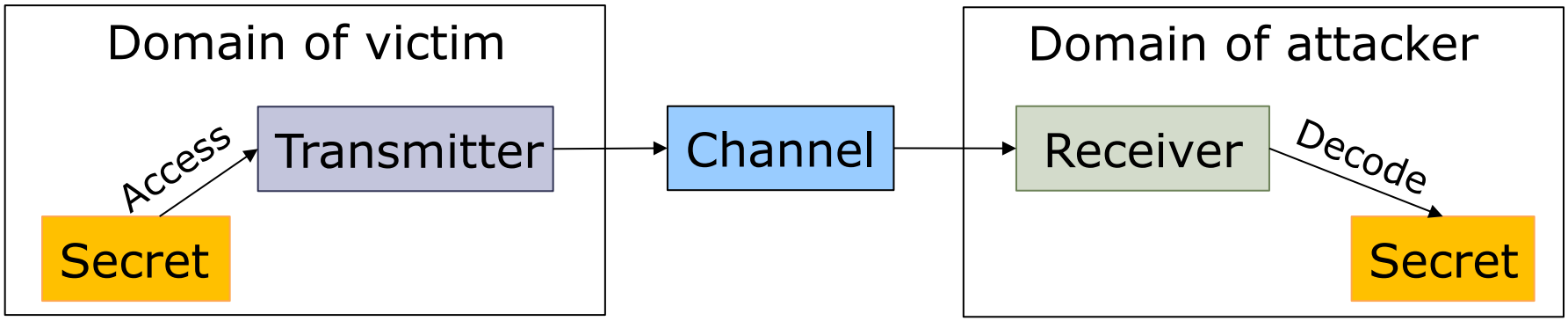

- Secret: Pin
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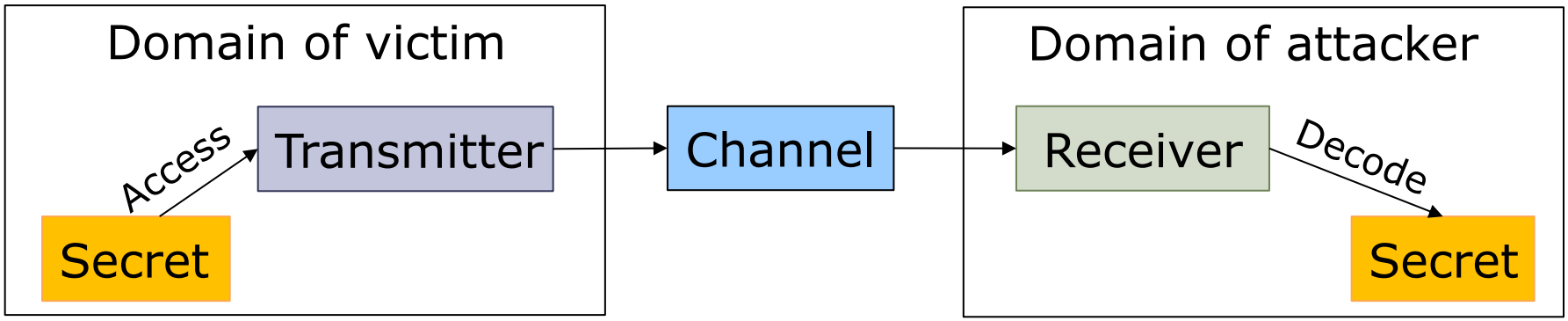

- Secret: Pin
- Transmitter: Keypad
- Channel: Air
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- Receiver:
- Decoders:

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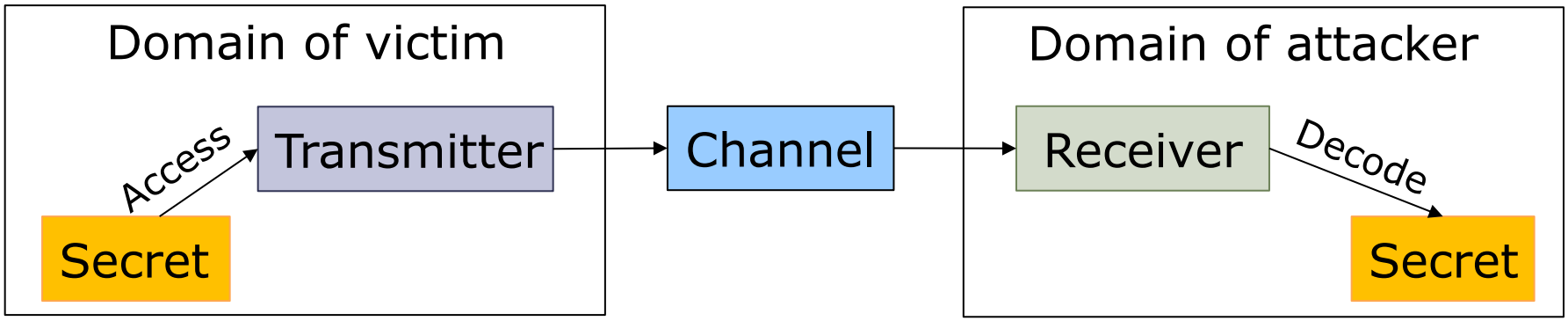

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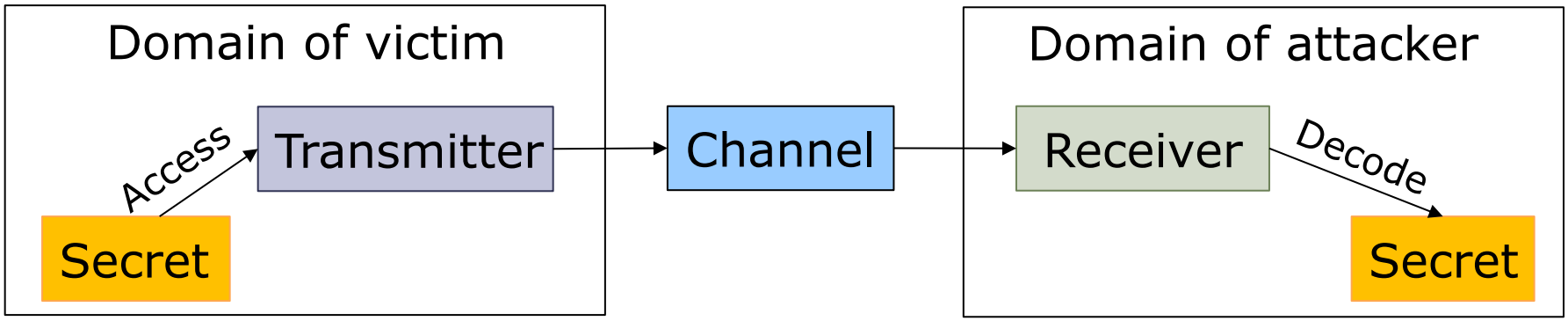

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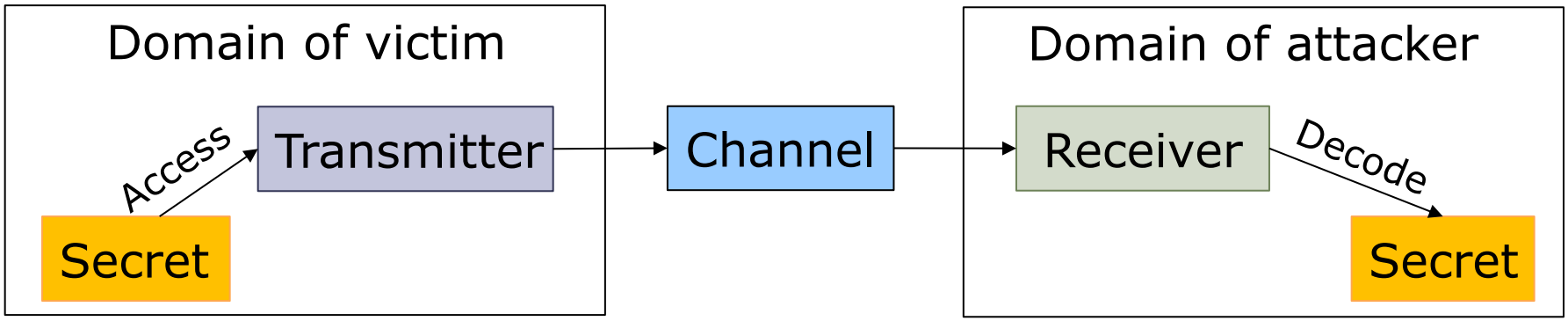

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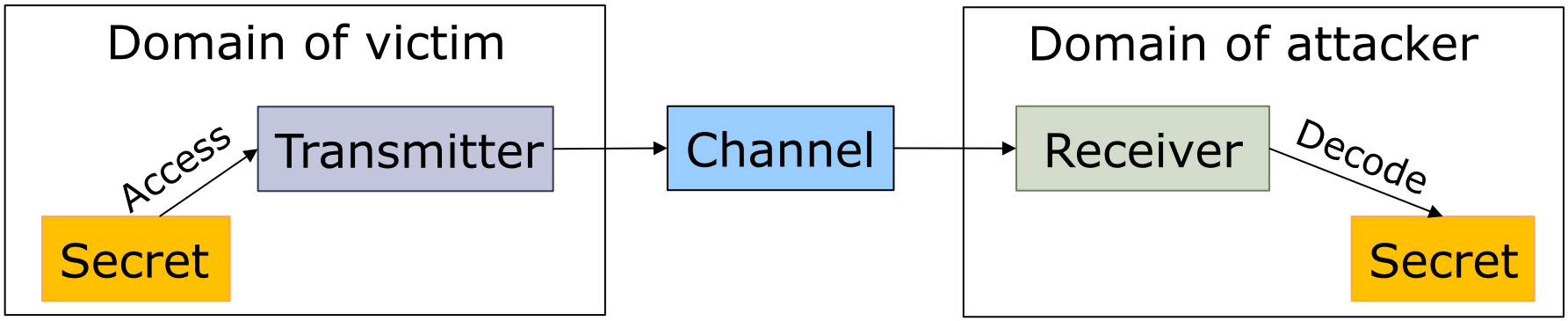

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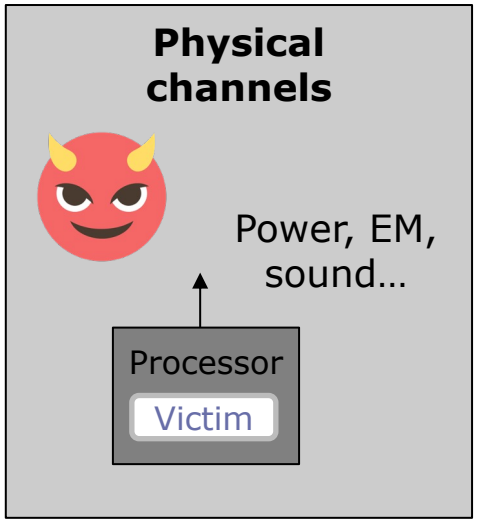
Physical vs Timing vs uArch Channel

- Types of channels



Attacker requires measurement equipment → physical access

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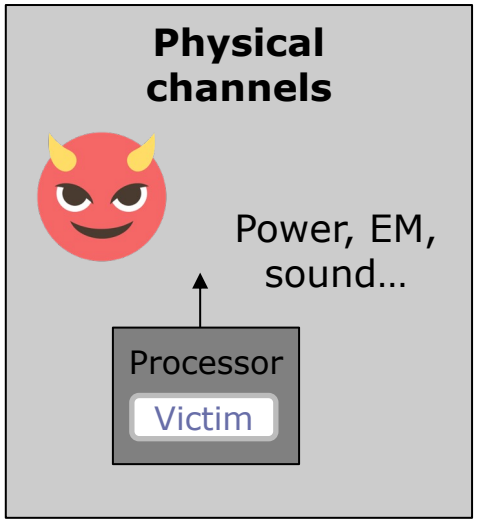

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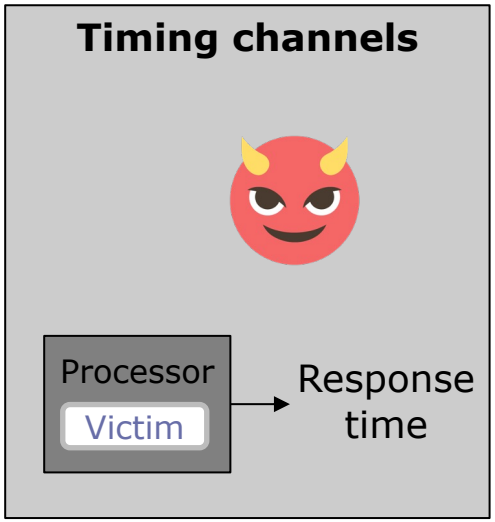

Attacker may be remote (e.g., over an internet connection)

Timing Channel Example

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def check(input):

  size = len(passwd);

  for i in range(0,size):
    if (input [i] == password[i]):
      return ("error");

  return (“success”)
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Can you guess the password by monitoring the execution time?

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Can you guess the password by monitoring the execution time?

The execution time is dependent on how many characters match between the input and the correct password. Attacker can brute-force each character.

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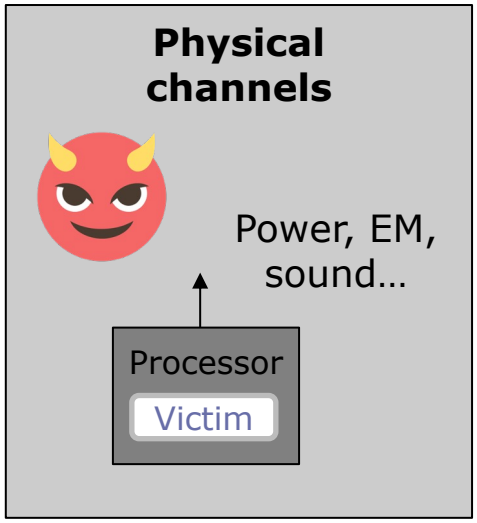

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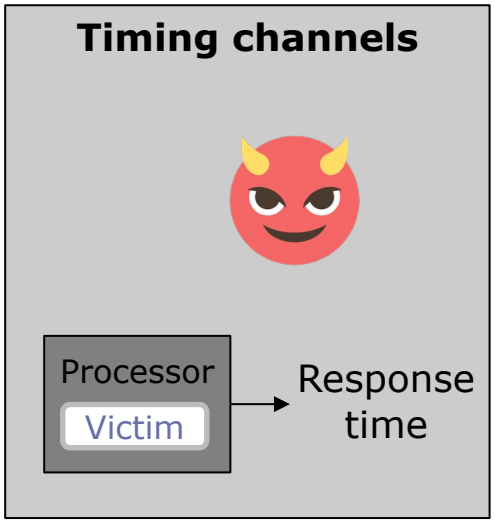

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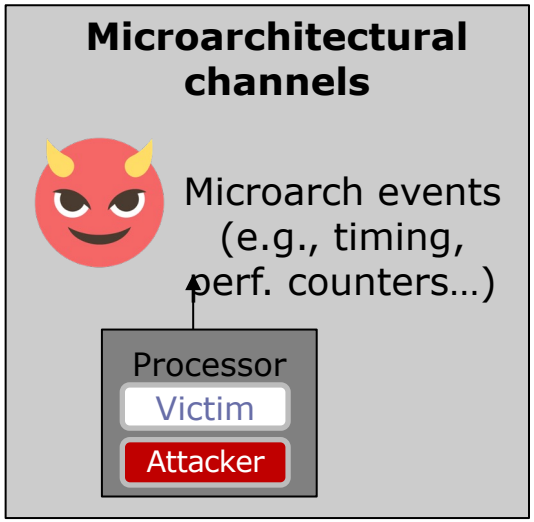

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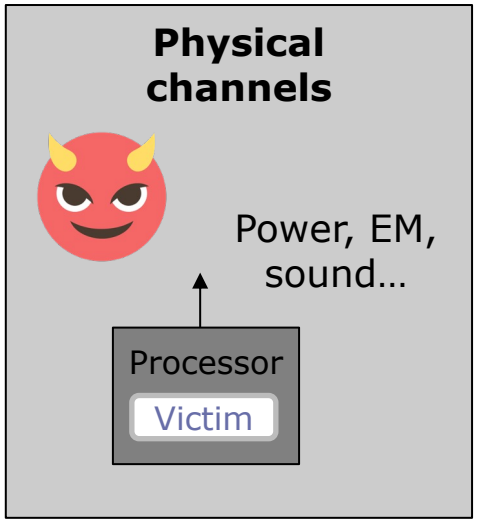

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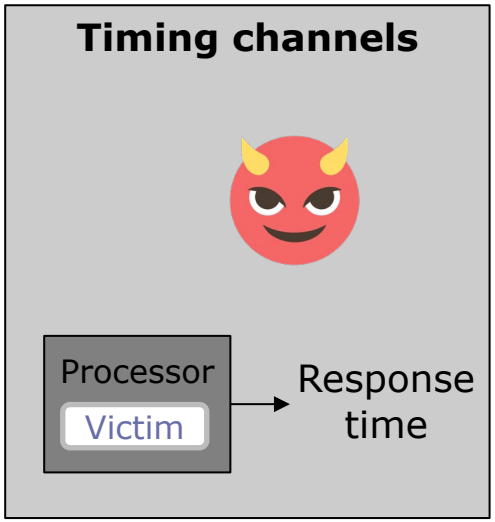

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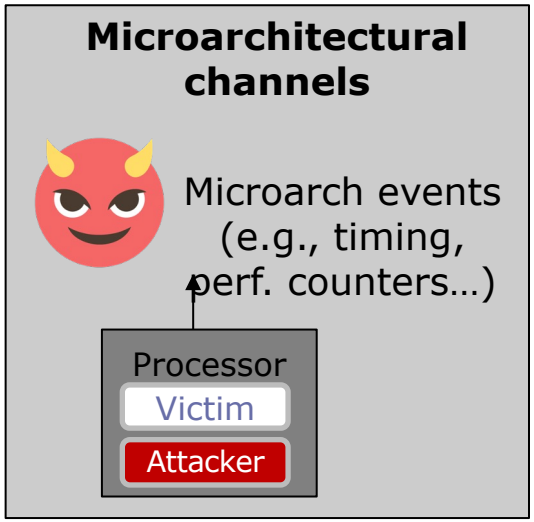

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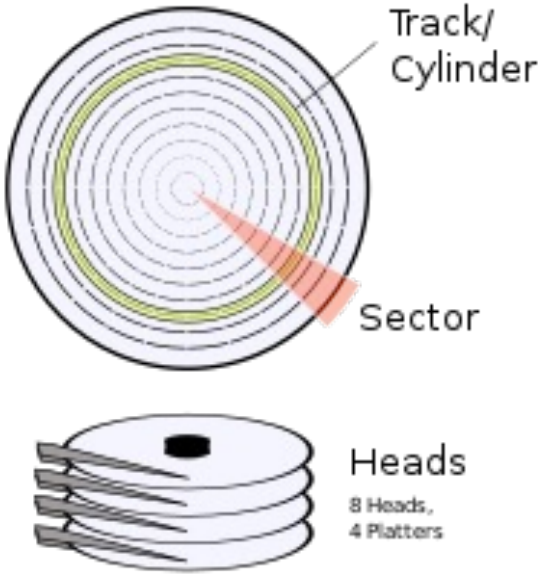
Different from traditional software or physical attacks:

- *Stealthy.* Sophisticated mechanisms needed to detect channel
- Usually, no permanent indication one has been exploited

Side Channel Attacks in 1977

- A side channel due to disk arm optimization
  - Enqueues requests by ascending cylinder number and dequeues (executes) them by the "elevator algorithm."



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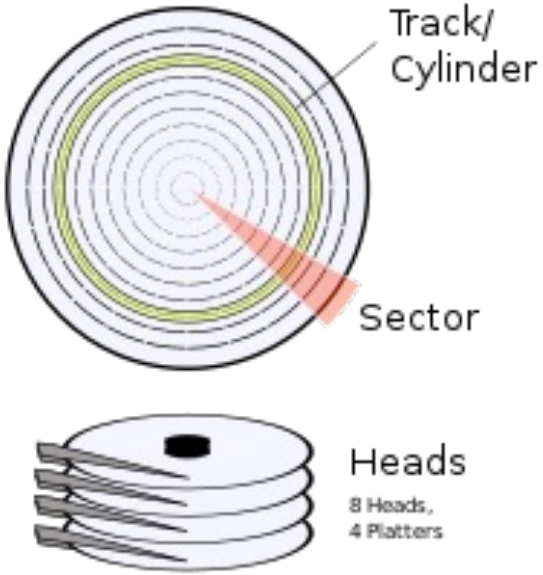

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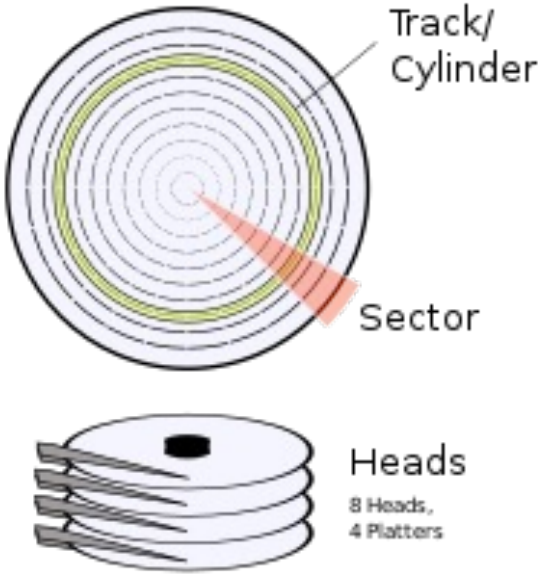

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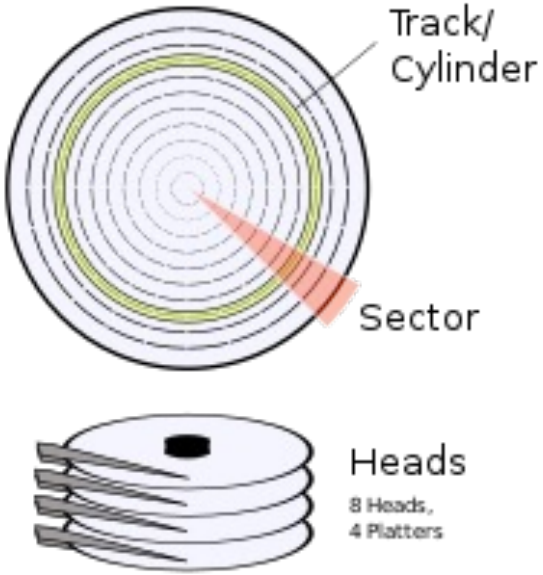

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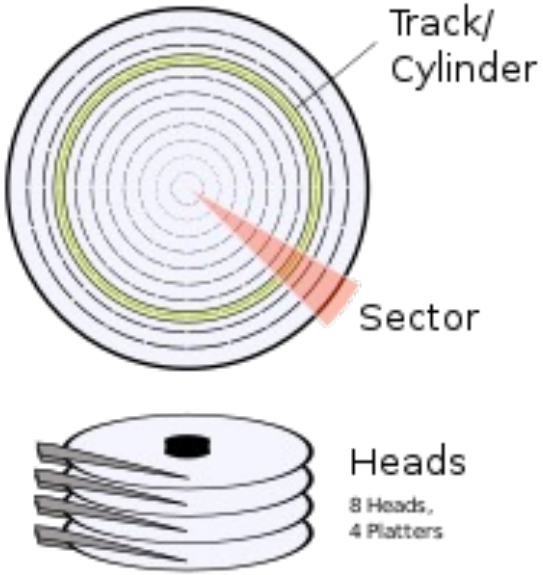

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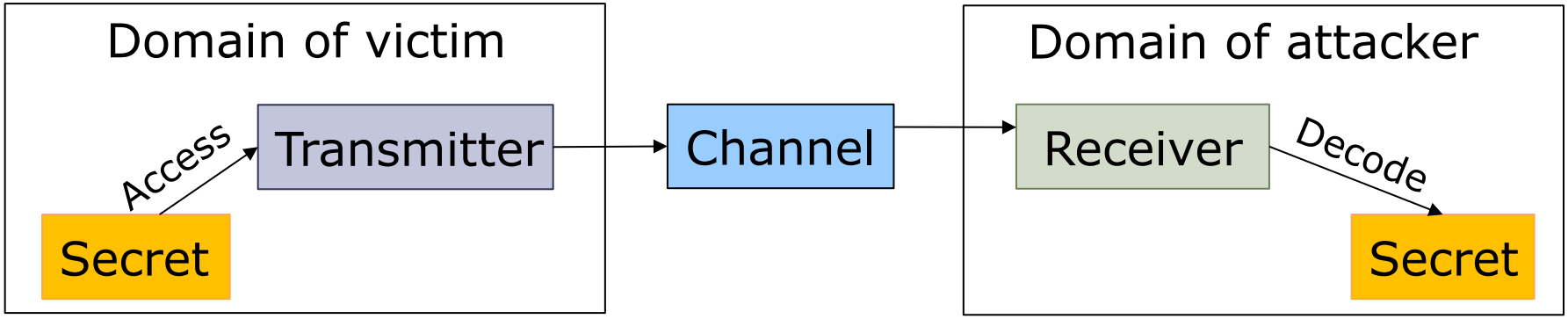
Note this requires an "active" receiver that preconditions the channel

Communication w/ Active Receiver



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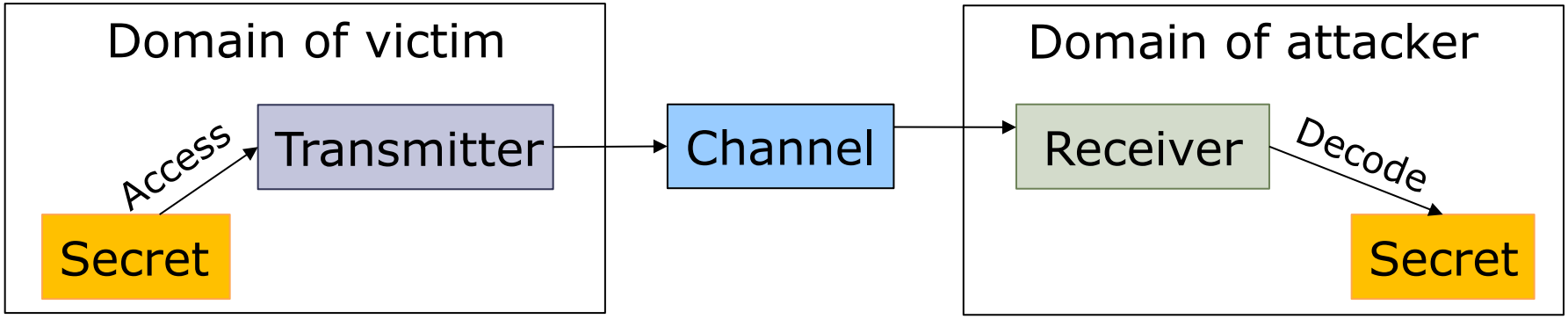

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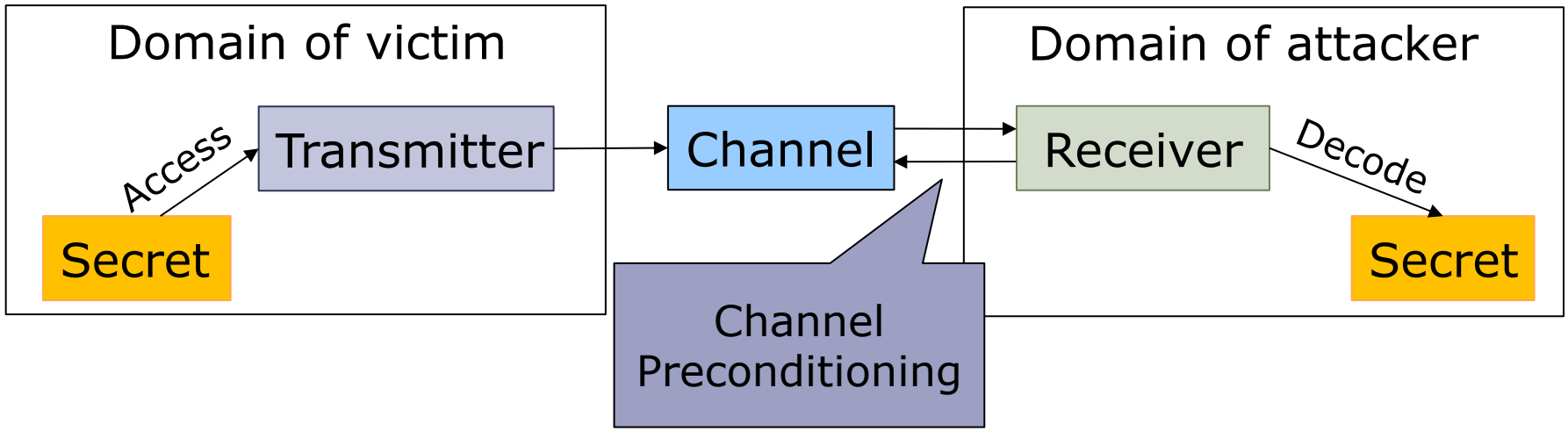

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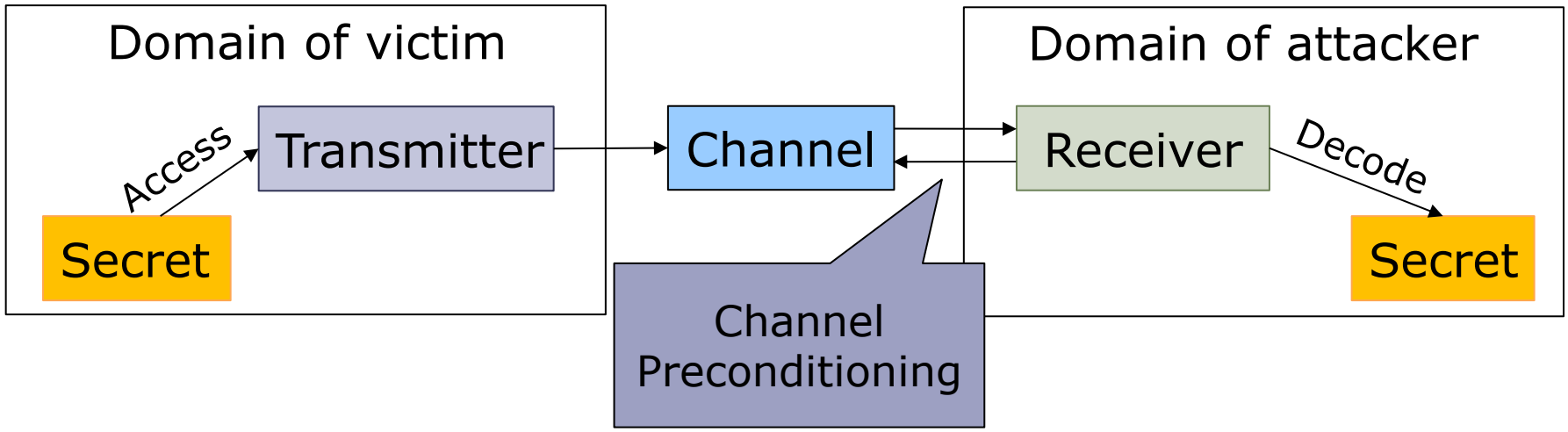
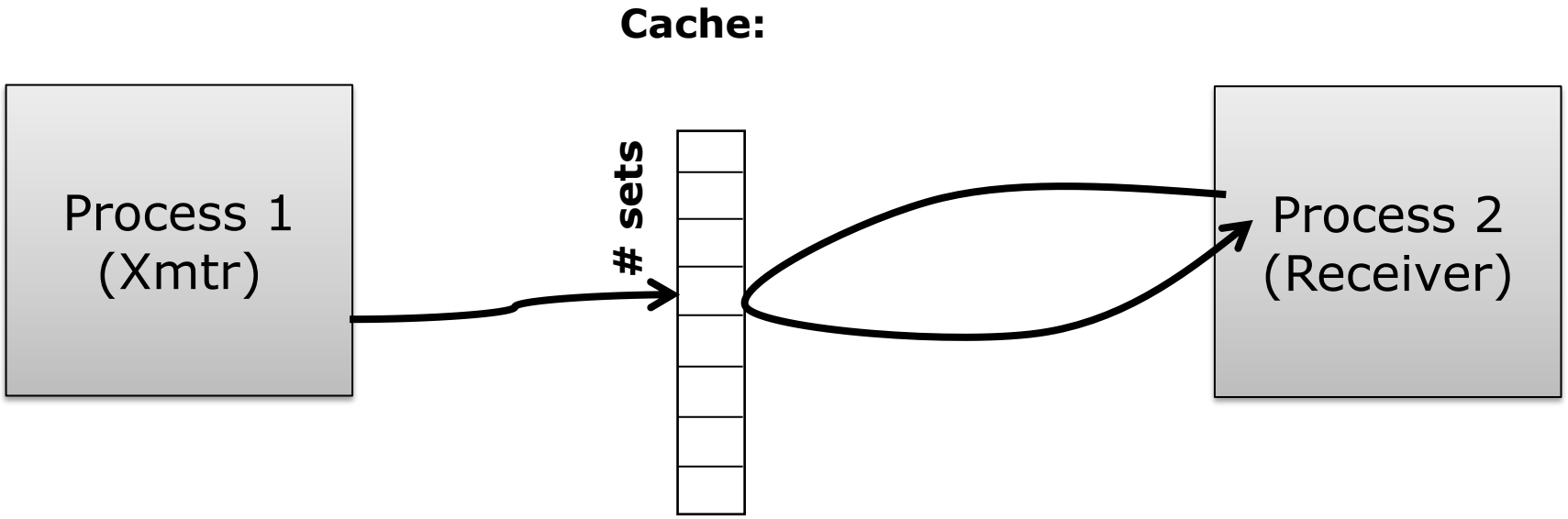


- An active receiver may need to "precondition" the channel to prepare for detecting modulation
- An active receiver also needs to deal with synchronization of transmission (modulation) activity with reception (demodulation) activity.

A Cache-based Channel



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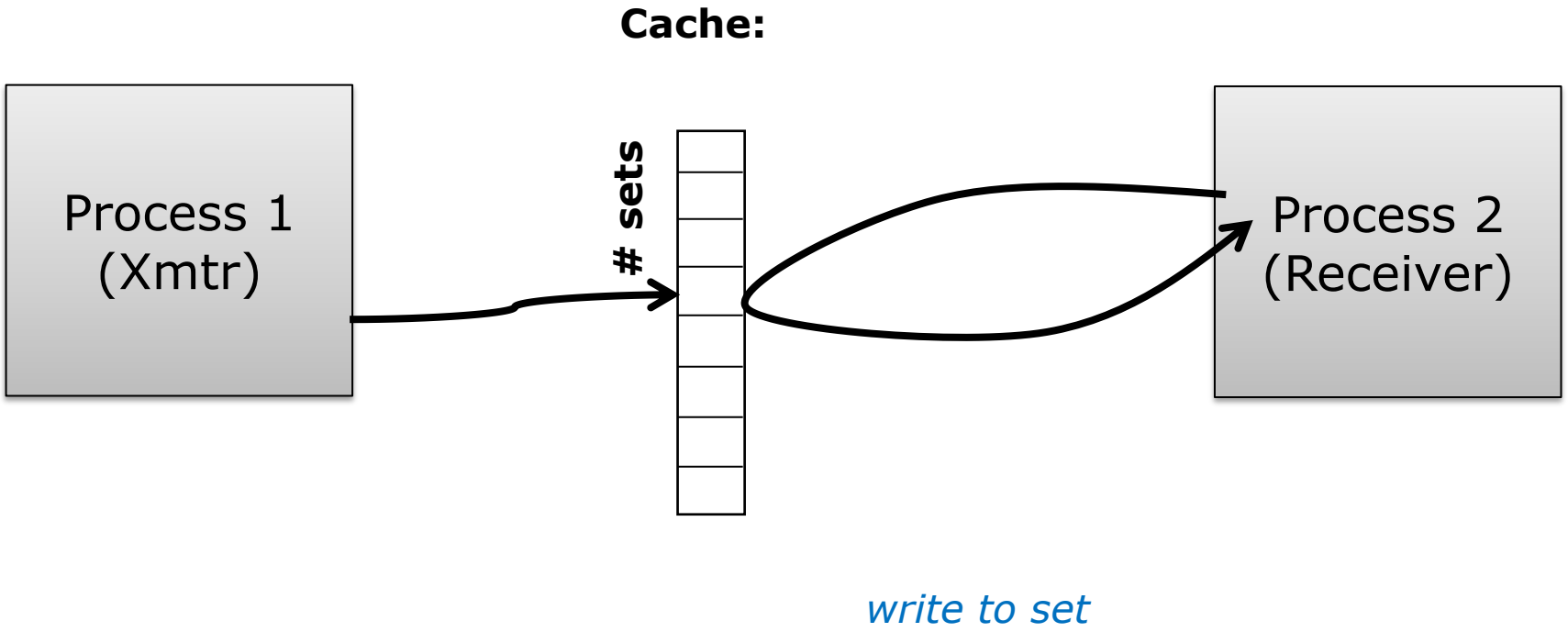

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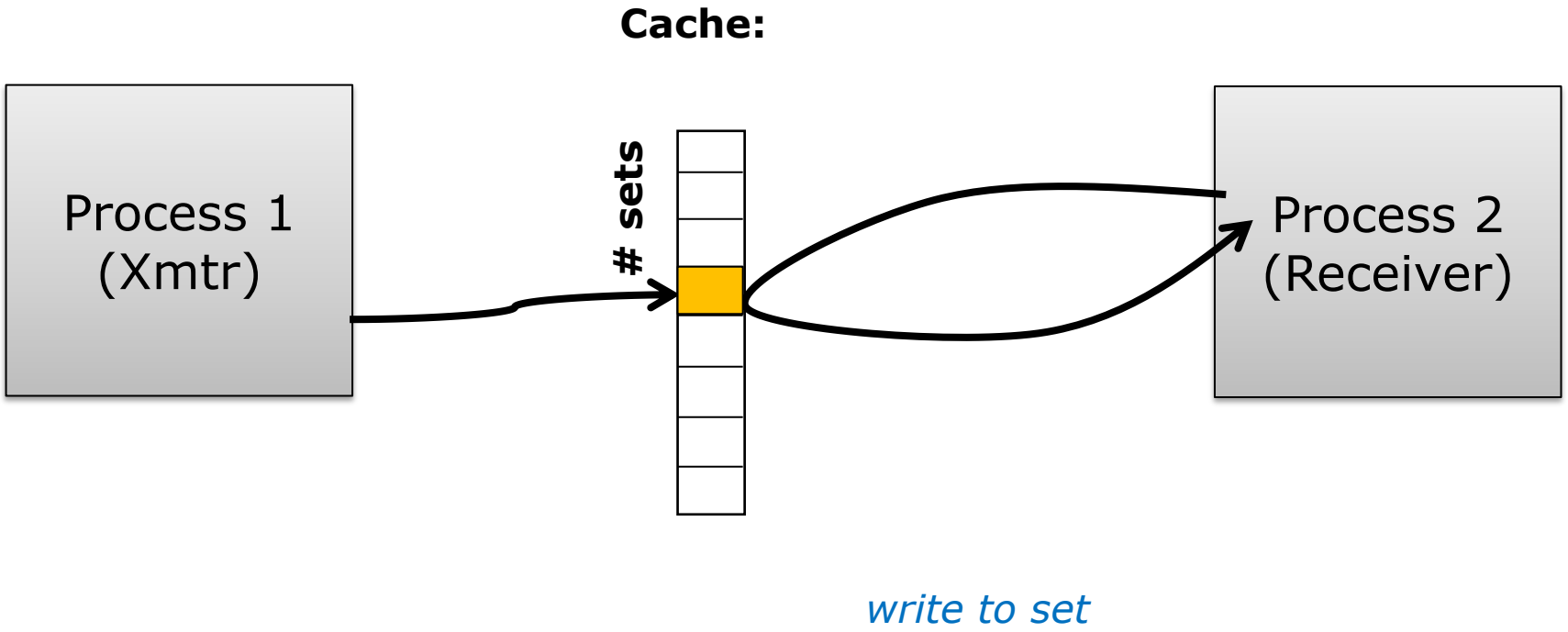

write to set

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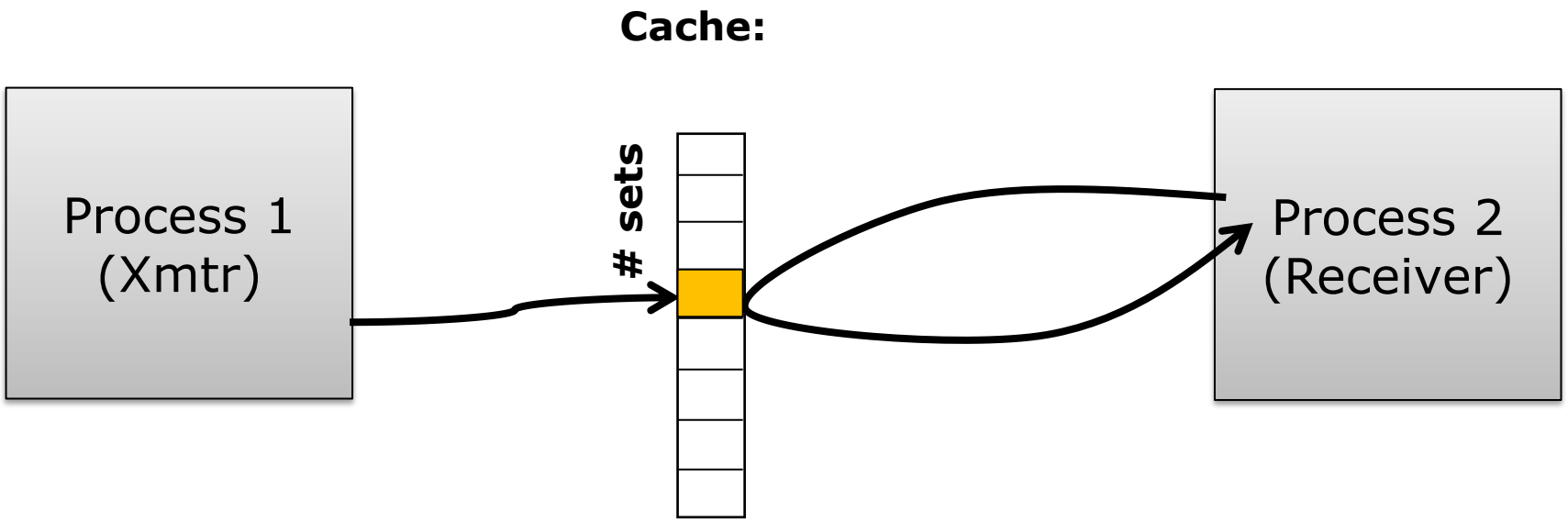

if (**send '0'**)
idle
else
write to a set

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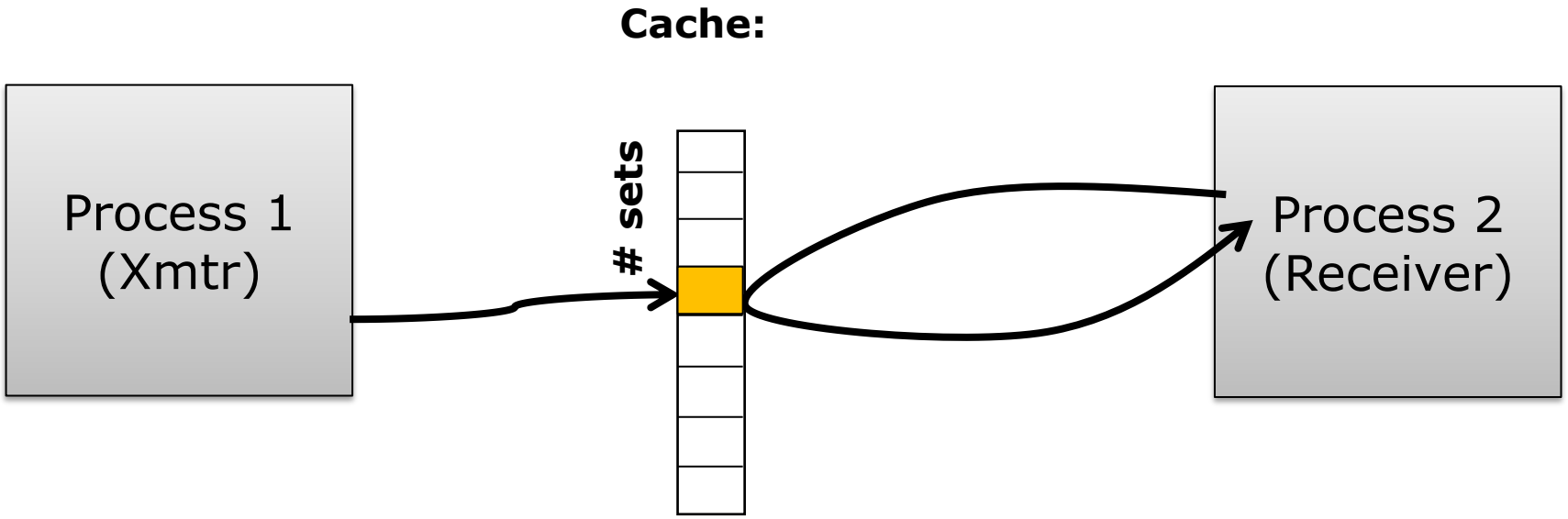

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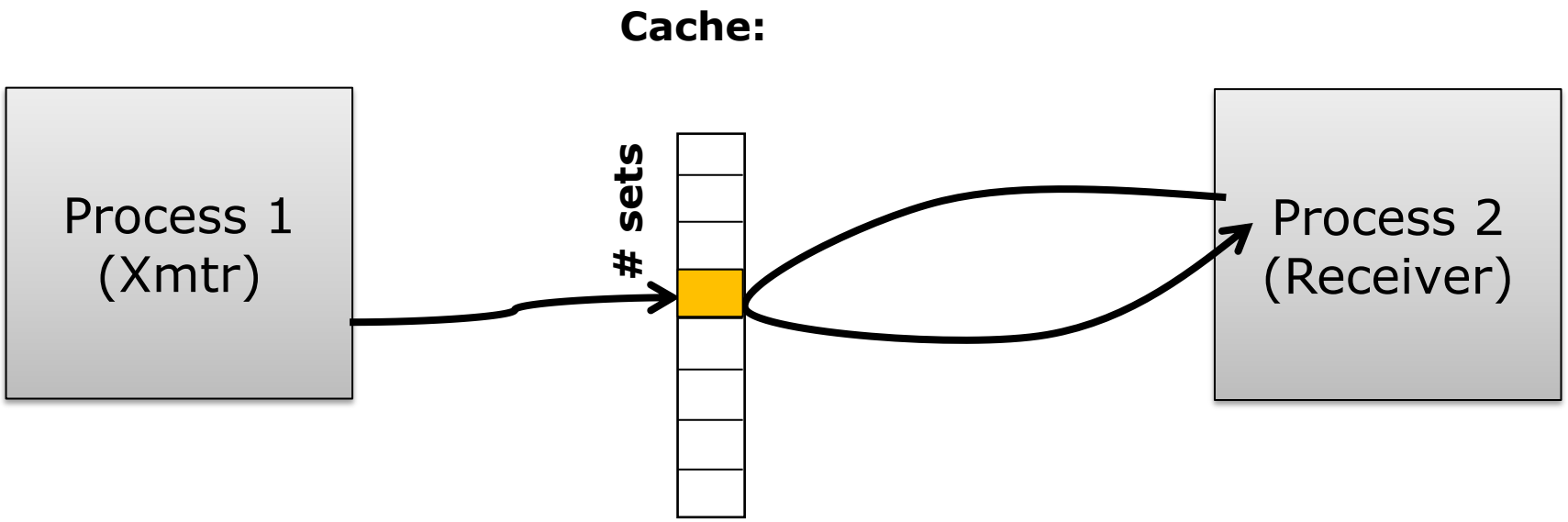

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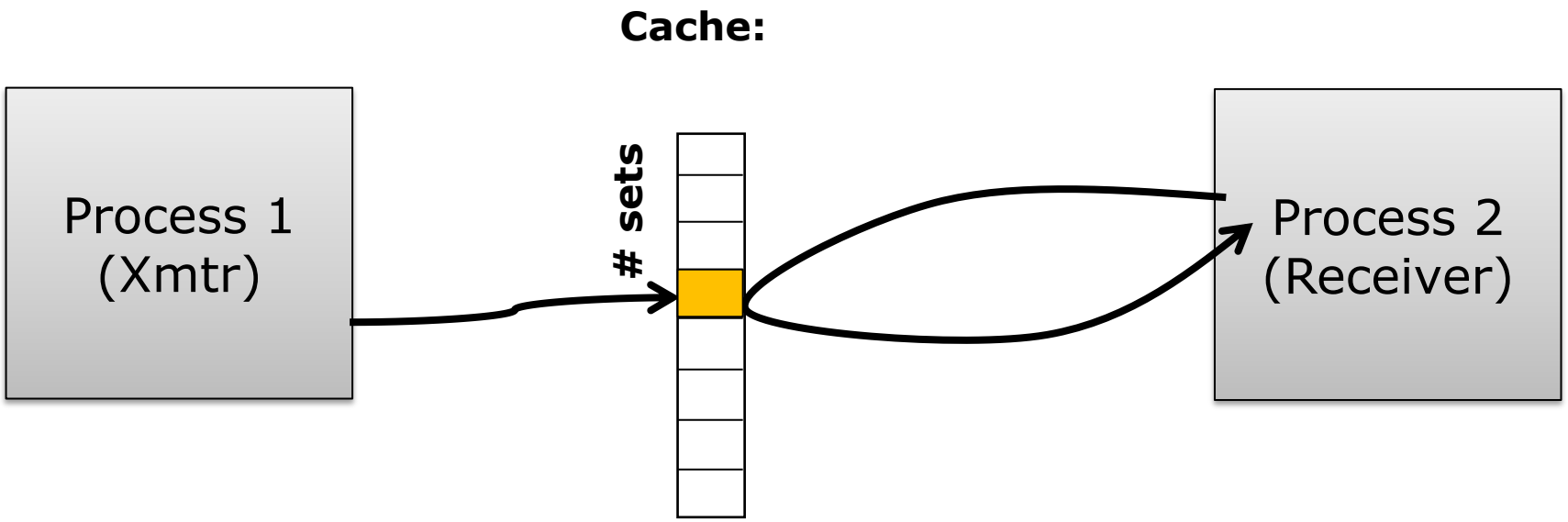

if (**send '0'**)
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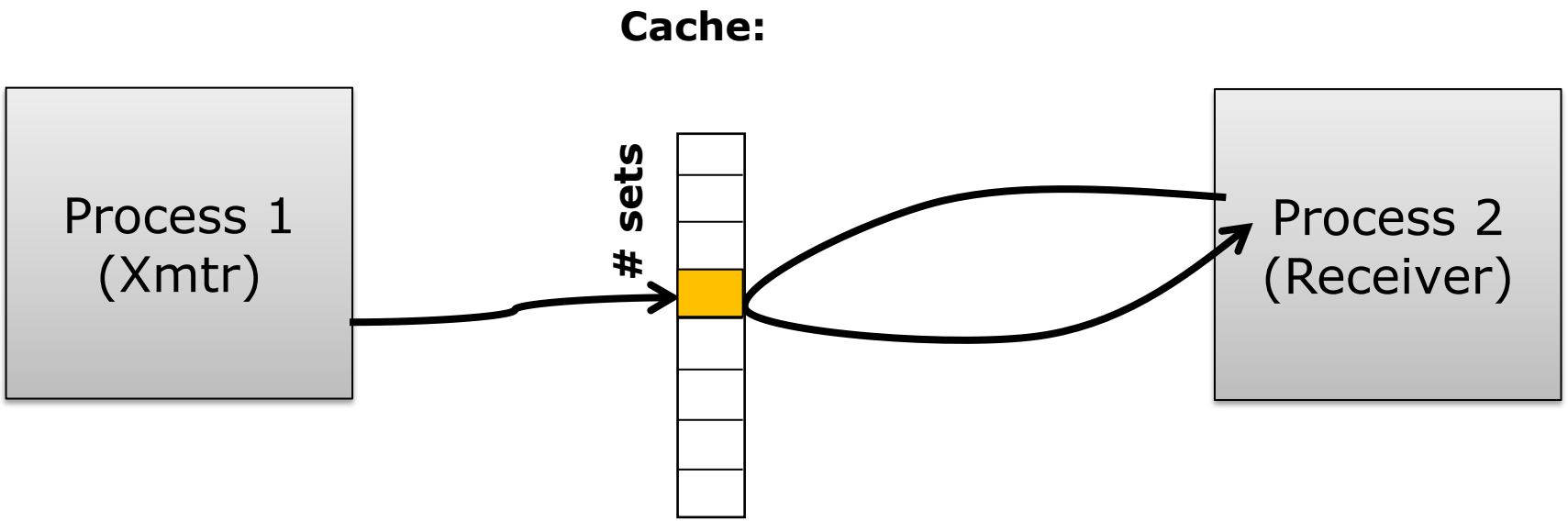
write to set

t1 = rdtsc()
read from the set
t2 = rdtsc()

if t2 – t1 > hit_time:
  decode '1'
else
  decode '0'

A Cache-based Channel



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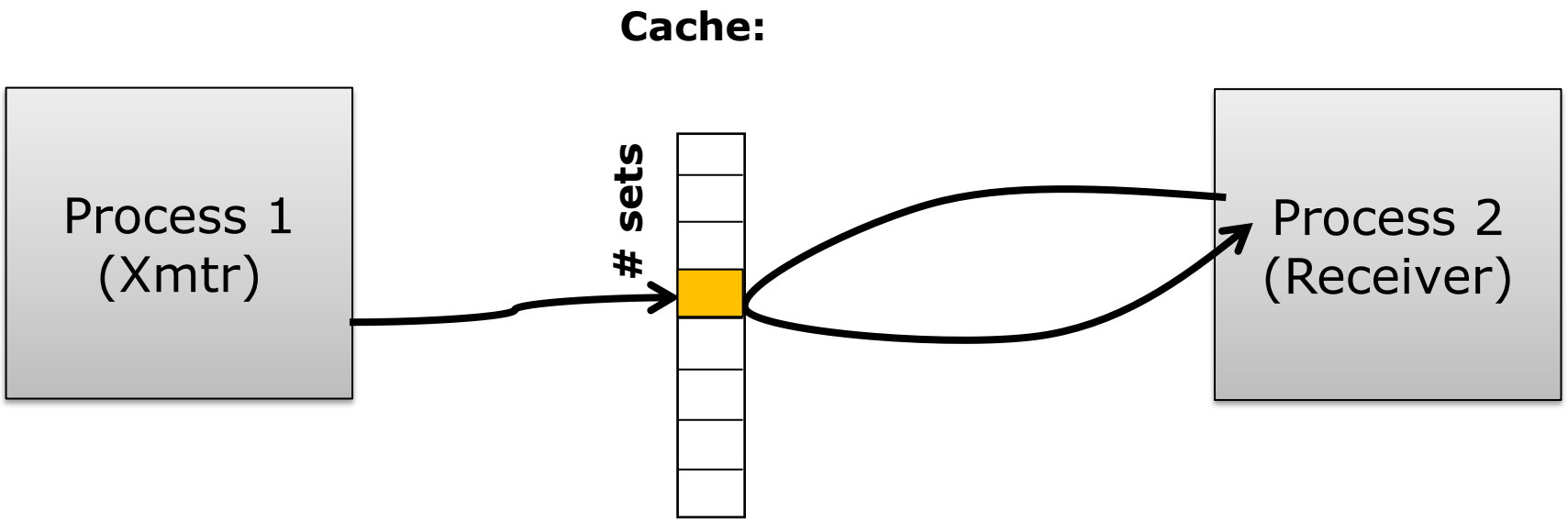

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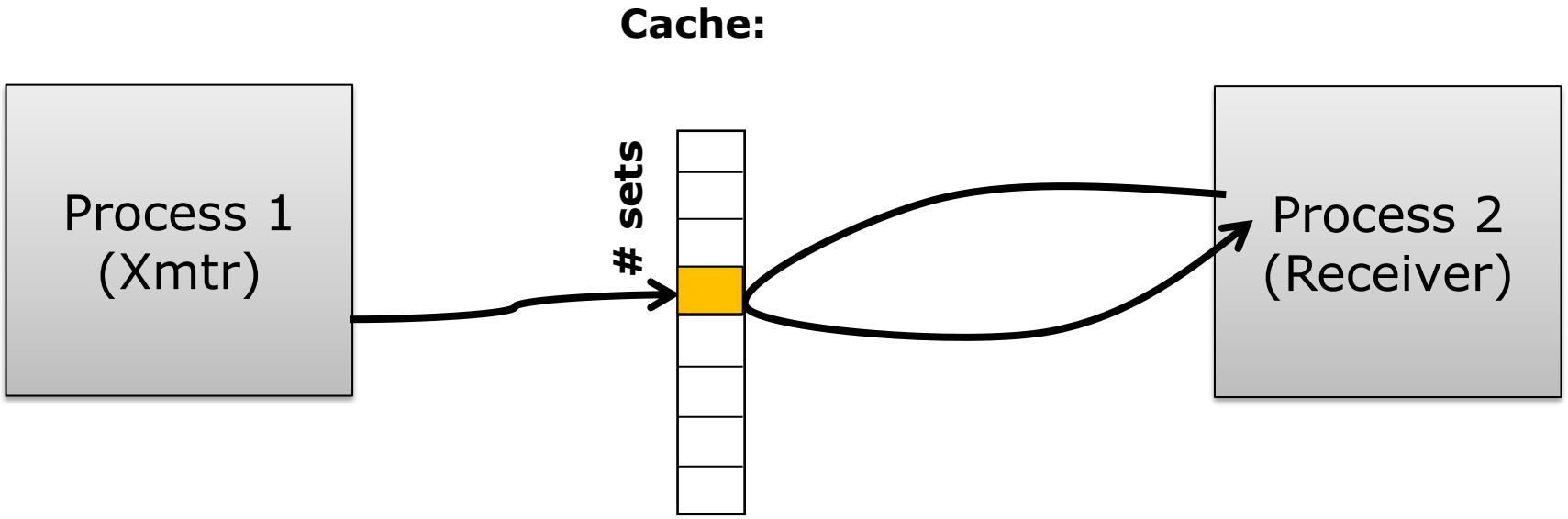

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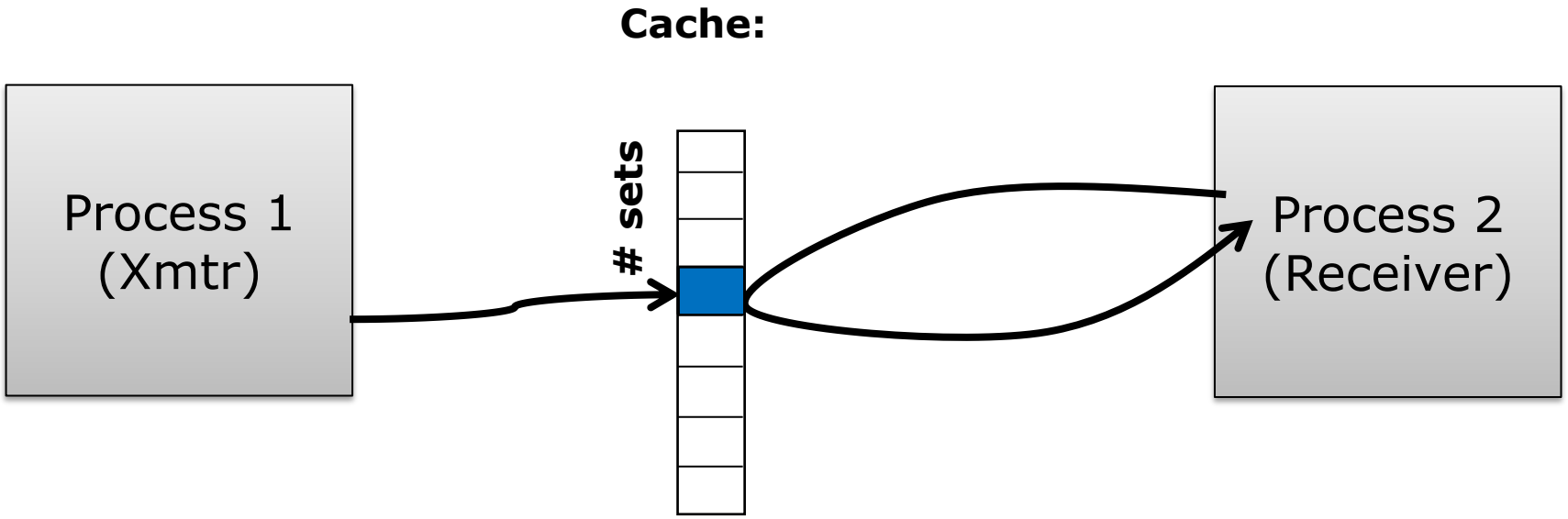

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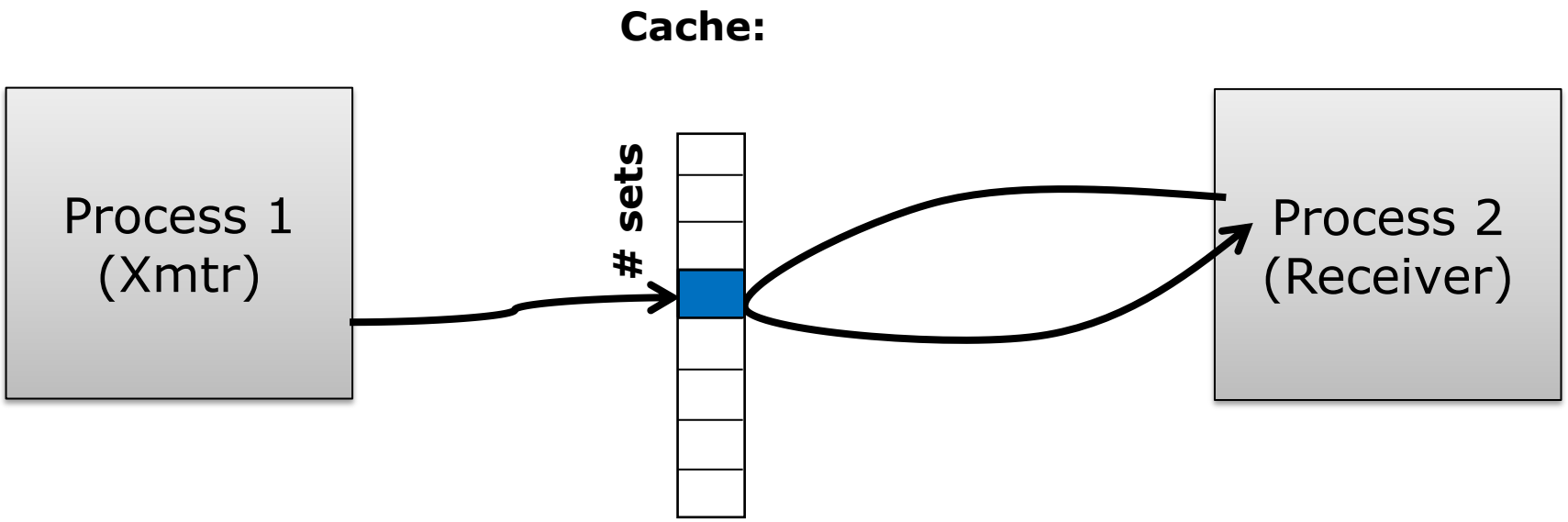

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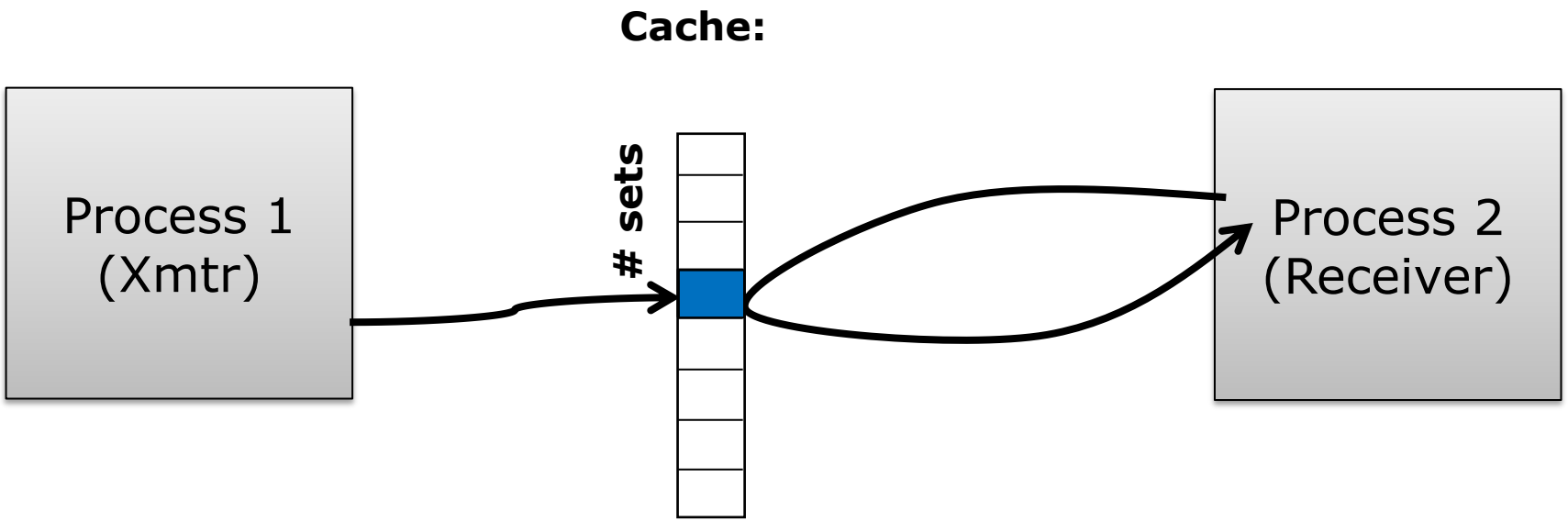

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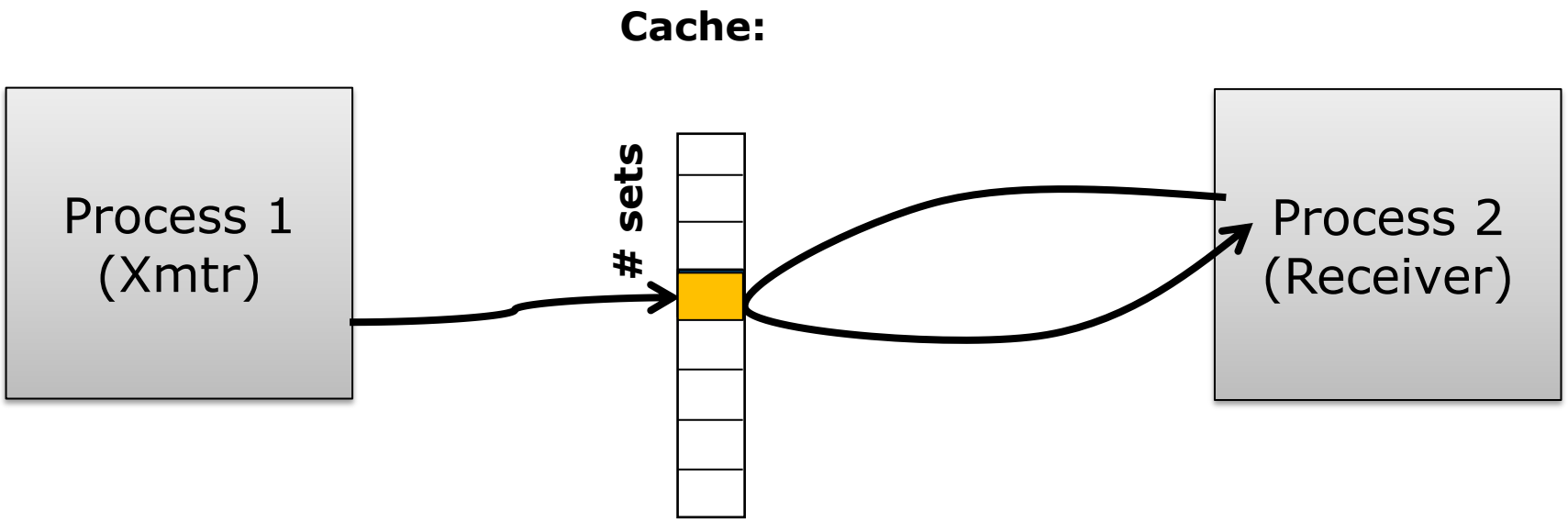

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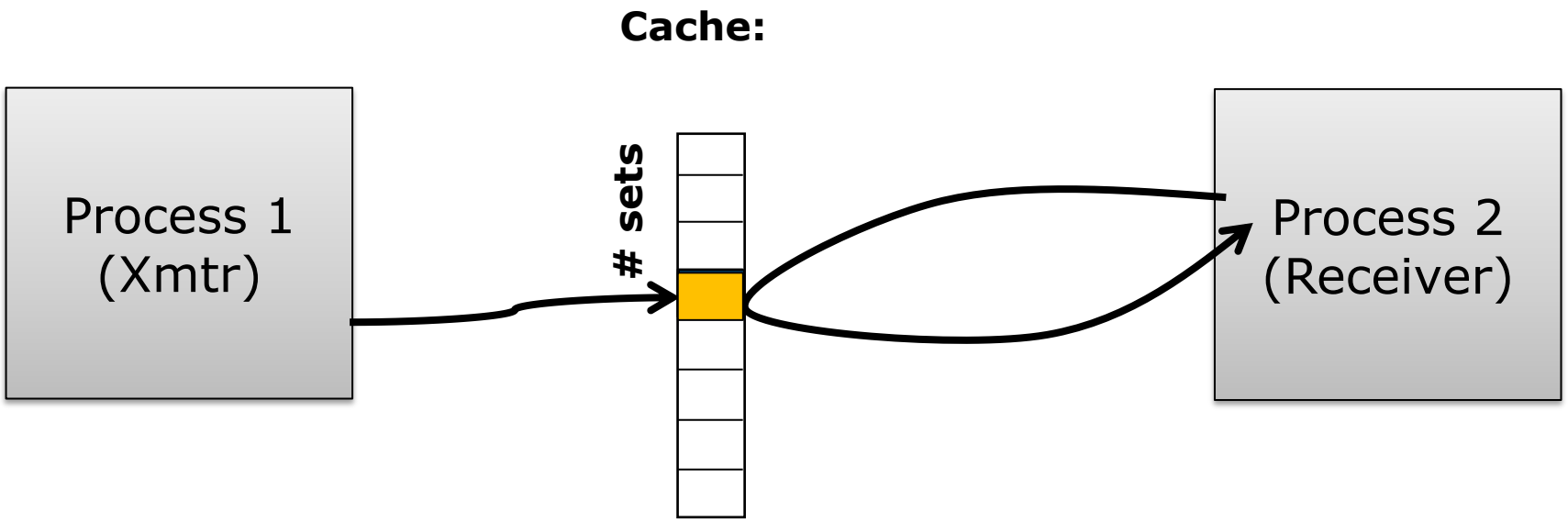

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Transmitter in RSA [Percival 2005]

- Assume square-and-multiply based exponentiation

Input : base **b**, modulo m,
exponent $\boldsymbol{e = (e_{n-1} \ldots e_0)_2}$
Output: $b^e \bmod m$
$r = 1$
for $i = n-1$ *down to* 0 do
    $r = sqrt(r)$
    $r = mod(r,m)$
    if $\boldsymbol{e_i}$ **== 1 then**
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    end
end
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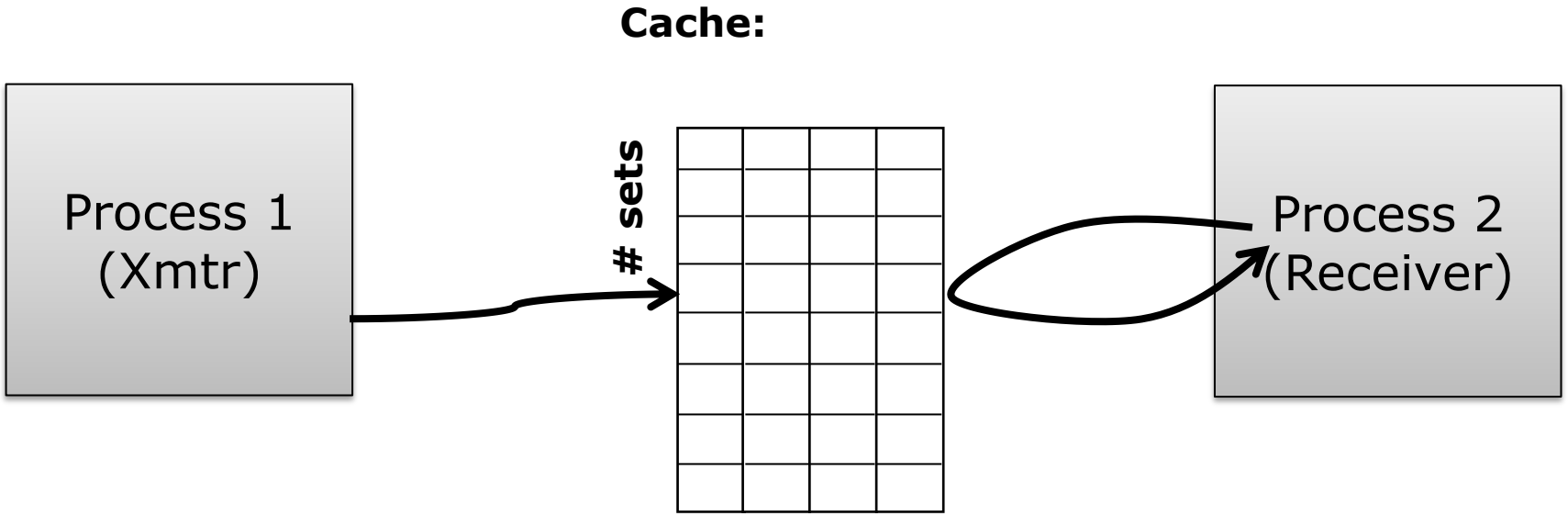
Secret-dependent memory access → transmitter

A Multi-way Cache-based Channel



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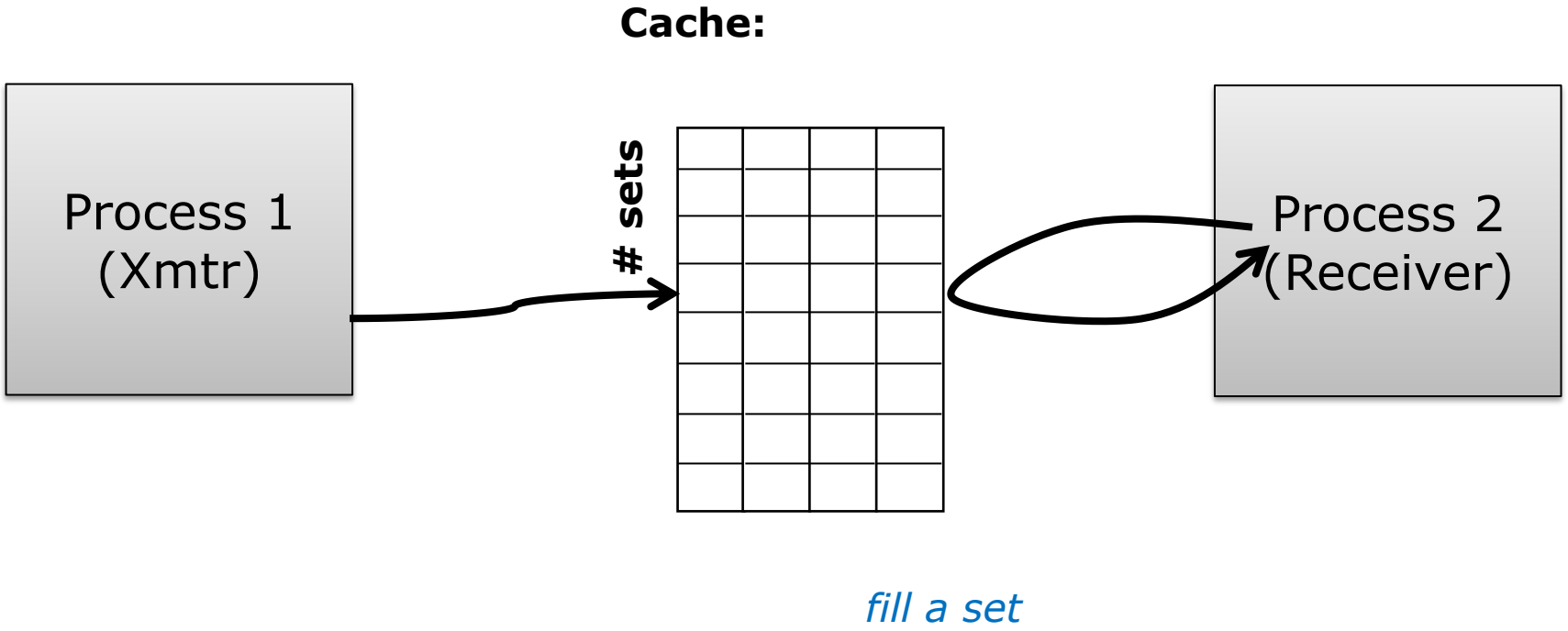

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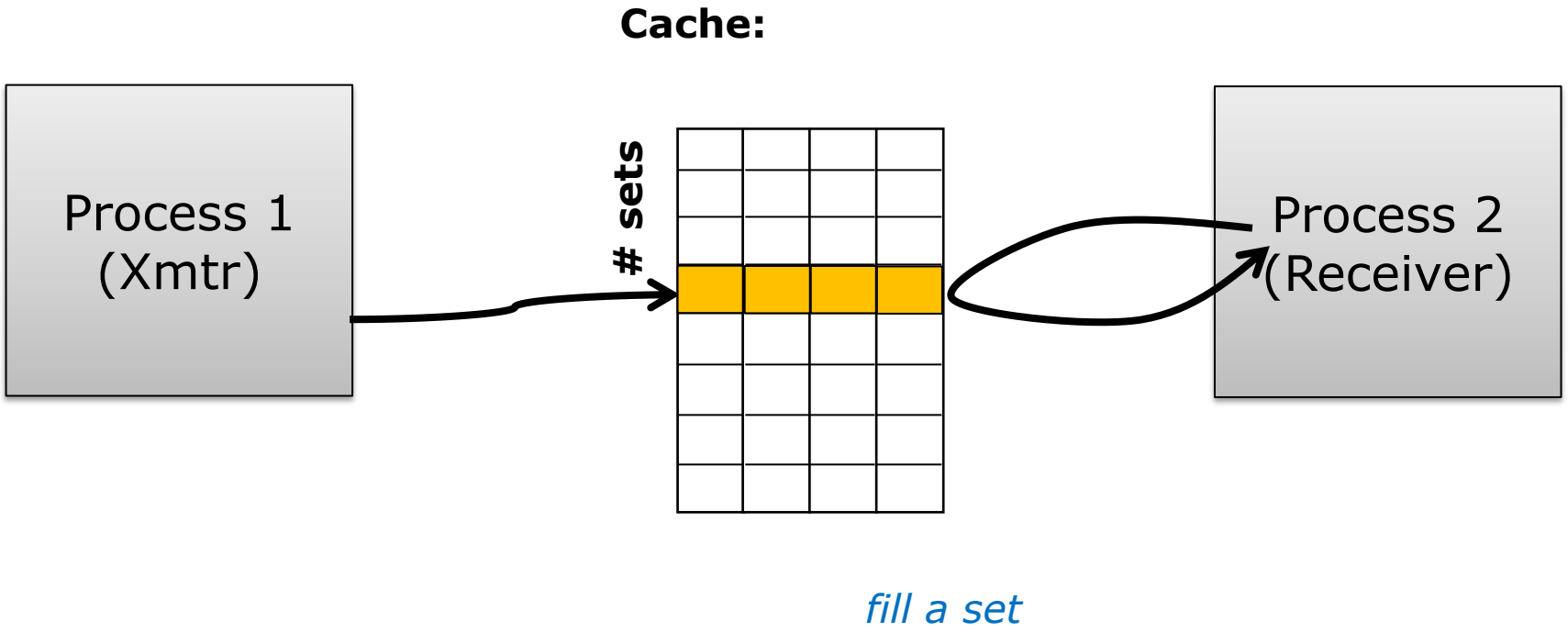

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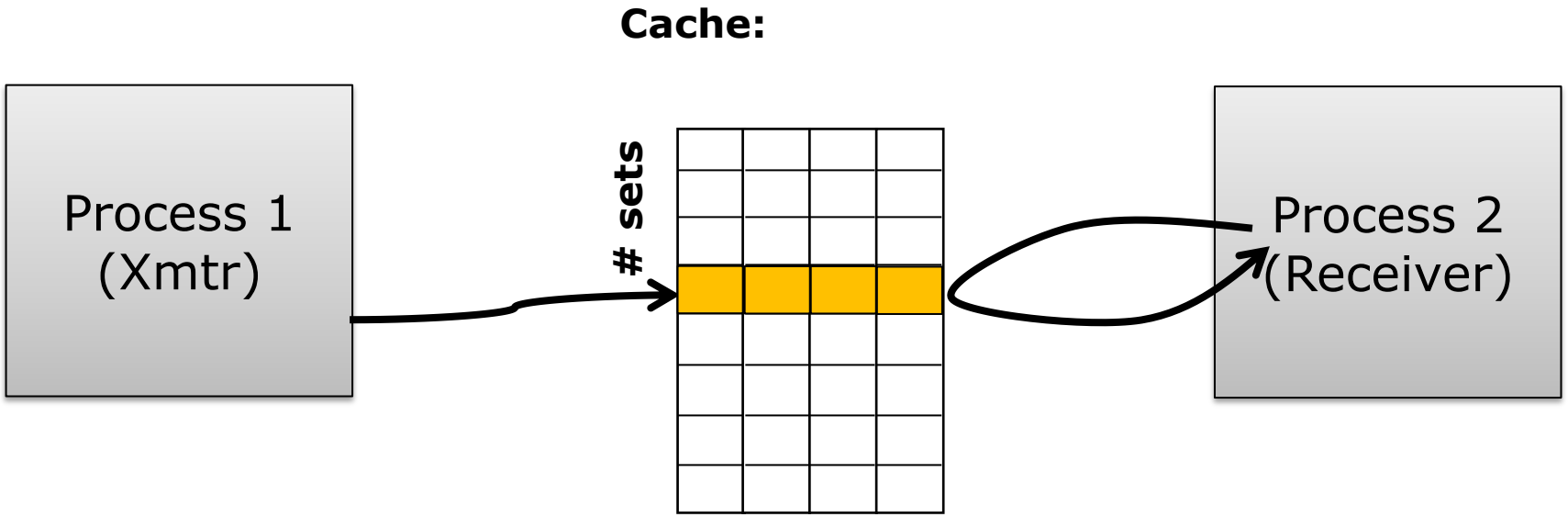

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fill a set

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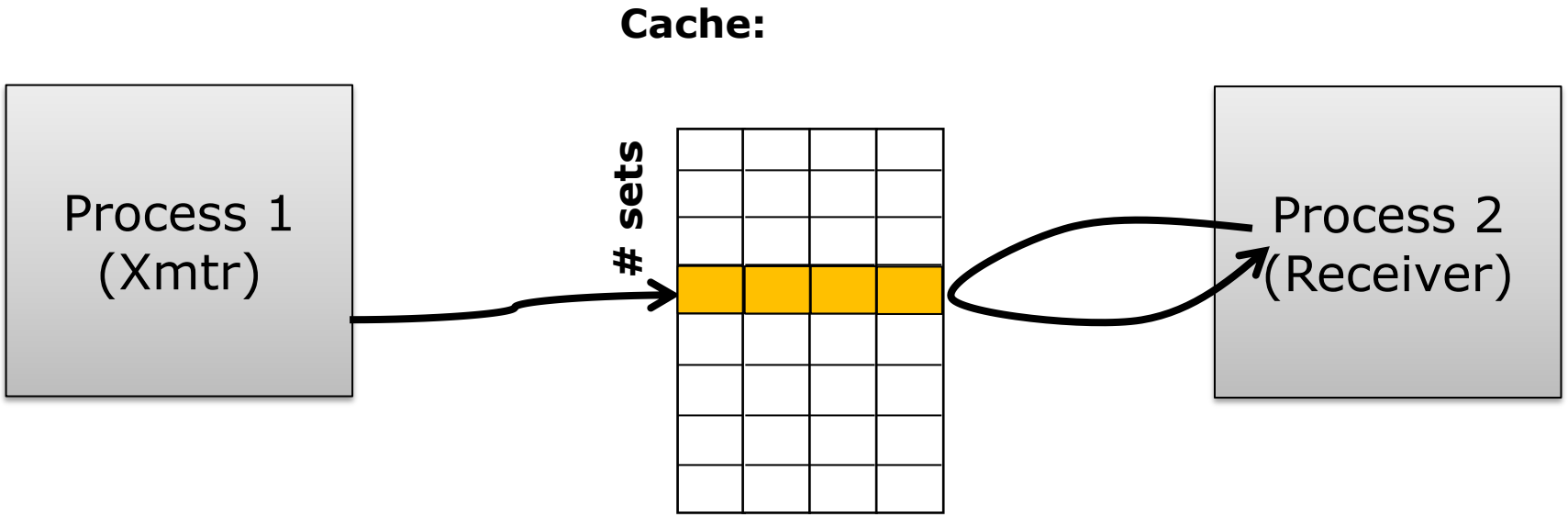

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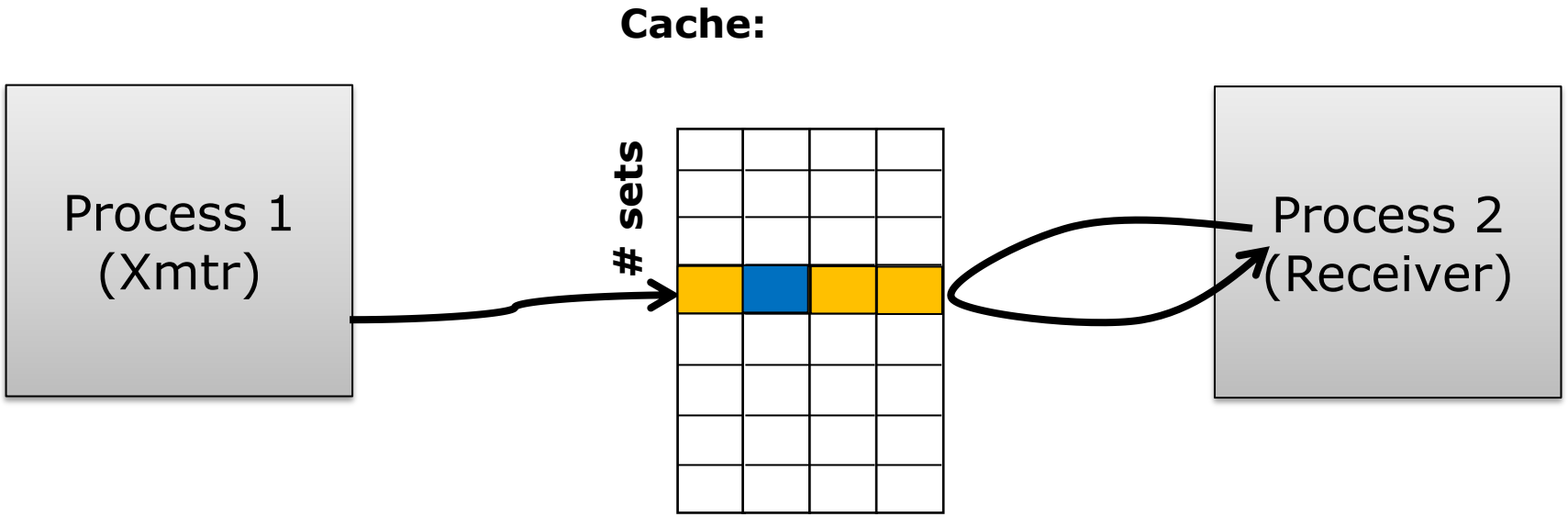

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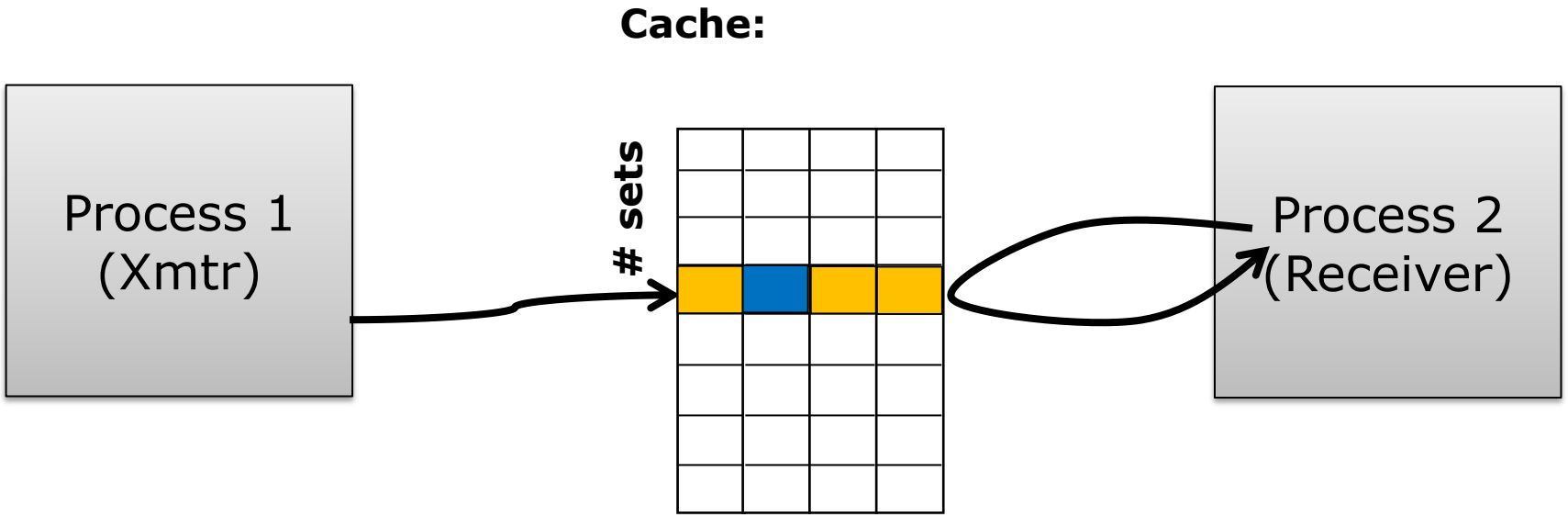

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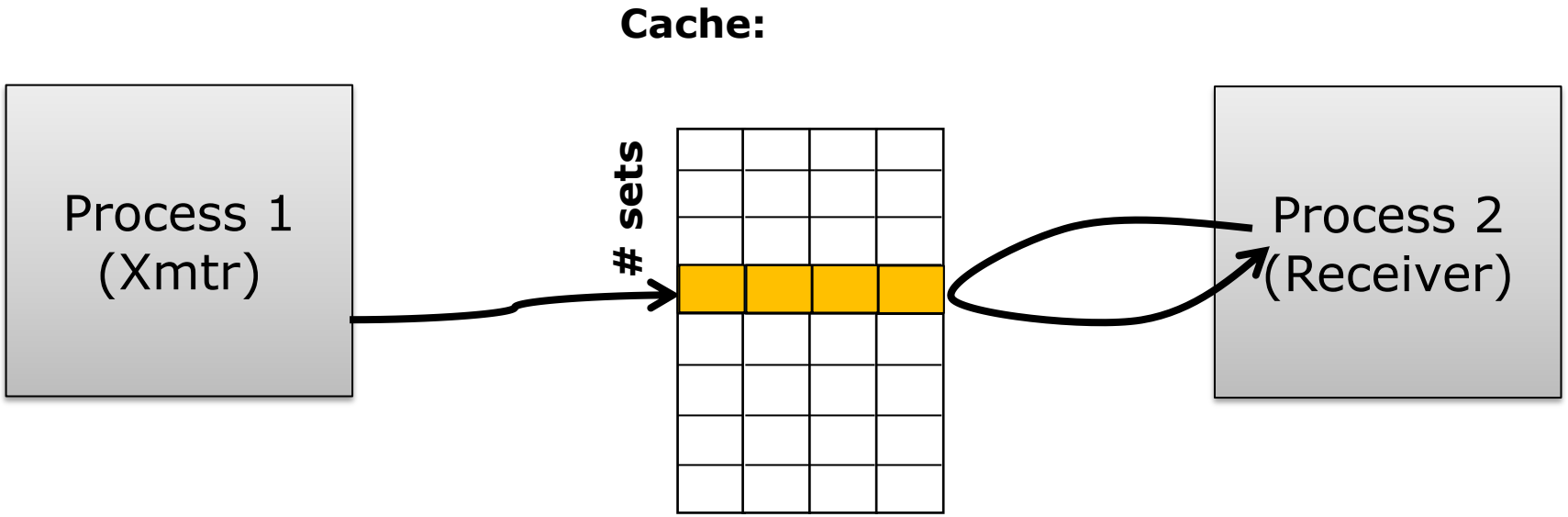

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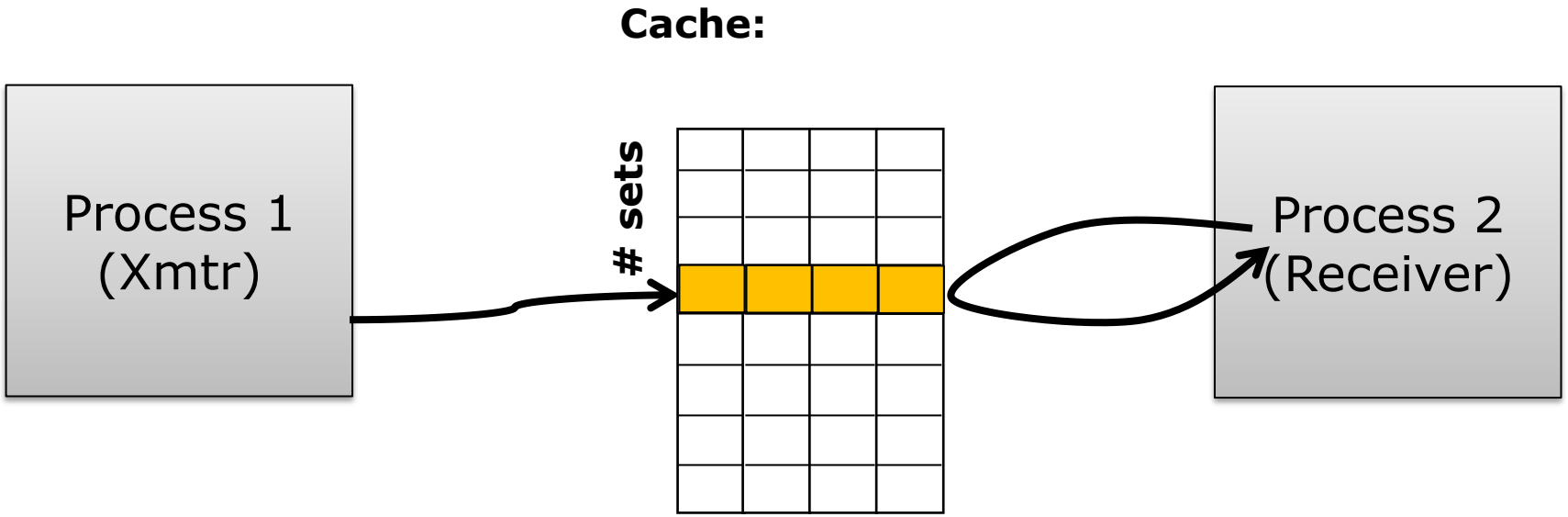

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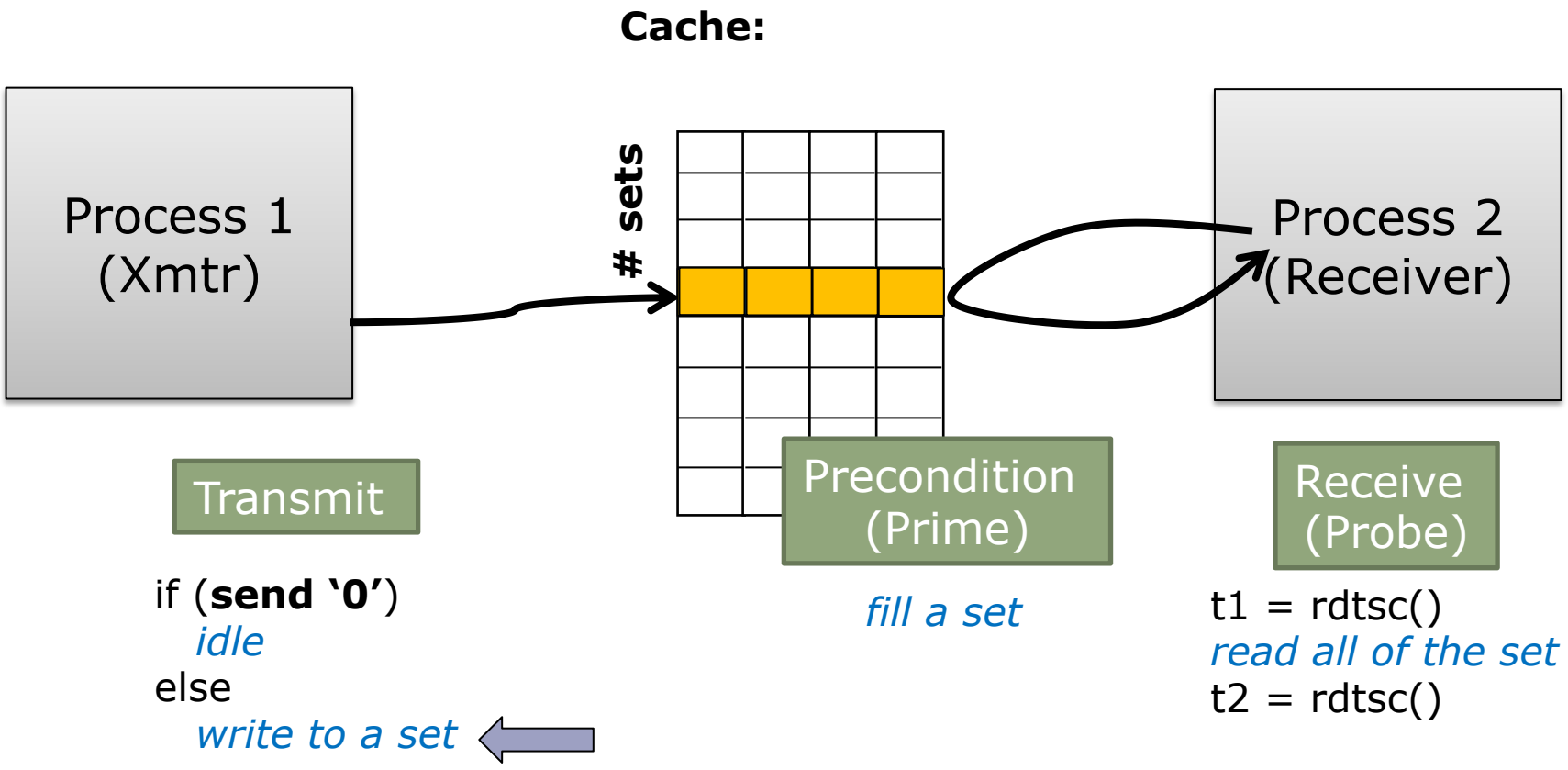
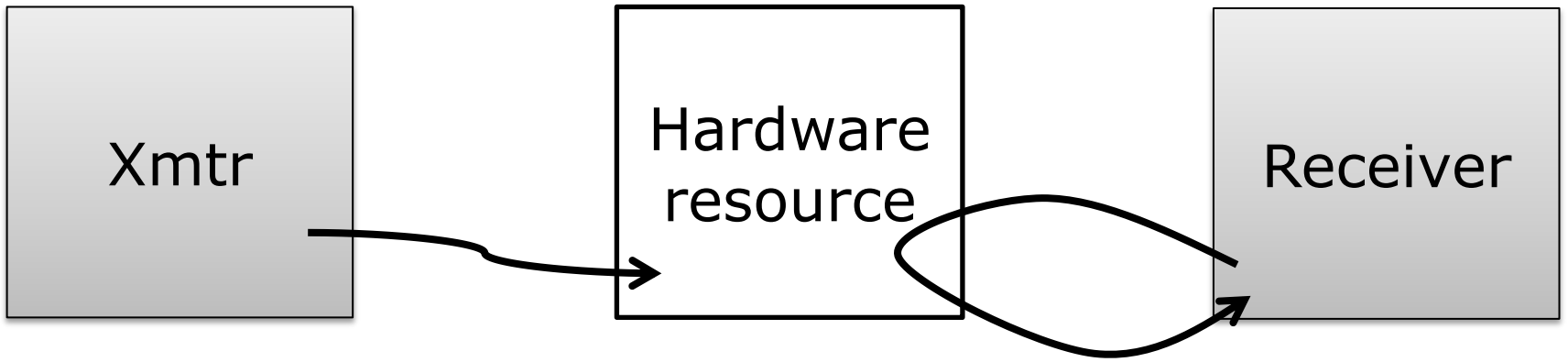


Generalizes to Other Resources




```
if (send '1')
  Use resource
else
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```

```
t1 = rdtsc()
Use resource
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```
if (t2 – t1 > THRESH)
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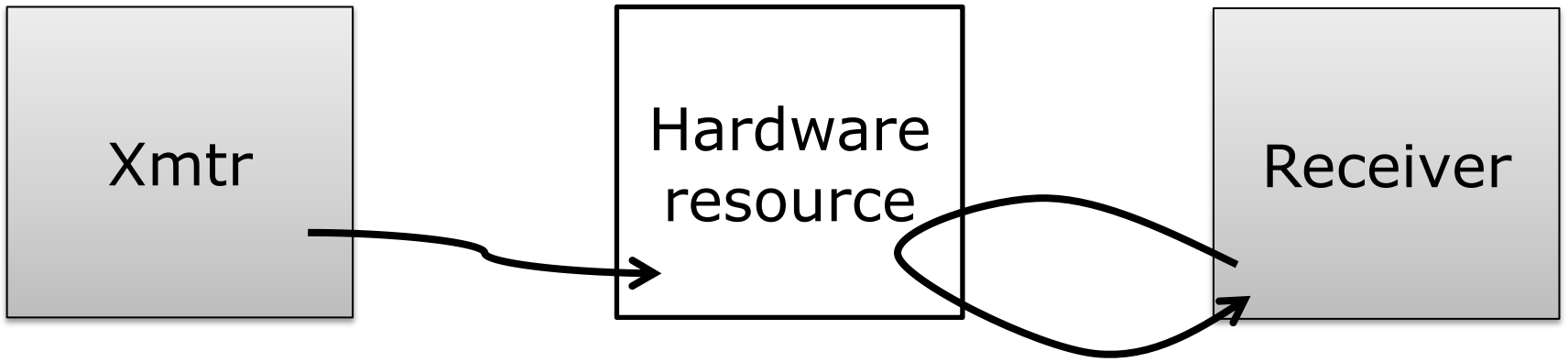


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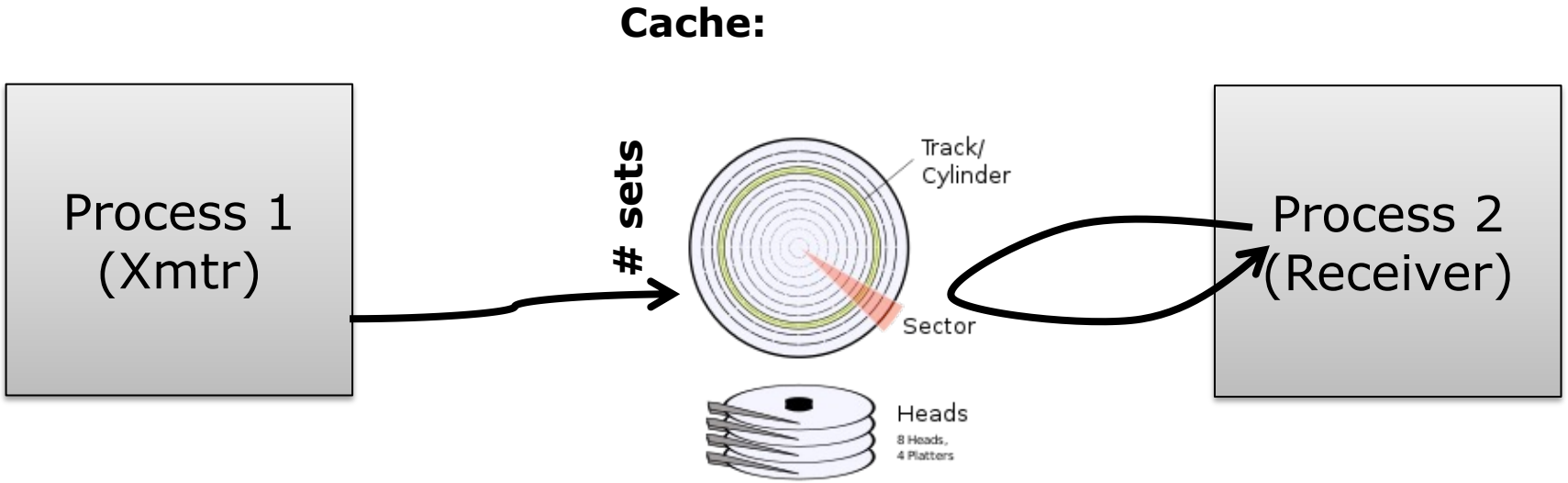
```

Any other exploitable structures?

Channel Examples

Resource	Shared by
Private cache (L1, L2)	Intra-core
Shared cache (LLC)	On-socket cross core
Cache directory	Cross socket
DRAM row buffer	Cross socket
TLB (private/shared)	Intra-core/Inter-core
Branch Predictor	Intra-core
Network-on-chip	On-socket cross core
…	…

Disrupting Communication



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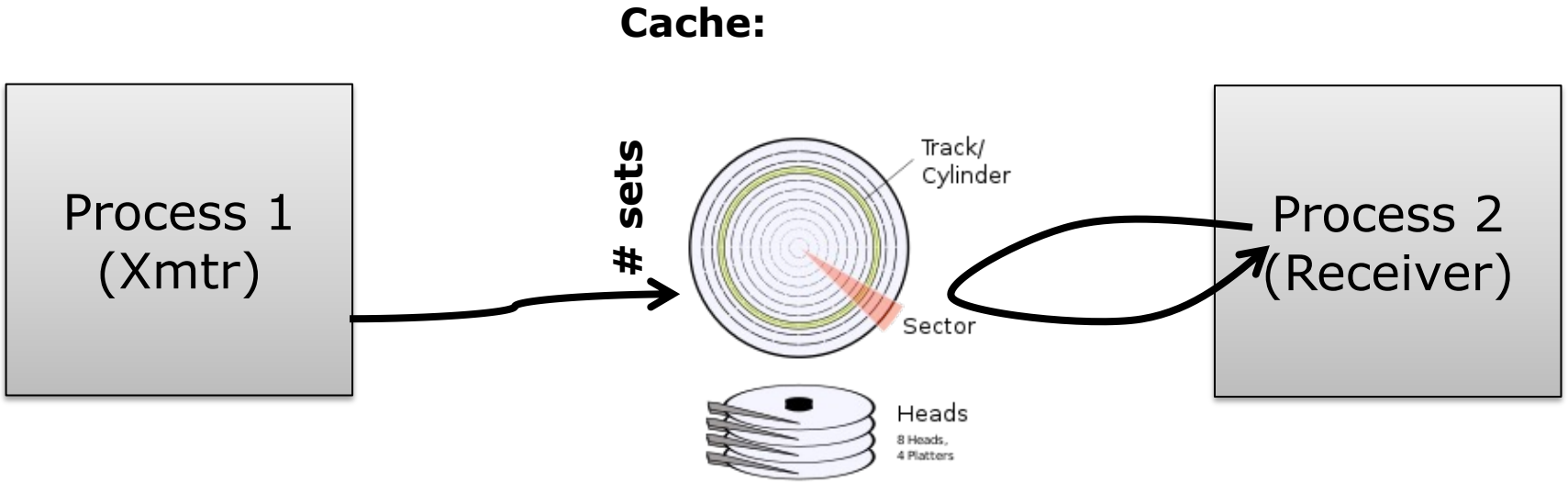
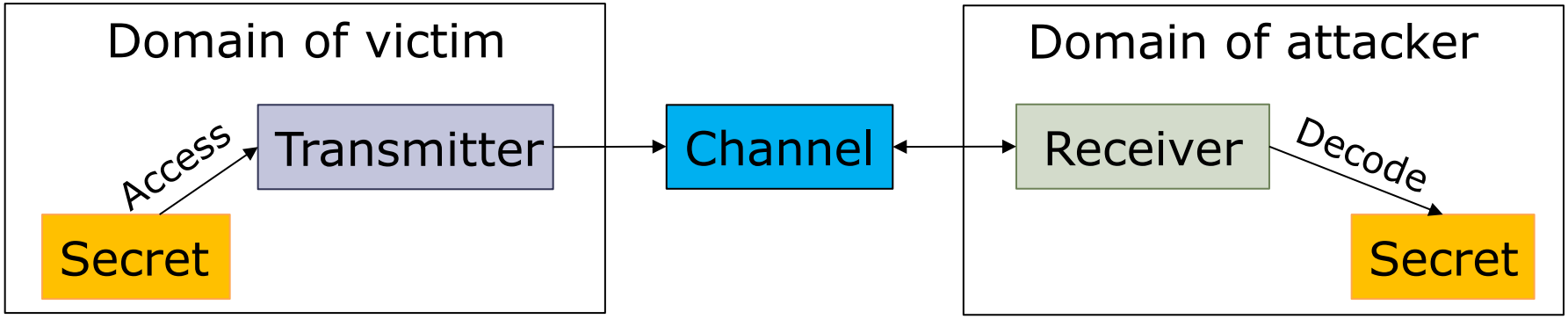


"We found that identifying all of the sources of accurate clocks was much **easier** than finding all of the possible timing channels in the system.
… If we could make the clocks less accurate, then the effective bandwidth of all timing channels in the system would be **lowered**." *(1991)*

Secret-independent Channel Modulation



- Different from conventional communication, this is a side channel (*unintended* communication).

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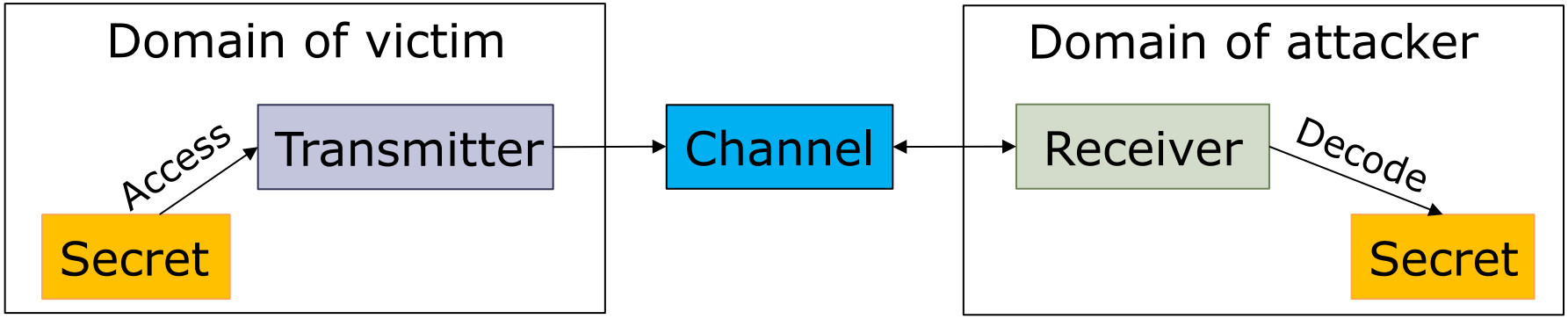

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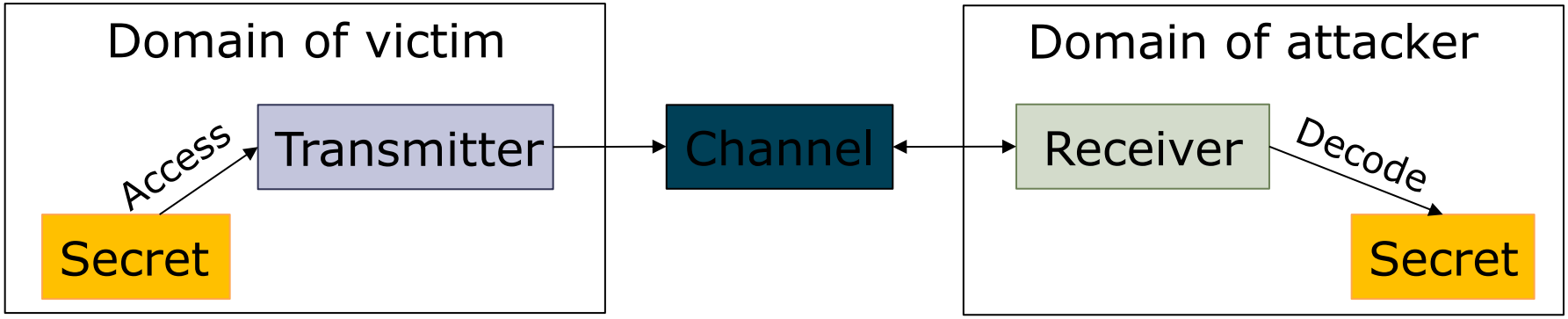

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-> ”data-oblivious execution” or “constant-time programming”.

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Input : base **b**, modulo *m*,
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Output: $b^e \bmod m$

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How to make the code execution independent of the secret?

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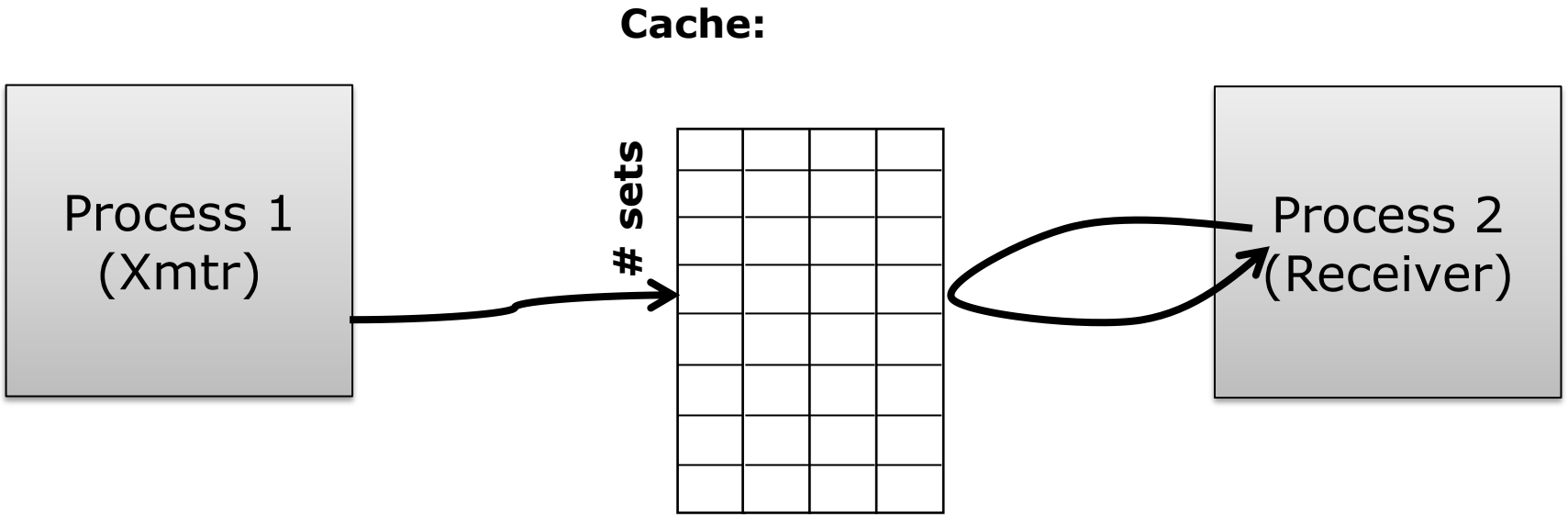
Constant-time programming is hard

Disrupting Communication



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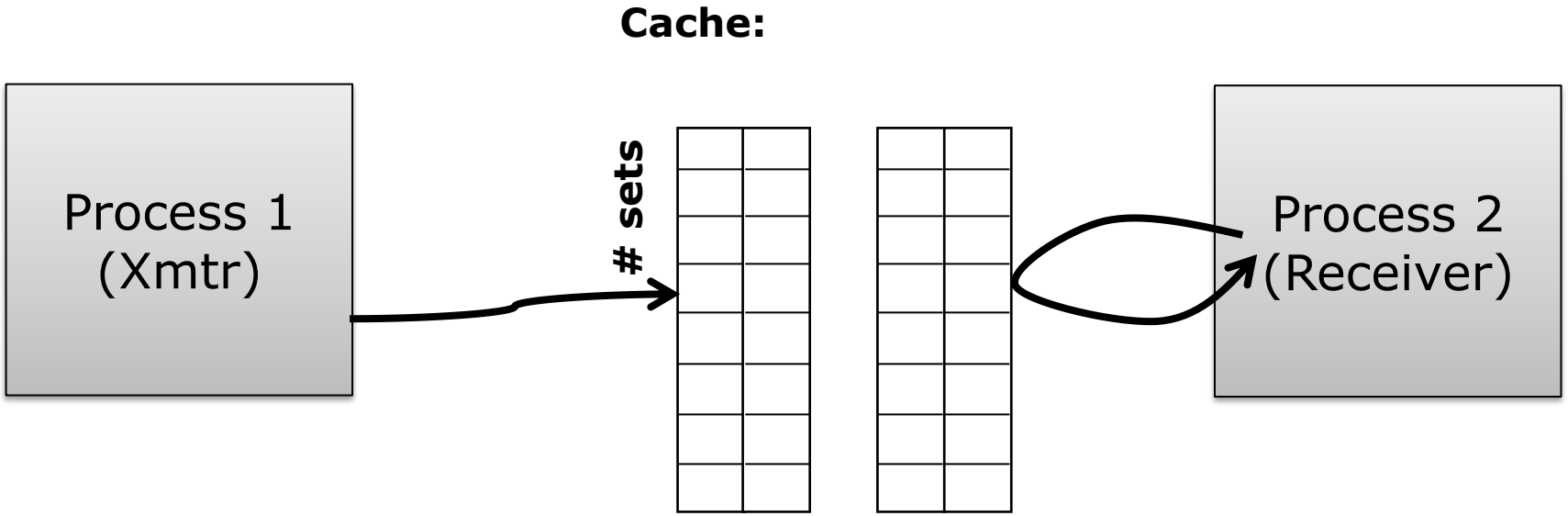

Kirianski et. al. Dawg, Micro'18

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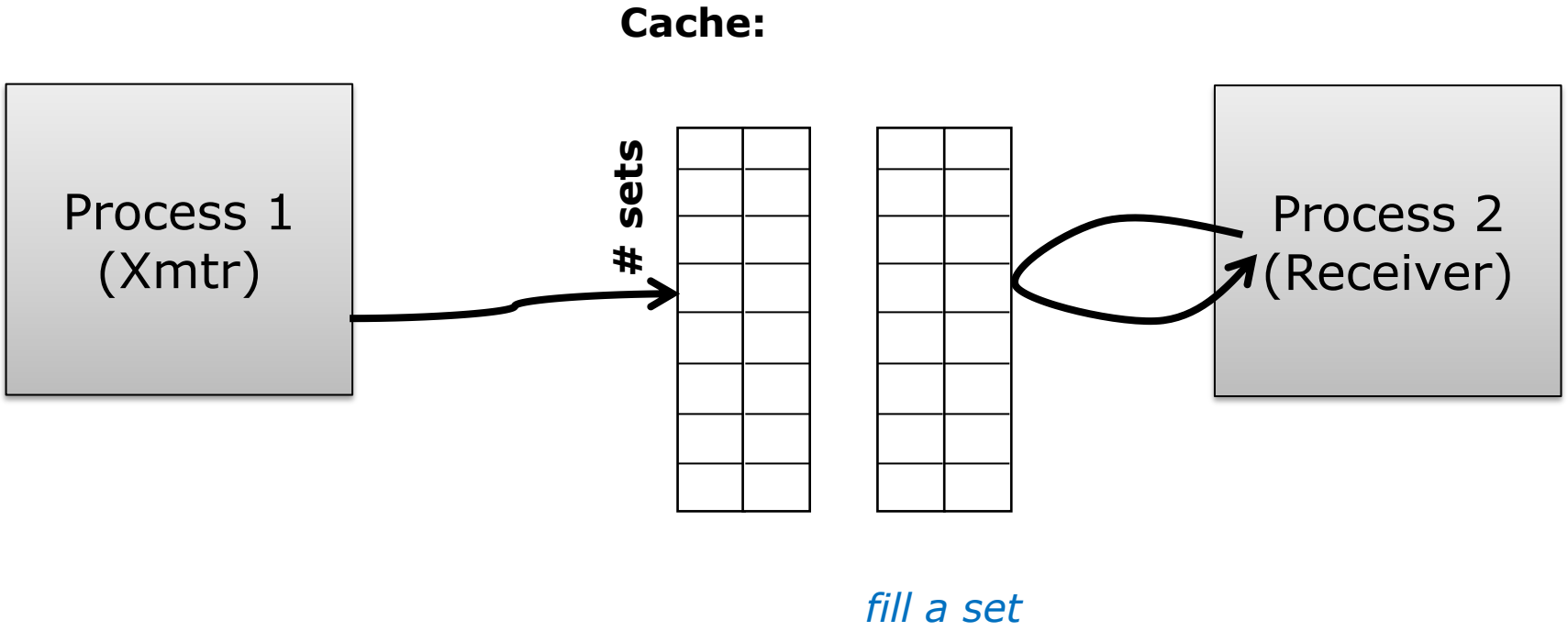

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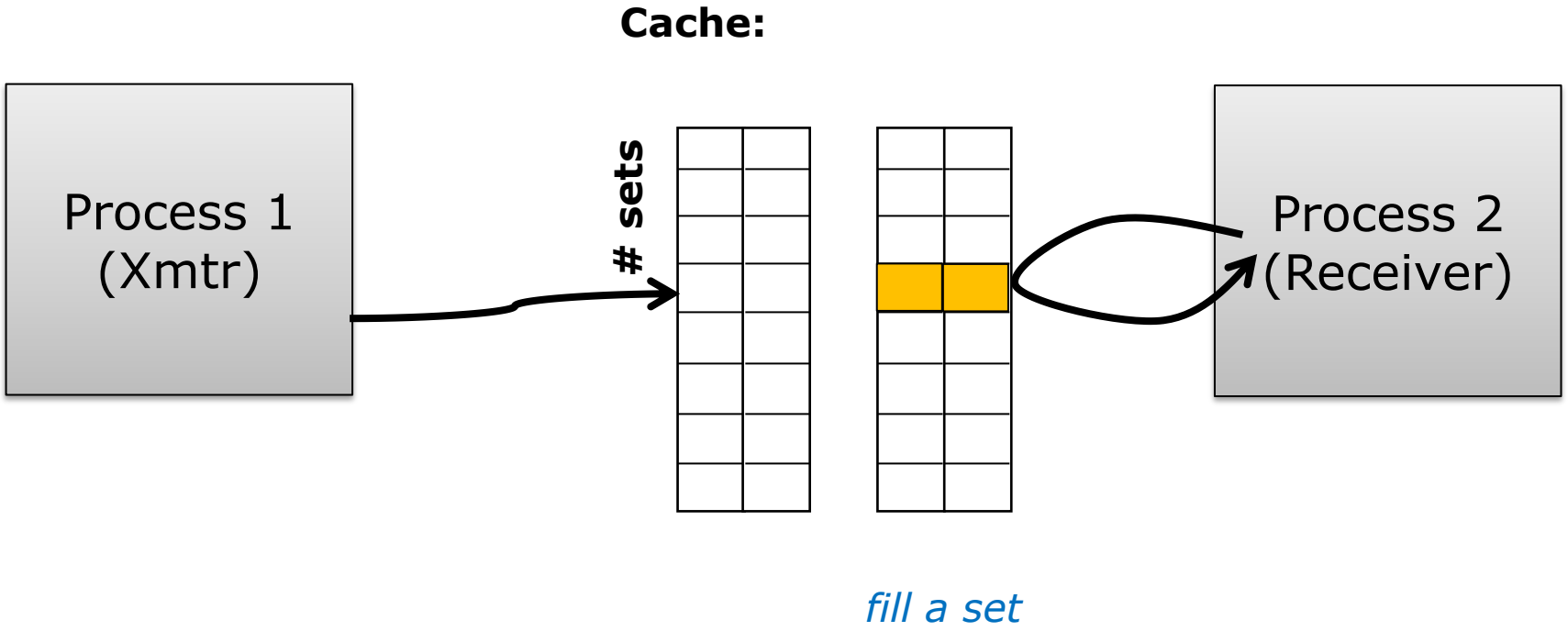

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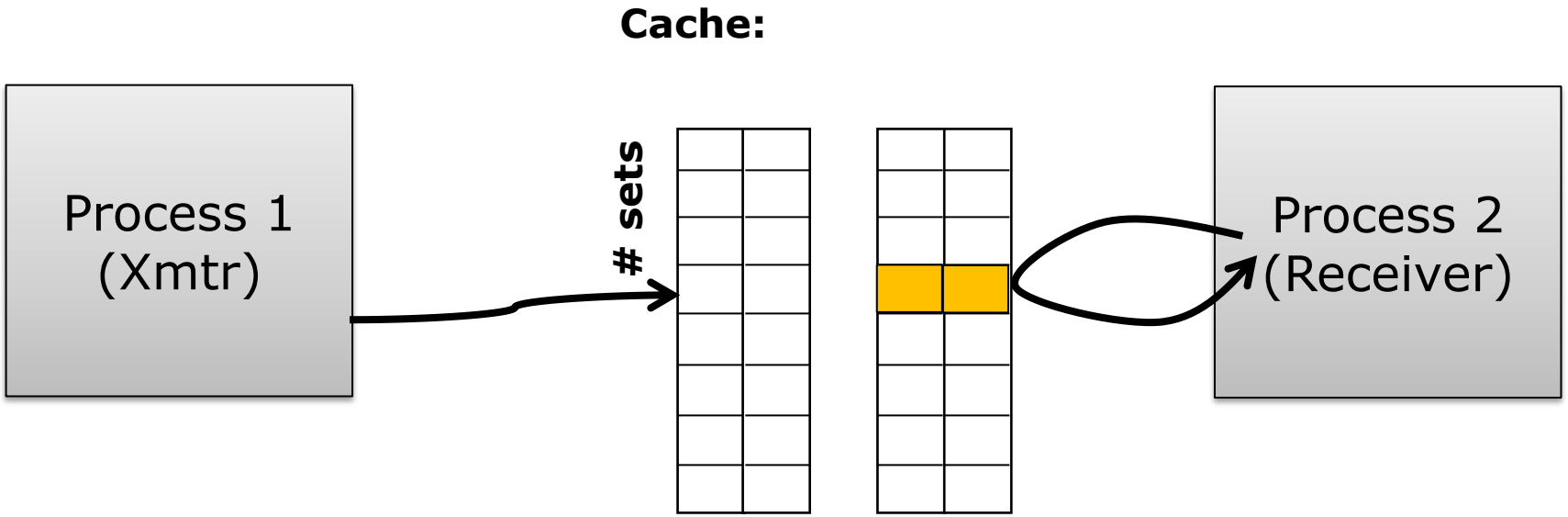

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Kirianski et. al. Dawg, Micro'18

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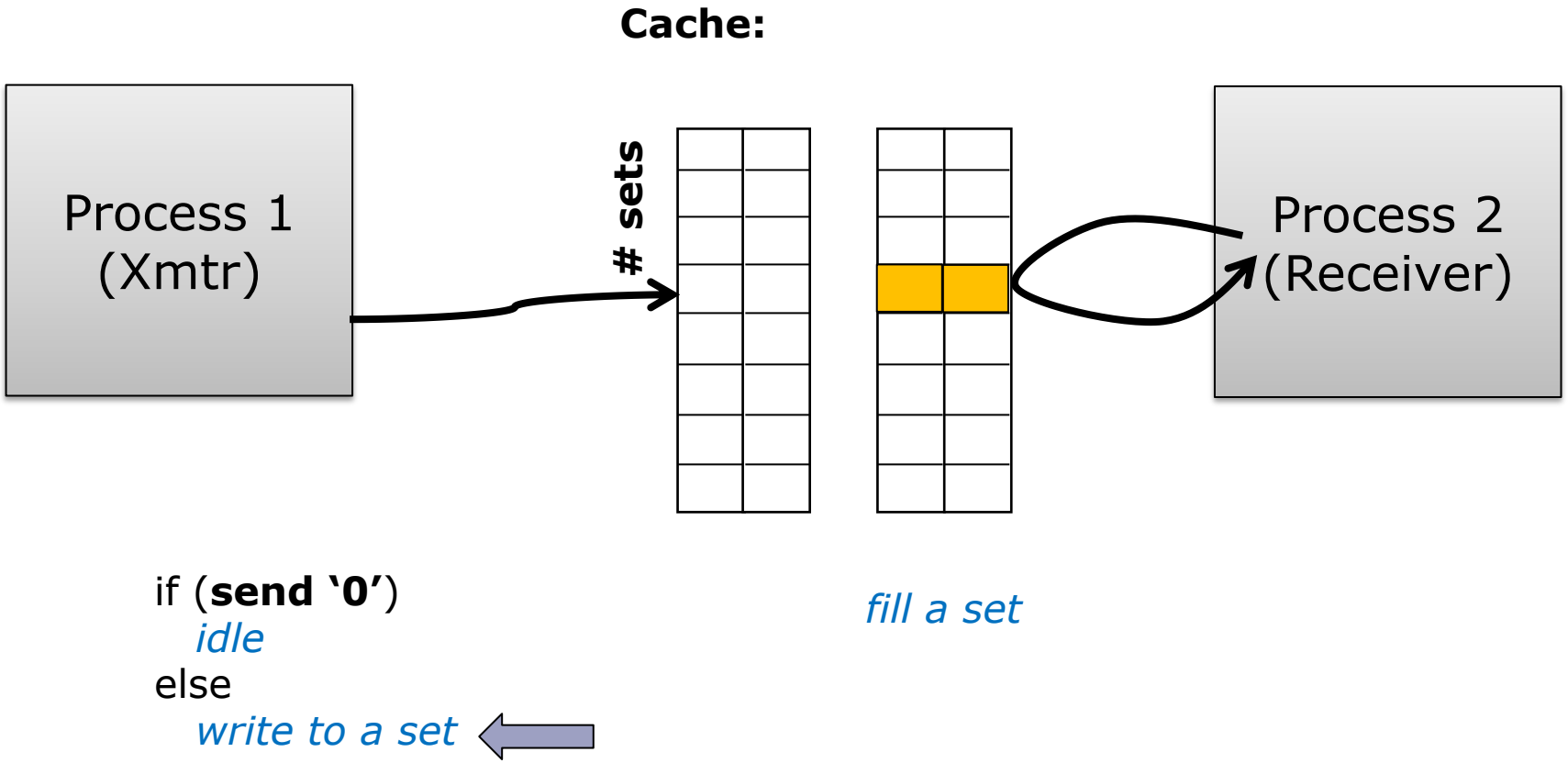

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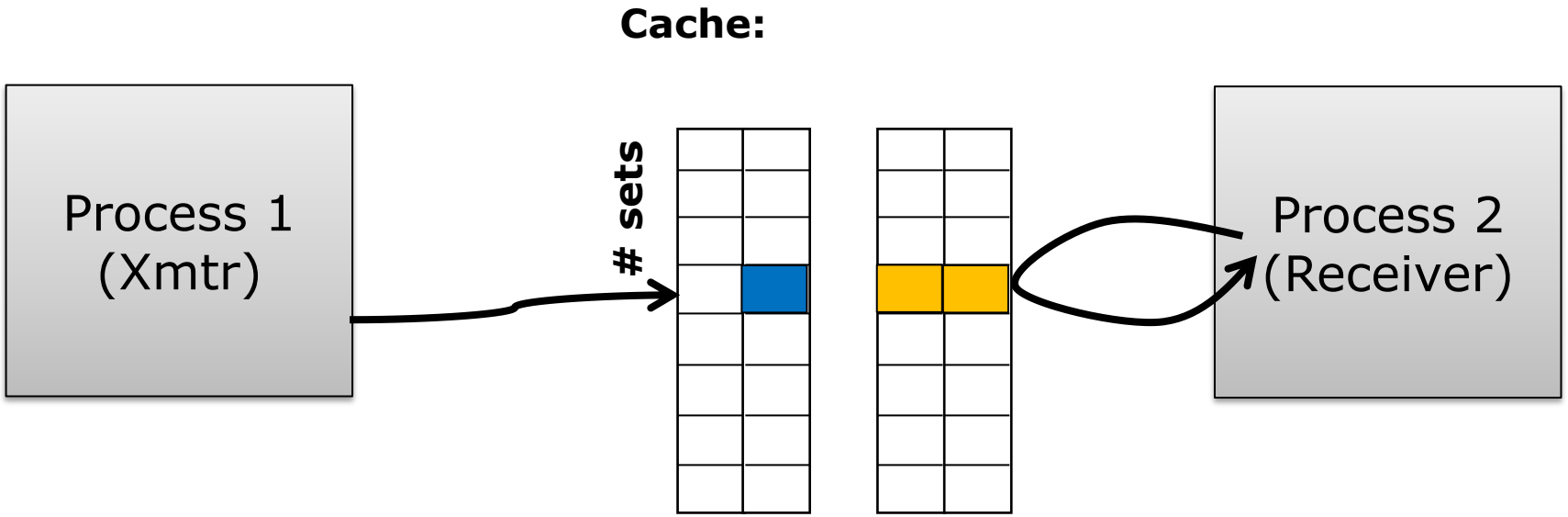

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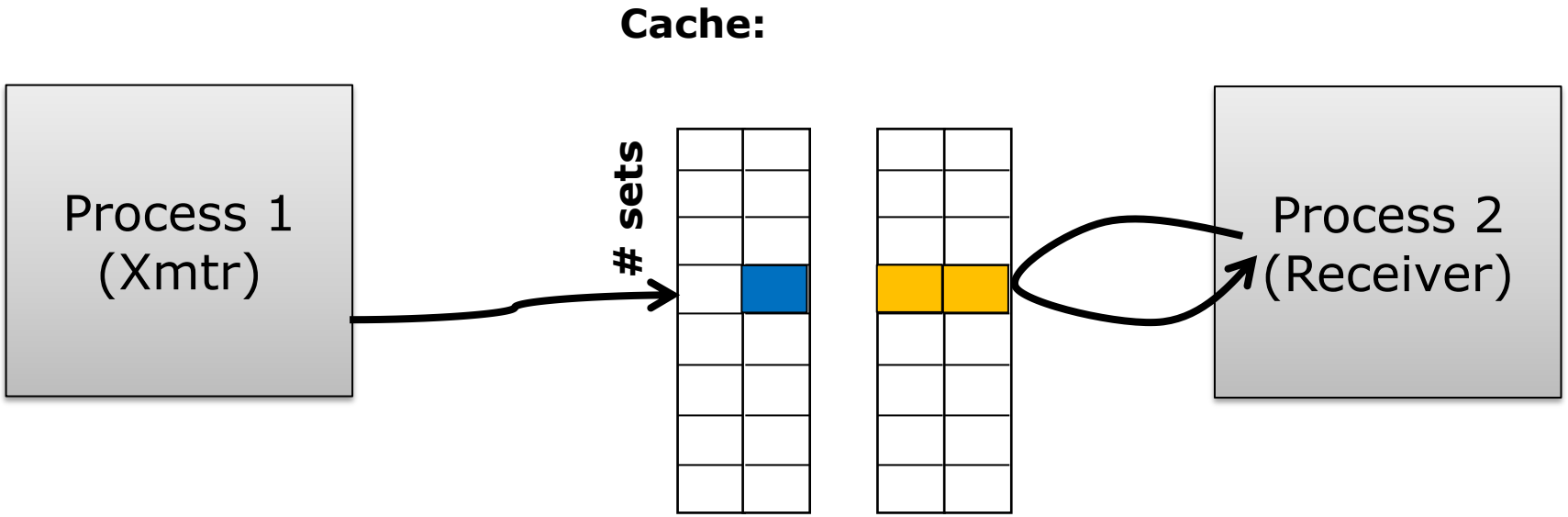

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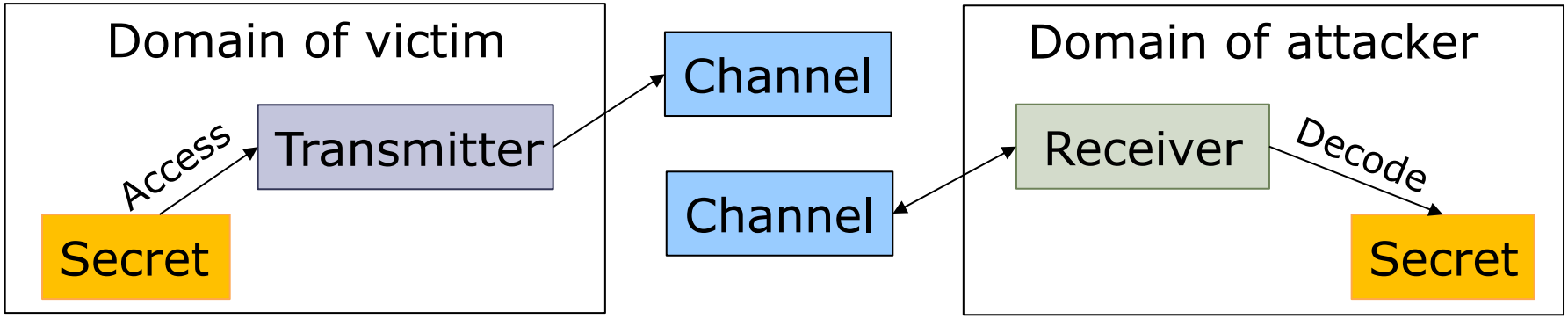
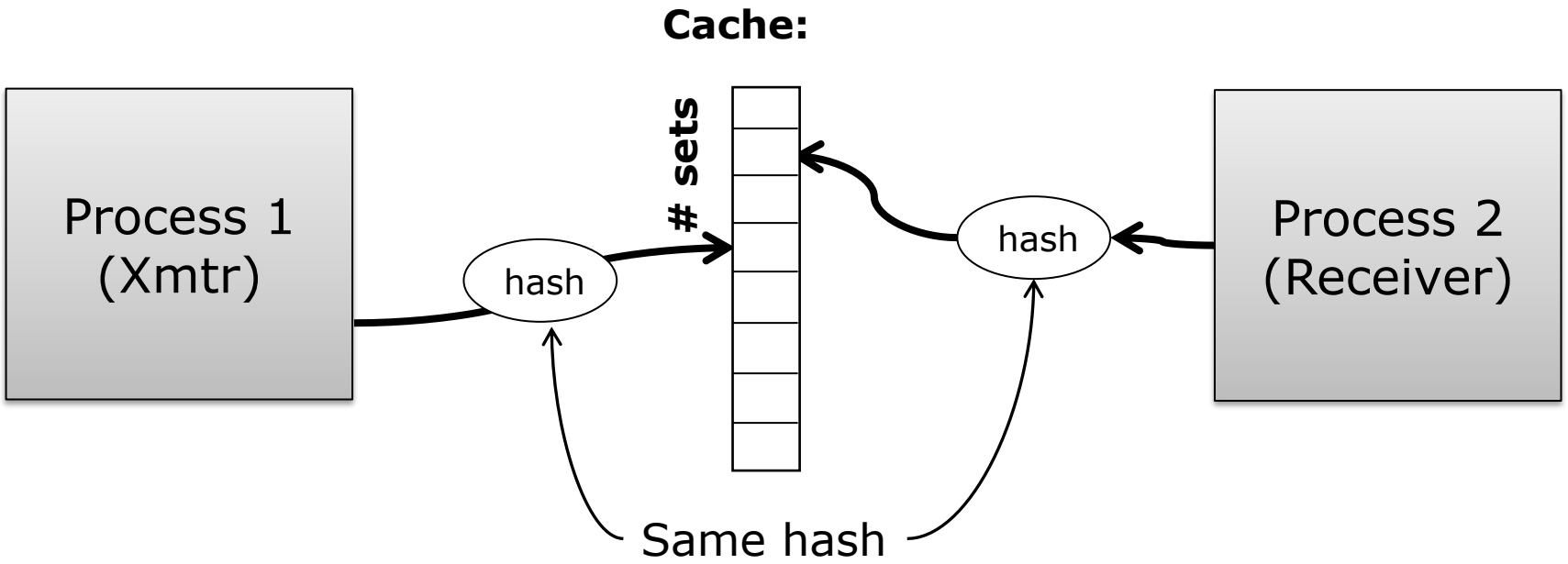
Kirianski et. al. Dawg, Micro'18

Disjoint Channels



- Making disjoint channels makes communication impossible.
- Channel can be allocated by "domain" and will need to be "cleaned" as processes enter and leave running state, so next process cannot see any "modulation" on the channel.

Obfuscating the channel (1)



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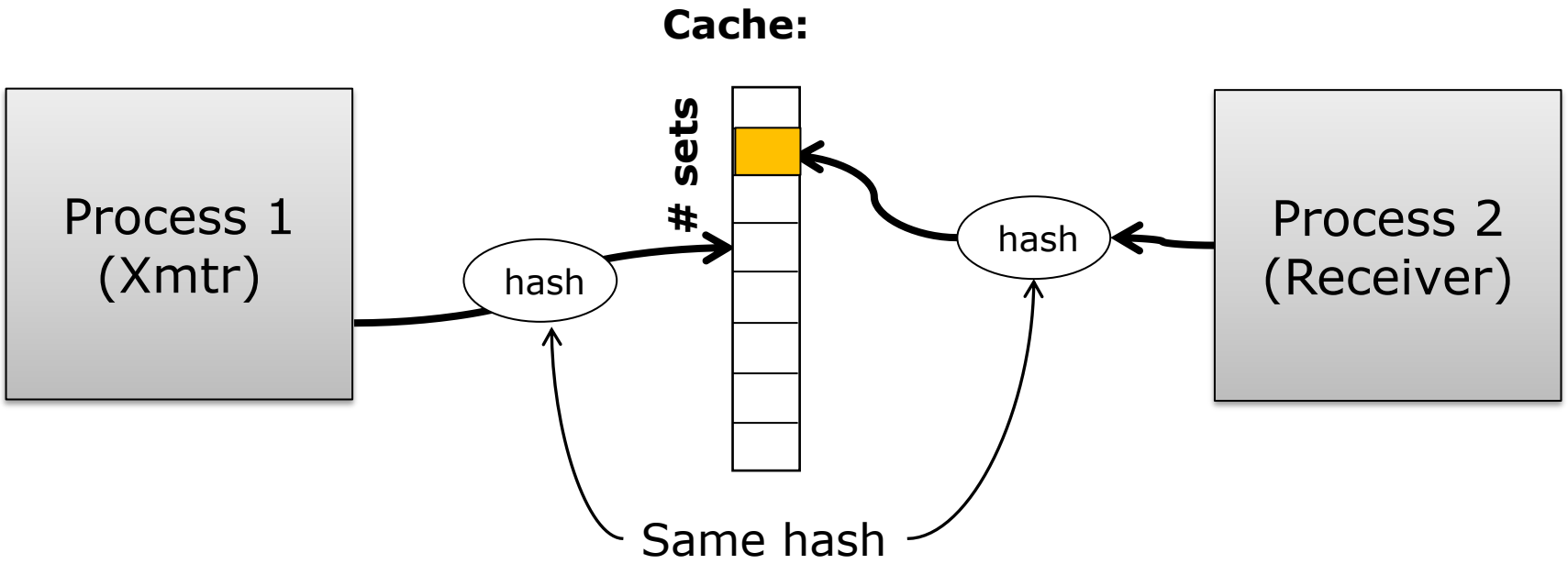

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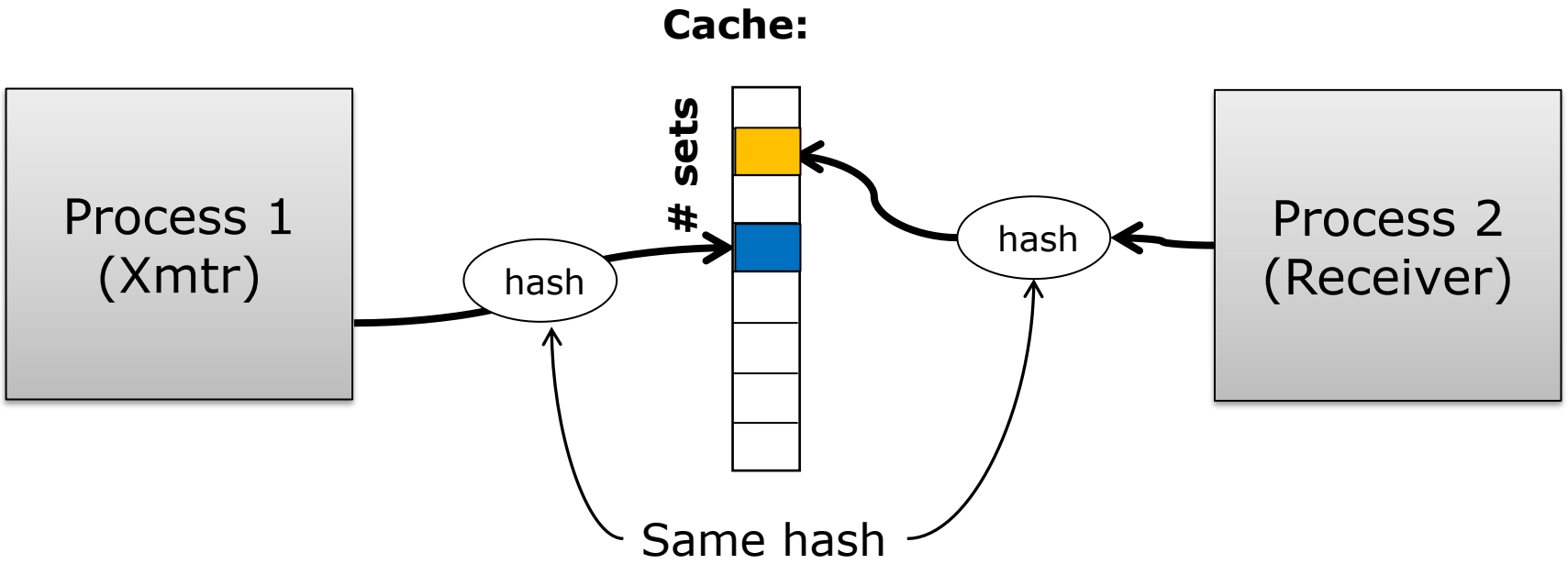

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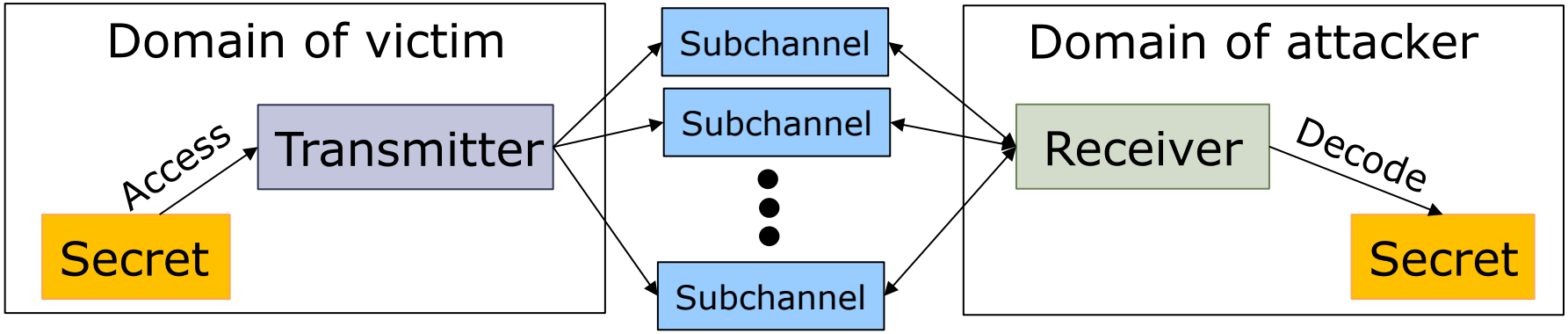

- Transmissions may now occur on one of many subchannels

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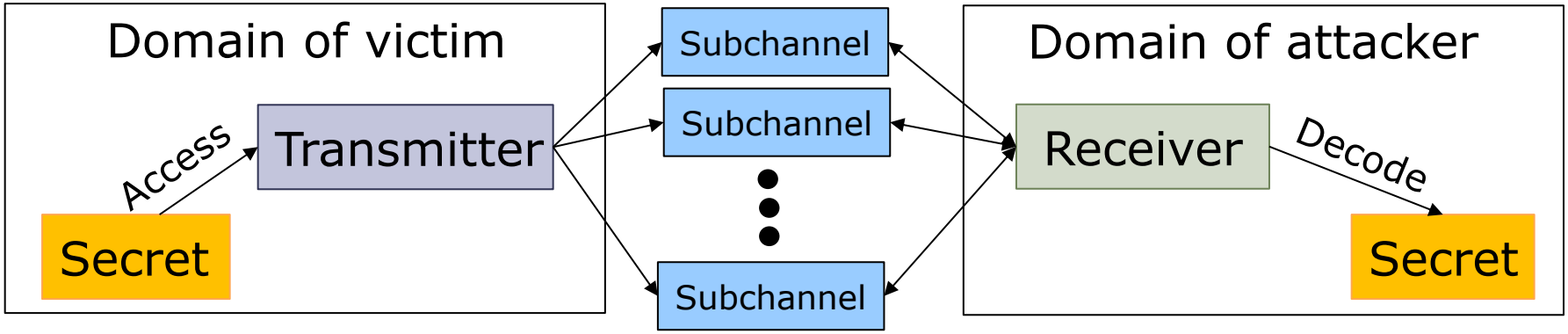

- Transmissions may now occur on one of many subchannels
- With a single hash, analysis by the receiver can, however, figure out (reverse engineer) which subchannel will be modulated.

Simple Transmitter

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secret = oneof(0..1)
if secret == 1:
    x = channel
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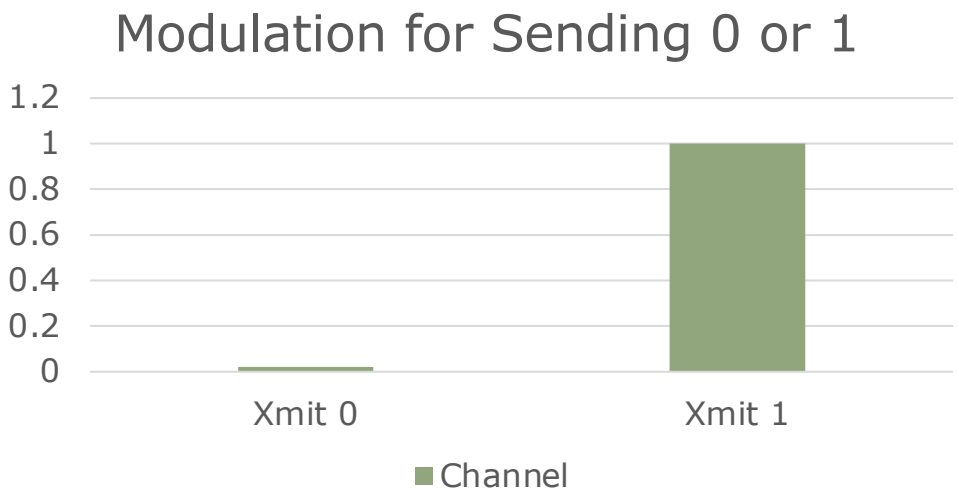

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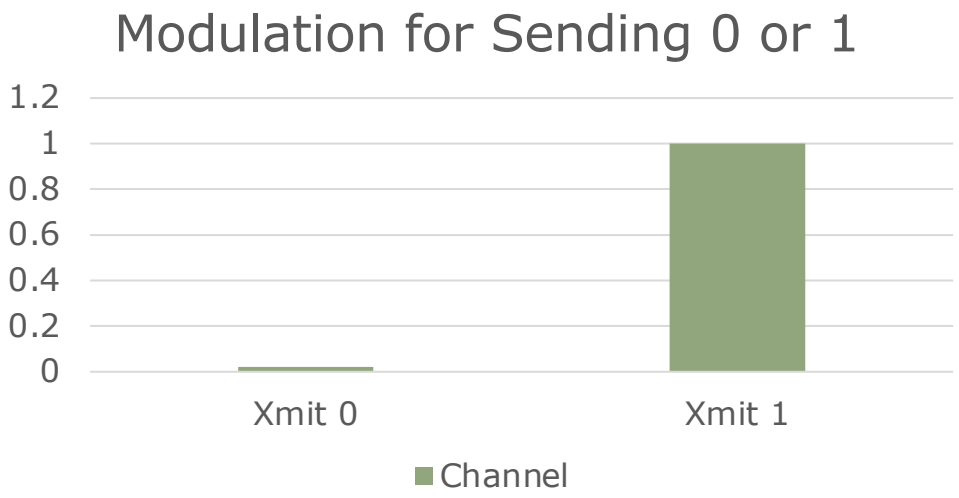

Like an amplitude modulated (AM) radio transmission (RSA example)

Another Transmitter

secret* = *oneof(0..3)

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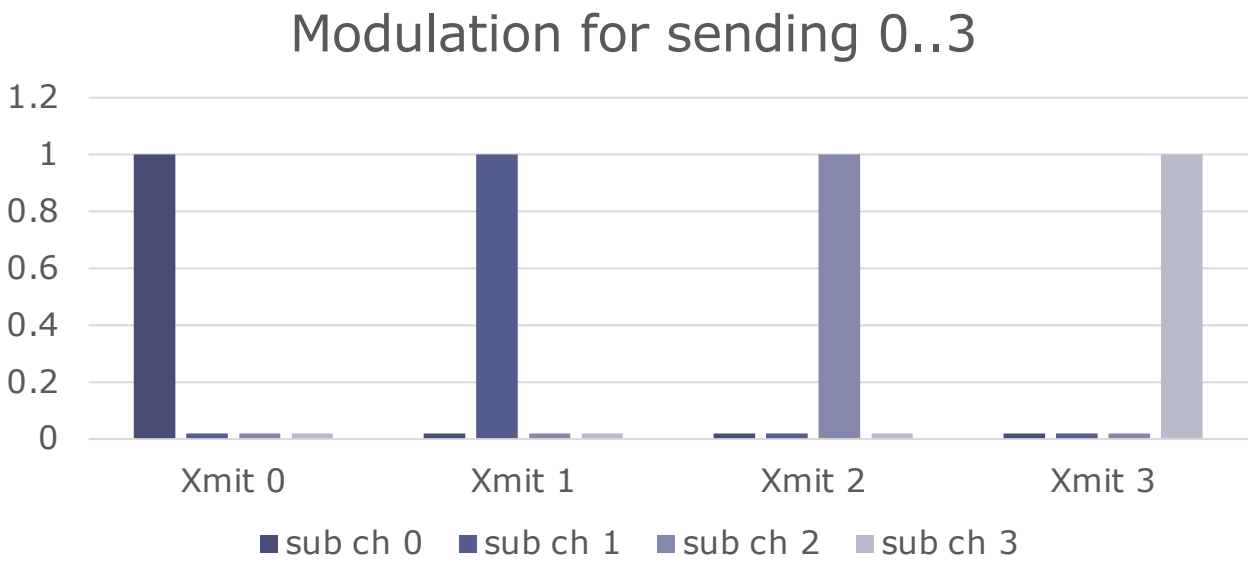

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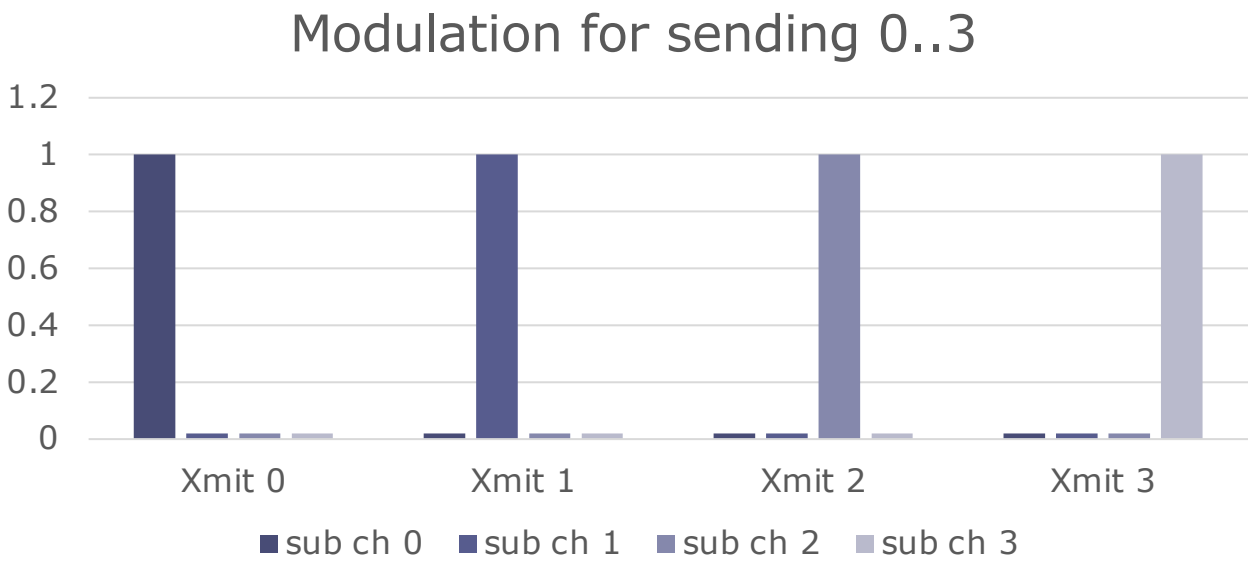
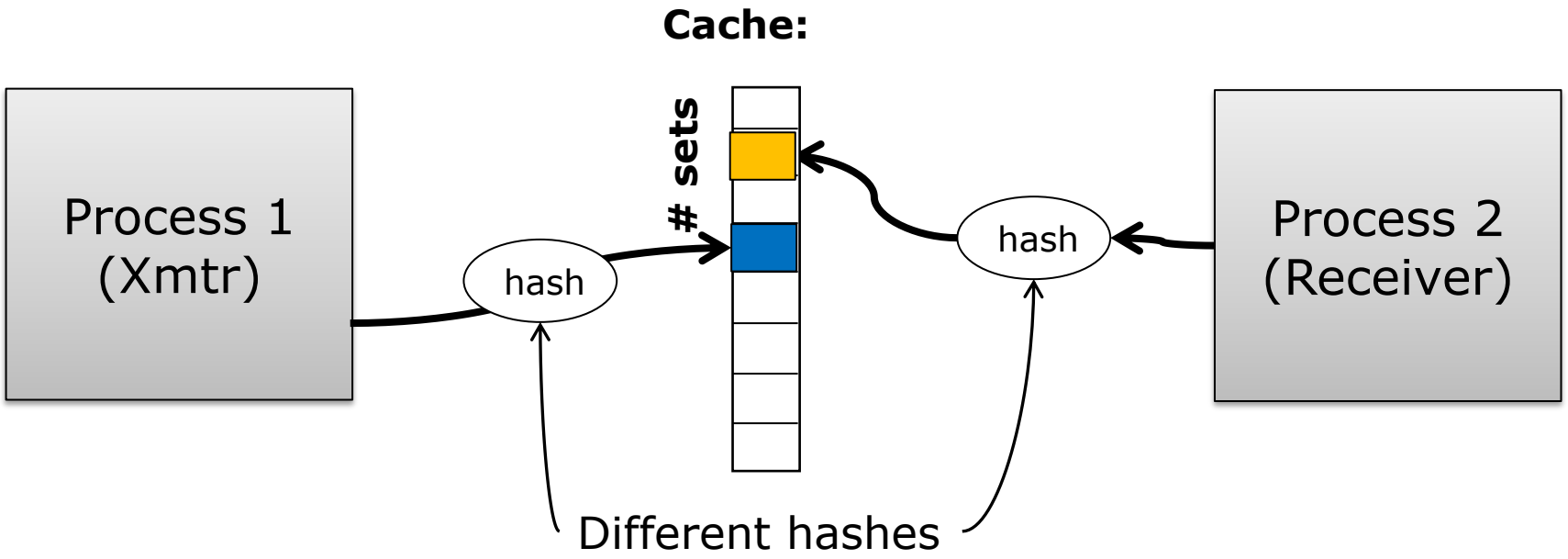


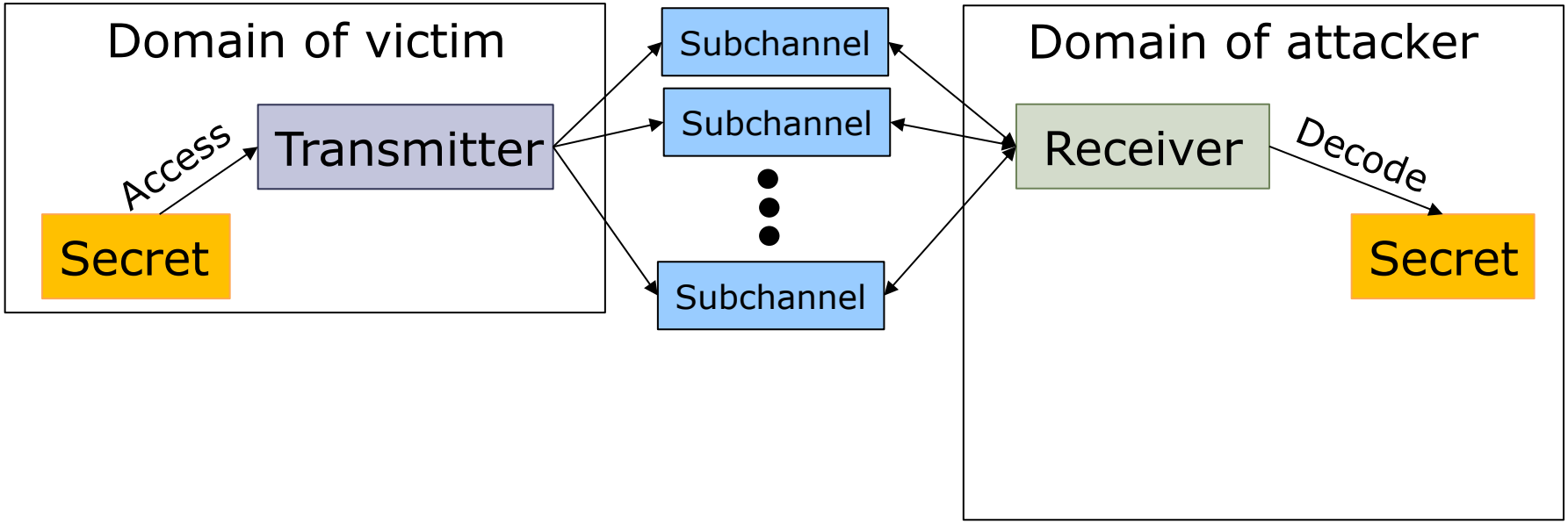
Like a frequency modulated (FM) radio transmission (See later Meltdown)

Obfuscating the channel (2)



- Adding a process dependent hash makes the needed cache collision probabilistic.
- Now the receiver needs an extra step to find a way to probe a variety of "channels" to detect modulation.

Receiver Calibration



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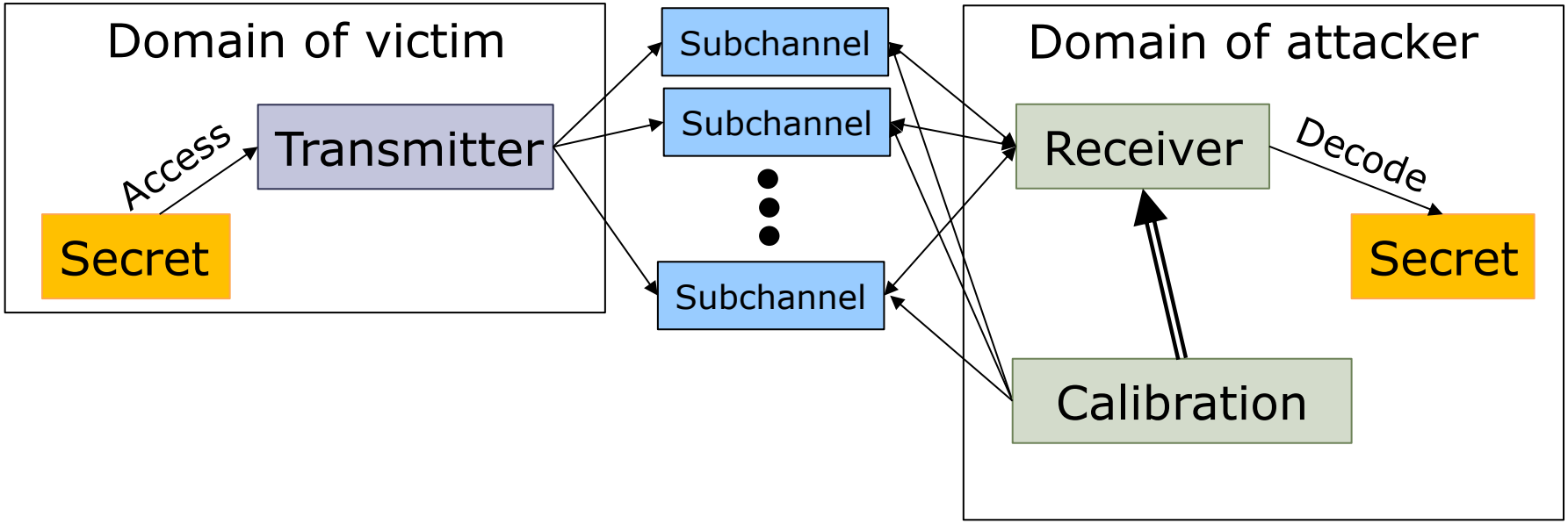

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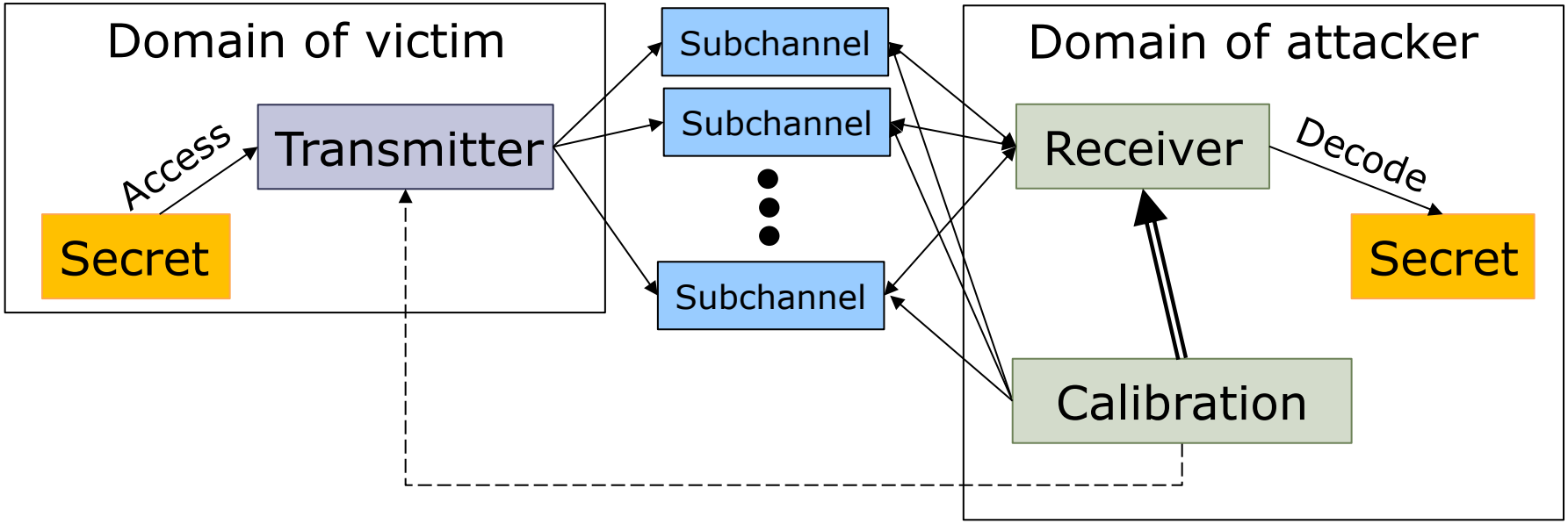

- The calibration unit determines which subchannels the receiver needs to use to detect modulation by a transmission
- During calibration, the receiver may just observe known transmissions by the transmitter or provoke the transmitter to make a particular transmission.

Hashing* variations

- Nature of hash
  - Well-known
  - Secret
  - Cryptographic (per machine key)

*Hash -> address to set index mapping

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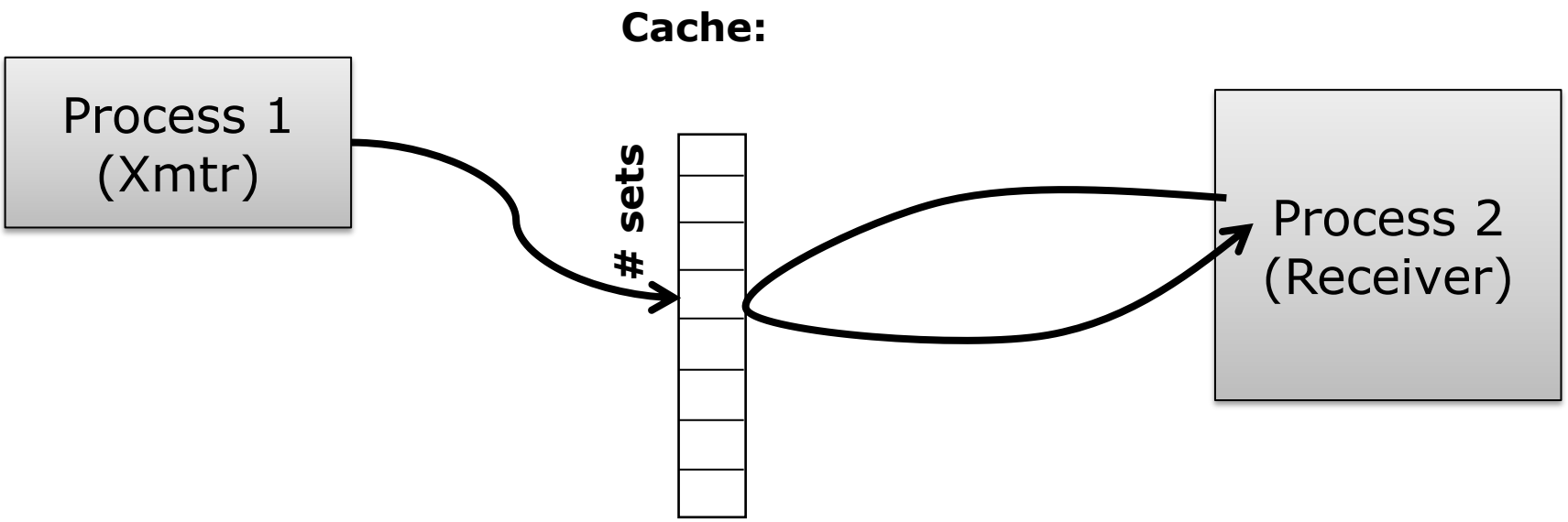
*Hash -> address to set index mapping

Noise in the channel



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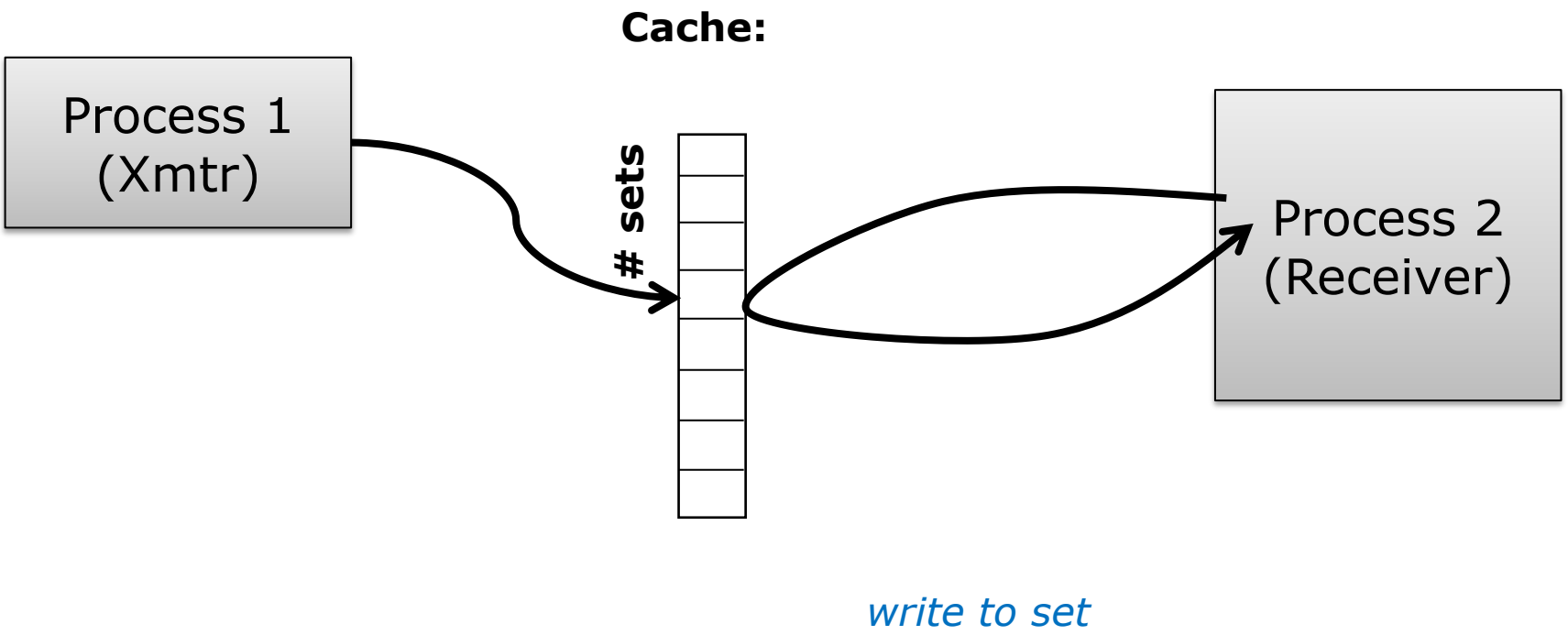

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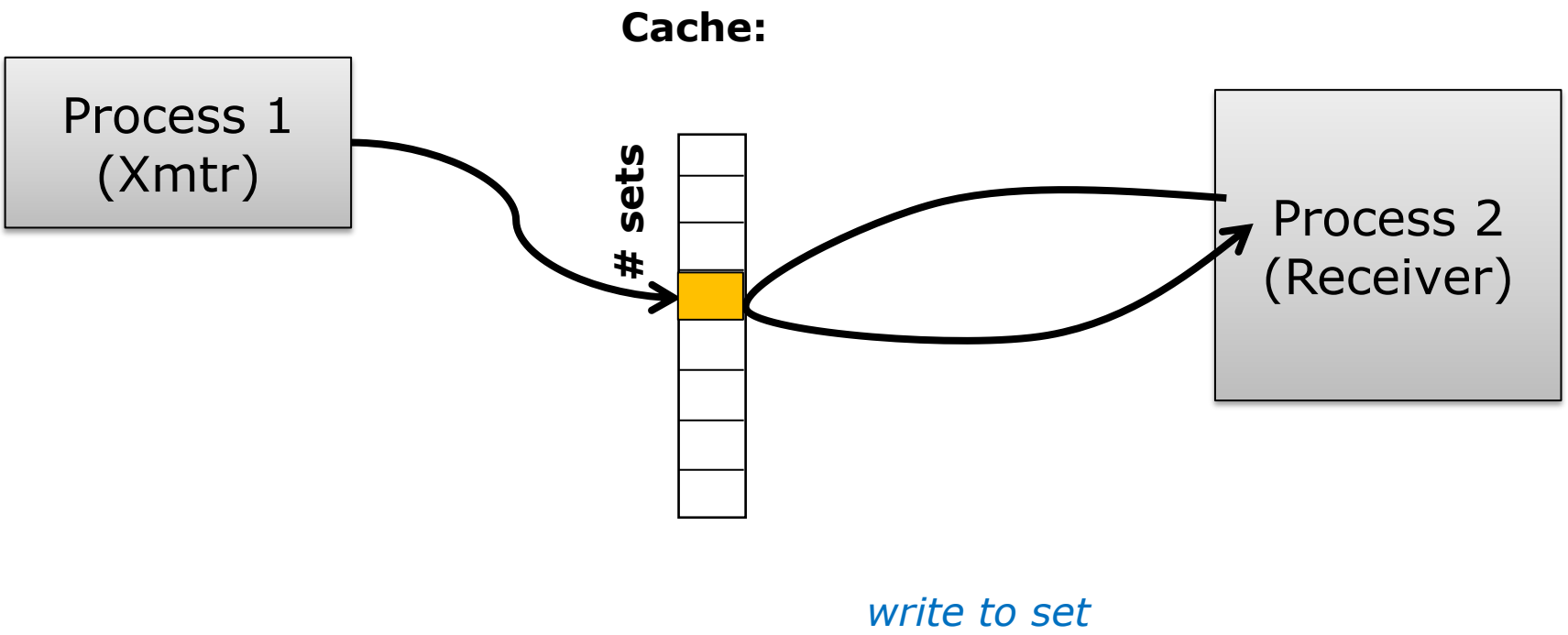

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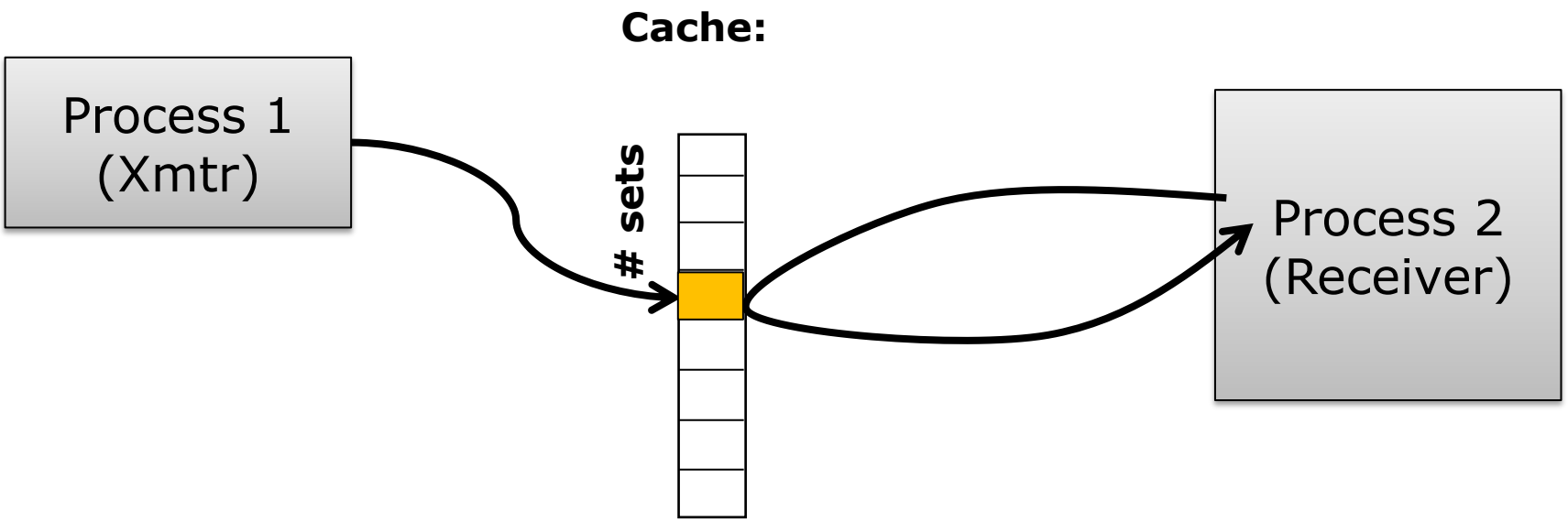

if (**send '0'**)
idle
else
write to a set

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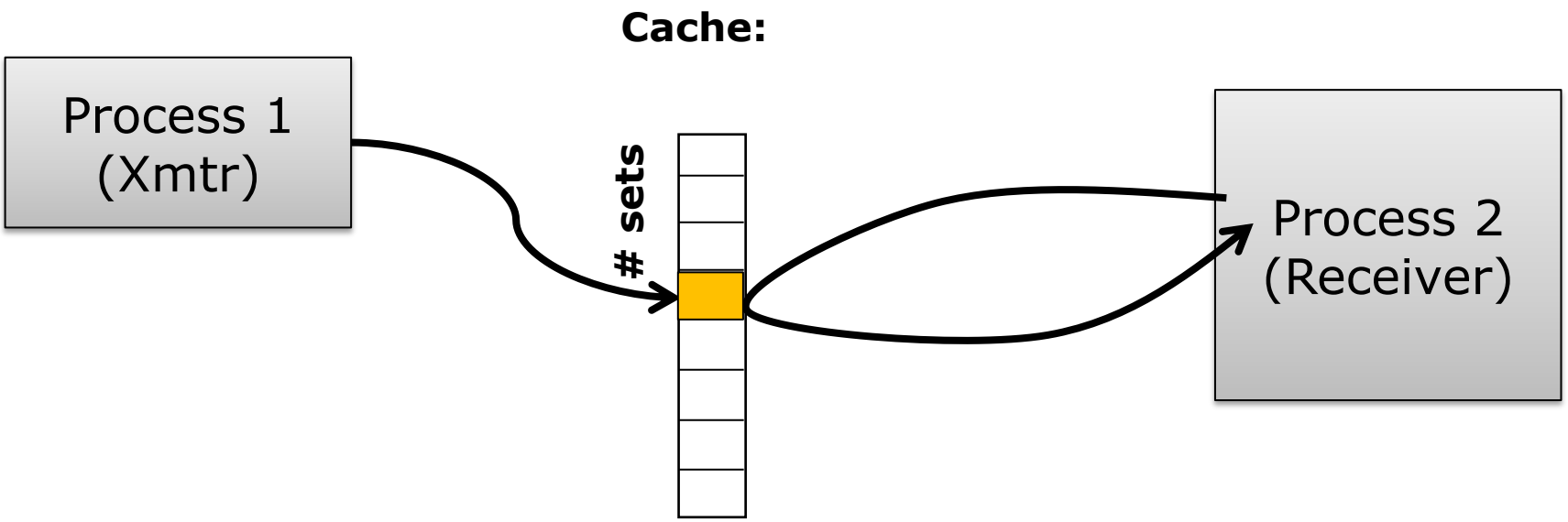

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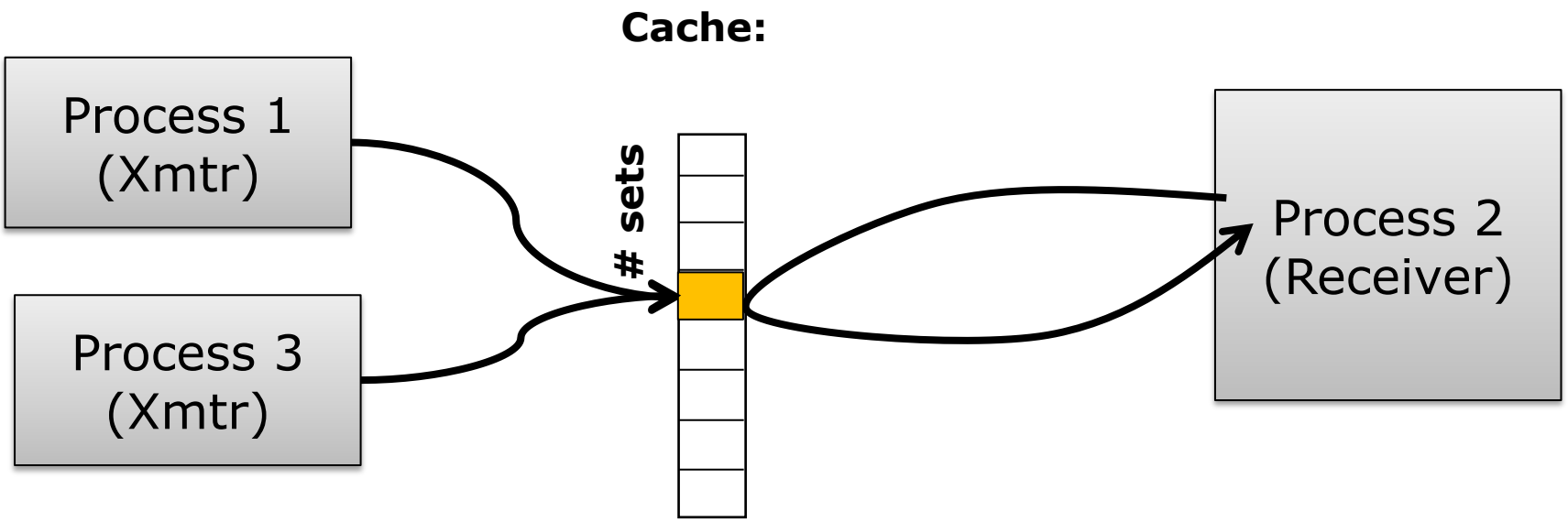

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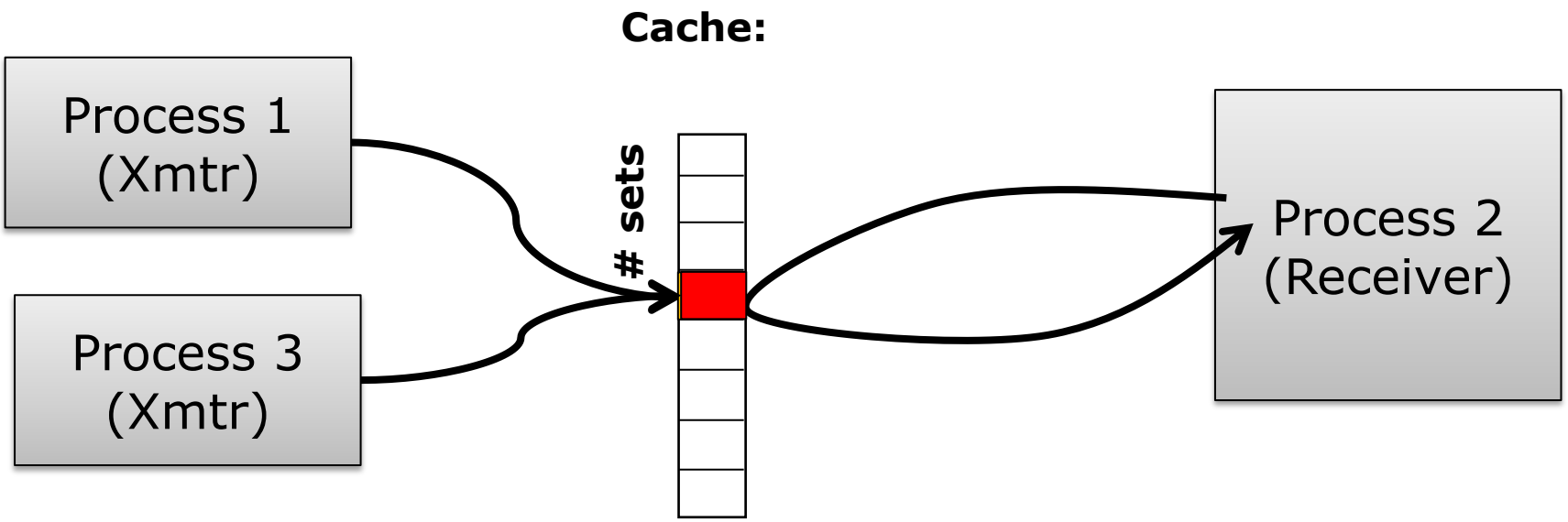

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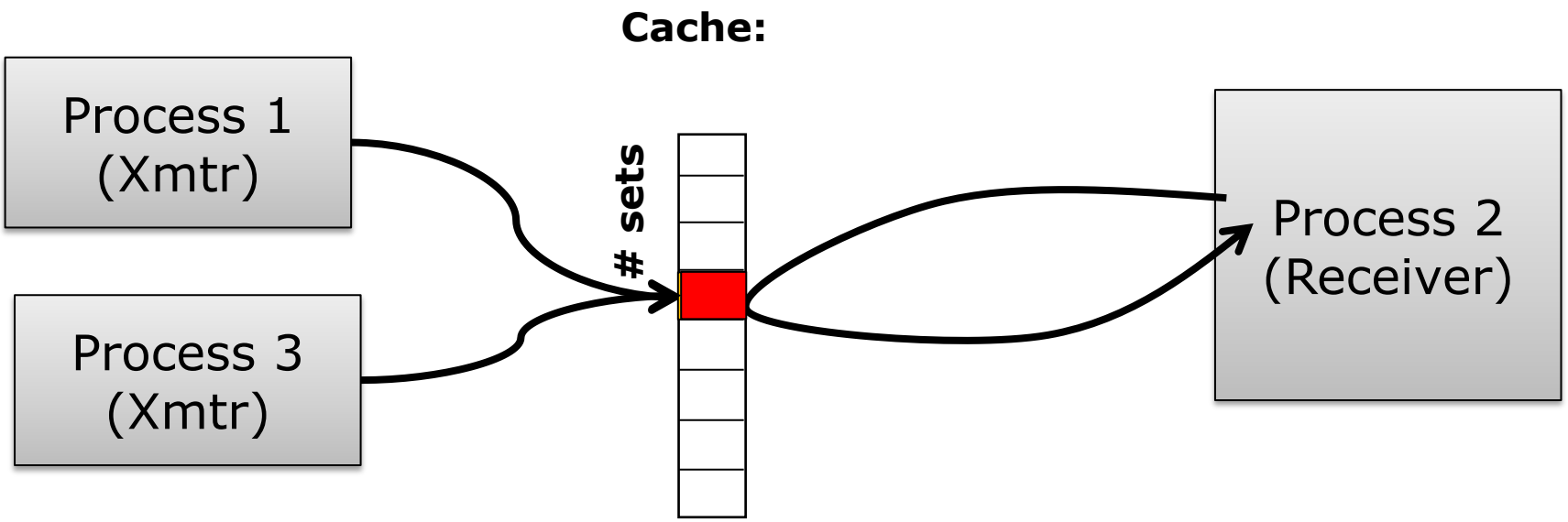

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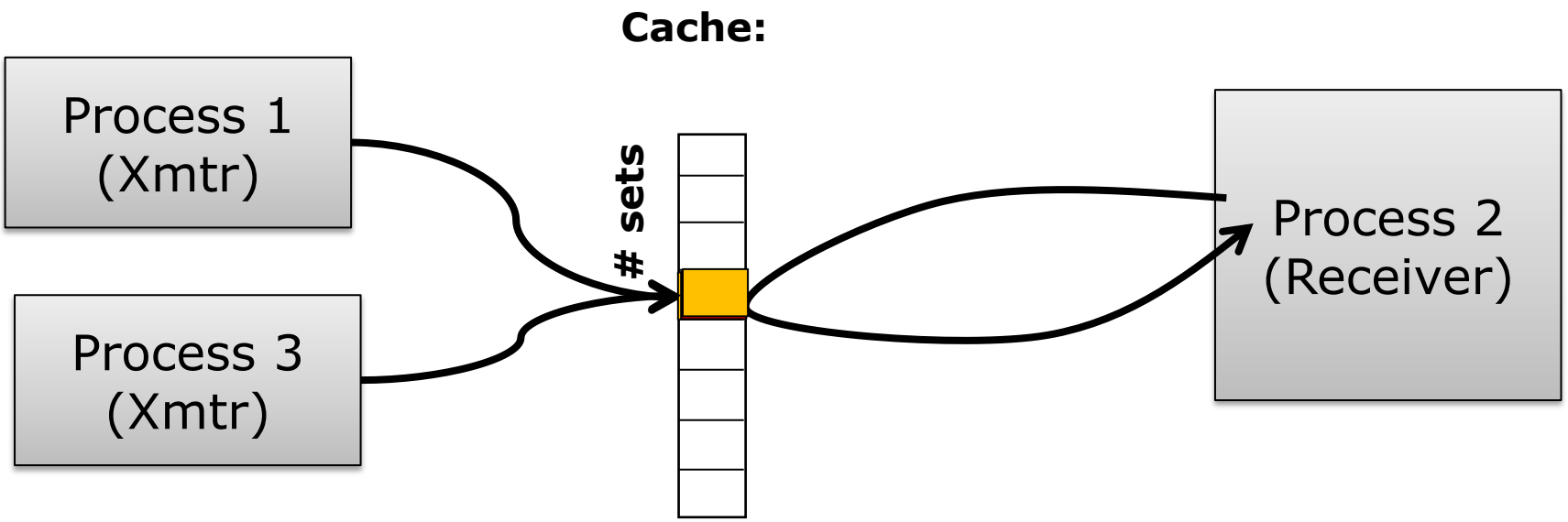

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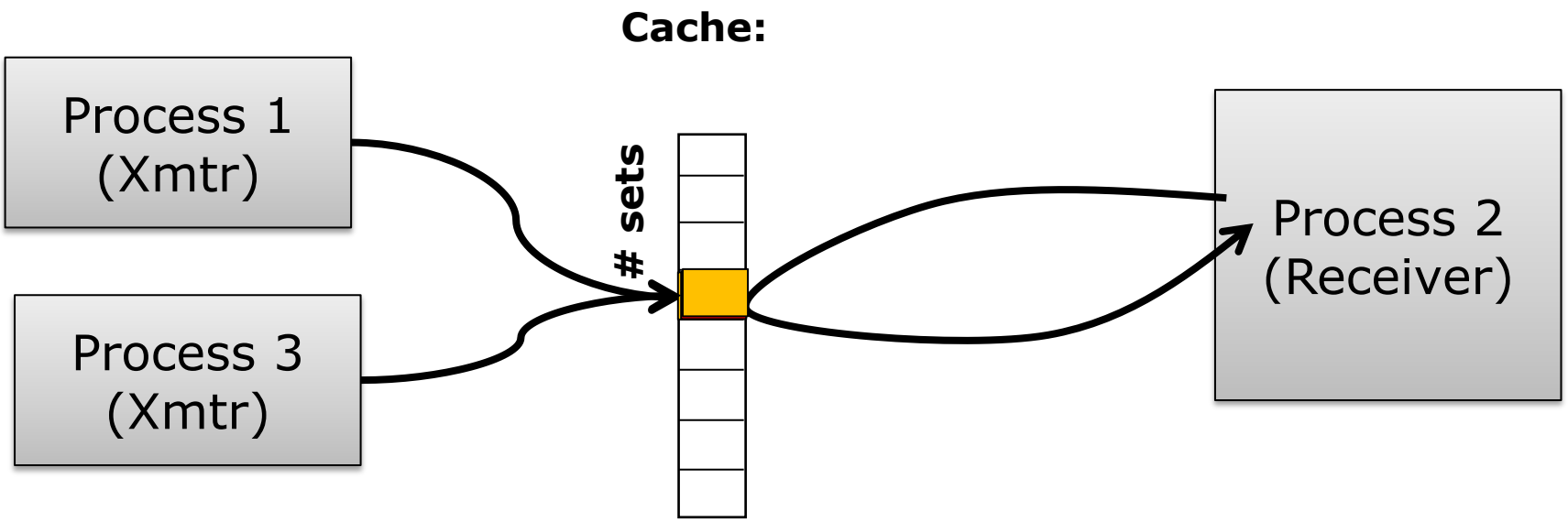

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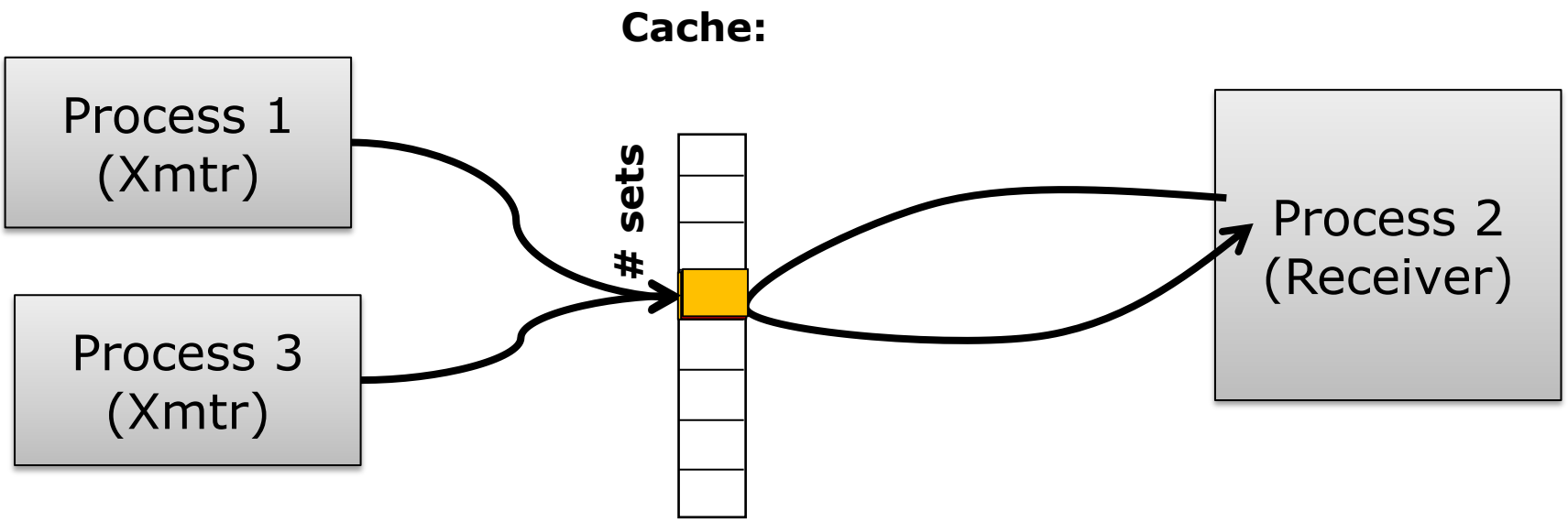

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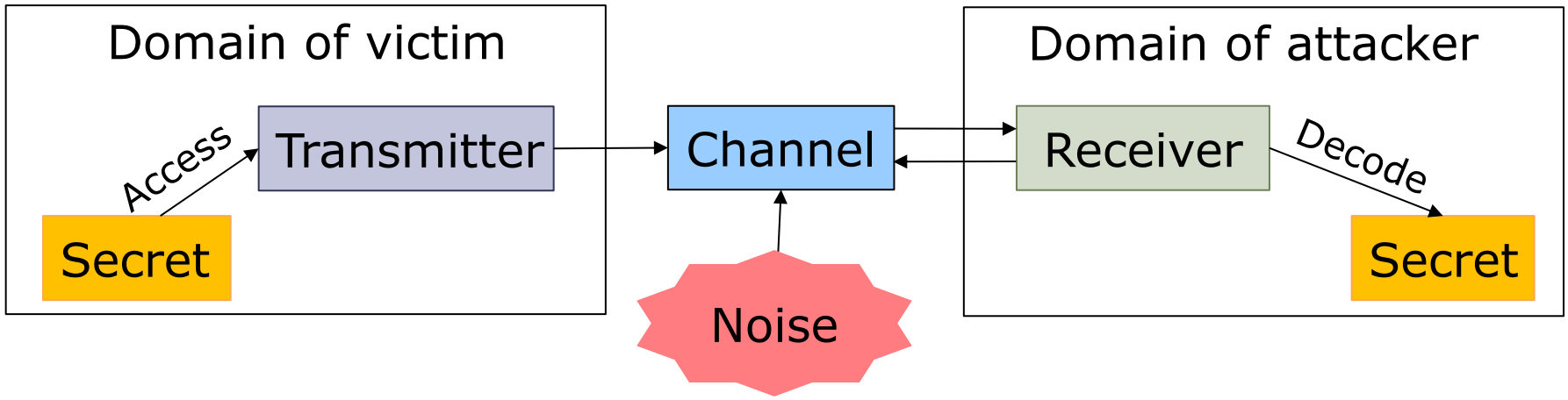
Receiver interprets "noise" as a signal!

Channel Noise



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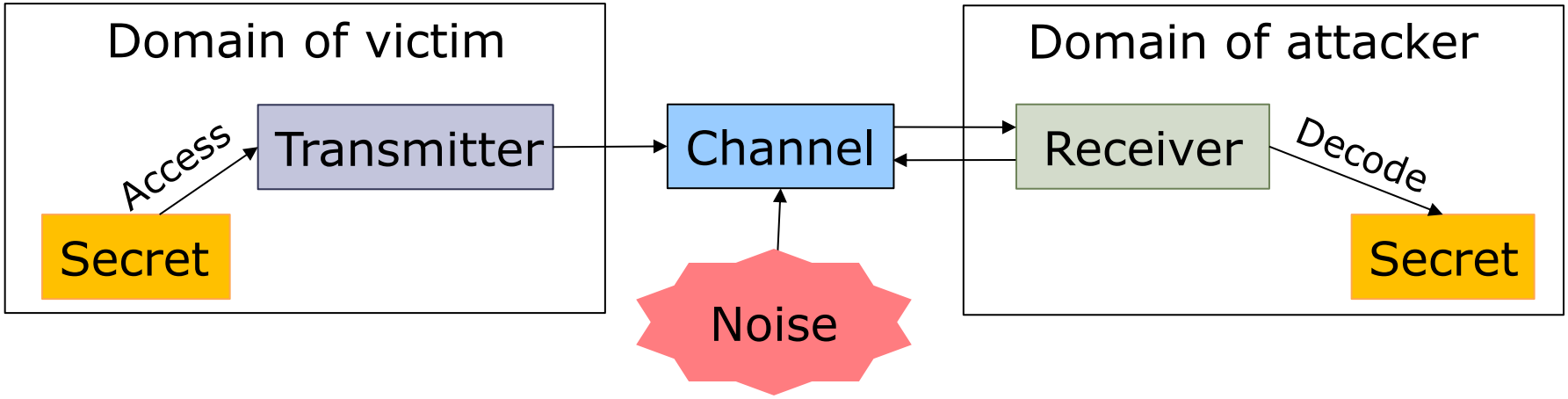

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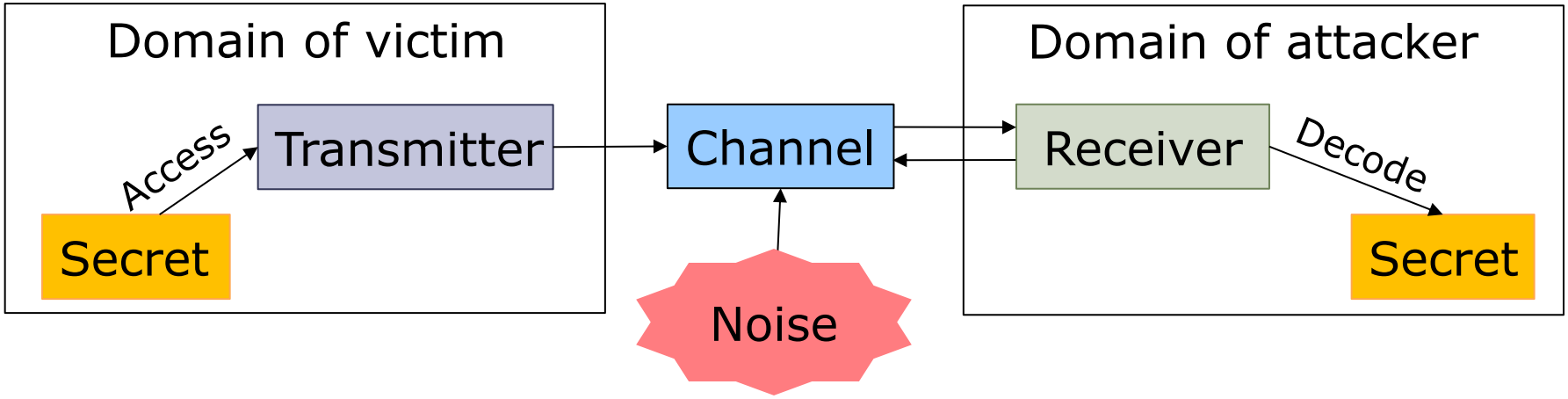

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- Increases in reliability of reception can be improved by improved message encoding, e.g., by repeating the message.

Noise makes signal probabilistic

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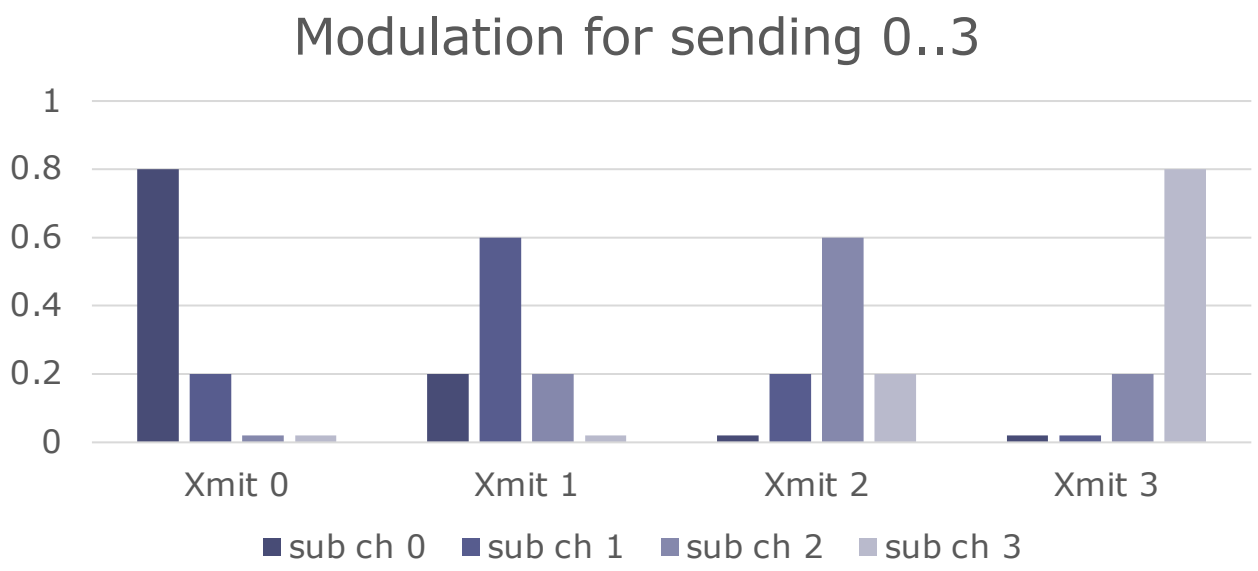

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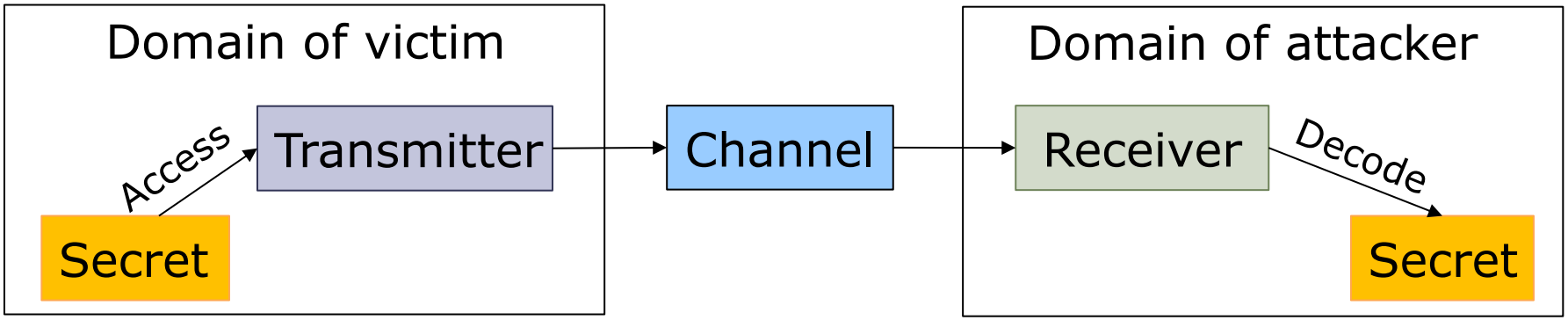

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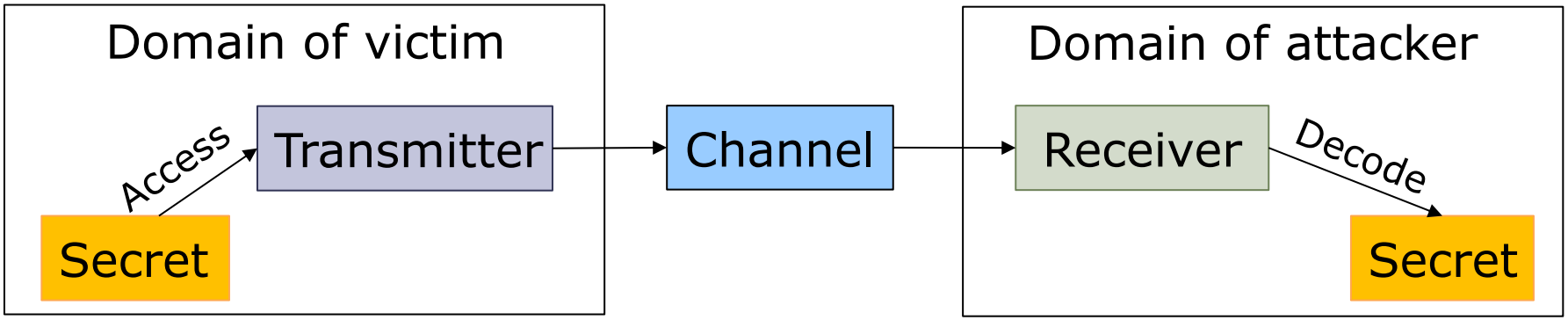

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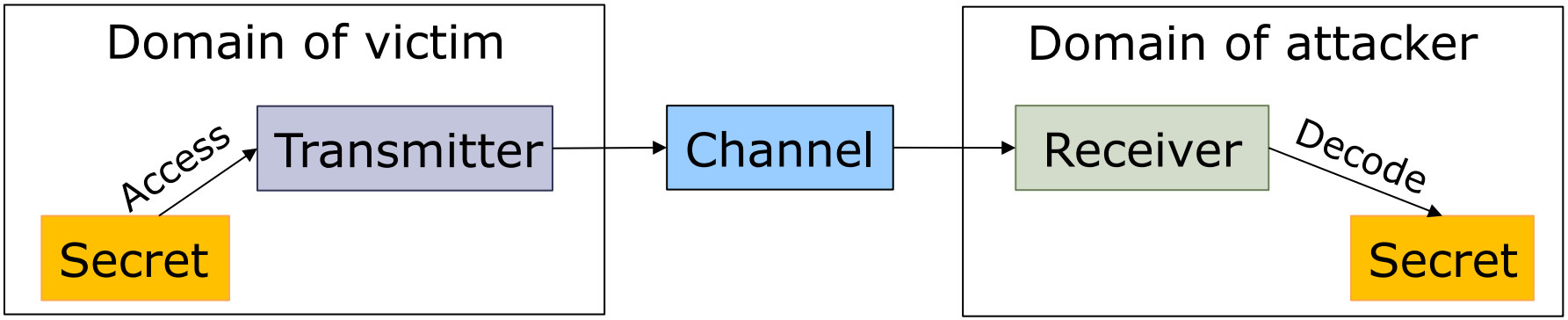
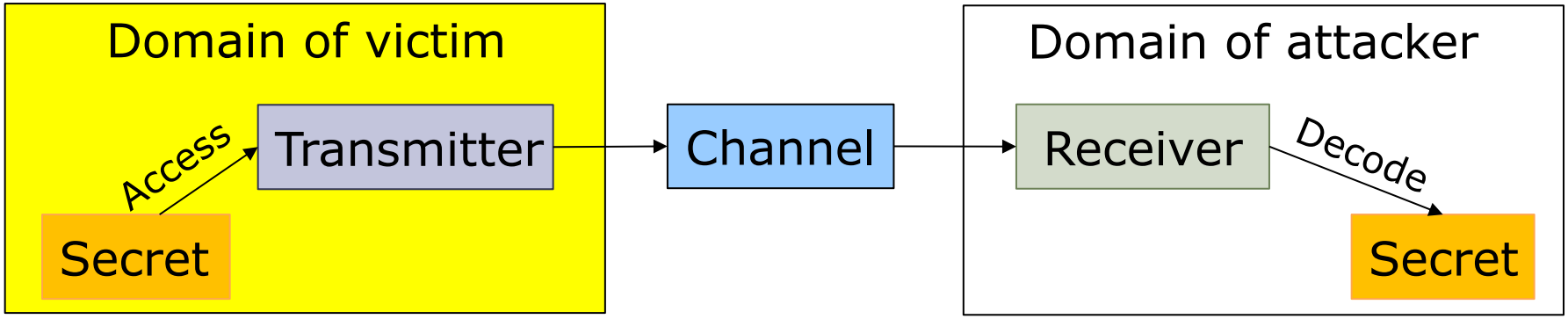


- The communication model provides a systematic way to reason about microarchitectural side channels
- Different attack strategies are usually different ways of modulating channels
- To improve channel precision, need precondition, calibration, decoding techniques, noise => all have analogies to telecommunication

Types of Transmitters



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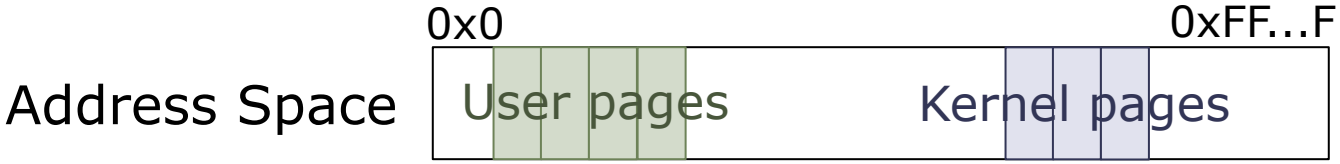
Reminder: Speculative Execution



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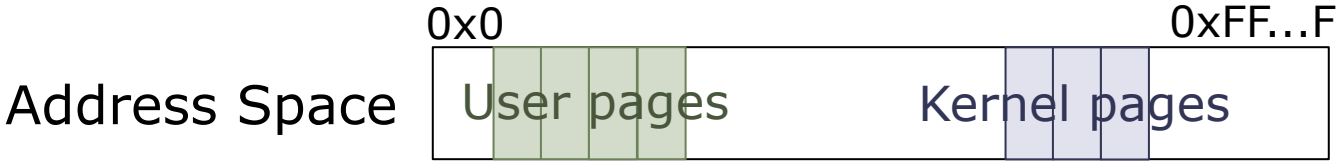

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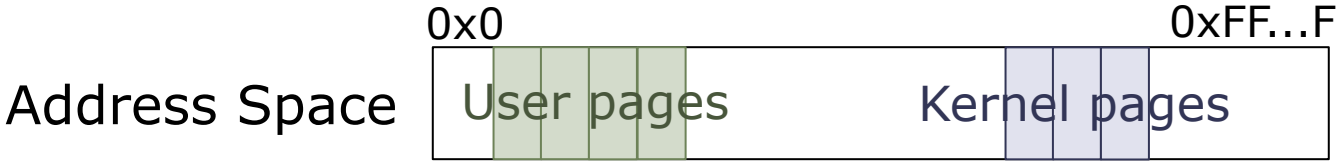

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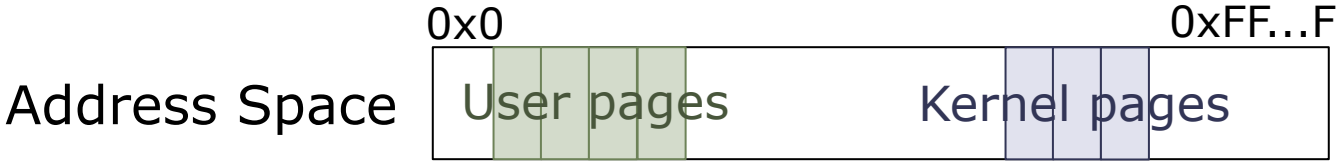

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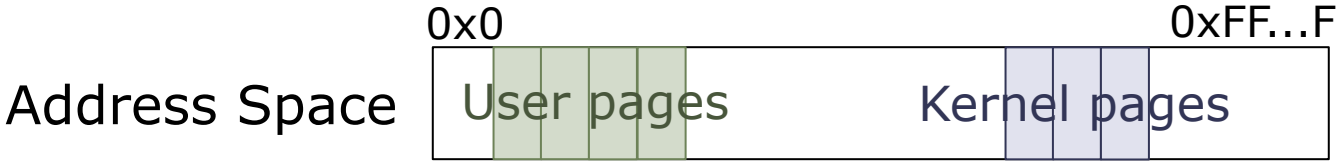

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- Causes a protection fault, but data at "kernel_address" is speculatively read and loaded into val!

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    Return zero upon permission check failure (supporting precise exception)

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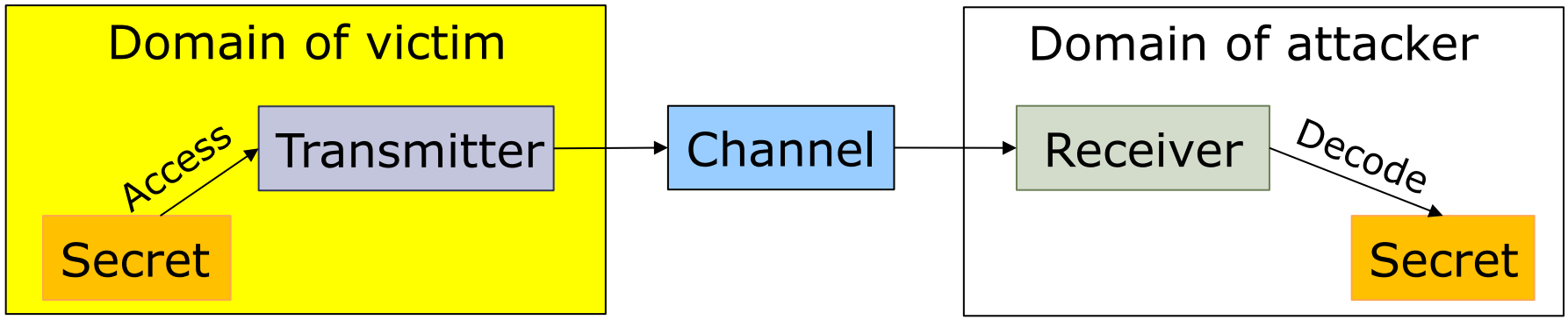

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[Kocher et al. 2018]

- Consider a situation where there is some kernel code that looks like the following:

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- Interpret that code as an FM transmitter:

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- Interpret that code as an FM transmitter:

```
xmit: uint8_t secret = *kernel_address;
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- But this kernel code is protected by a branch. *Can we make the kernel speculatively execute "xmit"?*

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if (kernel_address is public_region) {
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Spectre variant 1
[Kocher et al. 2018]

- Consider a situation where there is some kernel code that looks like the following:

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Conditional branch misprediction

Spectre variant 1
[Kocher et al. 2018]

- Consider the following kernel code, e.g., in a system call

```
if (x < array1_size)
  y = array2[array1[x] * 4096];
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1. Precondition: Flush all the elements in array2 from cache

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4. Receive: Attacker probes cache to infer which line of array2 was fetched, learns data at kernel address

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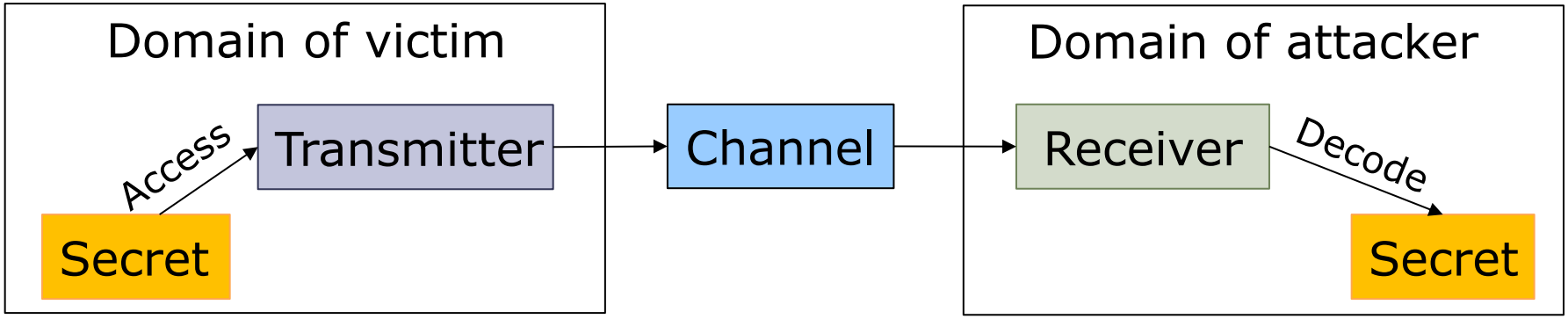
1. Train: trigger `xyz->xmit` many times
2. Transmit: '`abc`' and '`xyz`' alias in BTB, so we can speculatively trigger `abc->xmit`
3. Receive: similar to Spectre v1

Types of Transmitters



- Types of transmitter:
  1. Pre-existing so victim itself leaks secret, (e.g., RSA keys)
  2. Programmed and invoked by attacker (e.g., Meltdown)
  3. Synthesized from existing victim code and invoked by attacker (e.g., Spectre v2)

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- Short-term mitigations:
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- Long-term mitigations:
  - Disabling speculation?
  - Closing side channels?

Summary

- ISA is a timing-independent interface, and
  - Specify *what* should happen, not *when*
- ISA only specifies architectural updates
  - *Micro-architectural changes are left unspecified*
- So implementation details (e.g., speculative execution) and timing behaviors (e.g., microarchitectural state, power, etc.) have been exploited to breach security mechanisms.
- ISA, as a software-hardware contract, is insufficient for reasoning about microarchitectural security

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Graduate-Level/ AUS

12 Units (3-0-9)

MW 1:00 - 2:30

http://csg.csail.mit.edu/6.888Yan/

Thank you!