

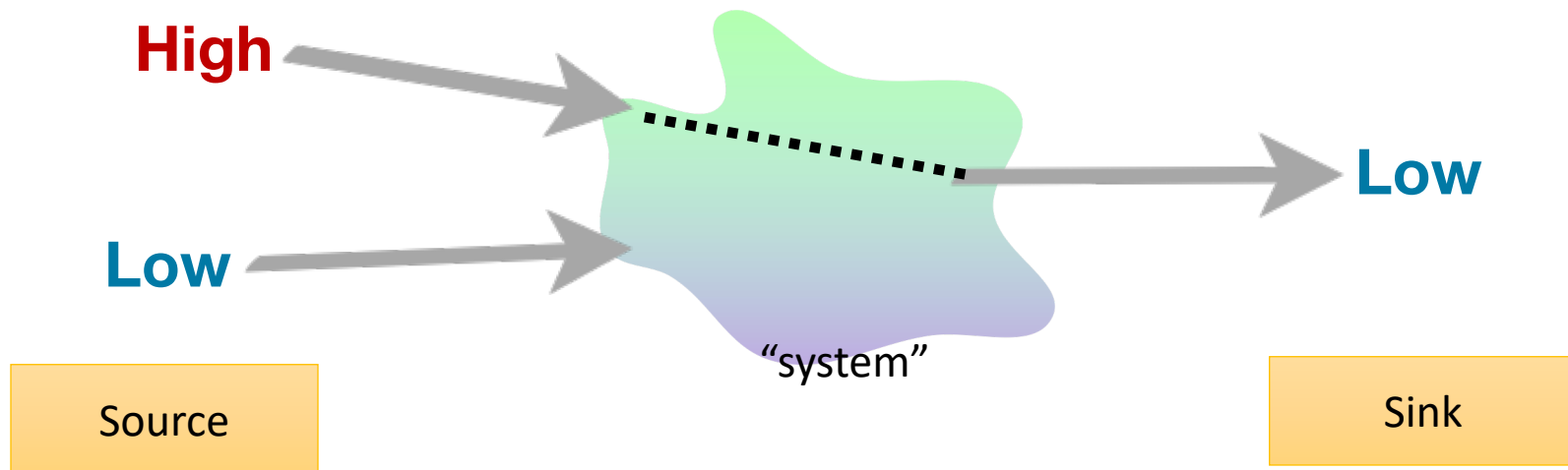
Complete Information Flow Tracking from Gates Up

Mohit Tiwari, Xun Li, Hassan M G Wassel, Frederic T Chong, Timothy Sherwood

Presented by Mengjia Yan

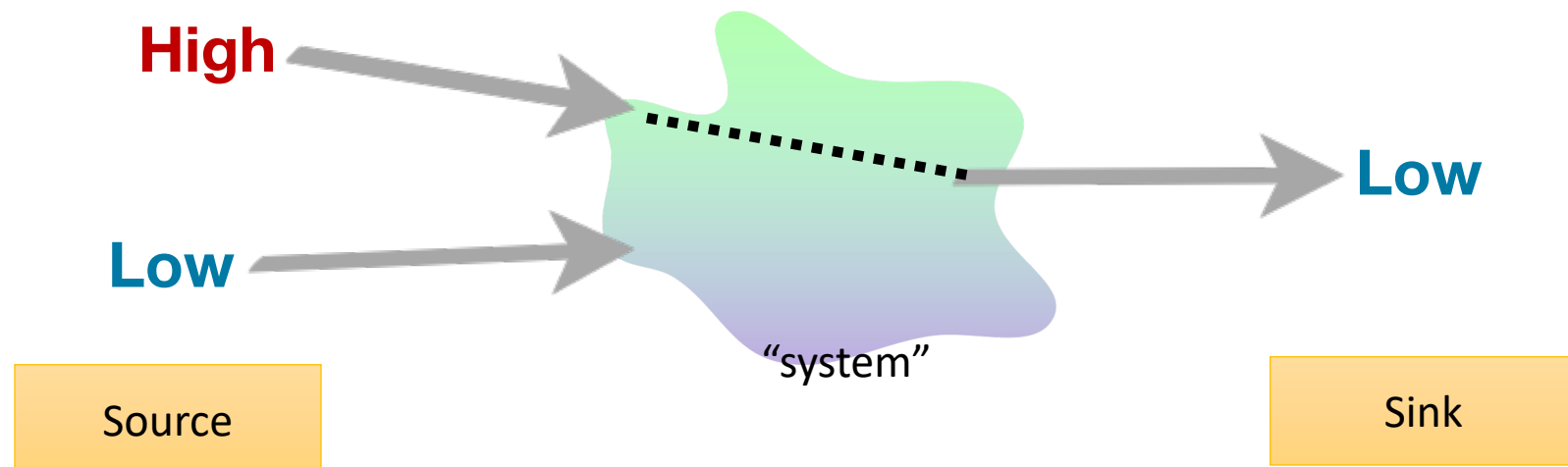
Based on slides from Mohit Tiwari

Goal: Non-Interference



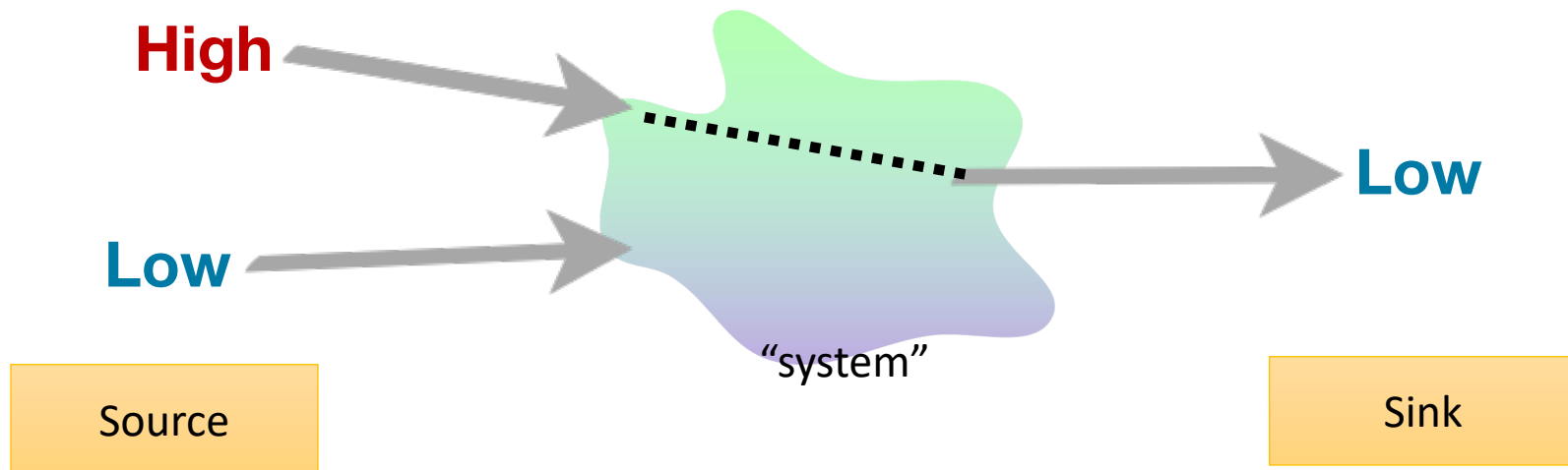
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- **Non-Interference:** a change in a High input can never be observed or inferred from changes in the Low output. That is, **High** data should never leak to **Low**



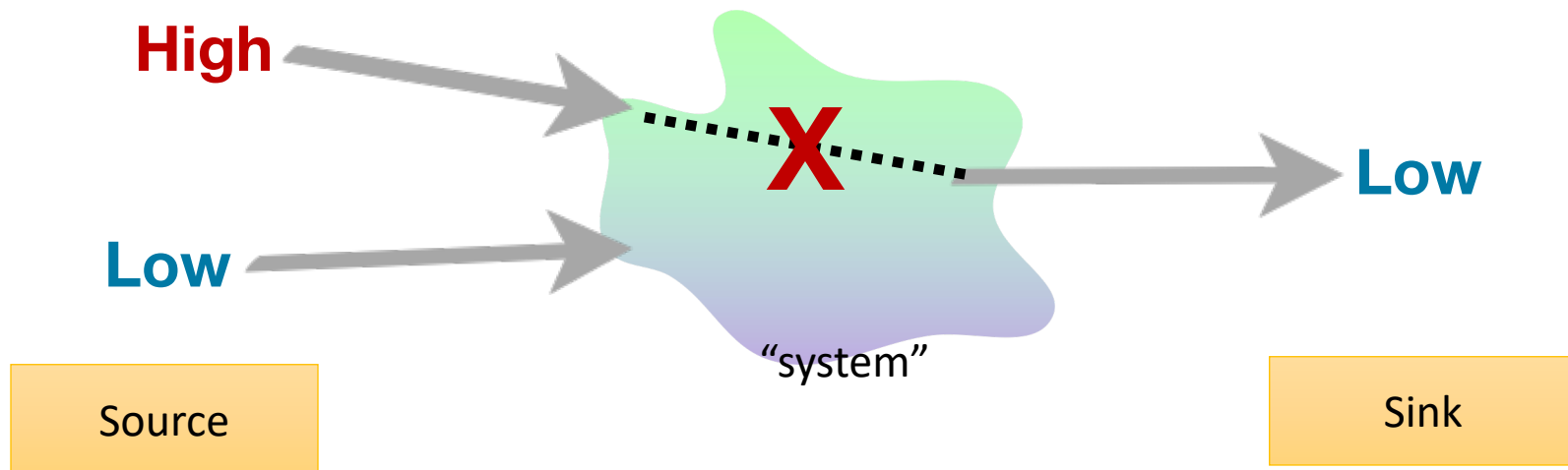
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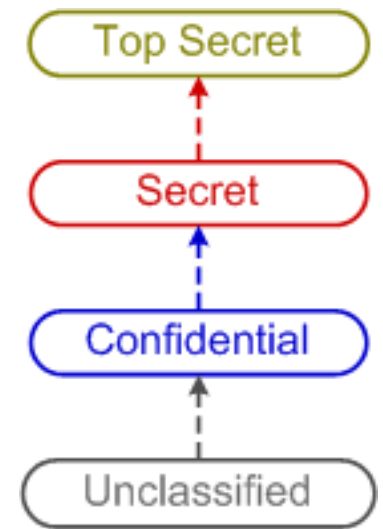
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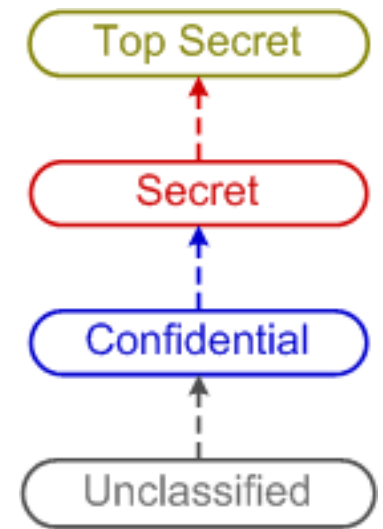
Information Flow for Privacy

- General lattice policies
- Secret vs. Unclassified Data
 - **Secret**: data with restricted access permission
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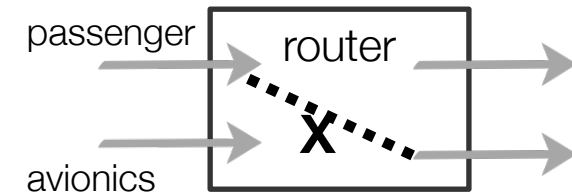
Information Flow for Privacy

- General lattice policies
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 - **Secret**: data with restricted access permission
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- Enforce the property of non-interference:
 - Verify information never flows from **high** to **low**.
 - **Secret** information is never used to modify **unclassified** data



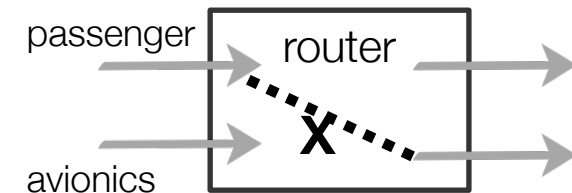
Information Flow for Integrity

- Trusted vs. Untrusted Tasks
 - **Trusted**: processes which are critical to the correct functionality of the space vehicle systems
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- Enforce the property of non-interference:
 - Verify information never flows from **high** to **low**.
 - **Untrusted** information is never used to make critical (**trusted**) decisions nor to determine the schedule (real-time)



Threat Model

- Low output can include
 - Program output
 - Timing
 - Contention on system resources

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- Low output can include
 - Program output
 - Timing
 - Contention on system resources
- Not include
 - Untrusted hardware component problem
 - Physical attacks that may tamper with memory
 - Non-digital side-channel attacks (power distribution and RF signals)

Highlights

- A secure SW/HW co-design **which is verifiable**
- Gate-level information flow tracking
 - More precise than conventional IFT
- ISA restrictions to prevent **taint explosion**
 - Handling conditional branch
 - Handling loops
 - Handling loads/stores

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A new way to look at IFT from a new perspective.

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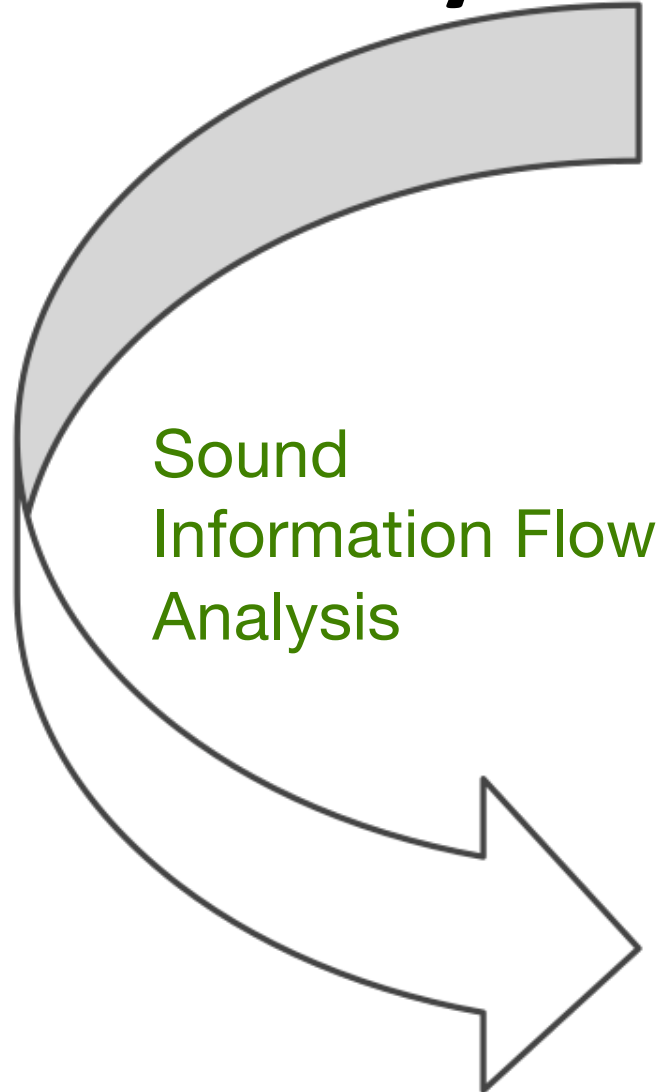
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Usage: GLIFT + Information Flow Policy

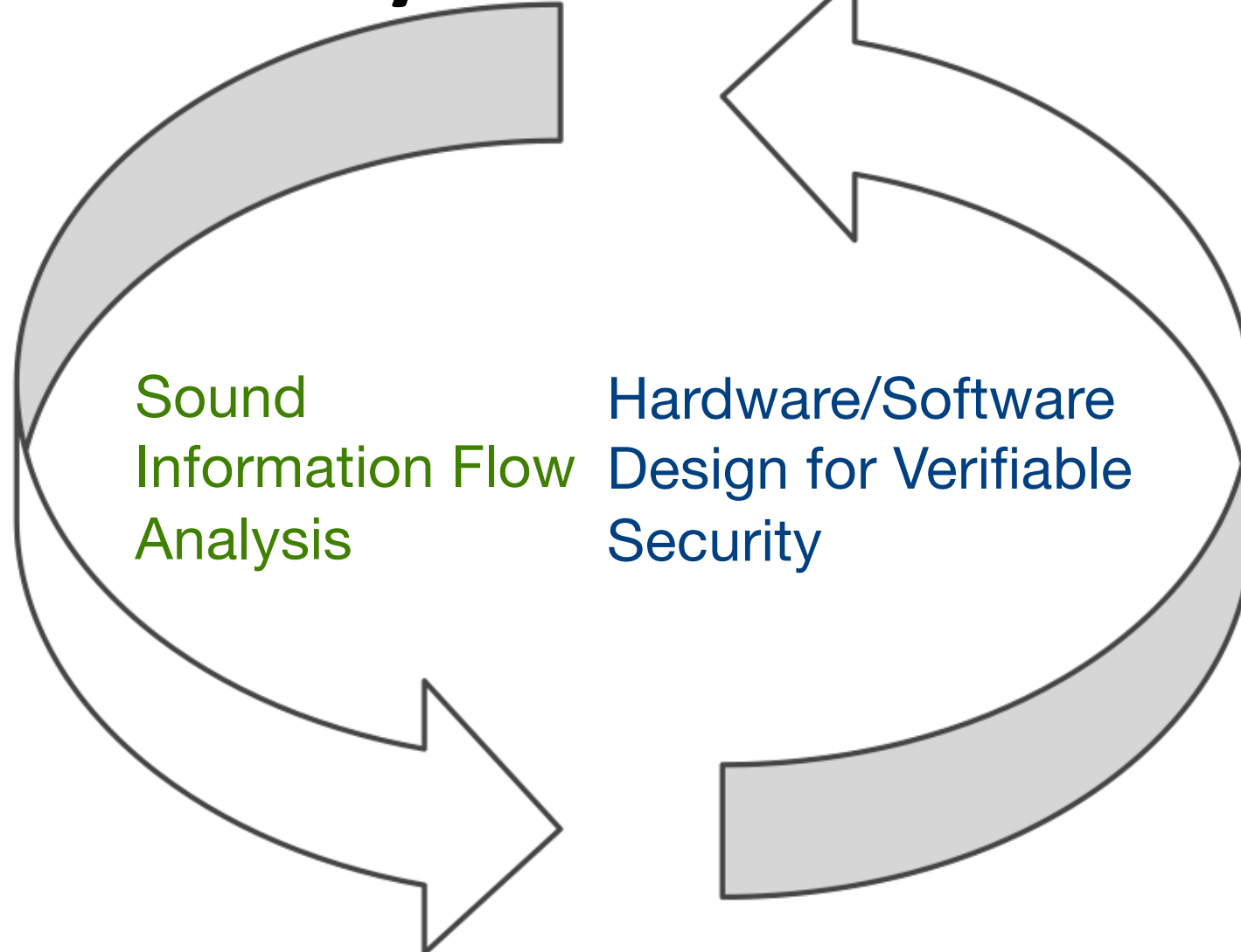


The Vision: Hardware Design for Software Security Verification

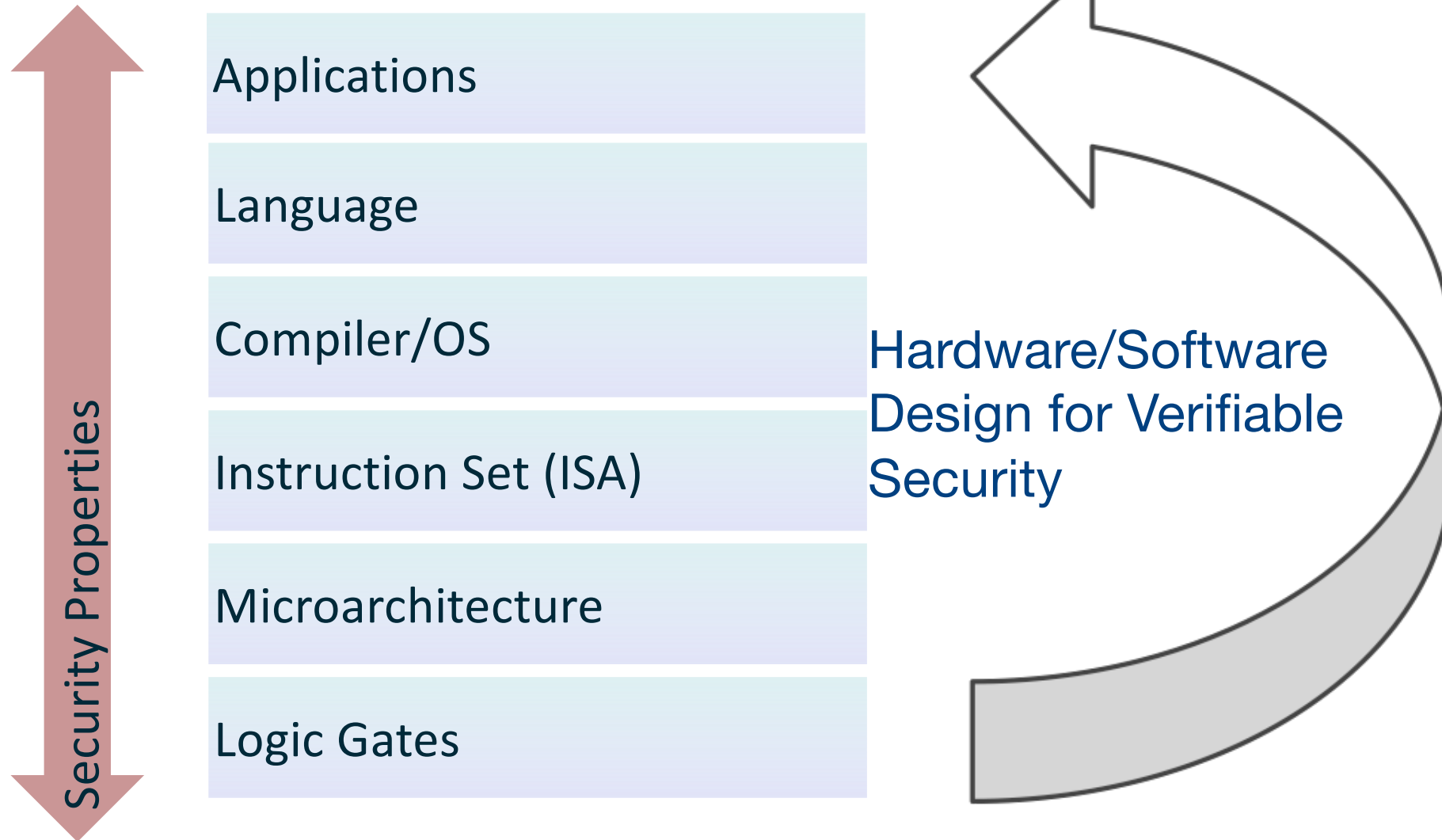
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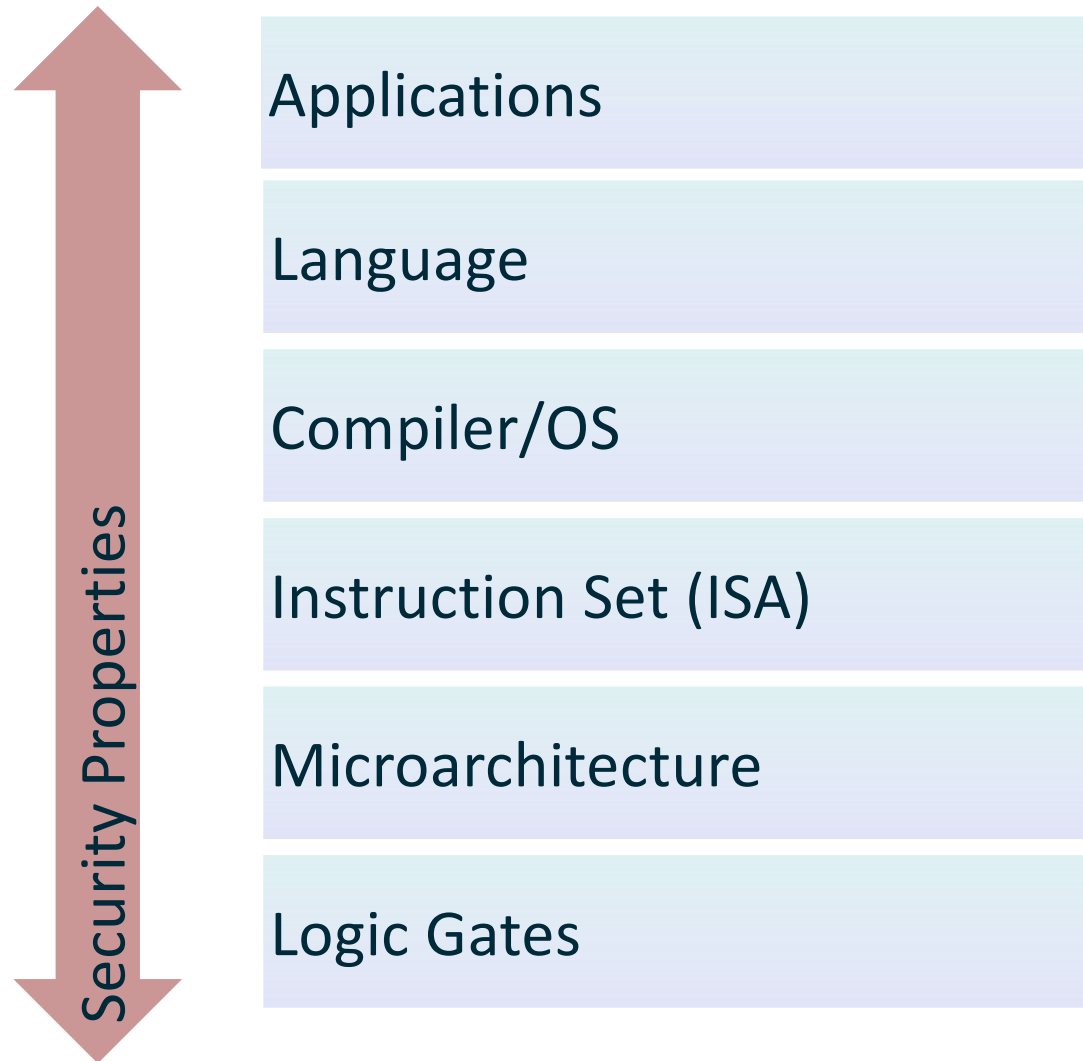
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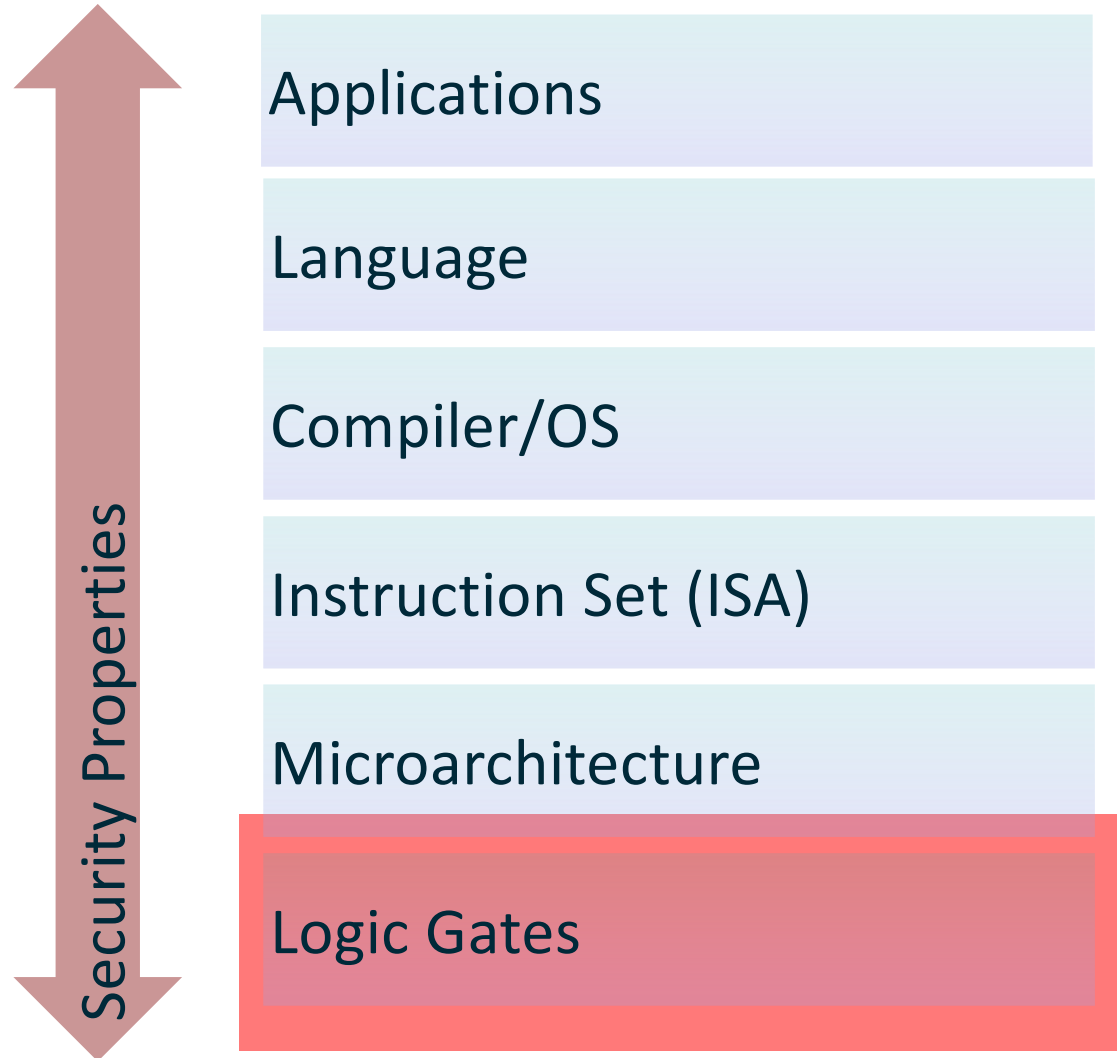
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Static and Dynamic Information Flow Tracking

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Static and Dynamic Information Flow Tracking

- Static analysis is conservative (need alias analysis for precise results)
- Dynamic analysis has difficulty in analyzing implicit flow

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- Static analysis is conservative (need alias analysis for precise results)
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out1 = ld(high)

out2 = ld(low)

out2 is tainted if the address or the memory value is tainted

(explicit flow)

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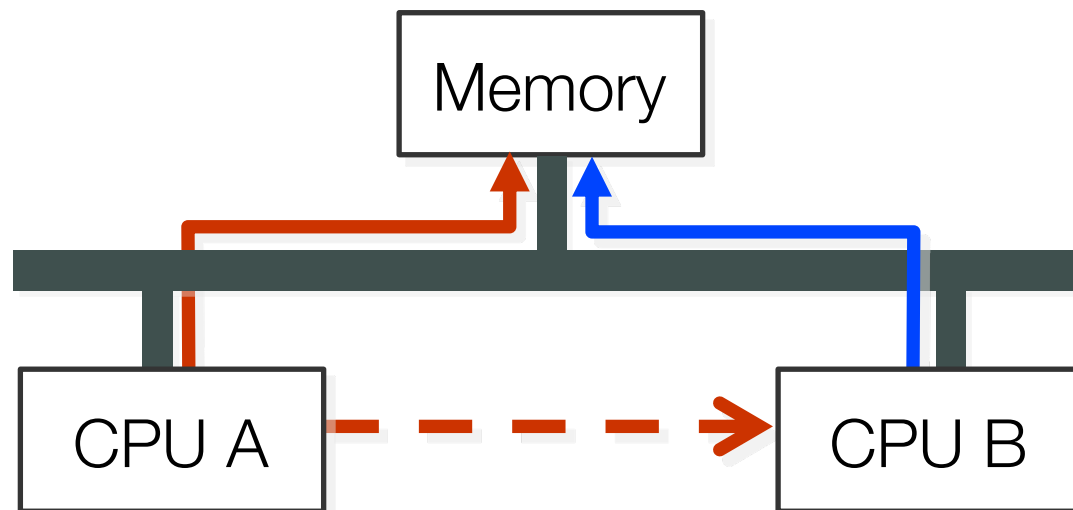
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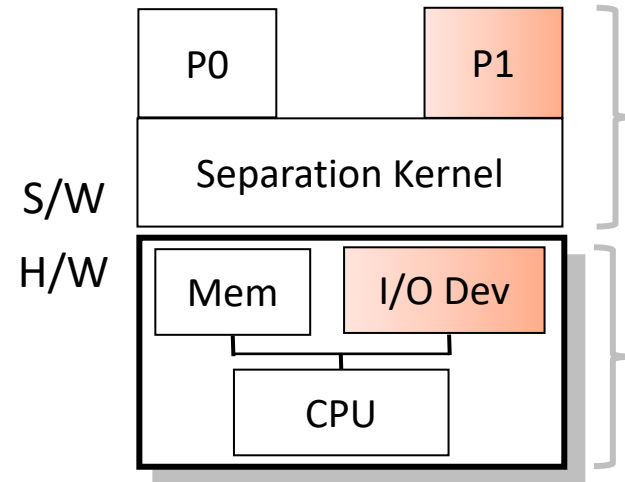
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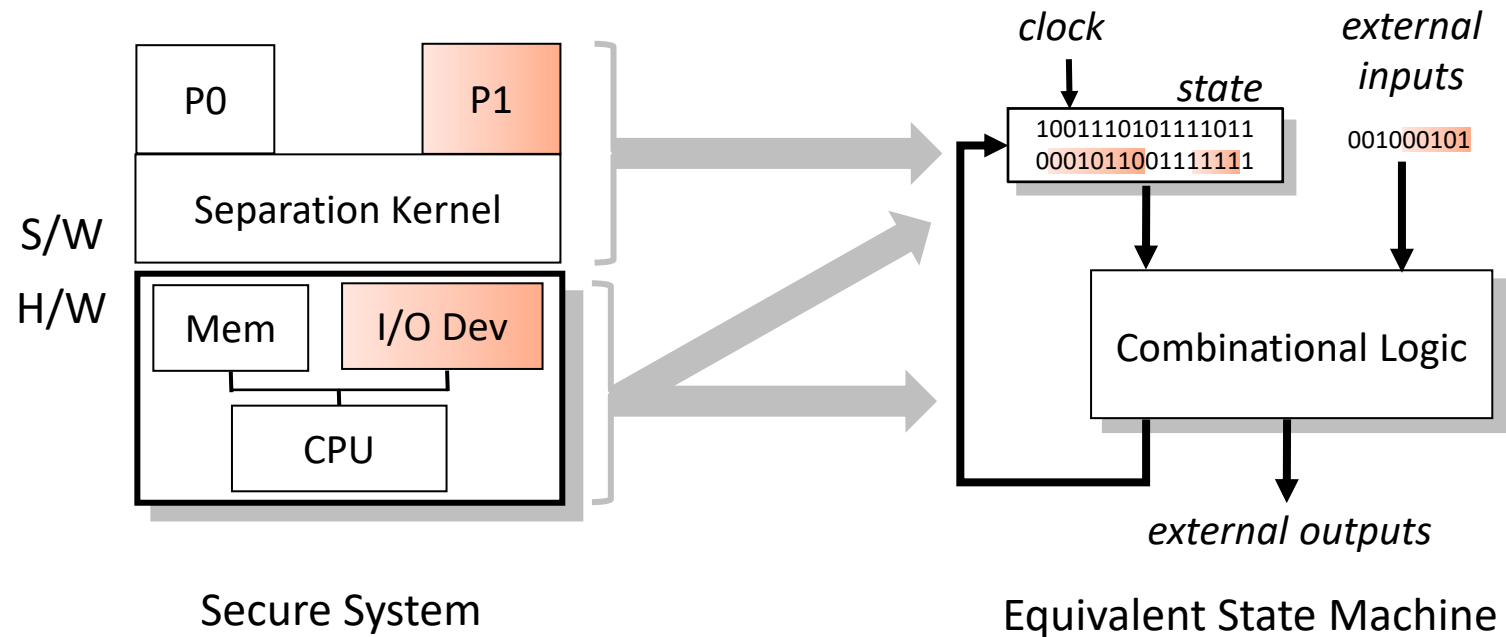
- How to account for all information flows in a system?
 - So that the security property can be verifiable
 - Avoid taint explosion
- How to construct practical systems that won't leak?
 - Use the concept of GLIFT to guide the design

High-level View: Track all flows



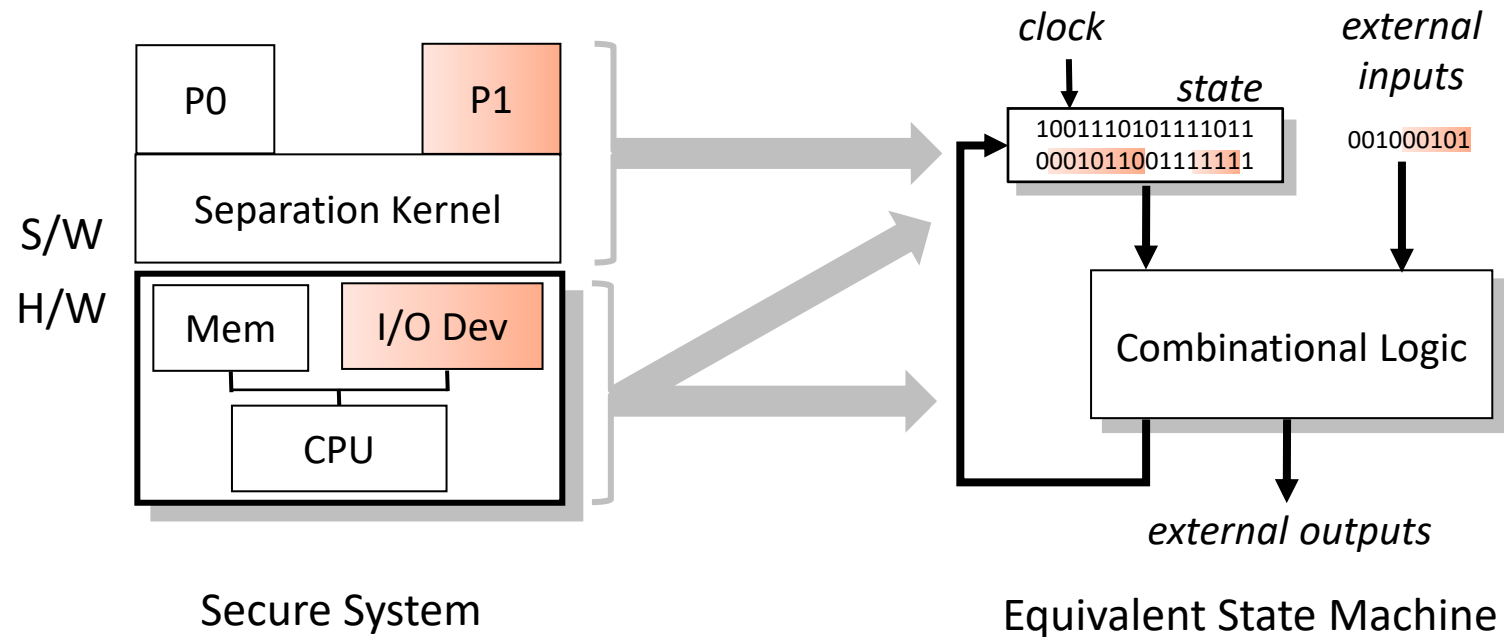
Secure System

High-level View: Track all flows



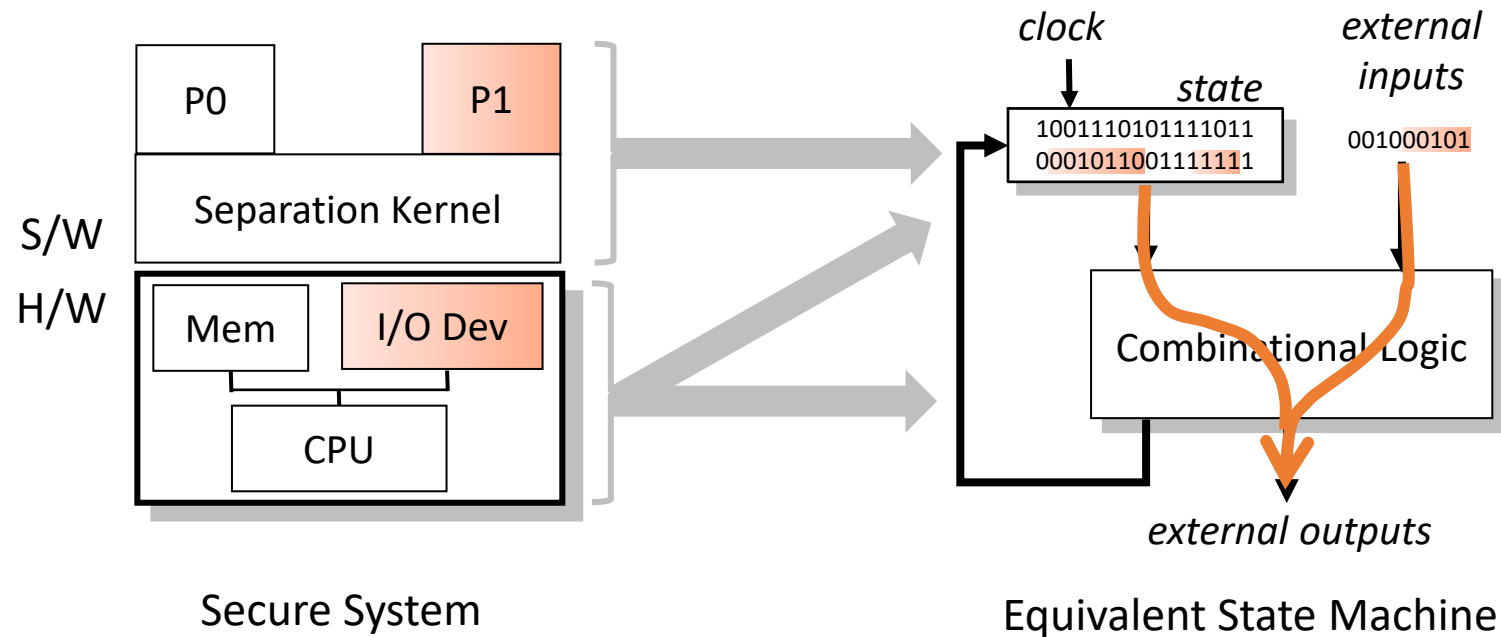
- Flatten design to a (giant) state machine

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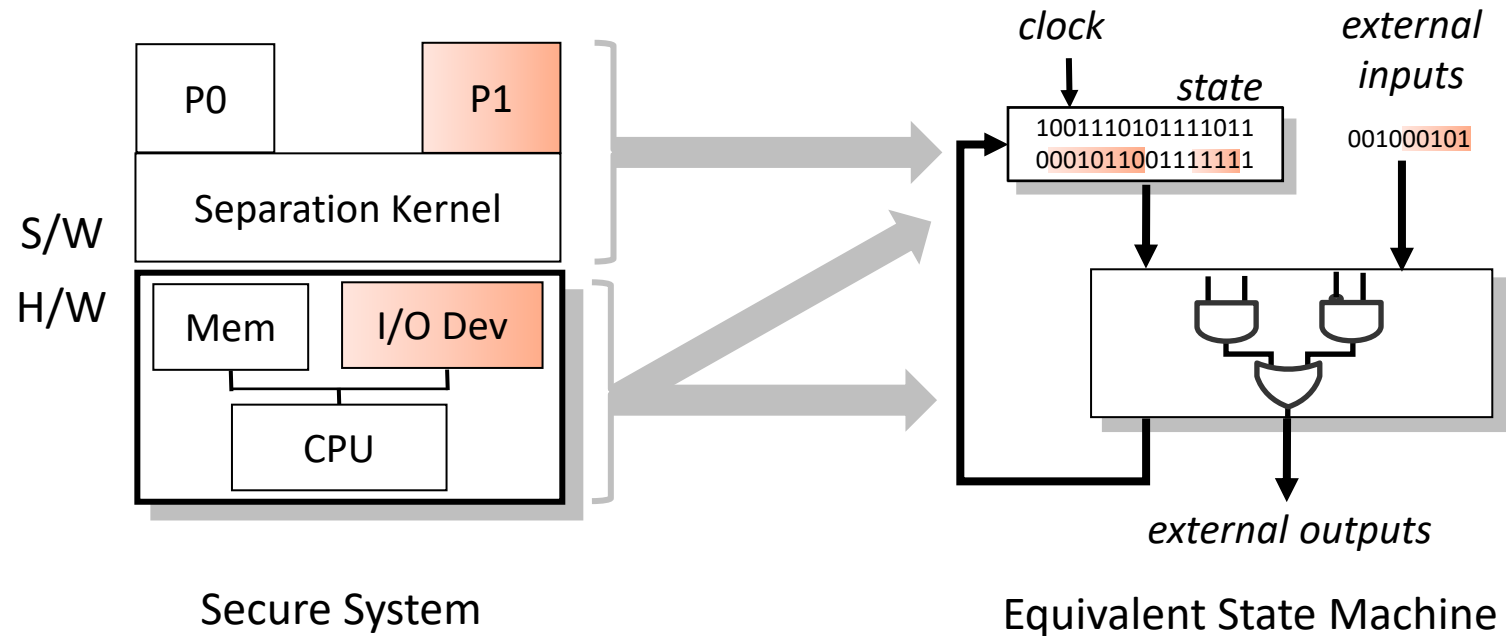
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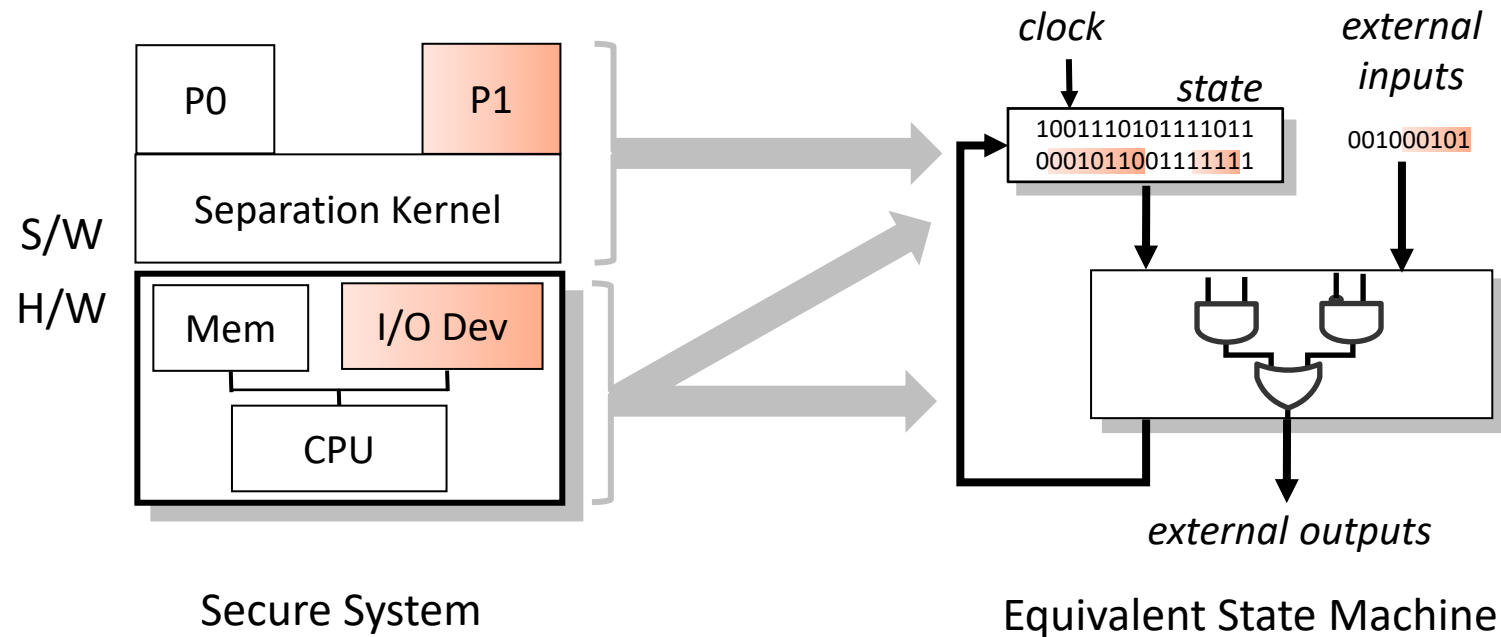
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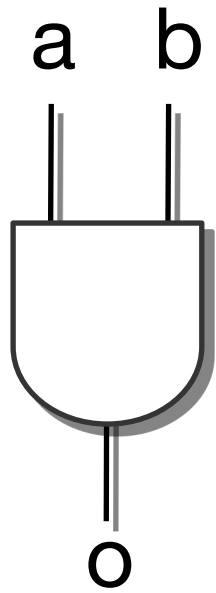
- **Insight:** All flows explicit at the **gate level**

High-level View: Track all flows



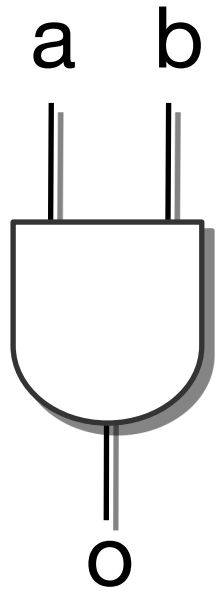
- **Outputs:** Logic function of state and inputs
- **Output Labels:** Logic func. of state, inputs, and labels

Analysis Technique: GLIFT

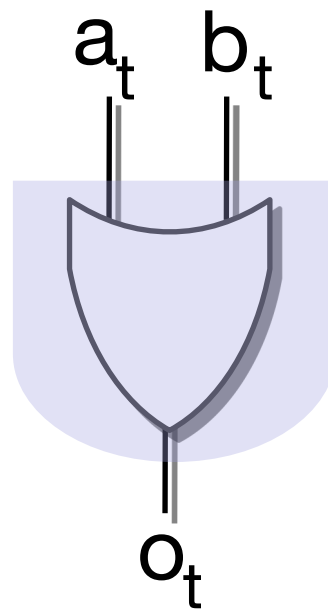


AND

Analysis Technique: GLIFT

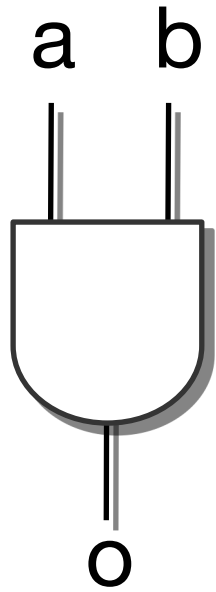


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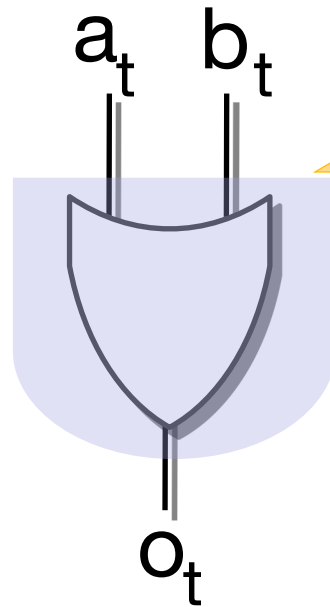


Shadow AND for labels

Analysis Technique: GLIFT



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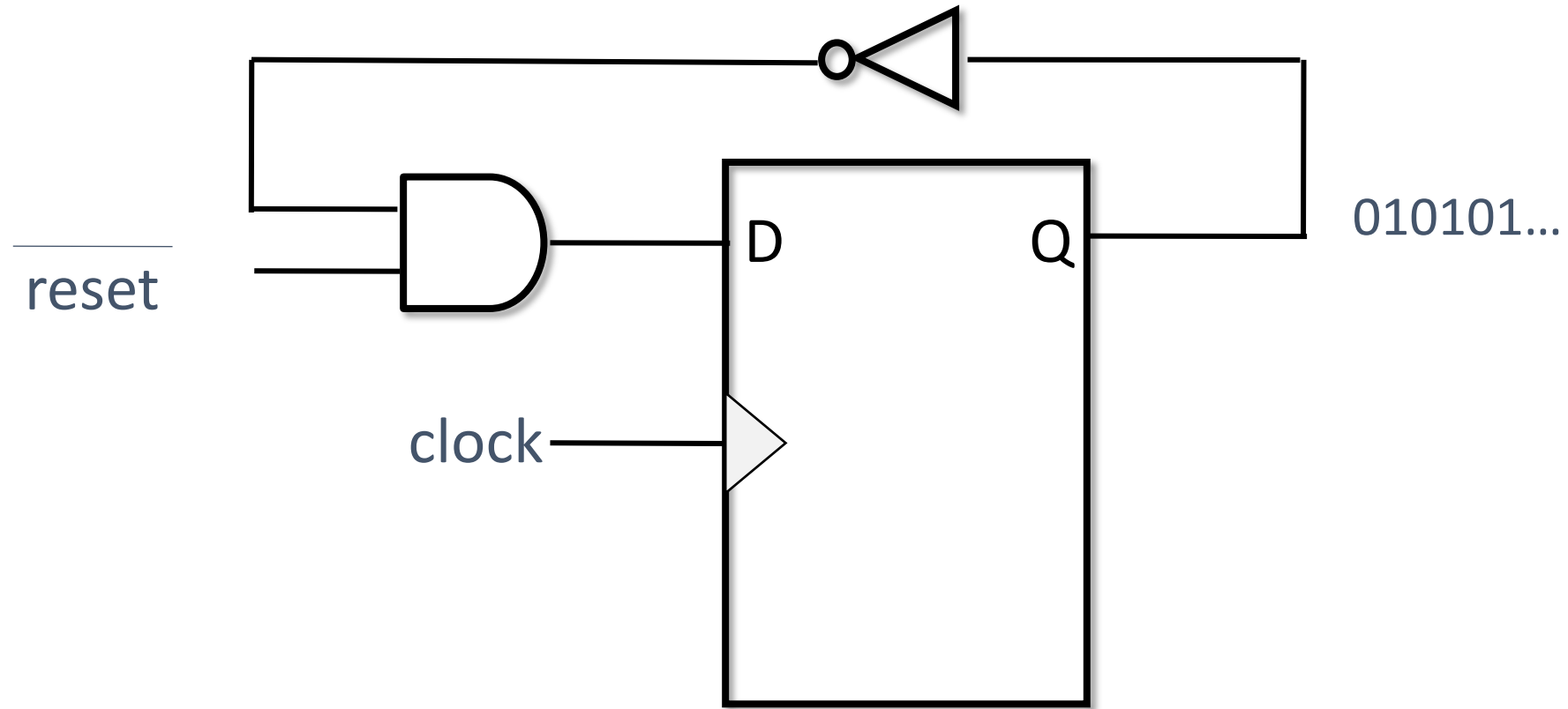


Shadow AND for labels

Conservative.

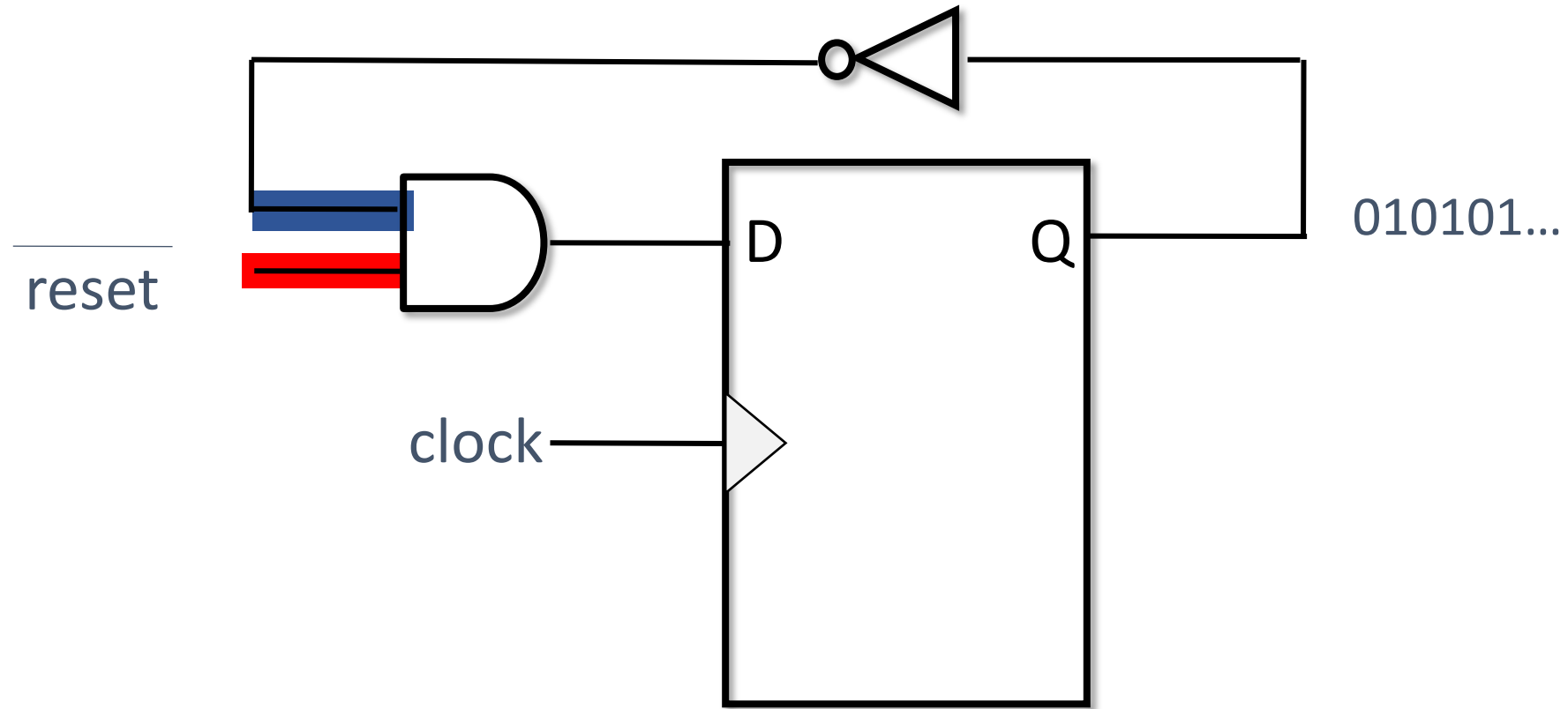
If one of a and b is tainted, the output is tainted.

Motivation: Require Precise Information Flow



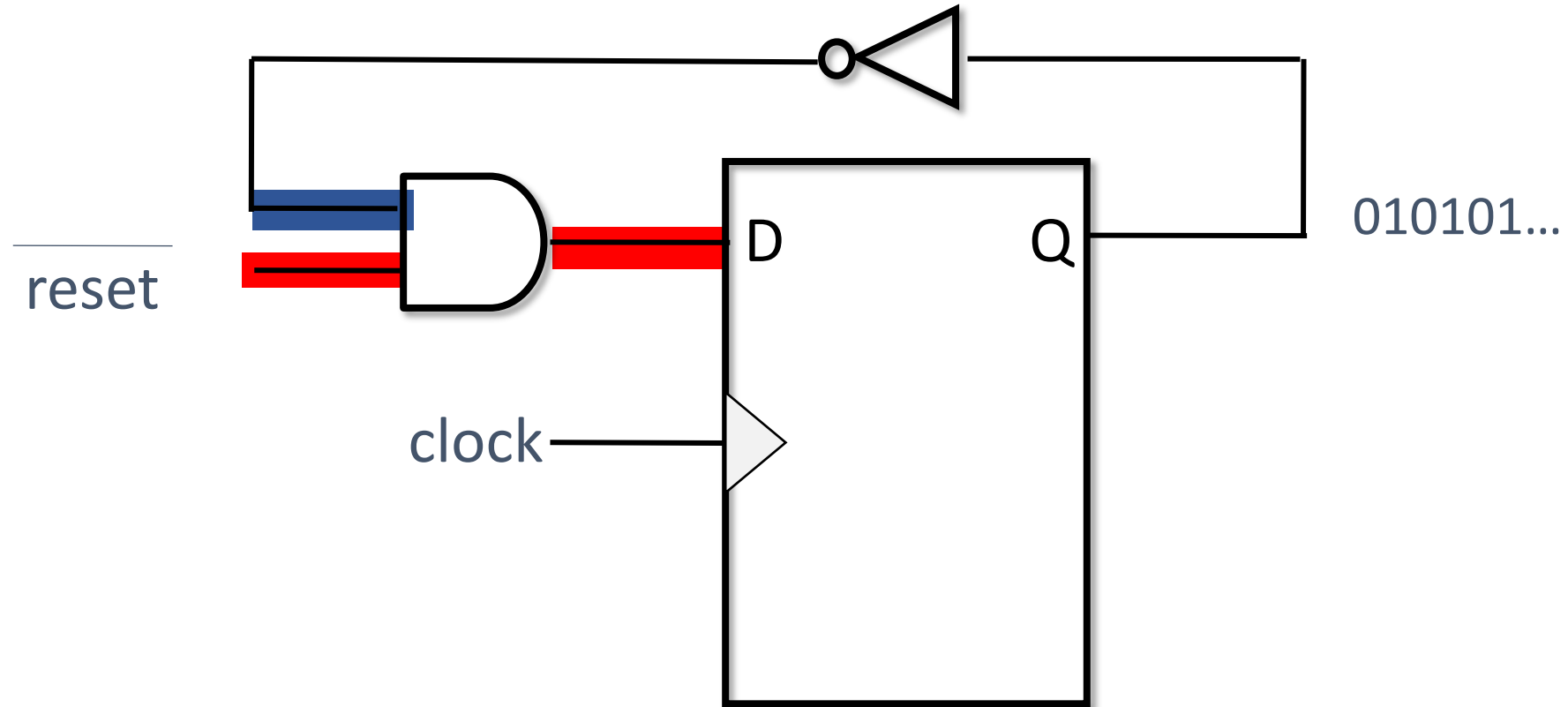
- Conventional OR-ing of labels *monotonic*

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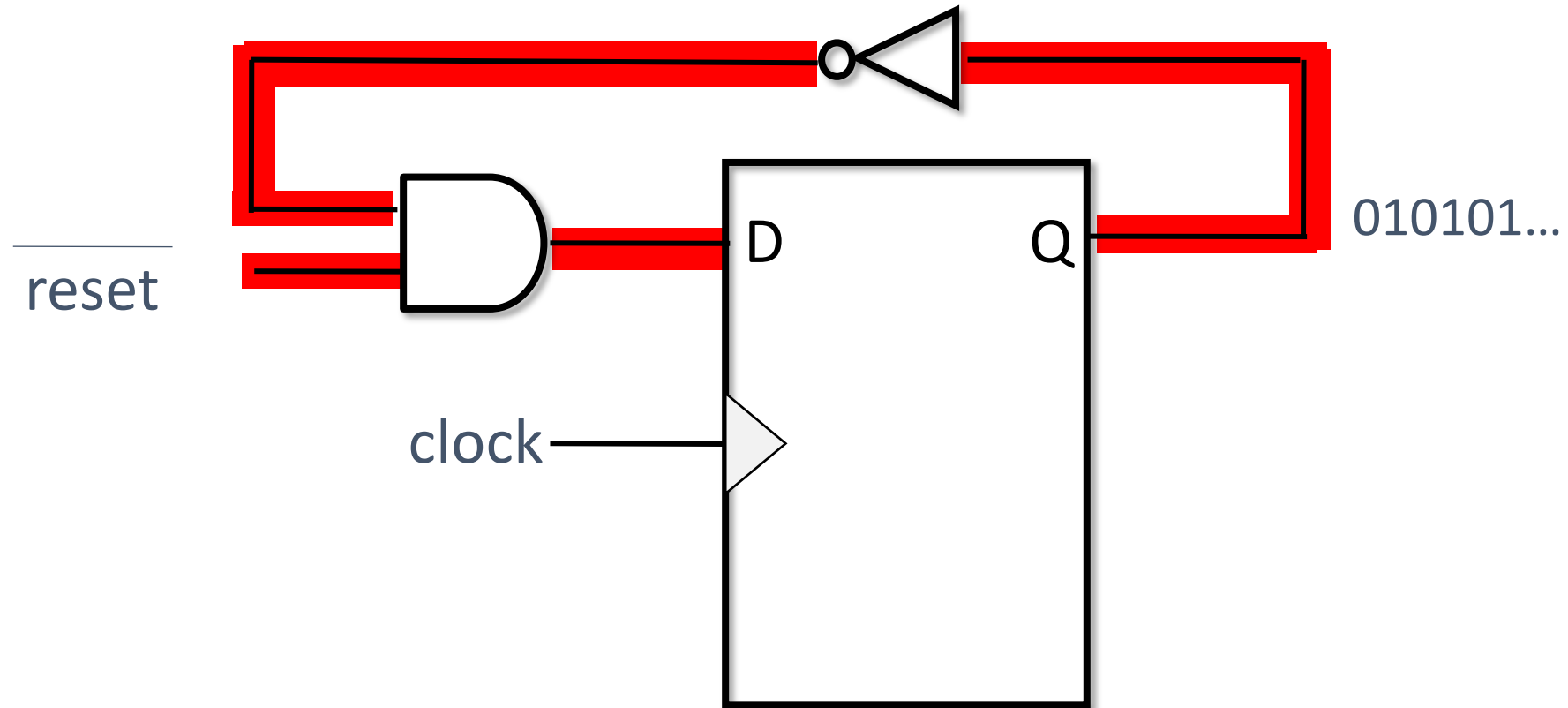
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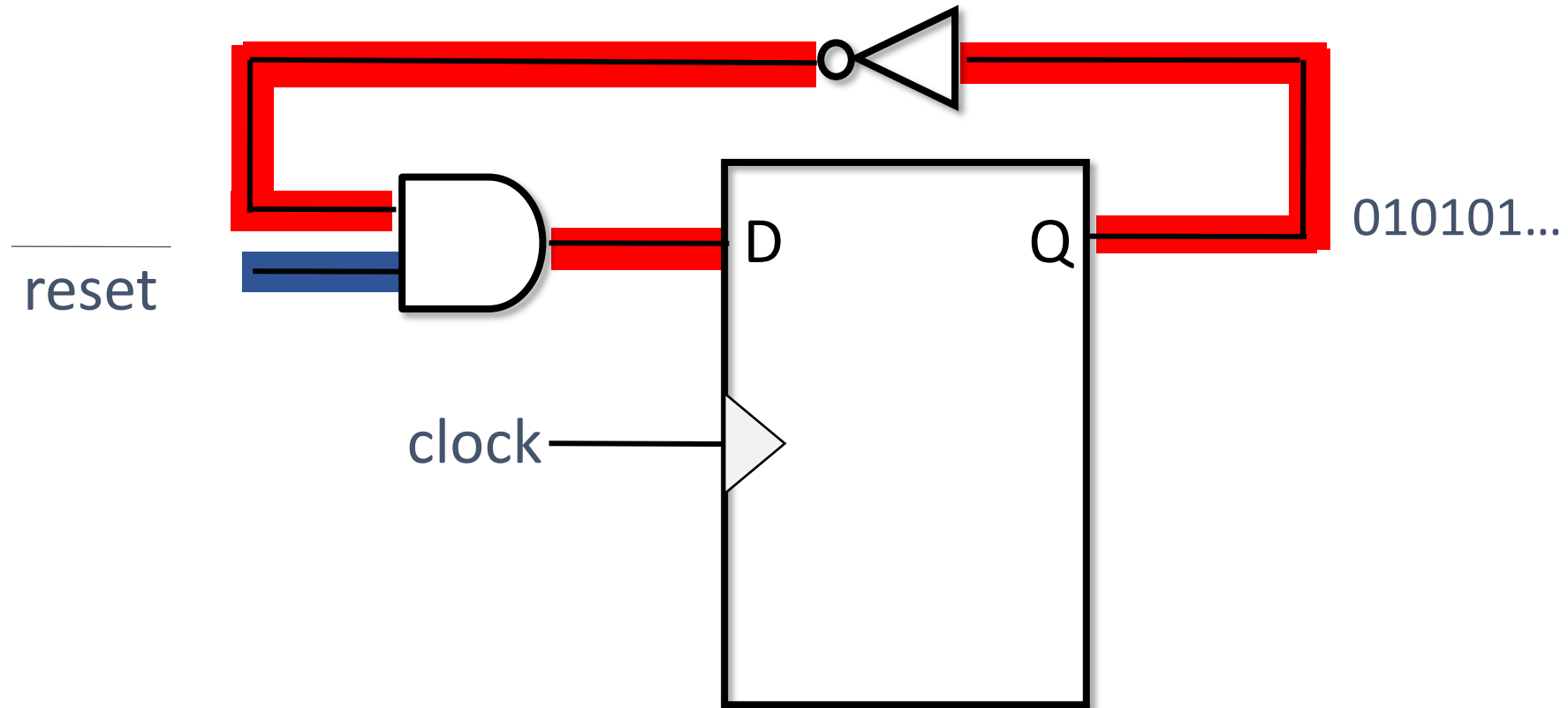
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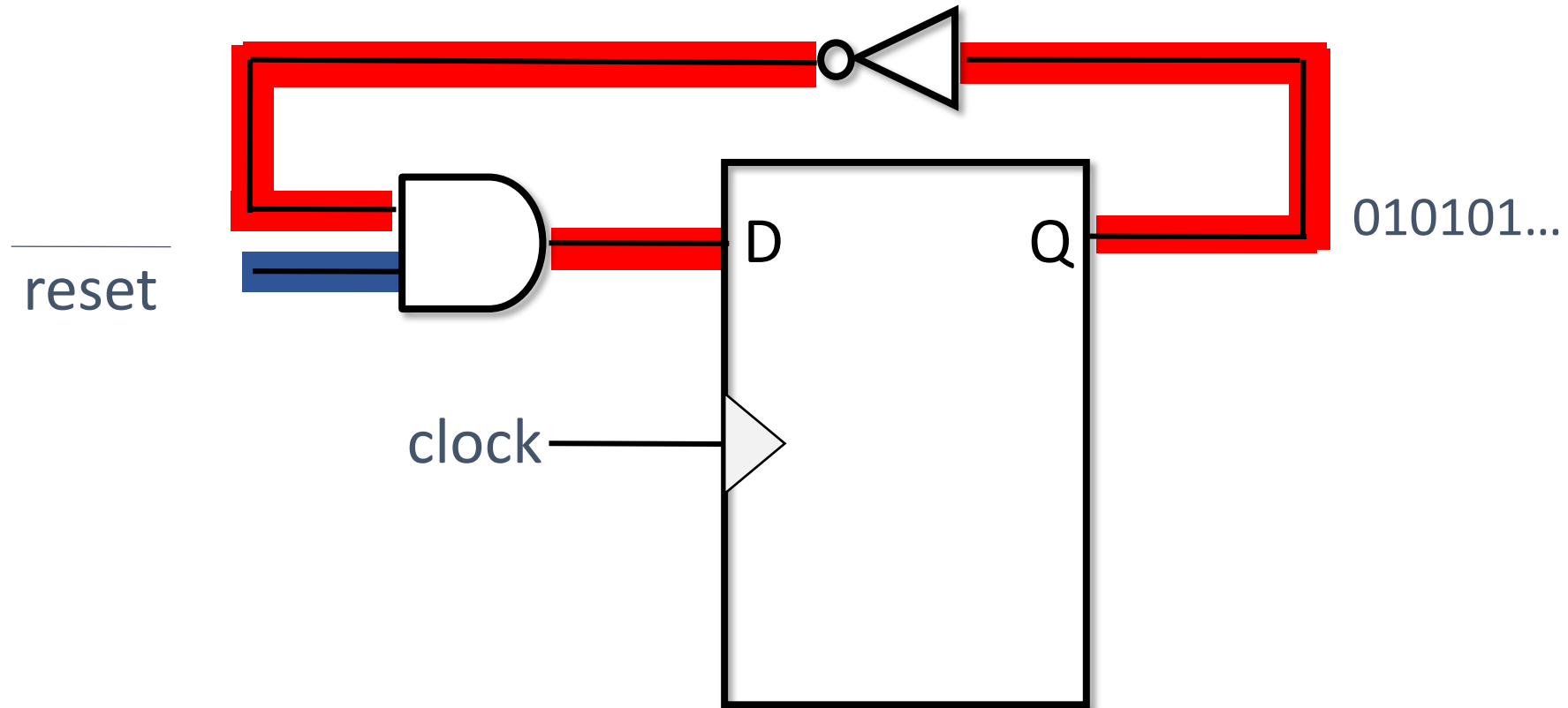
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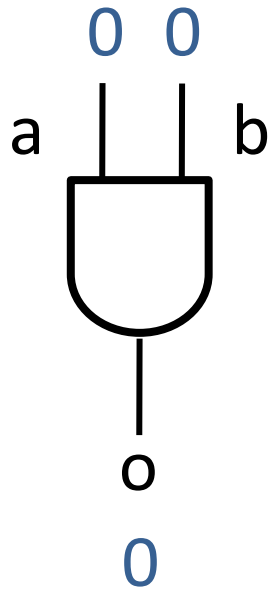
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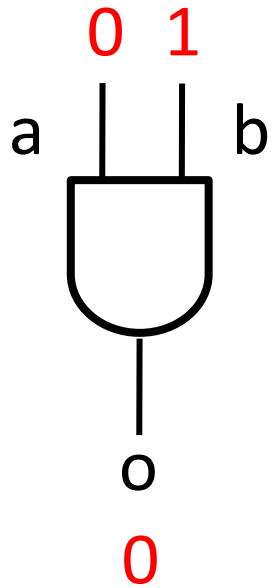
Precise Information Flow: AND Gate



untainted tainted

	a	b	o
untainted	0	0	0
tainted			
untainted			
tainted			
untainted			
tainted			
untainted			
tainted			

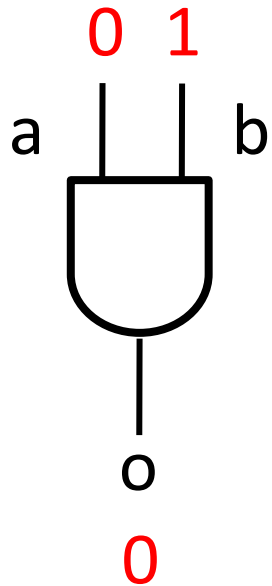
Precise Information Flow: AND Gate



untainted tainted

	a	b	o
untainted	0	0	0
tainted	0	1	0
untainted			
tainted			
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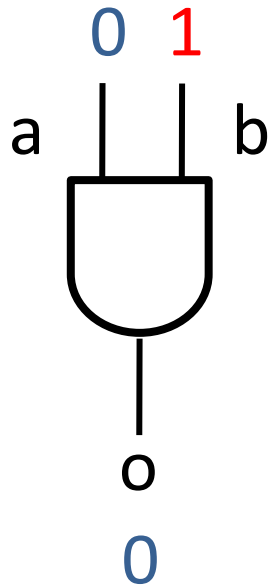
Precise Information Flow: AND Gate



	untainted	tainted	
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	0	0	0
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When $a=0$, b can not affect the value of the output.
→ no-interference

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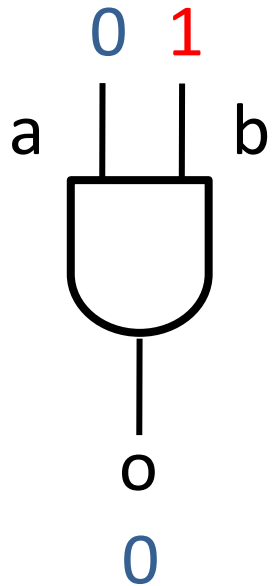


untainted tainted

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0	1	0
1	0	0
1	1	1
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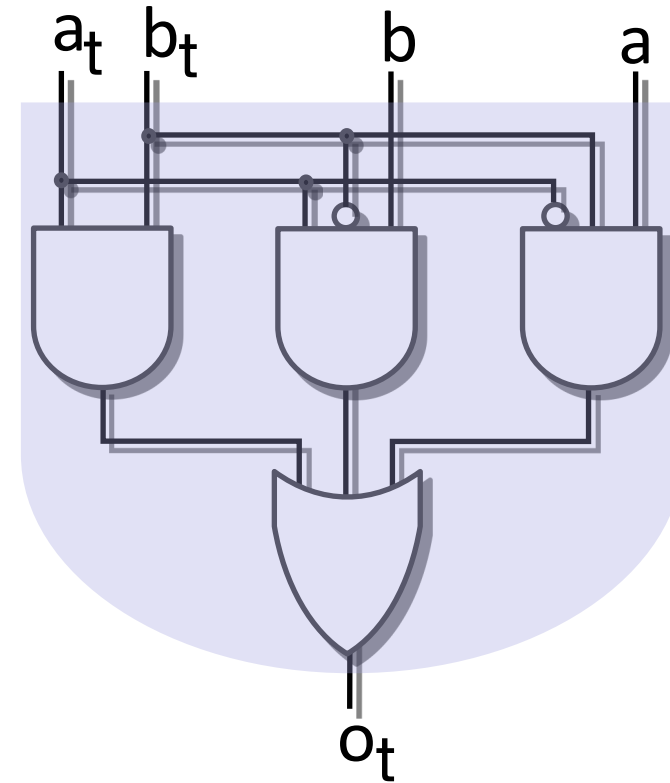
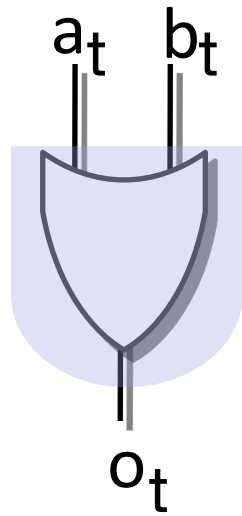
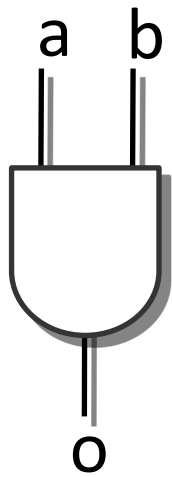


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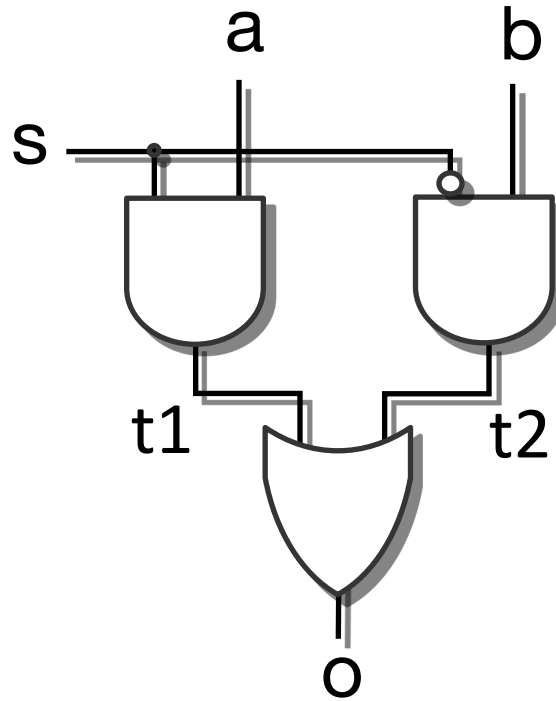
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Use both inputs and input labels

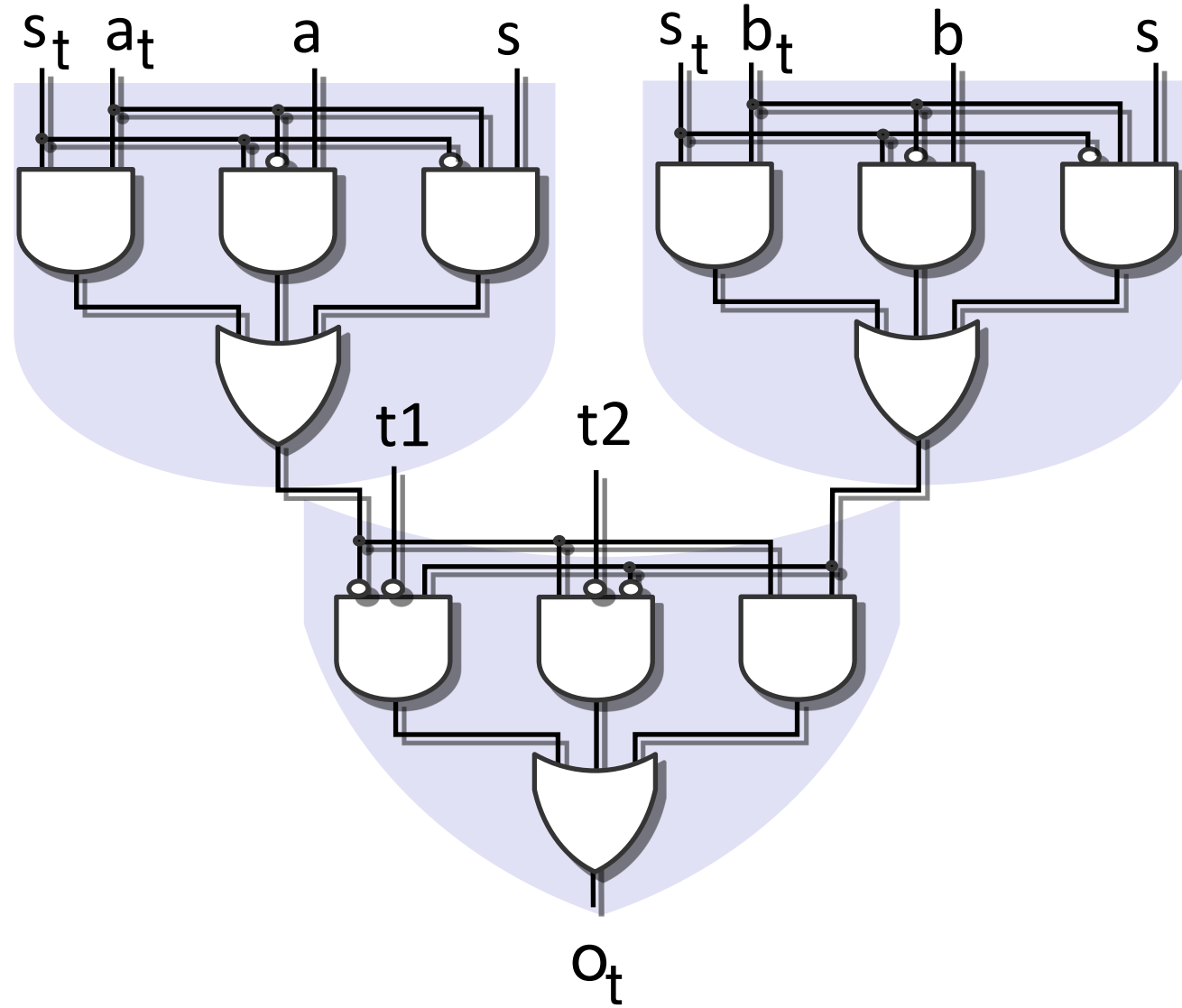
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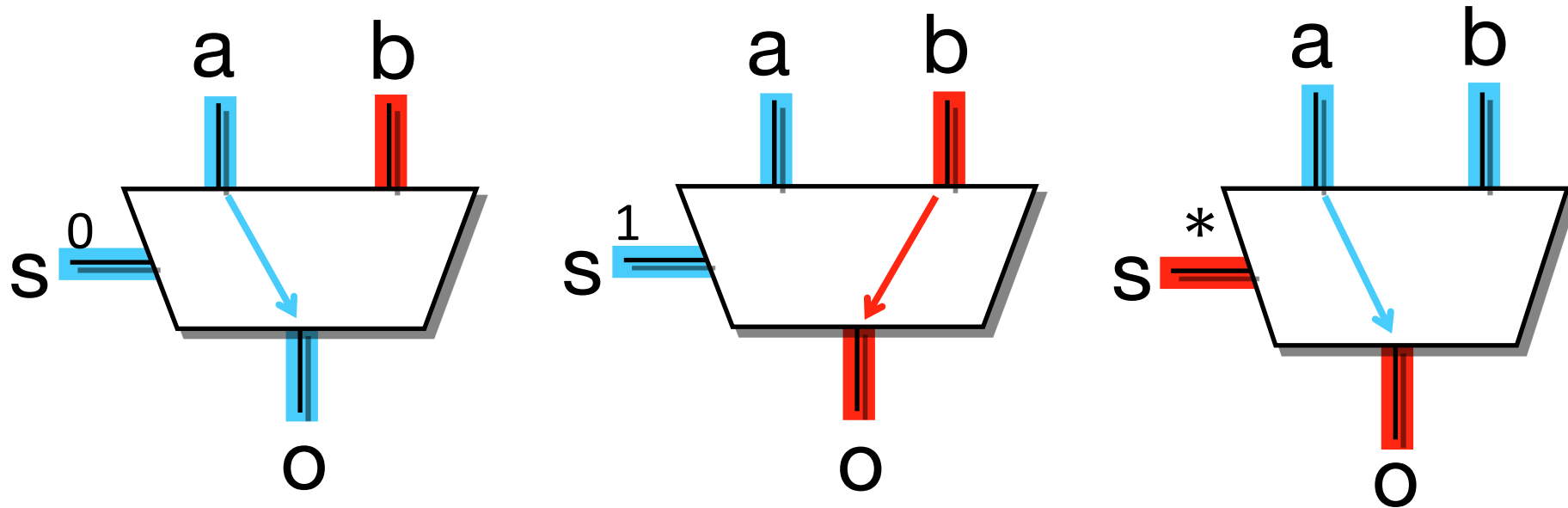
Sound Composition of Shadow Logic



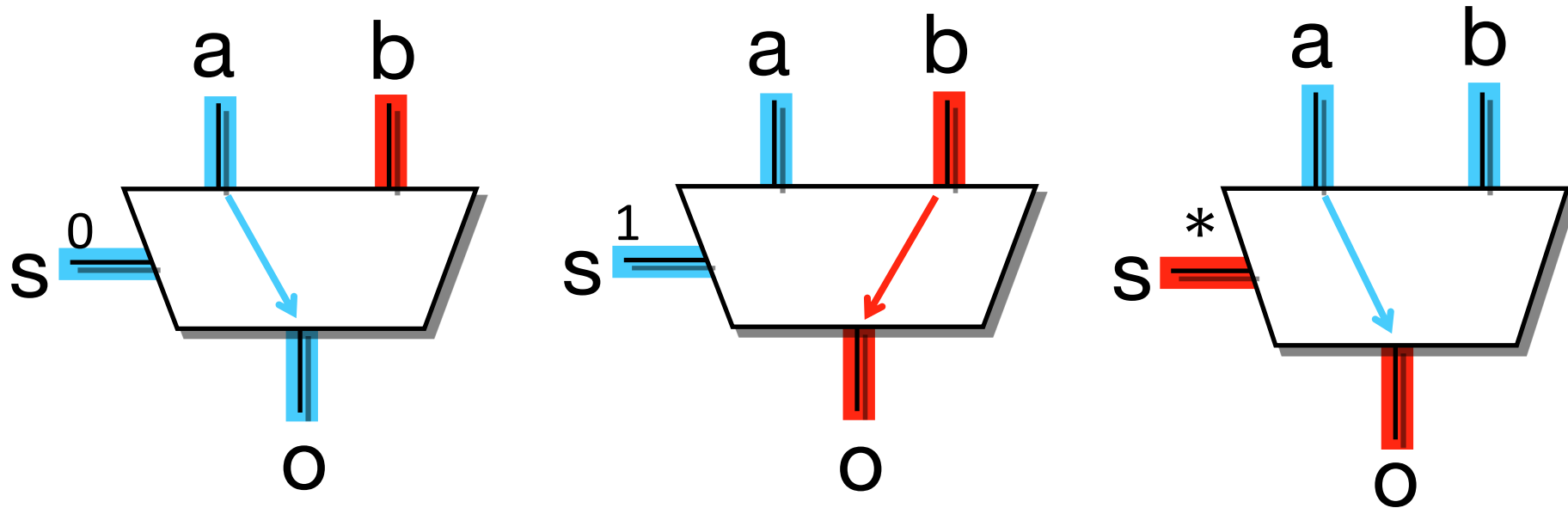
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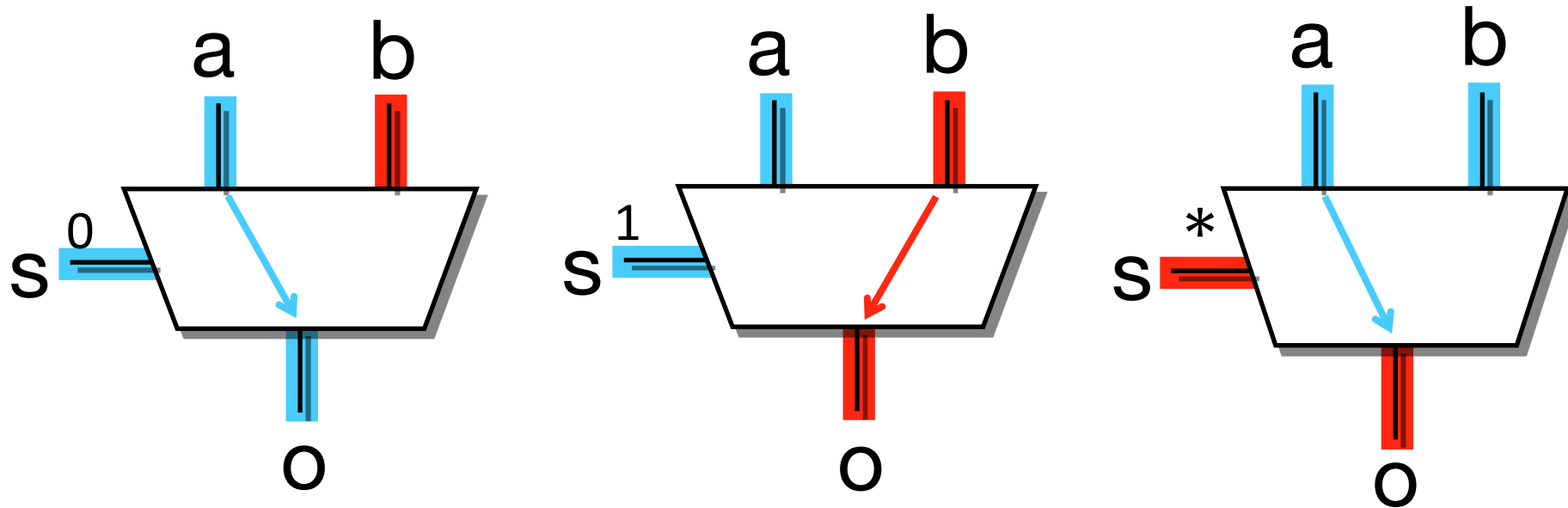
MUX: Gatekeeper of trust



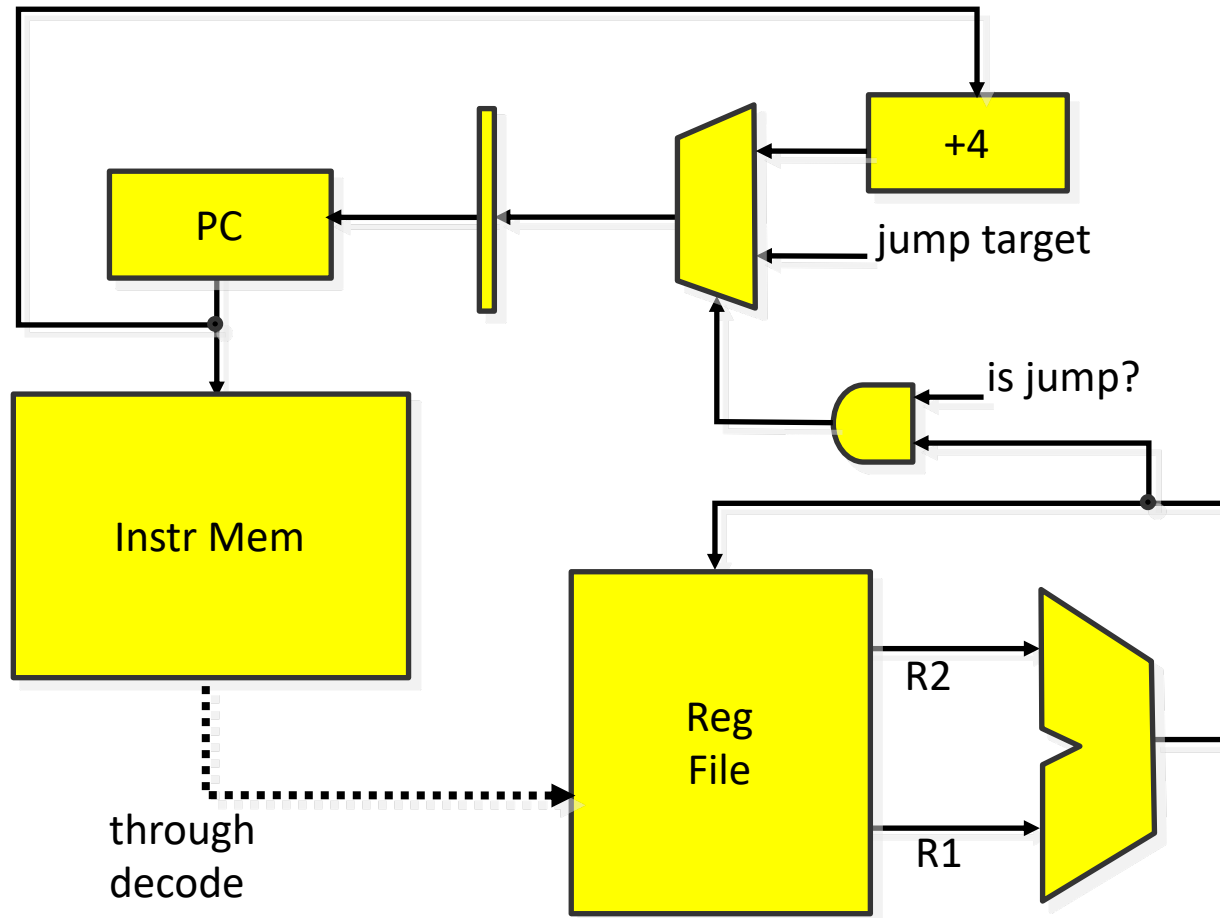
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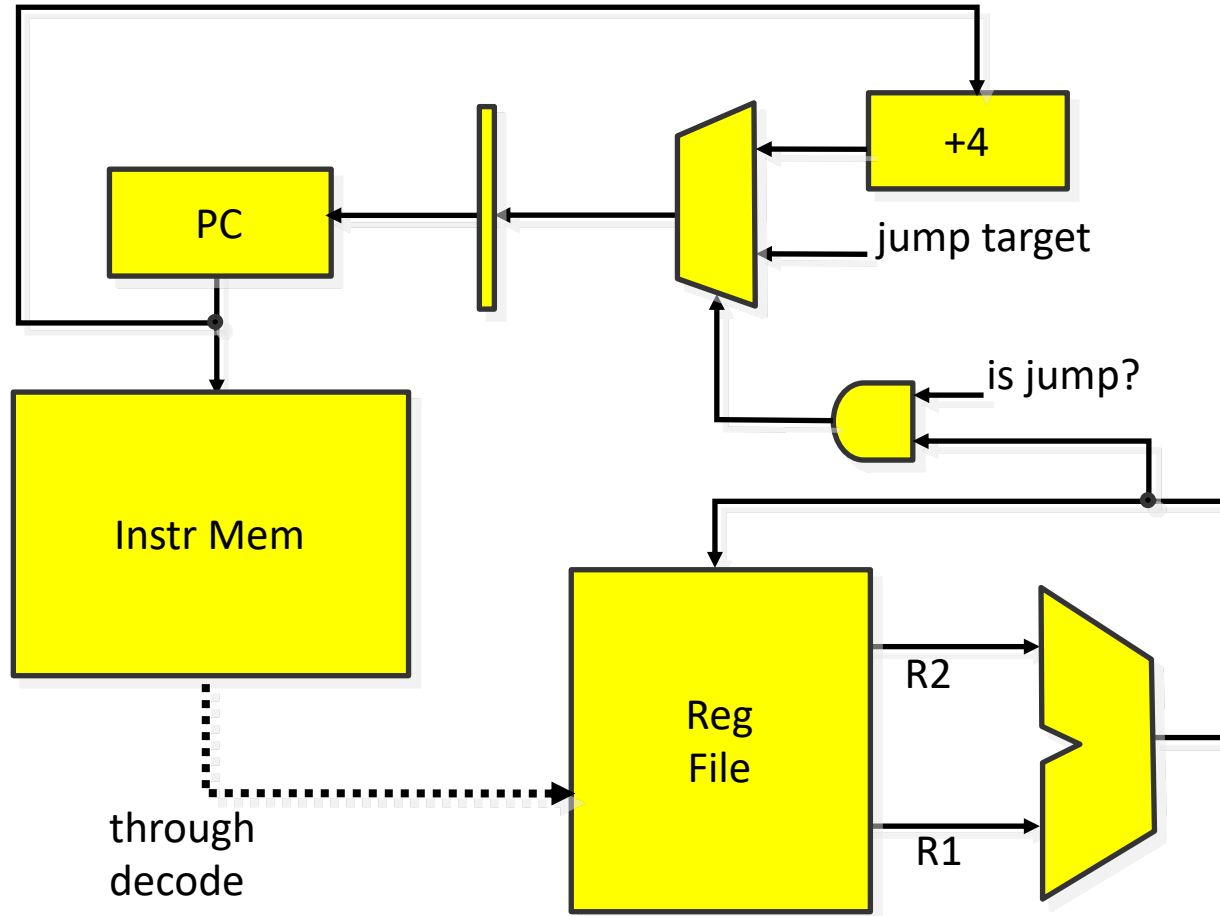
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Implicit Information Flows: Taint Explosion

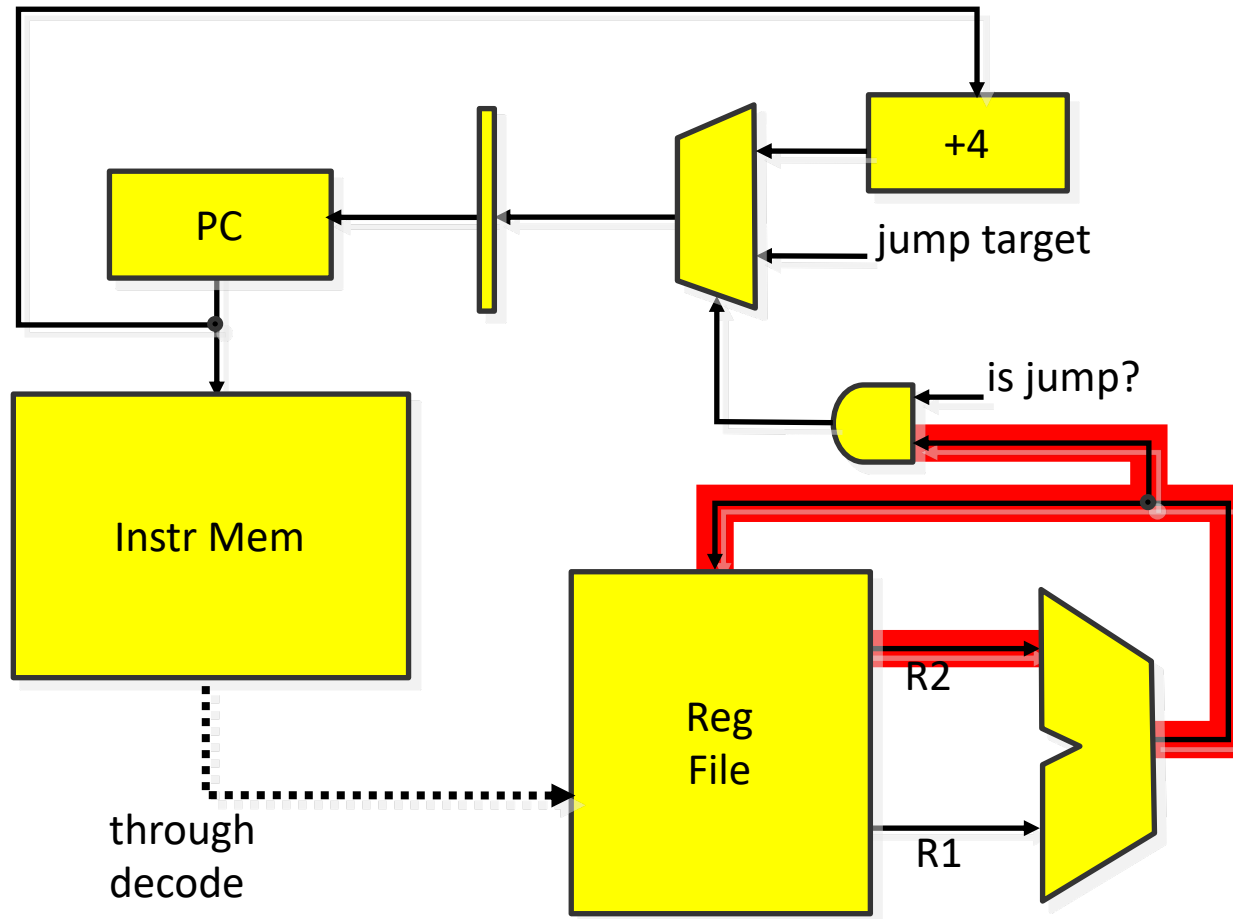


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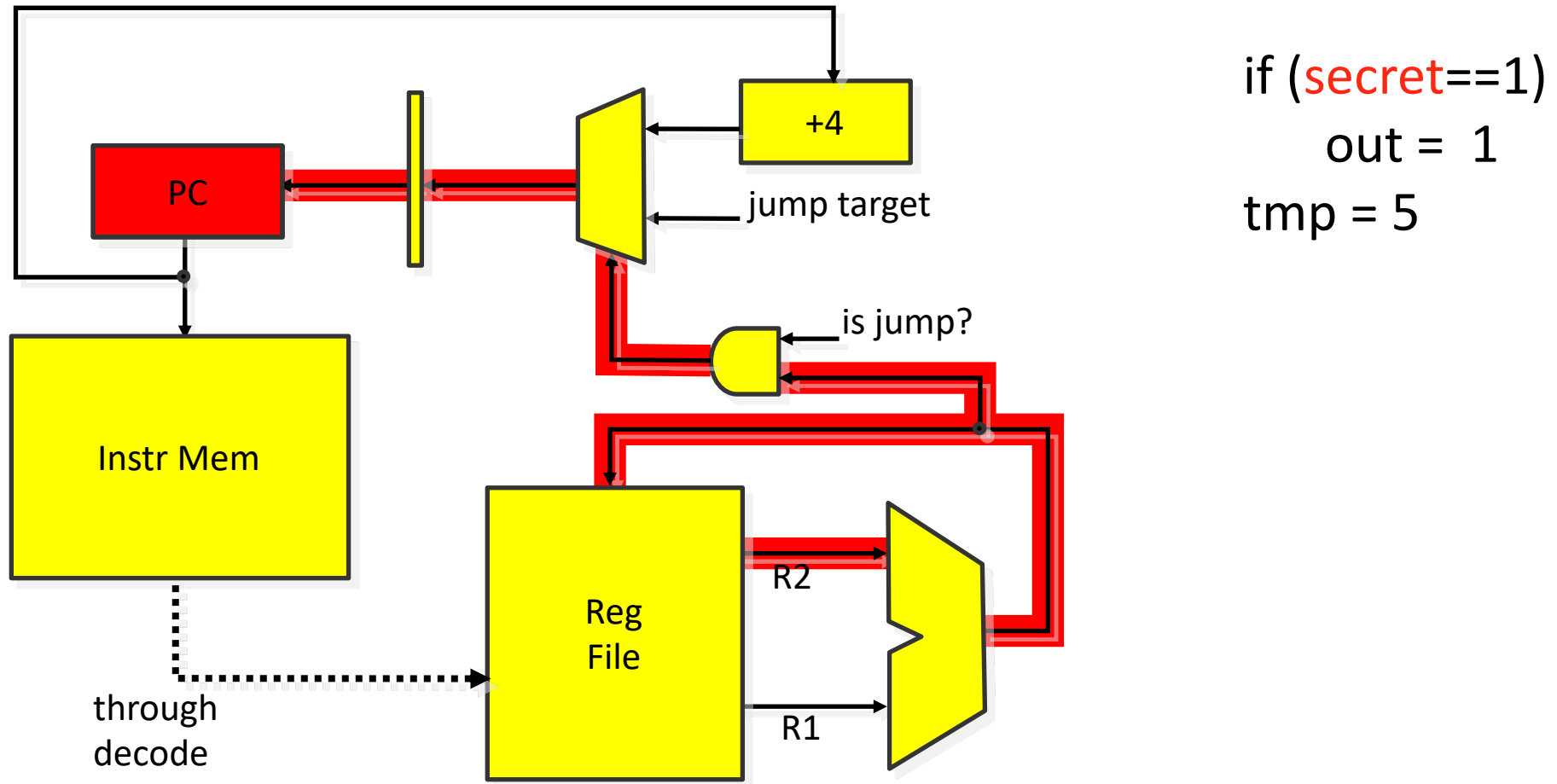
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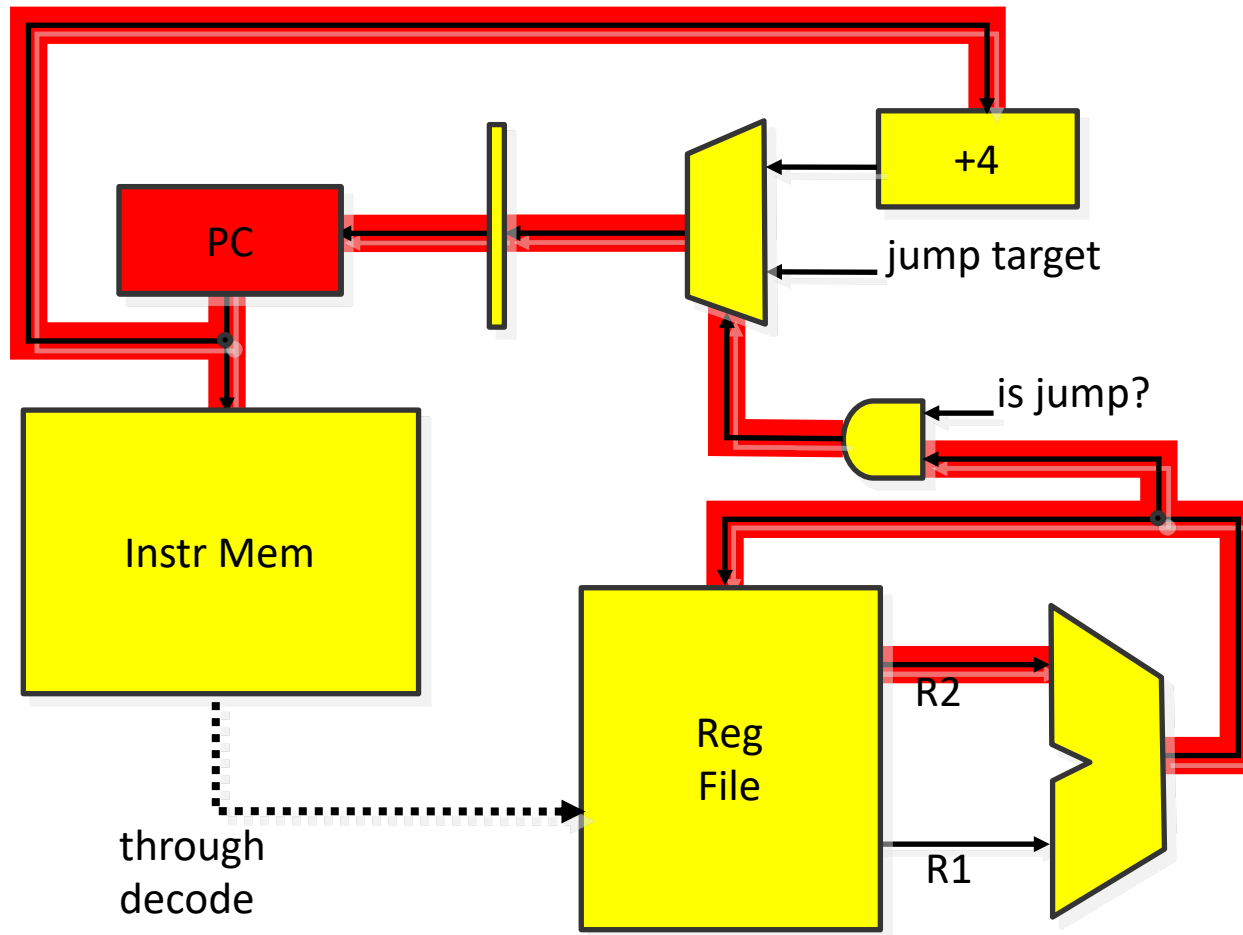
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Conditional execution taints critical state (PC)

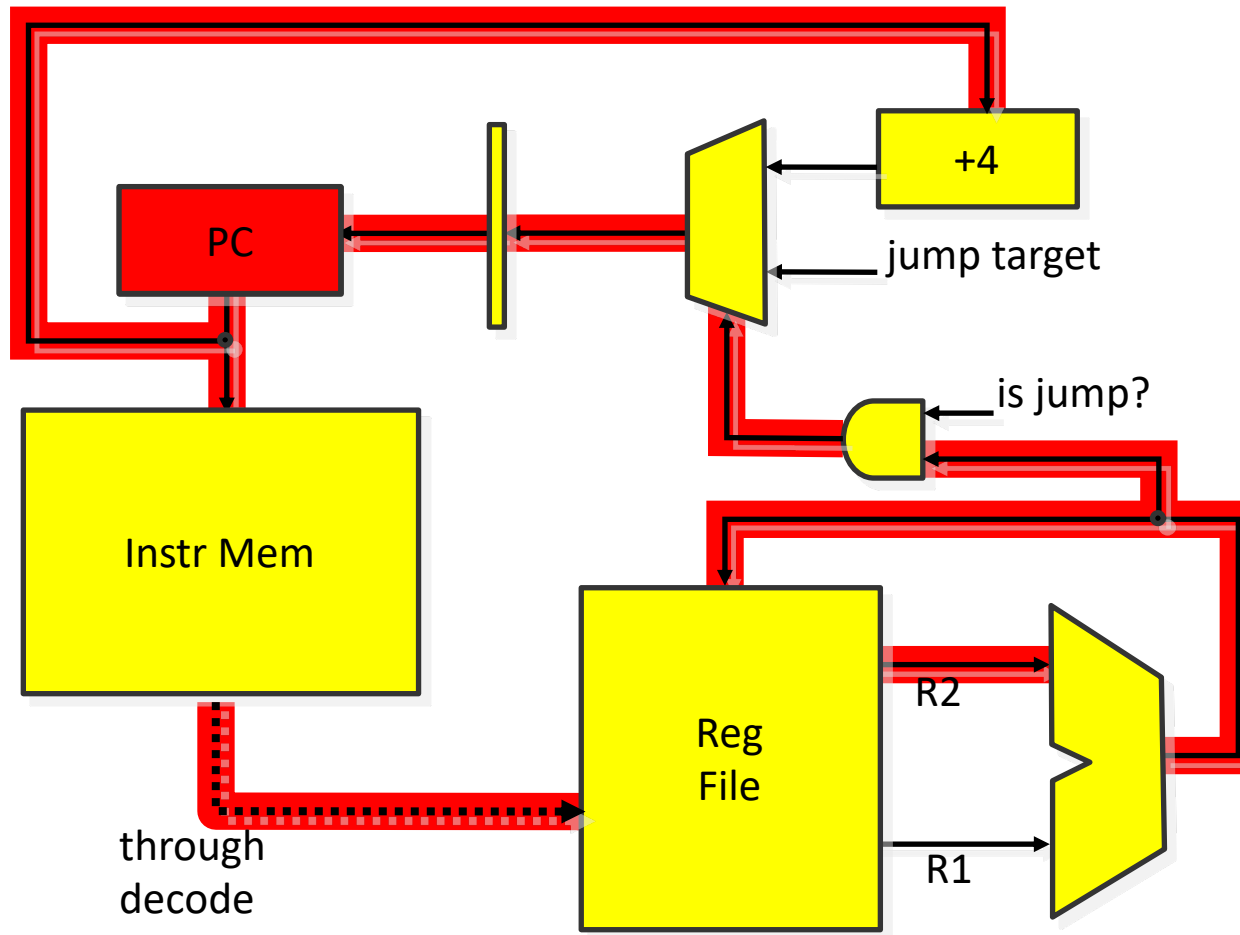
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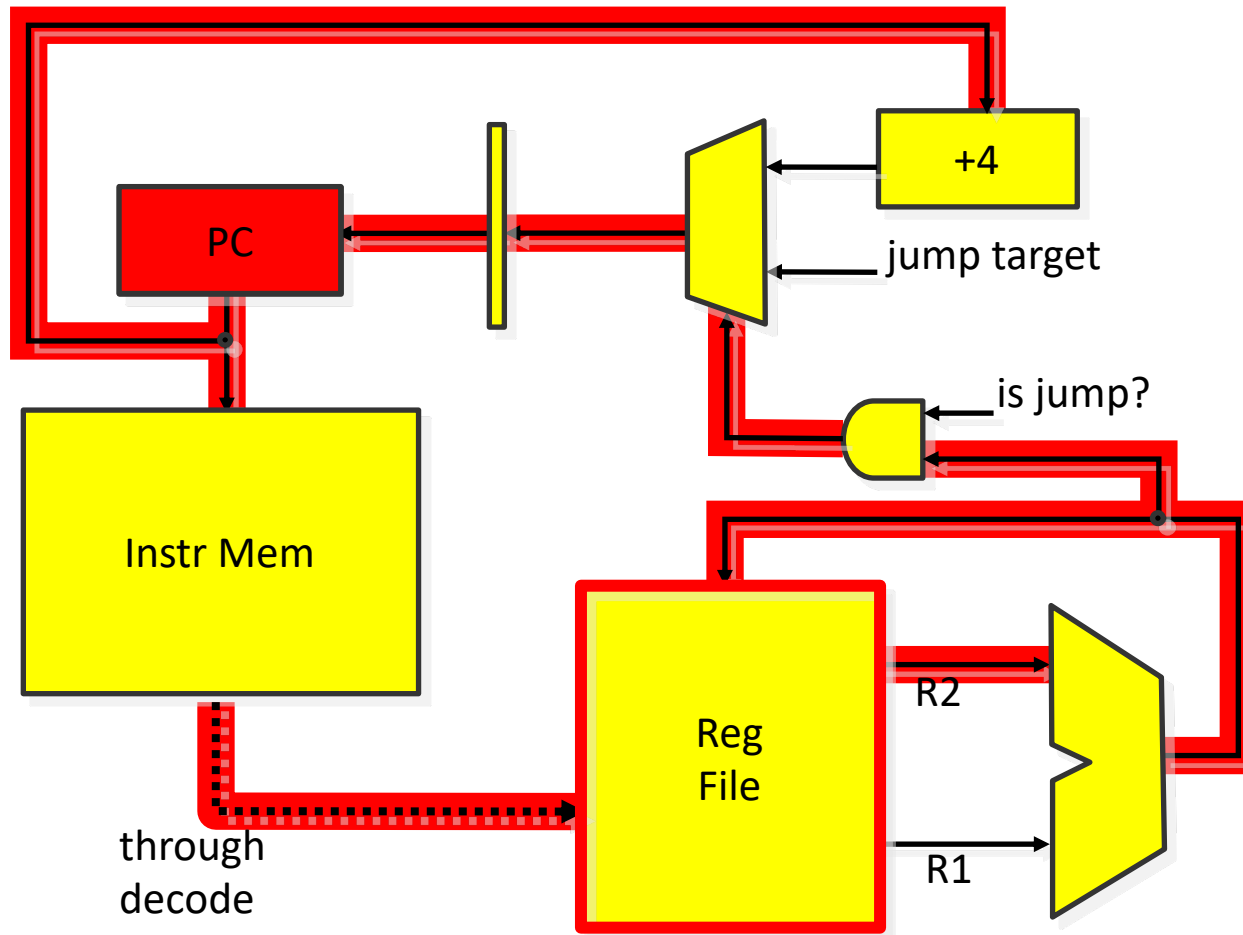
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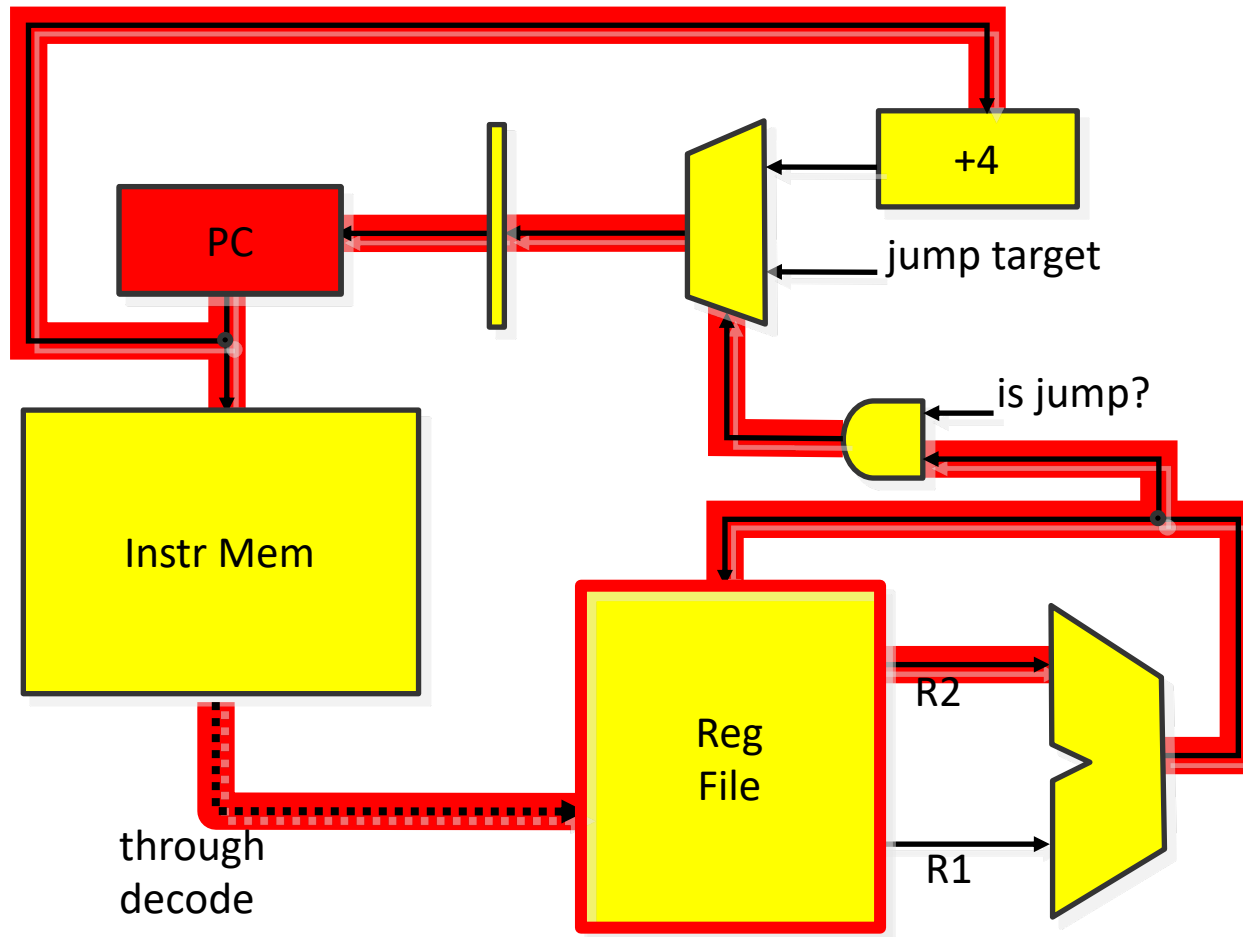
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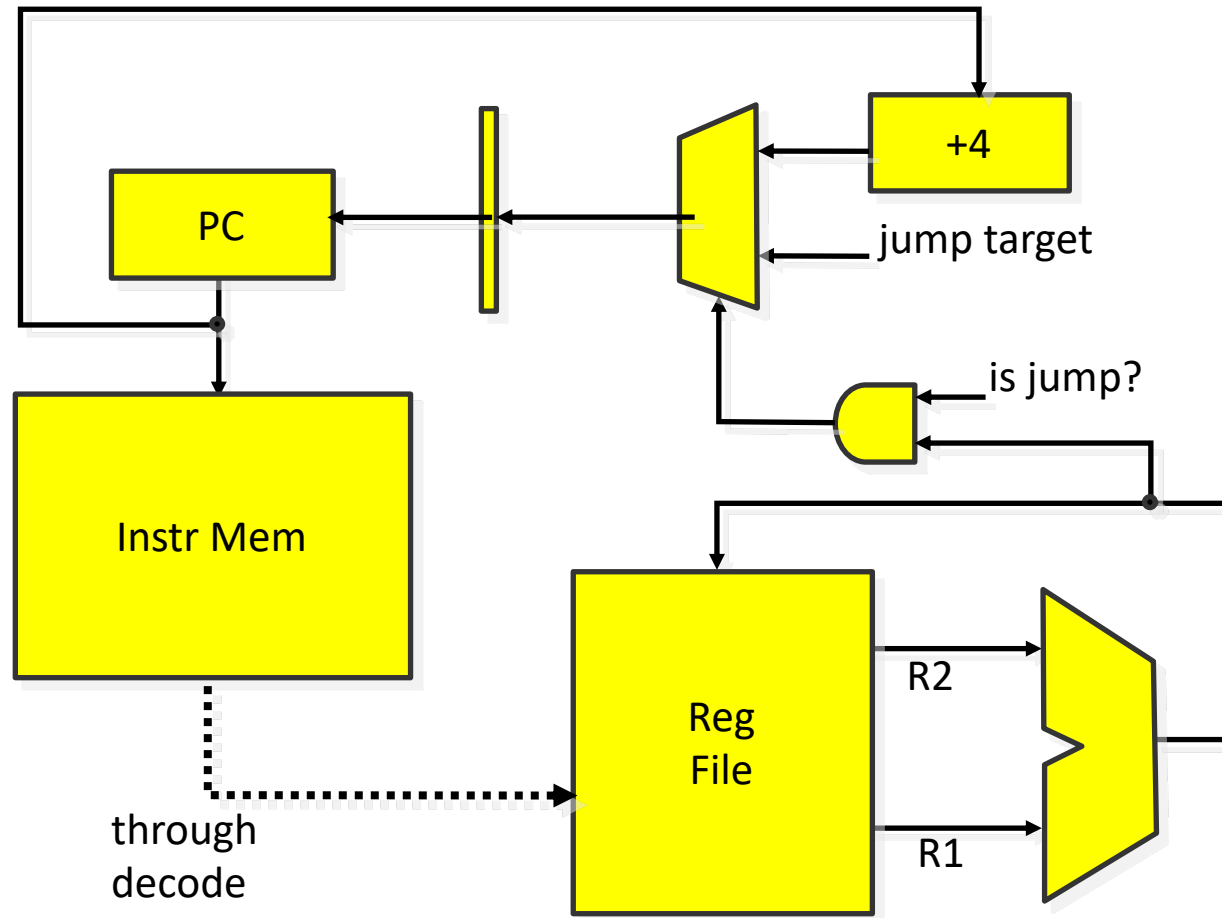
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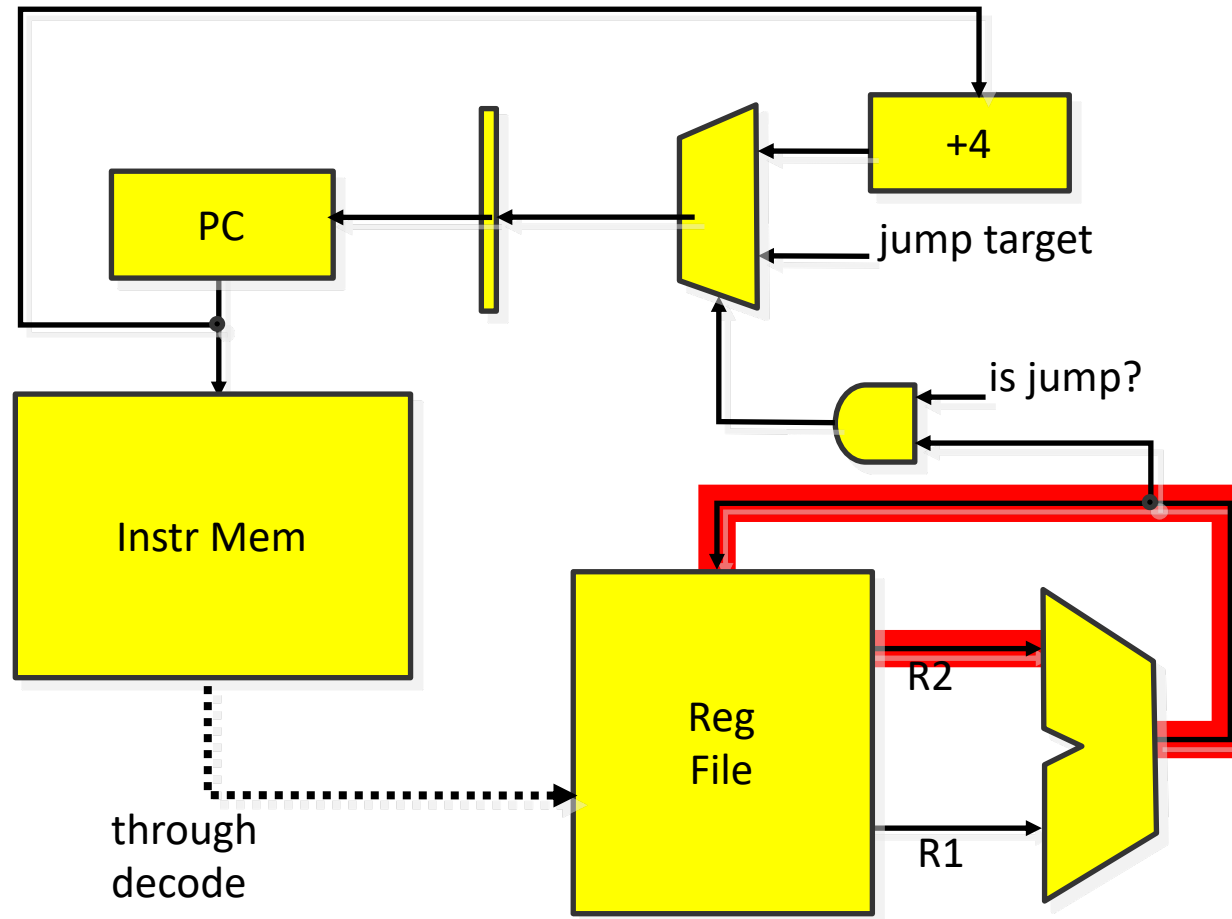
Convert Implicit Flow to Explicit Flow



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if (secret==1)
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P0 = secret
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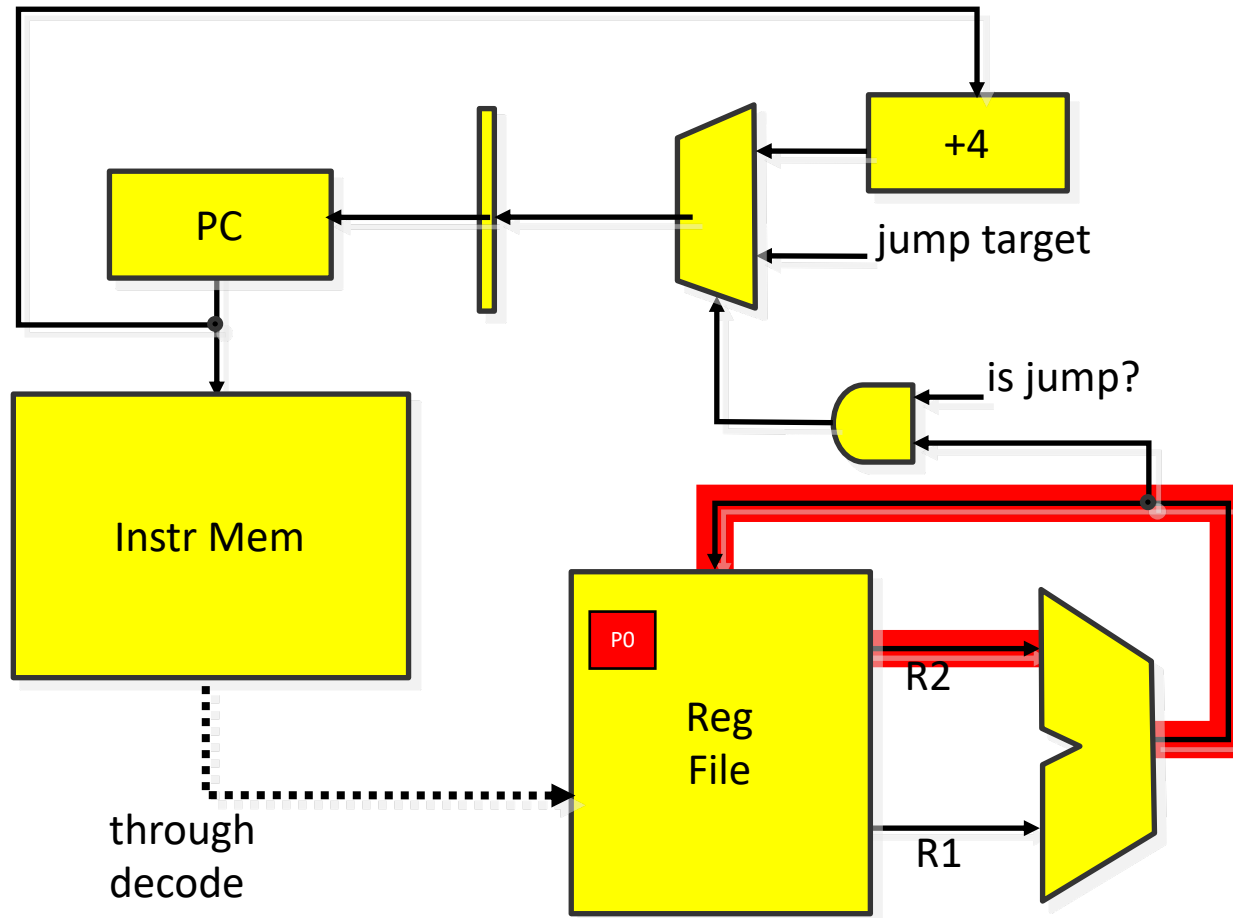
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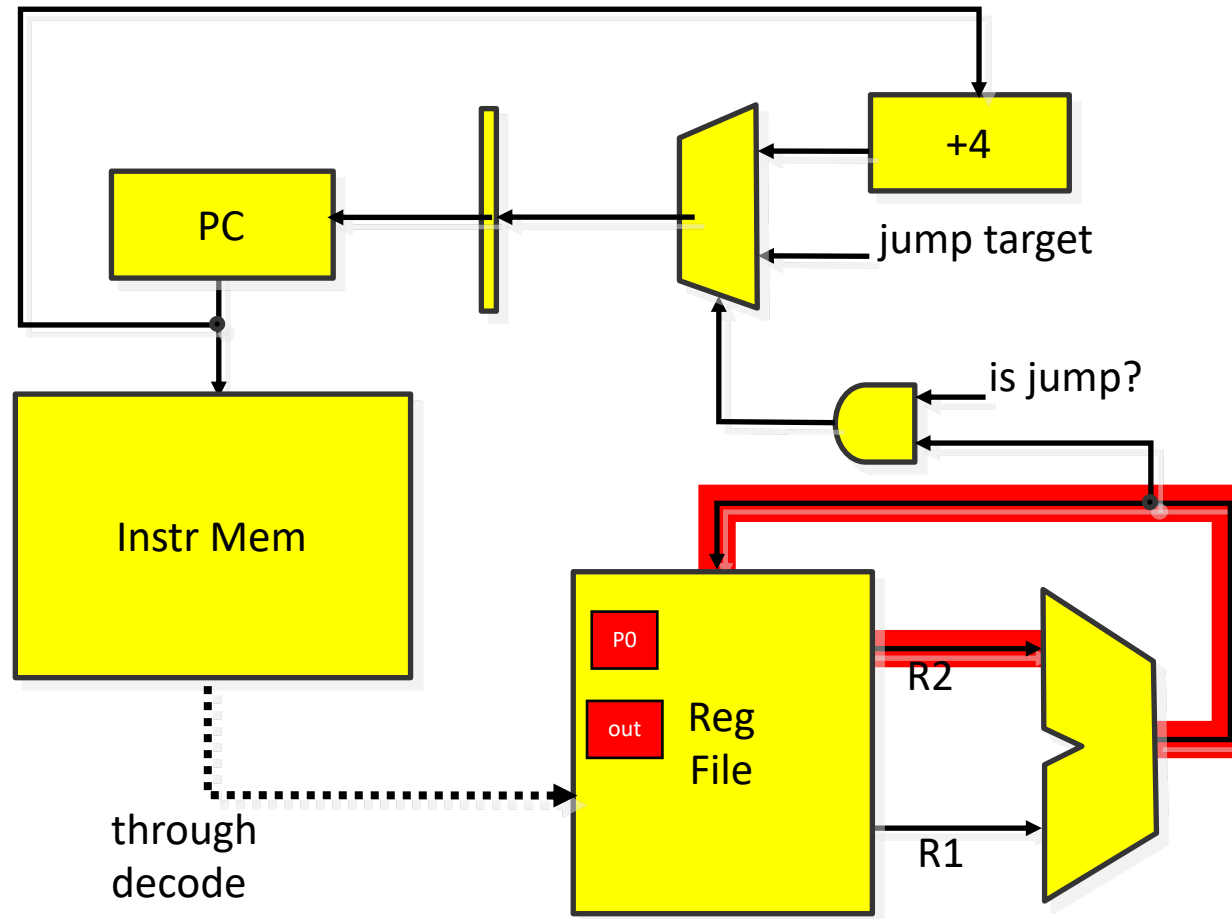
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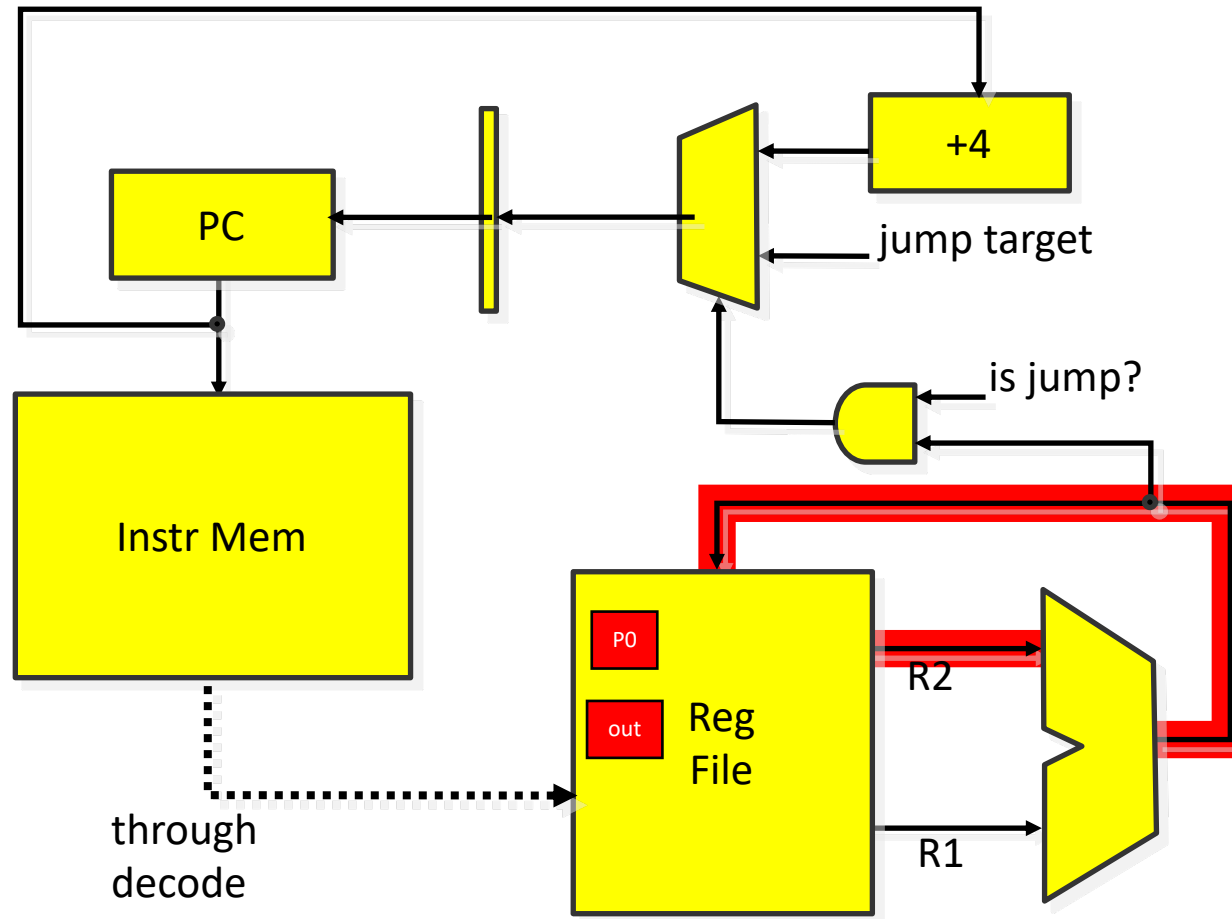
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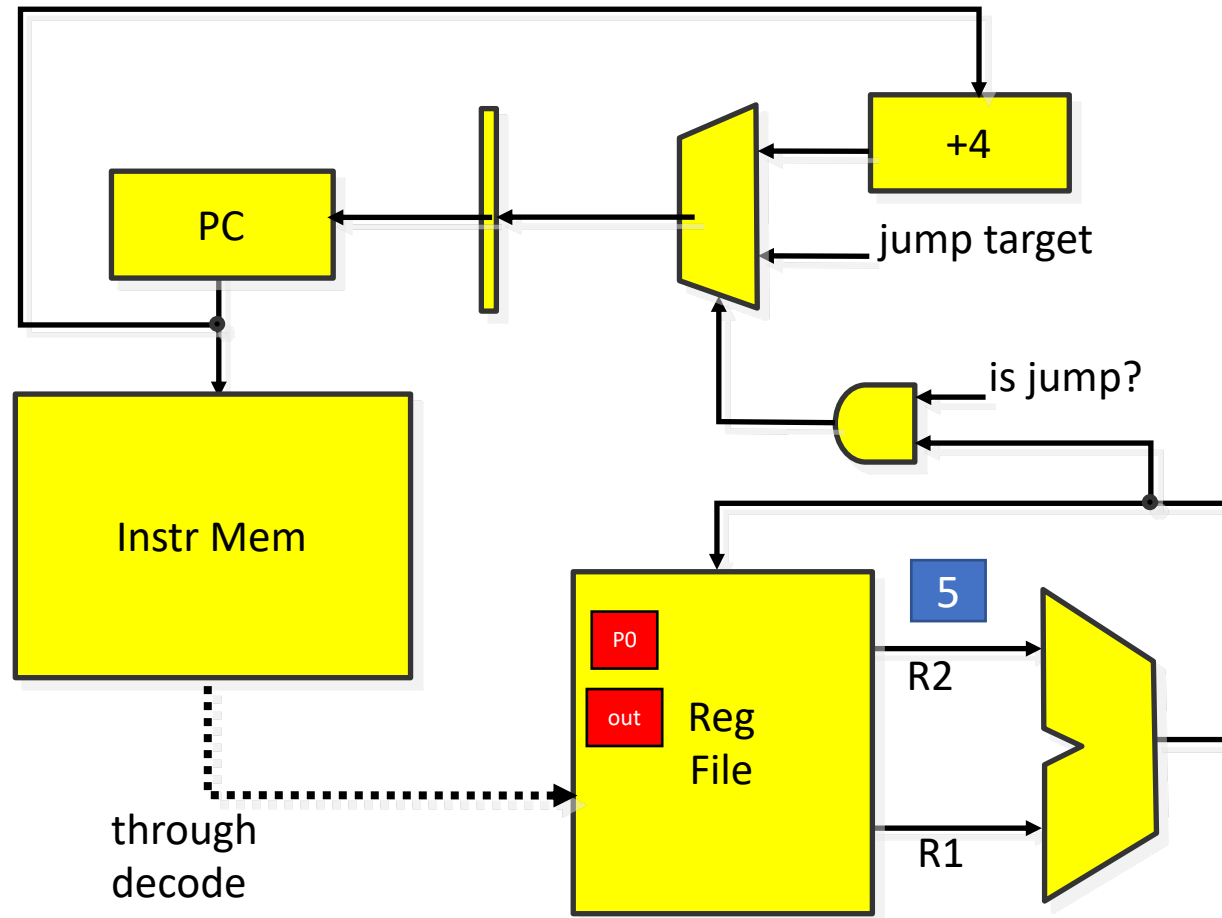
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P0 = secret
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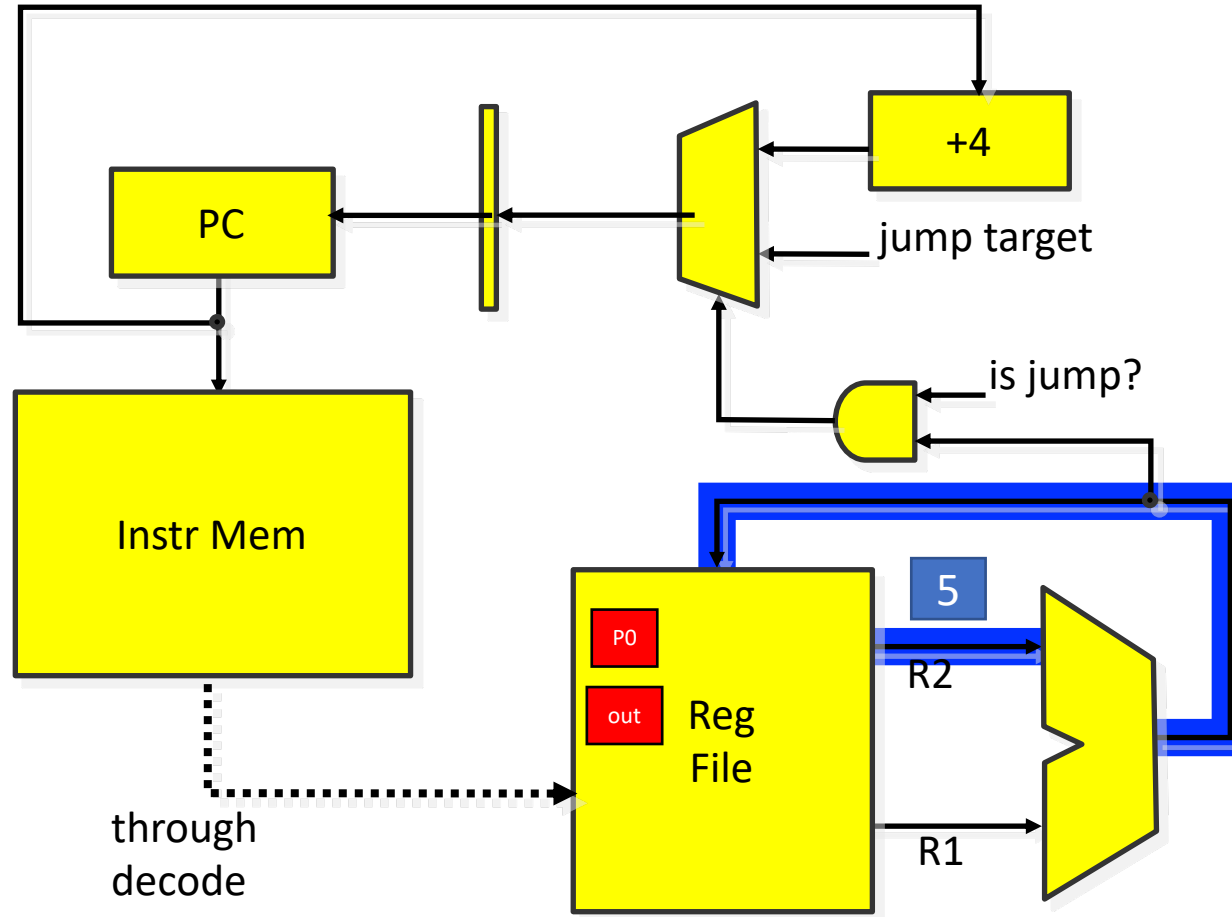
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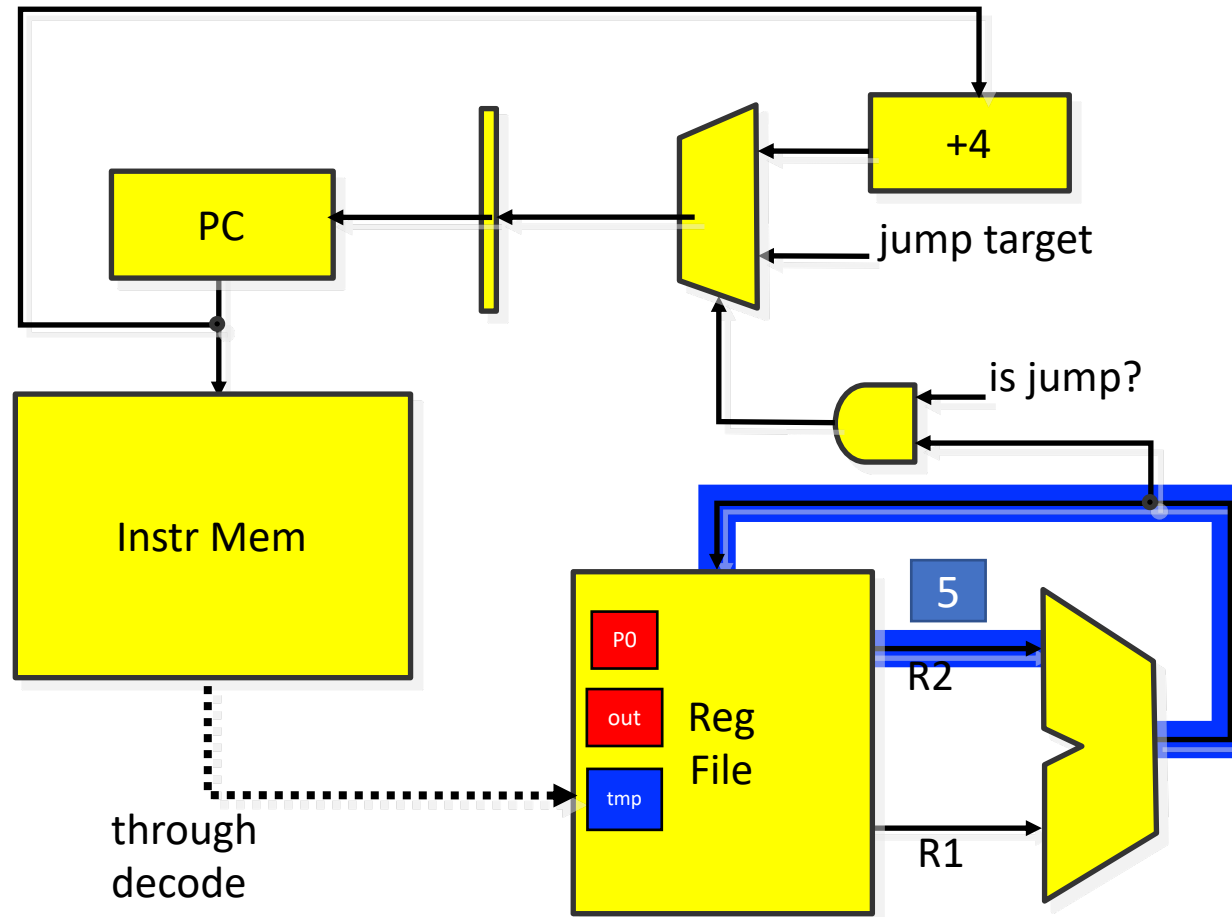

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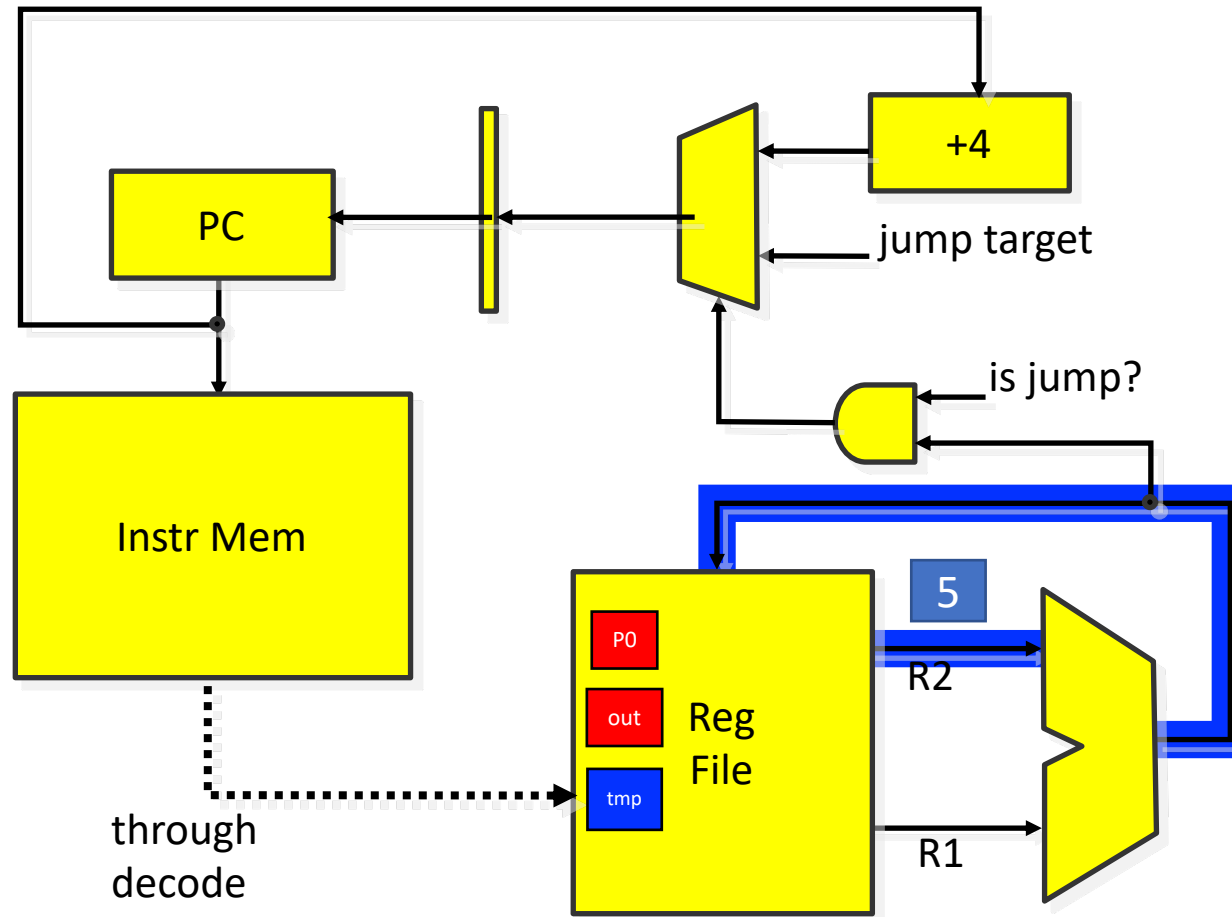
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- Recommend to read their follow-on work:
 - *Execution Leases: A Hardware-Supported Mechanism for Enforcing Strong Non-Interference*; Tiwari et al.; MICRO'09

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Appropriate use cases:

- When critical or sensitive operations need to be performed, a *co-processor* augmented with these abilities could be an attractive option.

Discussion Questions

Discussion Questions on Taint Tracking

- Who designates an input as untrusted/trusted? Where in the architecture/implementation does an input first get marked as untrustworthy?

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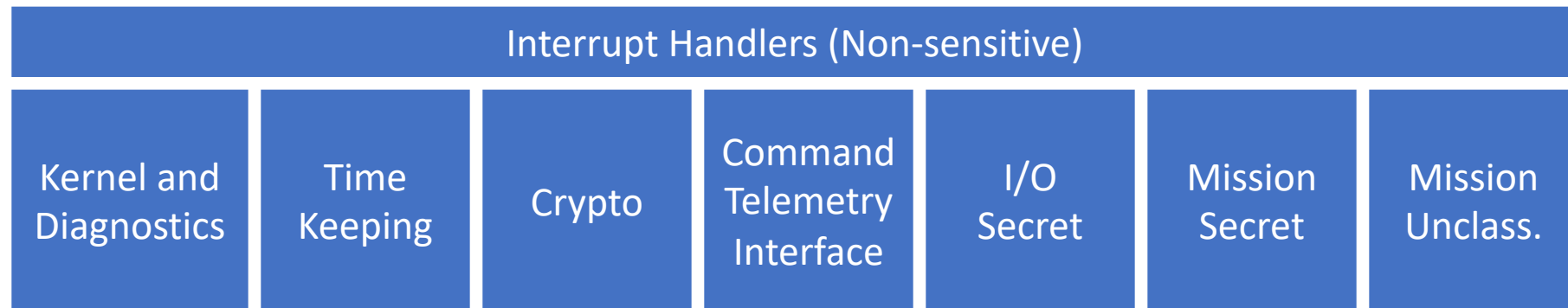
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- Can/should there be a method of promoting data from **untrusted** to **trusted**? (from **High** to **Low**)
- How does the GLIFT method handle optimizations such as out-of-order execution, speculation etc? Will the proposed architecture be able to detect covert and side channel attacks such as Meltdown and Spectre?

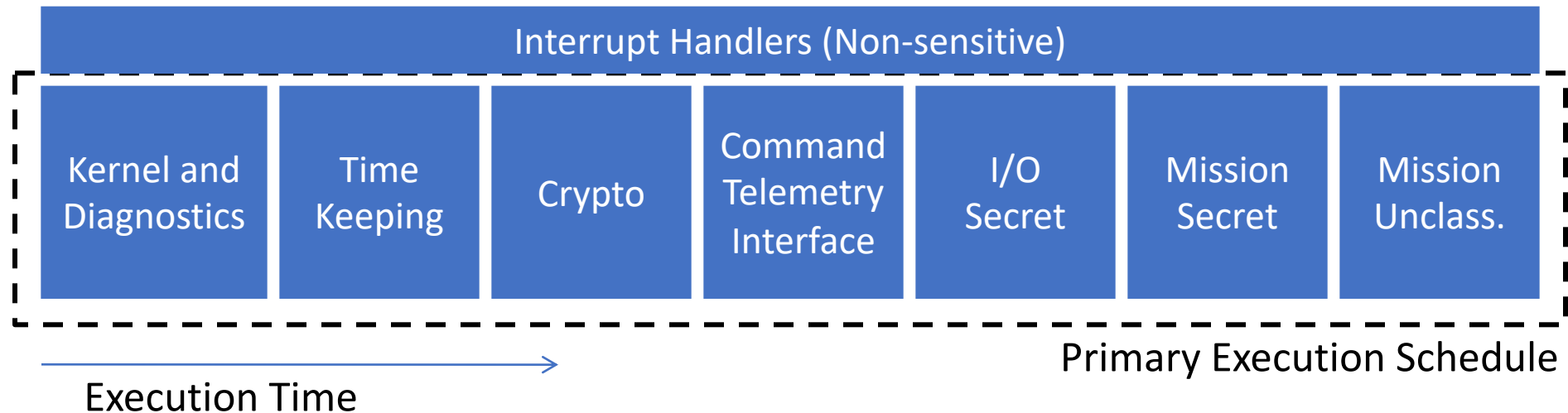
Example MLS System

Example Satellite Application. [Tzvetan Metodi, Aerospace Corp.]



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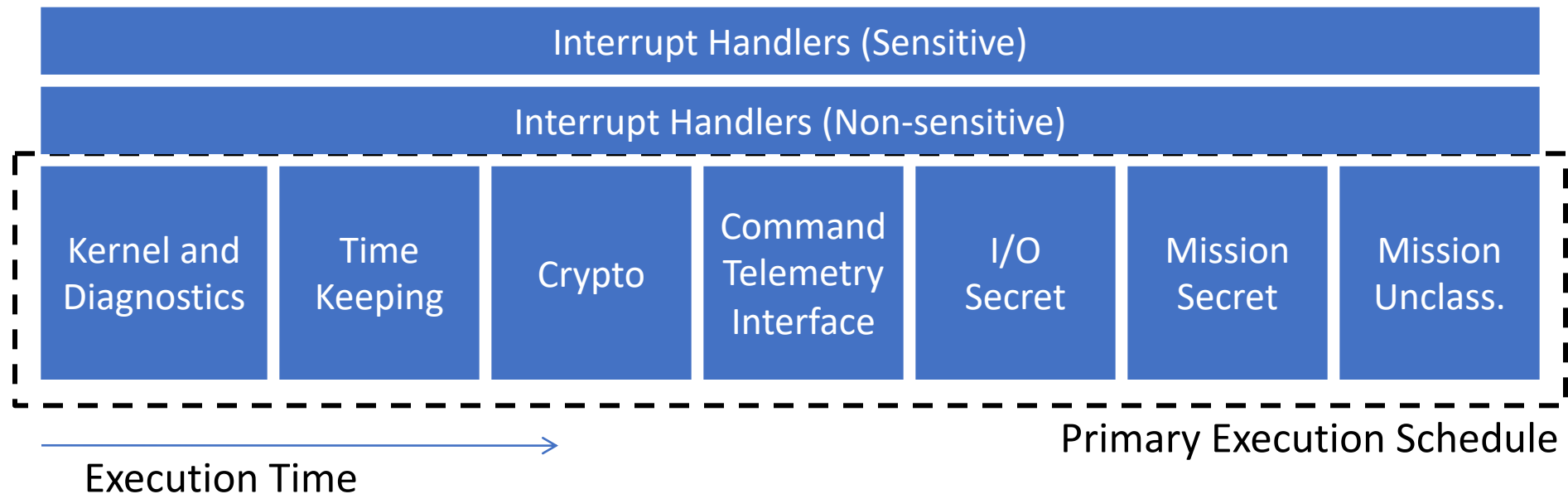
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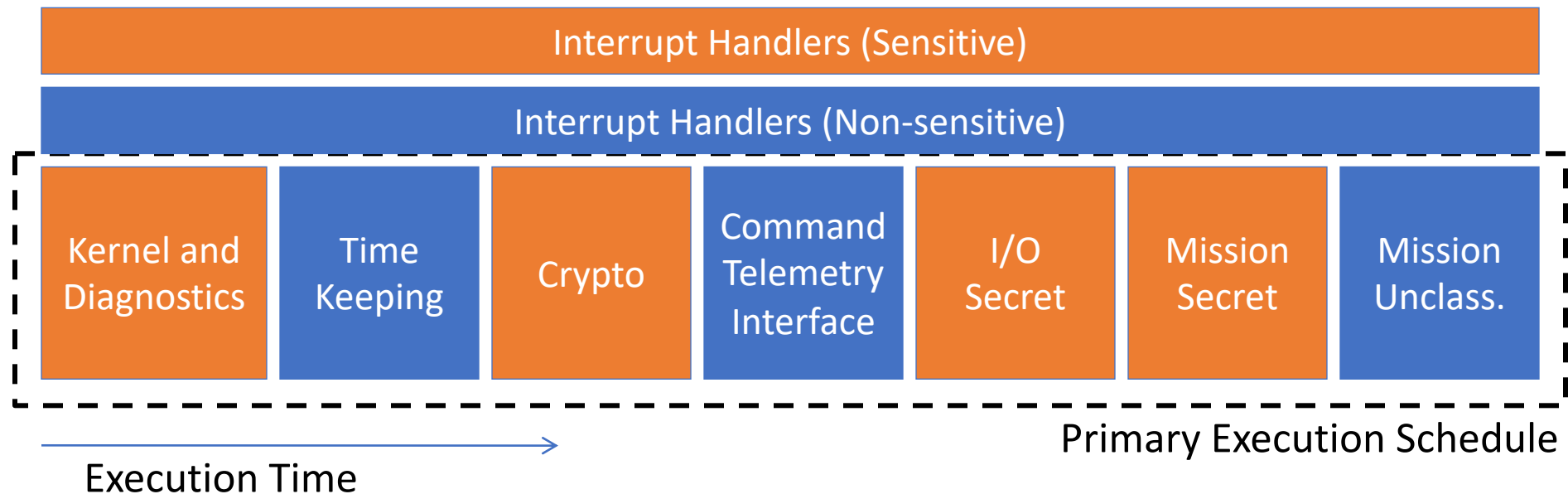
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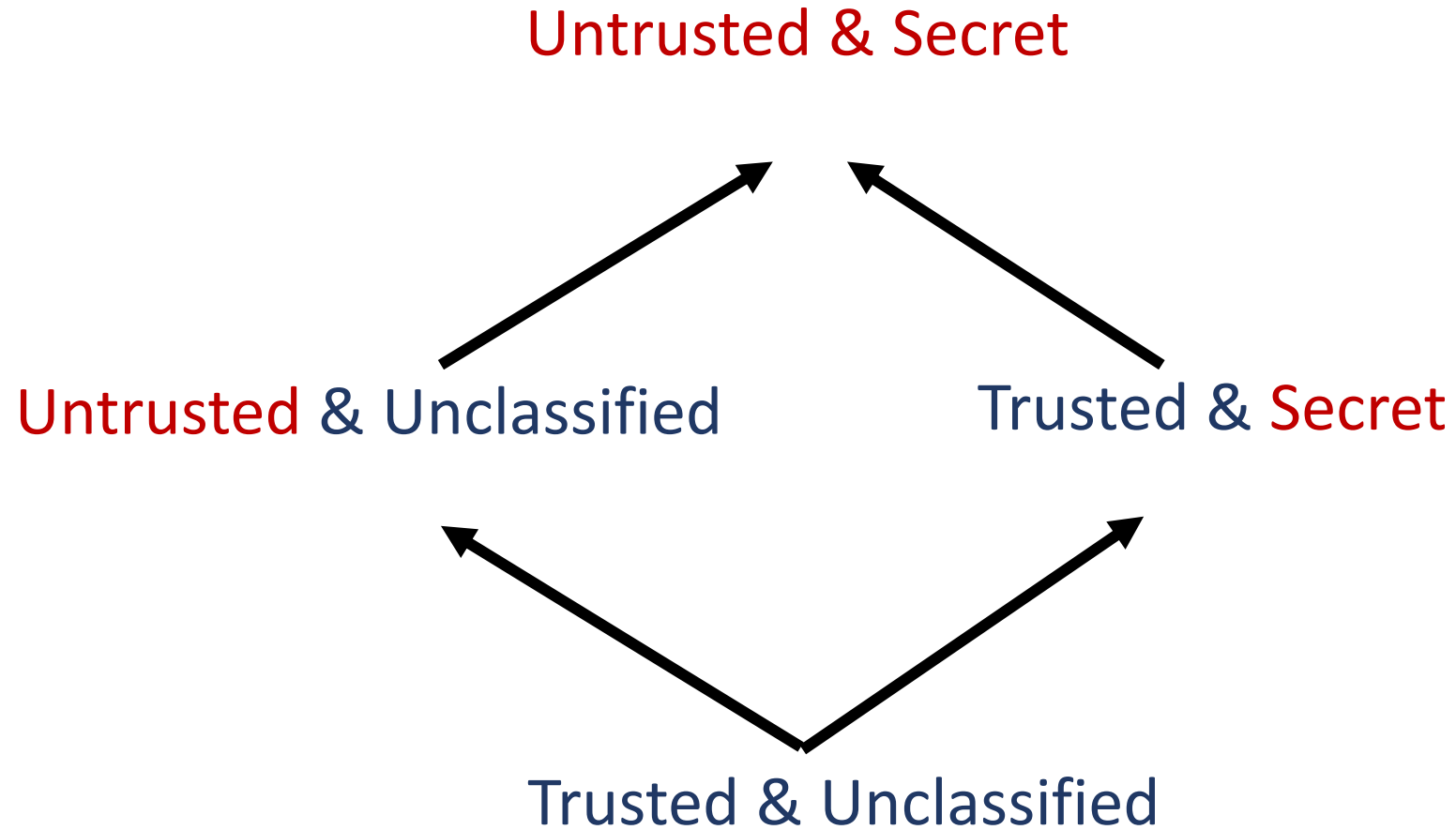
■ Non-sensitive

■ Sensitive

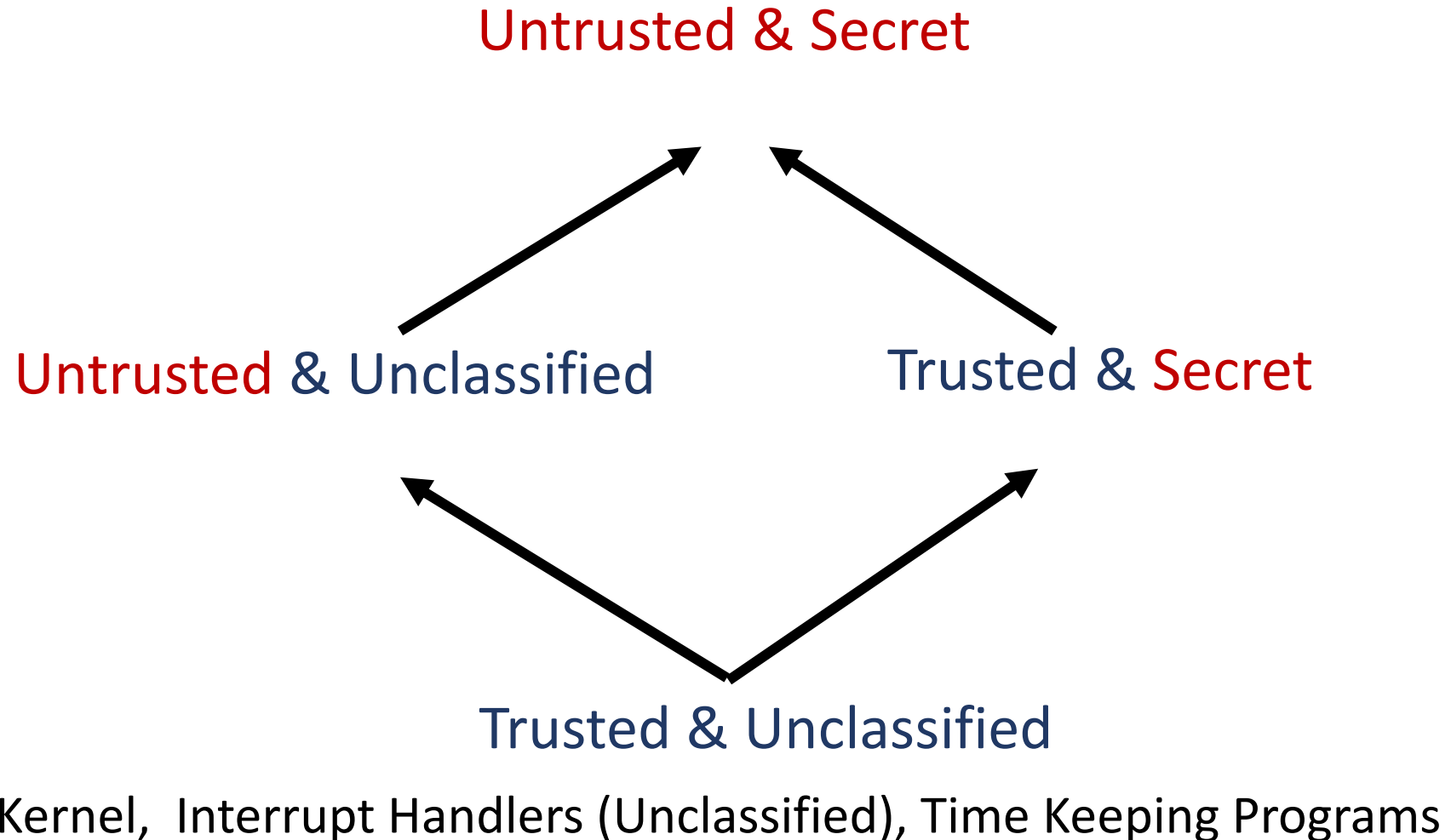


Example: Satellite System

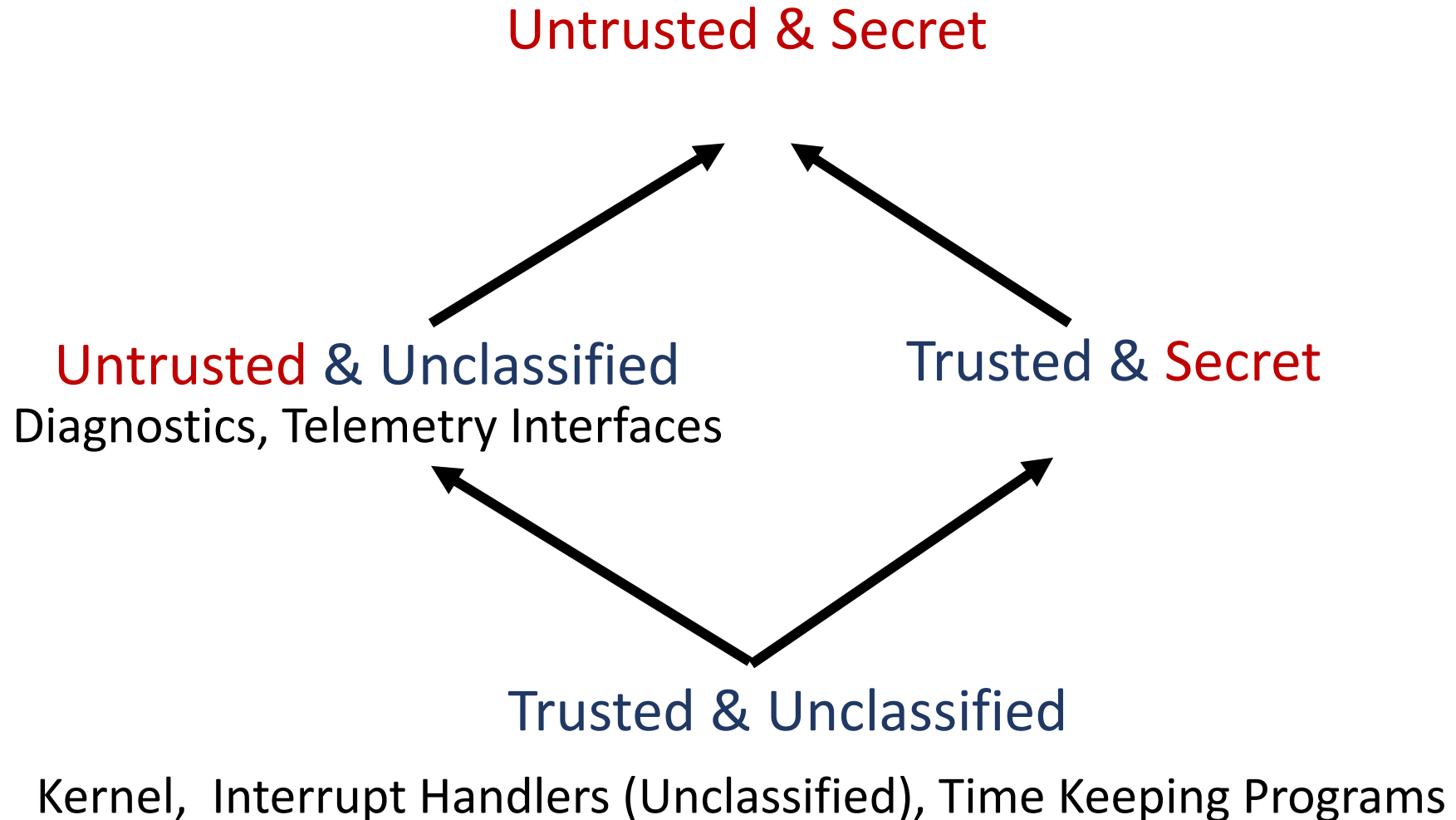
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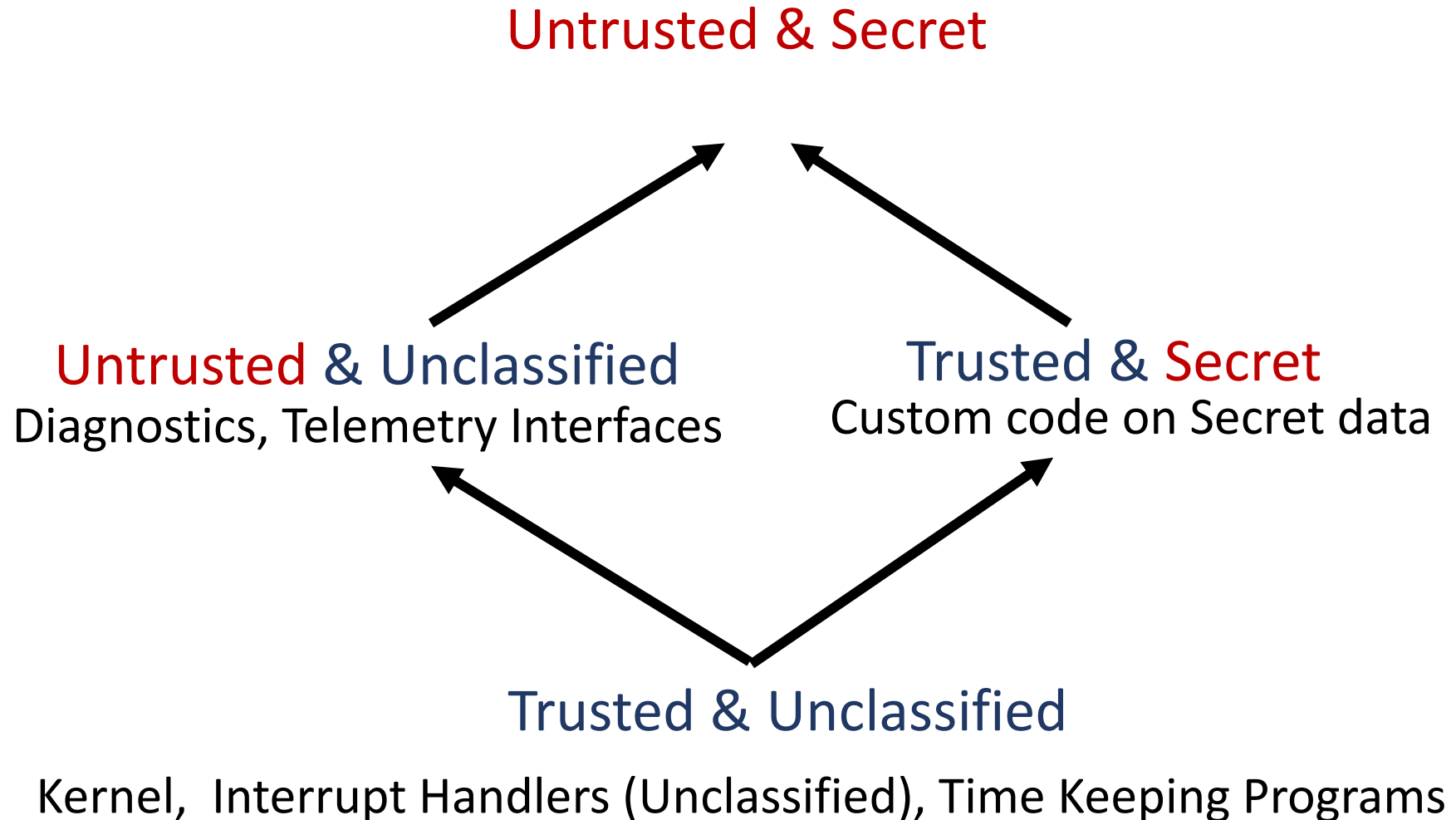
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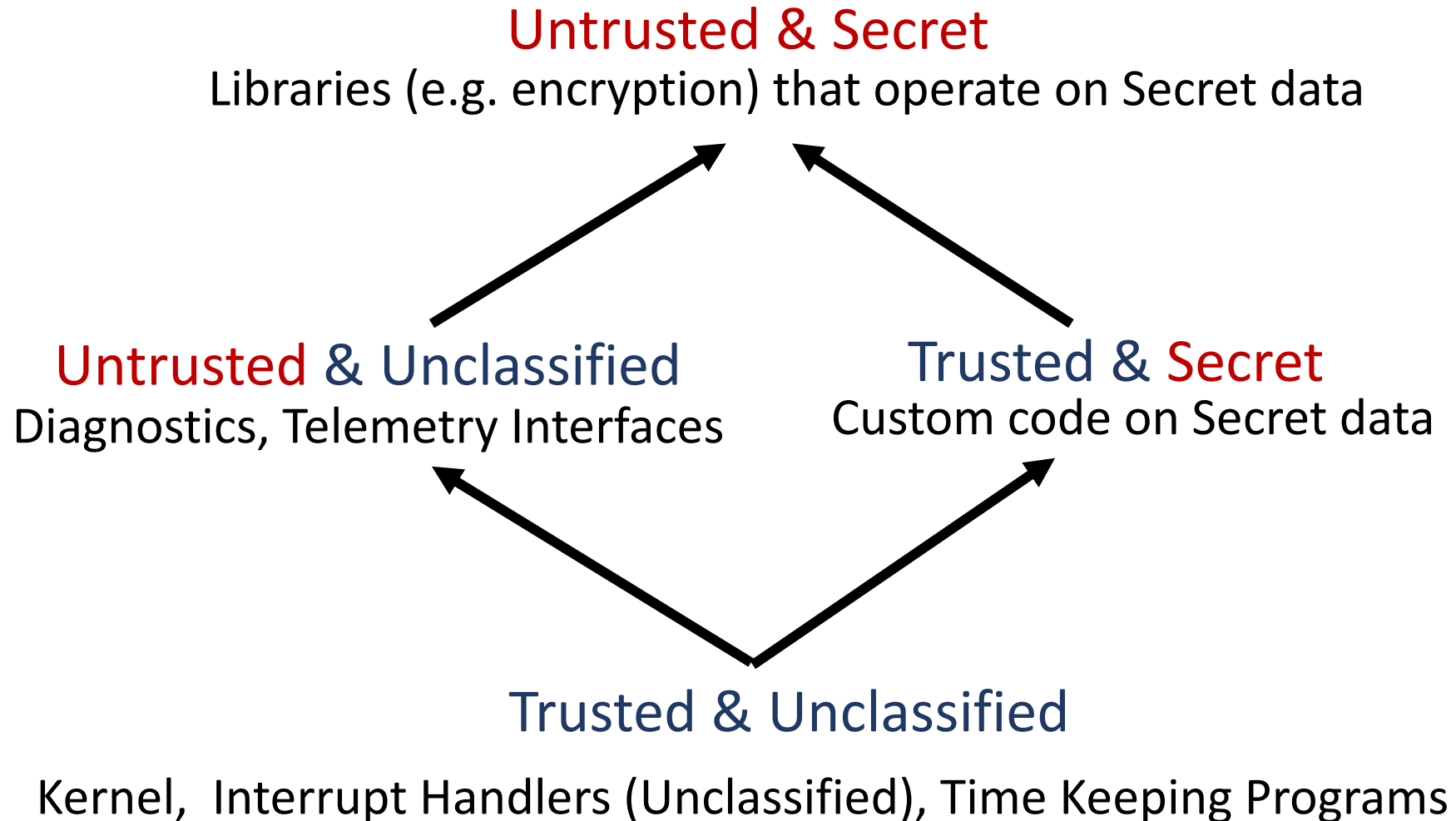
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- This kind of processor would be a pain to program. If most applications on it are small, important kernels, such as AES, would it not be better to produce a specially tuned ASIC/IP core?
- Are there any programs or algorithms that are rendered impossible (or extremely difficult) to write as a result of the limitations that they've placed on loops?

Discussion Questions on Future Work

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Great idea.

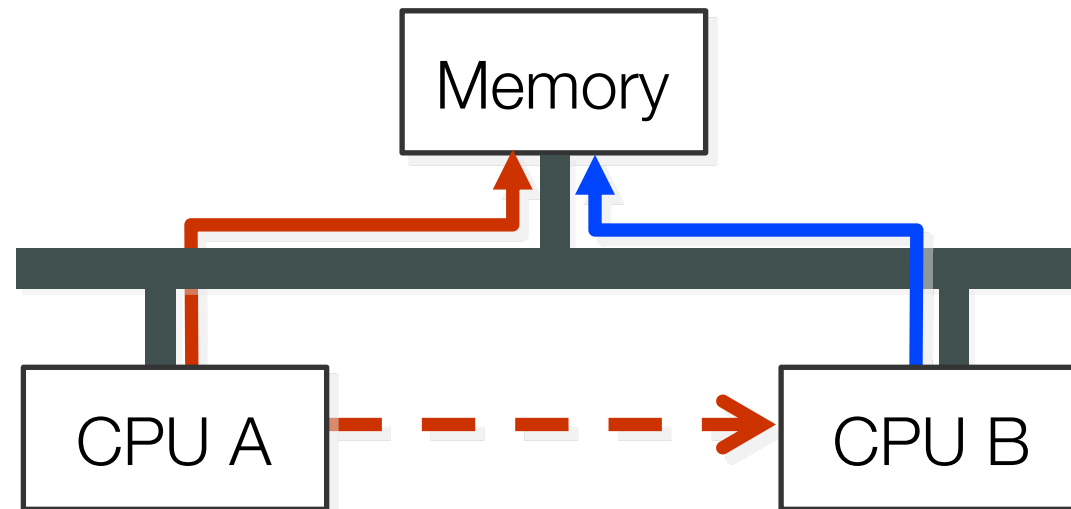
Read “HyperFlow: A Processor Architecture for Nonmalleable, Timing-Safe Information Flow Security”; Ferraiuolo et al. CCS’18

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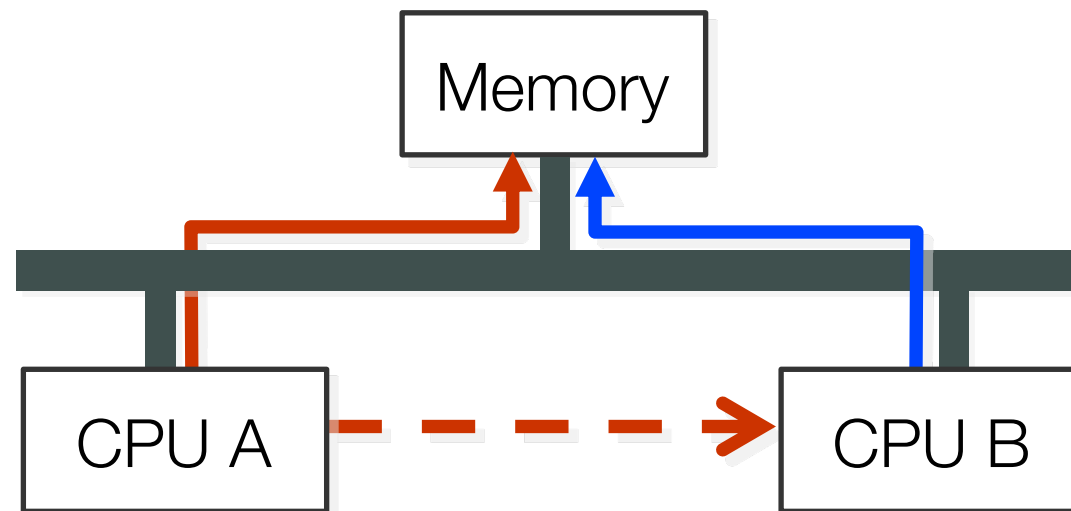
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- If we do not plan to use GLIFT to track side channel leakage, do we need to ISA restriction on indirect loads? (not indirect stores)
- How GLIFT different from static taint analysis and traditional dynamic taint analysis?

