Monday 13 July *(Room 32-155)*

9.00 Welcome and PC Report
James Hoe, Rodrick Bloem, Patrick Shaumount

9.10 Invited Talk
Chair: Rodrick Bloem (Graz Univesity of Tech.)

Amir Pnueli, (New York University)
Synthesis of Programs from Temporal Properties Specifications

10.10 *Break*

10.30 Session 1: System Verification
Chair: Klaus Schneider (U. of Kaiserslautern)

Malay Ganai and Weihong Li (NEC Labs America)
Bang for the Buck: Improvising and Scheduling Verification Engines for Effective Resource Utilization

Jeong-Han Yun, Chul-Joo Kim, Sunae Seo, Taisook Han and Kwang-Moo Choe - (KAIST)
Refining Schizophrenia via Graph Reachability in Esterel

Luigi Di Guglielmo, Franco Fummi and Graziano Pravadelli (University of Verona)
The Role of Mutation Analysis for Property Qualification

12.00 *Lunch (3rd floor open area)*

13.30 Session 2: Applications of Verification
Chair: Clark Barrett (New York University)

Peter Böhm (Oxford University)
Incremental Modelling and Verification of the PCI Express Transaction Layer

Hubert Garavel, Claude Helmstetter, Olivier Ponsini and Wendelin Serwe (INRIA Grenoble – Rhône-Alpes / Vasy)
Verification of an Industrial SystemC/TLM Model using Lotos and CADP

Omid Sarbishei[1], Mahmoud Tabandeh[1], Bijan Alizadeh[2] and Masahiro Fujita[2] (Sharif University of Technology[1], University of Tokyo – VDEC[2])
High-Level Optimization of Integer Multipliers over a Finite Bit-Width with Verification Capabilities

15.00 *Break*

15.30 Design Contest Presentation

Forrest Brewer[1] and James Hoe[2] (UCSB[1], CMU[2])
2009 Memocode Co-Design Contest

Daniel L. Rosenband[1] and Till Rosenband (RedShift Semiconductor)
A Design Case Study: CPU vs. GPGPU vs. FPGA

Abhinav Agrawal, Nirav Dave, Kermin Fleming, Asif Khan, Myron King, Man Cheuk Ng and Muralidaran Vijayaraghavan (MIT)
Implementing a Fast Cartesian-Polar Matrix Interpolator

16.45 Short poster presentations
Chair: Rodrick Bloem, Patrick Schaumont

Roderick Bloem, Krishnendu Chatterjee, Karin Greimel, Thomas Henzinger and Barbara Jobstmann
Quality through Quantity

Vyas Venkataraman, Di Wang, Wei Qin, Mrinal Bose and Jayanta Bhadra
Lyra : A Rendezvous-based High-Level Modeling Approach for Digital Hardware

Mary Ellen Tie and Miriam Leeser
Accelerating Explicit State Model Checking on FPGAs: PHAST

17.00 Poster exhibition with wine and cheese

19.00 End

17.30 Panel - Esperanto, Polyglot, or Babel: The Future of Design Languages

Moderator: Stephen Edwards (Columbia Univ.)

Panelists:
Arvind (MIT)
Gael Clave (Texas Instruments, Nice)
Rainer Doemer (University of California, Irvine)
Michael Kishinevsky (Intel)
Karen Piepe (Tabula)
Klaus Schneider (University of Kaiserslautern)
Satnam Singh (Microsoft Research, Cambridge)

Tuesday 14 July *(Room 32-155)*

9.00 Invited Talk
Chair: Patrick Schaumont (Virginia Tech)

David Harel (Weizmann Institute of Science)
Can we Computerize an Elephant?

10.00 *Break + Poster exhibition*

10.30 Session 3: Microprocessors and Multicore
Chair: Barbara Jobsmann (EPFL)

Anita Lungu[1], Pradip Bose[2], Daniel Sorin[1], Steven German[1] and Geert Janssen[2] (Duke University[1], IBM – T.J. Watson[2])
Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification

Daniel Williams, Aprotim Sanyal, Dan Upton, Jason Mars, Sudeep Ghosh and Kim Hazelwood (University of Virginia)
A Cross-Layer Approach to Heterogeneity and Reliability

Eric Chung and James Hoe (CMU)
Real World Microprocessor Design Using High-level Approaches

12.00 *Lunch (3rd floor open area)*

13.30 Tutorial

Thomas Popp (Graz U of Technology)
Implementation Attacks & Countermeasures

15.00 Break

15.30 Tutorial ctd.

17.00 Break

18.00 Reception - R&D area - 4th floor Stata

19:00 Banquet - R&D area - 4th floor Stata

Wednesday 15 July *(Room 32-155)*

9.00 Invited Talk
Chair: Arvind (MIT)

Martin Rinard (MIT)
Survival Strategies for Synthesized Hardware

10.00 Break + Poster exhibition

10.30 Session 4: Codesign
Chair: Rainer Doemer (University of California, Irvine)

Marco Bozzano[1], Alessandro Cimatti[1], Marco Roveri[1], Joost-Pieter Katoen[2], Viet Yen Nguyen[2] and Thomas Noll[2] (Fondazione Bruno Kessler[1], RWTH Aachen University[2])
Codesign of Dependable Systems: A Component-Based Approach

Fabrizio Ferrandi, Marco Lattuada, Christian Pilato and Antonino Tumeo (Politecnico di Milano)
Performance Estimation for Task Graphs Combining Sequential Path Profiling and Control Dependence Regions

Jeannet Bertrand and Briand Xavier (INRIA Grenoble – Rhône-Alpes)
Combining Control and Data Abstraction in the Verification of Hybrid Systems

12:00 ***Lunch (3rd floor open area)***

13:00 Session 5: Dataflow
Chair: Satnam Singh (MSR – Cambridge)

Nalini Vasudevan and Stephen A. Edwards (Columbia University)
Buffer Sharing in CSP-like Programs

Jens Brandt and Klaus Schneider (University of Kaiserslautern)
Static Data-Flow Analysis of Synchronous Programs

Muralidaran Vijayaraghavan and Arvind (MIT)
Bounded Dataflow Networks and Latency-Insensitive Circuits

14:30 End of conference

MemoCODE

Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2009)

Stata Center
Room 32-155
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