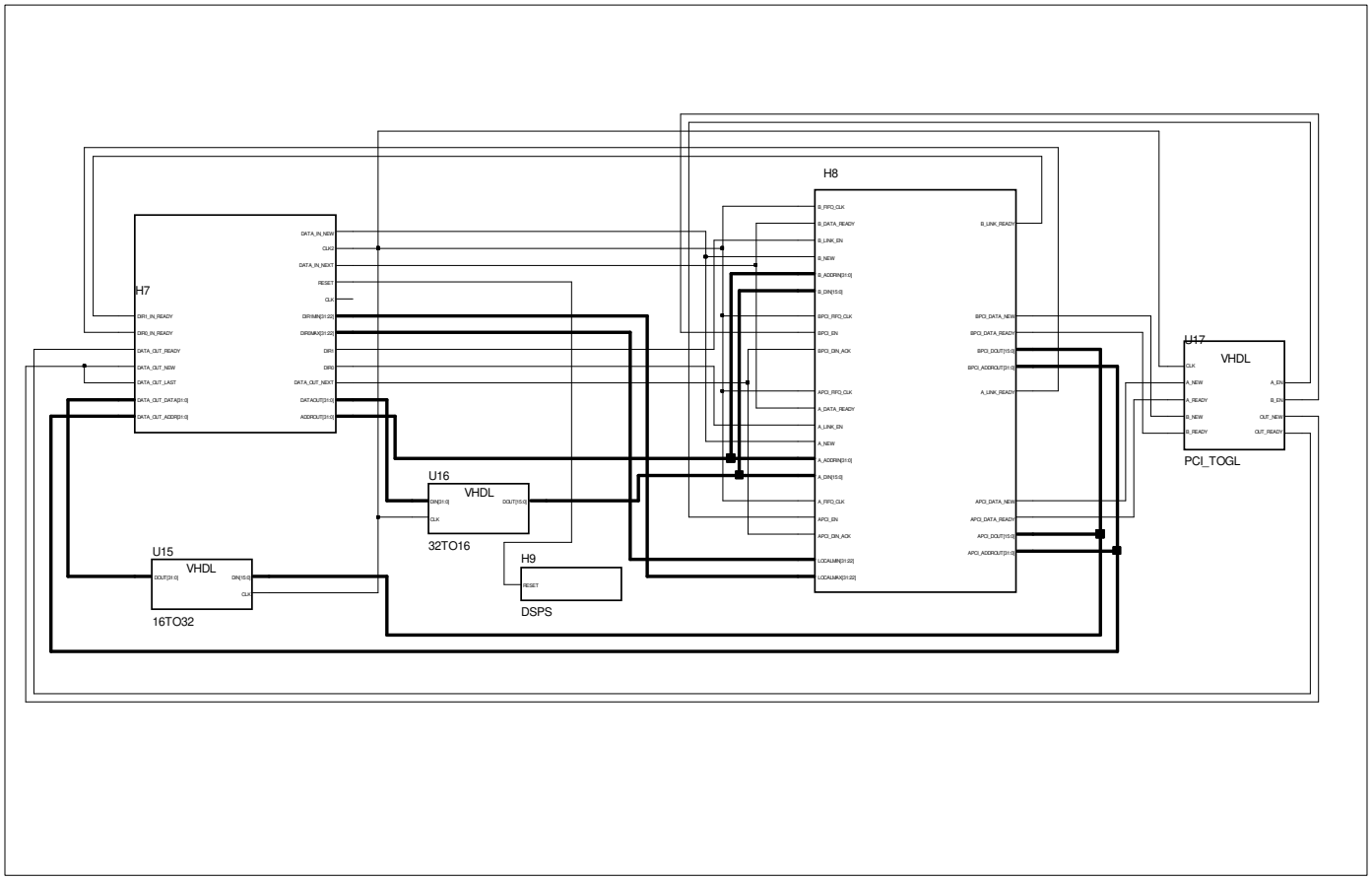
H7
DATA_IN_NEW
CLK2
DATA_IN_NEXT
RESET
CLK
DIR1_IN_READY
DIR0_IN_READY
DATA_OUT_READY
DATA_OUT_NEW
DATA_OUT_LAST
DATA_OUT_DATA[15:0]
DATA_OUT_ADDR[15:0]
DIR1MM[31:22]
DIR0MM[31:22]
DIR1
DIR0
DATA_OUT_NEXT
DATAOUT[31:0]
ADDROUT[31:0]
H8
B_FIFO_CLK
B_DATA_READY
B_LINK_EN
B_NEW
B_ADDRMM[31:0]
B_DIN[15:0]
BPCI_FIFO_CLK
BPCI_EN
BPCI_DIN_ACK
APCI_FIFO_CLK
A_DATA_READY
A_LINK_EN
A_NEW
A_ADDRMM[31:0]
A_DIN[15:0]
A_FIFO_CLK
APCI_EN
APCI_DIN_ACK
LOCALMM[31:22]
LOCALMM[31:22]
B_LINK_READY
BPCI_DATA_NEW
BPCI_DATA_READY
BPCI_DOUT[15:0]
BPCI_ADDROUT[31:0]
A_LINK_READY
APCI_DATA_NEW
APCI_DATA_READY
APCI_DOUT[15:0]
APCI_ADDROUT[31:0]
U17
VHDL
CLK
A_NEW
A_READY
B_NEW
B_READY
A_EN
B_EN
OUT_NEW
OUT_READY
PCI_TOGL
U16
VHDL
DIN[31:0]
CLK
DOUT[15:0]
32TO16
U15
VHDL
DOUT[31:0]
DIN[15:0]
CLK
16TO32
H9
RESET
DSPS