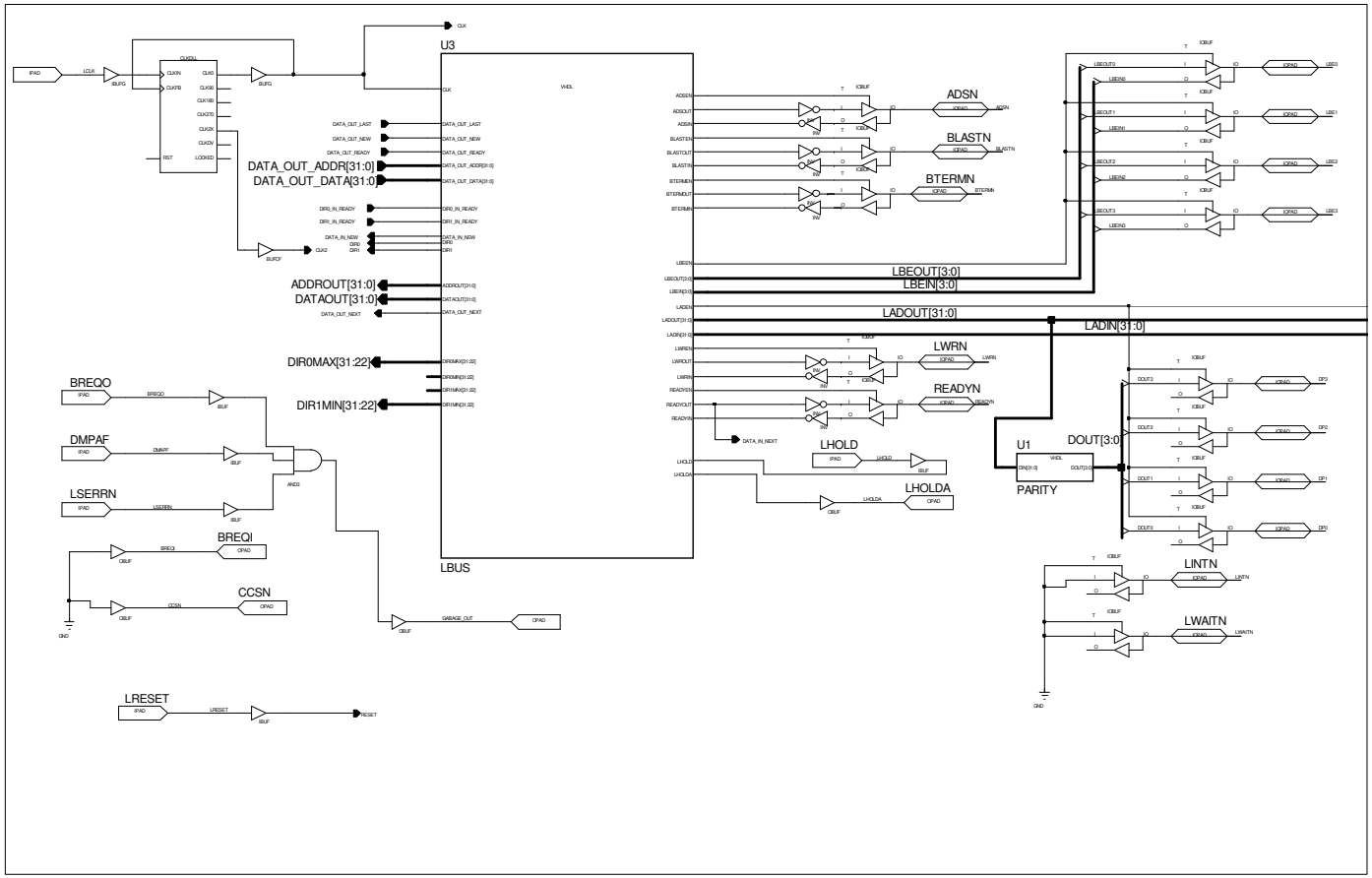
U3
LBUS
VHDL
CLK
LCLK
IPAD
IBUFG
CLKDLL
CLKIN
CLK0
CLK90
CLK180
CLK270
CLK2X
CLKDV
RST
LOCKED
BUFG
BUFGF
CLK2
DATA_OUT_LAST
DATA_OUT_NEW
DATA_OUT_READY
DATA_OUT_ADDR[31:0]
DATA_OUT_DATA[31:0]
DIR0_IN_READY
DIR1_IN_READY
DATA_IN_NEW
DIR0
DIR1
ADDROUT[31:0]
DATAOUT[31:0]
DATA_OUT_NEXT
DIR0MAX[31:22]
DIR1MIN[31:22]
BREQO
DMPAF
LSERRN
BREQI
CCSN
GARBAGE_OUT
LRESET
RESET
GND
AND3
OBUF
IBUF
OPAD
ADSN
BLASTN
BTERMN
LBEIN
LBEOUT
LBEOUT[3:0]
LBEIN[3:0]
LADOUT[31:0]
LADIN[31:0]
LWRN
READYN
DATA_IN_NEXT
LHOLD
LHOLDA
U1
PARITY
DOUT[3:0]
LINTN
LWAITN
IOBUF
IOPAD
INV