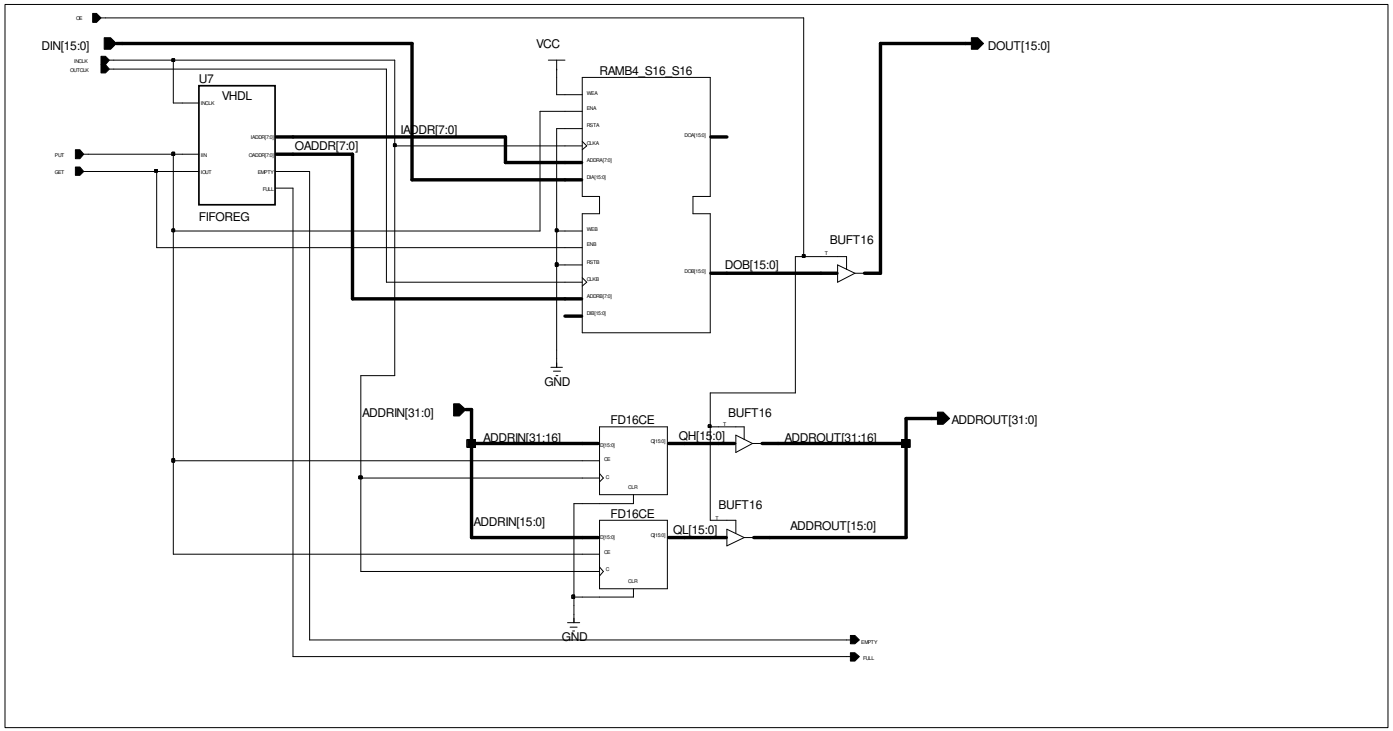
OE
DIN[15:0]
INCLK
OUTCLK
U7
VHDL
INCLK
IADDR[7:0]
OADDR[7:0]
PUT
GET
IN
IOUT
EMPTY
FULL
FIFOREG
VCC
RAMB4_S16_S16
WEA
ENA
RSTA
CLKA
ADDRA[7:0]
DIA[15:0]
DOA[15:0]
WEB
ENB
RSTB
CLKB
ADDRB[7:0]
DIB[15:0]
DOB[15:0]
GND
DOUT[15:0]
BUFT16
T
ADDRIN[31:0]
ADDRIN[31:16]
FD16CE
D[15:0]
Q[15:0]
CE
C
CLR
QH[15:0]
ADDROUT[31:16]
ADDROUT[31:0]
ADDRIN[15:0]
QL[15:0]
ADDROUT[15:0]
EMPTY
FULL